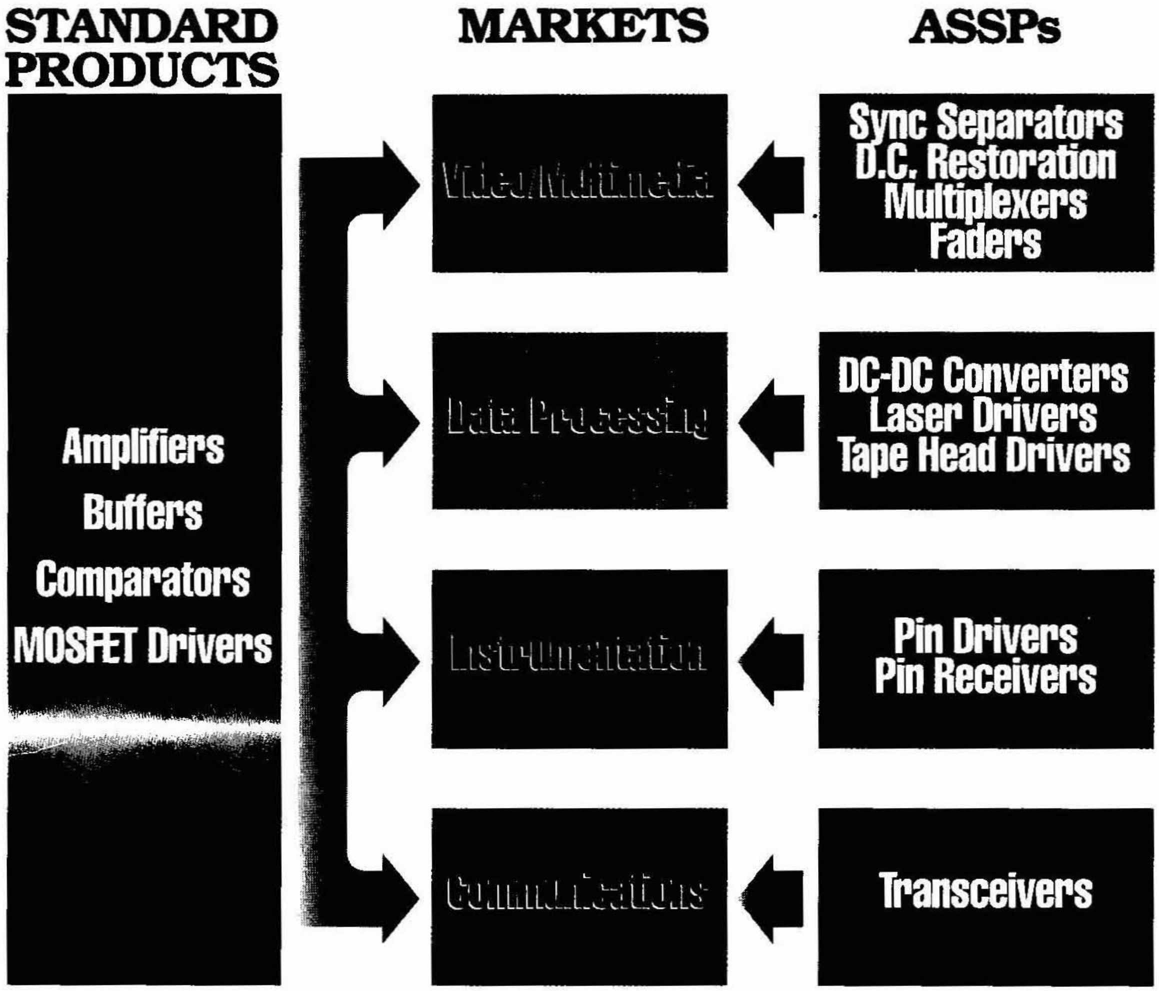
1997 Data Book



STANDARD PRODUCTS

Amplifiers
Buffers
Comparators
MOSFET Drivers

MARKETS

Video/Multimedia
Data Processing
Instrumentation
Communications

ASSPs

Sync Separators
D.C. Restoration
Multiplexers
Faders

DC-DC Converters
Laser Drivers
Tape Head Drivers

Pin Drivers
Pin Receivers

Transceivers

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1997 Full Product Line Databook

WARNING—Life Support Applications Policy

Elantec, Inc. products are not authorized for and should not be used within Life Support Systems without the specific written consent of Elantec, Inc. Life Support systems are equipment intended to support or sustain life and whose failure to perform when properly used in accordance with instructions provided can be reasonably expected to result in significant personal injury or death. Users contemplating application of Elantec, Inc. products in Life Support Systems are requested to contact Elantec, Inc. factory headquarters to establish suitable terms and conditions for these applications. Elantec, Inc.'s warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.

General Disclaimer

Specifications contained in this databook are current as of the publication date shown. Each datasheet is a controlled document. Current revisions, if any, to these specifications are maintained at the factory and are available upon request. Elantec, Inc. reserves the right to make changes in the circuitry or specifications contained herein at any time without notice. Elantec, Inc. assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement. Products contained in this databook may be covered by one or more of the following patents. Additional patents are pending. For specific information, refer to the individual datasheets:

US Patent Numbers: 4,746,877 • 4,827,223 • 4,837,523 • 4,833,424 • 4,935,704 • 4,910,477 • 5,128,564 • 4,878,034 • 4,963,802 • 5,179,355 • 5,321,371 • 5,334,883 • 5,341,047 • 5,352,987 • 5,352,389 • 5,351,012 • 5,374,898 • 5,389,840 • 5,418,495 • 5,426,396 • 5,420,542 • 5,430,670 • 5,469,104 • 5,469,106 • 5,479,133 • 5,475,343 • 5,528,303

UK Patent Numbers: 2217135 • 2217134 • 2261786

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Introduction

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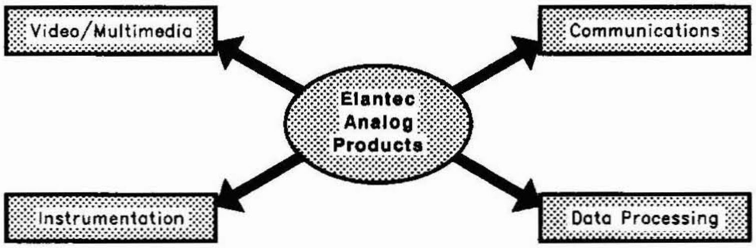
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Mission

"To be a leading supplier of high performance analog solutions for the video/multimedia, data processing, communications and instrumentation markets."

Elantec, Inc., founded in 1983 and located in Milpitas, California, is a fully integrated semiconductor company focused on providing high performance analog intensive functions for growing markets. These markets are driven by the rapid advances in digital technology which in turn creates a demand for high speed and low power analog functions to complete the overall system. Elantec serves these markets with standard and application specific standard products (ASSP) using advanced bipolar and CMOS technologies.

Our strategy is to provide effective and timely solutions through market knowledge, advanced technologies, design expertise and close customer interface.



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Market	Typical Applications	Representative Elantec Products
Video/Multimedia	Displays	Cathode Ray Tube Drivers
	Personal Computer Add-on Boards	Video ASSPs, Faders, DC Restoration
	Set Top Converters	Video ASSPs, Faders, Amplifiers
	Special Effects Generators	Video ASSPs, Multipliers, PLL, Faders
	Studio Equipment	Video Amplifiers, Faders, Multiplexers
	Switchers/Routers	Multiplexers, Power Amplifiers
	Video Distribution Networks	High Power Amplifiers
	Workstations	Video Timing Circuits
	Video Cameras	CCD Drivers, Amplifiers
Instrumentation	Analyzers	High Speed Amplifiers, Comparators
	Automatic Testers	Pin Drivers/Receivers
	Measuring Instruments	High Speed Amplifiers, Comparators
	Medical Instrumentation	Mosfet Drivers
	Recorders	High Speed Amplifiers
	Portable Instrumentation	Low Power Amplifiers
Data Processing	Copiers	Video Amplifiers
	Document Scanners	Video Amplifiers
	Magnetic Disk Drives	Servo Motor Drivers
	Optical Disk Drives	High Speed Amplifiers, Laser Drivers
	Personal Computers	Video ASSPs, DC to DC Converters, System Managers
	Power Supplies	Mosfet Drivers
Communications	Fax Machines	High Speed Amplifiers
	Modems	High Speed Amplifiers
	Transmission Line Drivers	Power Amplifiers
	Transmission Line Receivers	High Speed Amplifiers, Transceivers
	Networks	Twisted Pair Drivers

Markets and Products

Elantec has over 125+ products in its catalog to serve the target markets. Many of the standard products, such as amplifiers, are used in multiple markets while the application specific products are targeted for specific applications and group of customers.

The preceding table outlines the ranges of markets, applications and products which the company serves.

Technology

The company uses a variety of technologies for its products. In particular, Elantec has focused on developing an advanced complementary bipolar technology using dielectric isolation and silicon on insulator techniques for its high speed circuits. Complementary bipolar technology allows high speed analog signals to be processed efficiently in either signal polarity which greatly simplifies design methodology and substantially improves power dissipation. Because of the dielectric isolation technique, Elantec's complementary process has the additional inherent advantages of low capacitance, low crosstalk, no latch-up, high voltage, high temperature operation and improved speed.

For low power, analog switching and mixed signal applications, Elantec uses a variety of advanced CMOS technologies featuring dual poly and dual metal.

Advances in technology together with outstanding design expertise will continue to provide superior solutions for Elantec's target markets.

Design Capabilities

Elantec's engineering team has many years of experience defining, designing, manufacturing and testing analog and mixed signal devices, utilizing both Bipolar and CMOS technologies.

Functions we currently supply are: current and voltage feedback amplifiers, multipliers, video specific standard products, pin drivers and receivers, C.R.T. drivers, buffers, servo electronics, MOSFET and IGBT drivers, DC converters, instrumentation amplifiers, and precision amplifiers. Elantec also designs customer specific products where the unique technical and volume requirements of the system make this more desirable. Customers can discuss their challenging system requirements with out talented technical team of field and factory applications engineers.

Elantec provides each circuit designer and layout artist with the most up to date workstations at their desk. All stations are networked together to a server. Extra "computing engines" are also available on the network. Elantec uses Cadence and MicroSim design software and Cadence IC layout software and design verification tools. The design tool suite can use the computing capability of the entire network to allow extensive simulations covering the variations of the wafer fabrication process, based on data derived from capability studies.

Test Automation/Equipment Capability

Elantec utilizes automatic test stations for primarily DC testing operational amplifiers, buffers, comparators, and other linear devices. In general, custom socket adaptors have been developed for unique devices such as current feedback amplifiers, DC restored video amplifiers, sync separators and disk drive servo motors. A wide range of automatic handlers allow high speed, room temperature and extended range temperature testing of Dual in Line (DIP), Small Outline (SO) packages, and special packages.

The DC test capability is augmented with AC test systems which are integrated into the main test system. The time domain systems, which are used to measure very fast rise times, slew rates and propagation delays, are comprised of programmable pulse generators and 1 GHz digitizing oscilloscopes and are capable of measurements under 10 pS. The frequency domain systems which are used to measure band-width, differential phase, differential gain, phase linearity, gain flatness, distortion, etc. are composed of programmable signal sources and network analyzers and are capable of measurements to 500 MHz.

Packaging Capability

Elantec supports most industry standard package types. Currently we are manufacturing standard products in the packages shown below:

P-DIP:	8, 14, 16, 18 Pins
SOIC:	8, 14, 16, 20, 28 Pins
SOT-23:	5 Pins

Additionally, we can supply special packages upon request for volume and special applications. Contact Elantec's marketing department for availability.

Quality and Service

Elantec's commitment to quality begins with the product definition, design and characterization and continues through the complete process. Elantec continually improves its manufacturing and quality methods using SPC, Total Quality Management and ISO 9000 compatible techniques. The company is ISO 9001 certified.

Superior product performance and quality are augmented by a commitment to customer service and technical support in order to make our customers successful. Technical customer support is provided through corporate applications, field applications engineers and technical seminars. Sales support is provided through the Elantec field sales force which directs a worldwide network of technical representatives and distributors.

Amplifiers and Buffers/Broadband/Video

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Comparison of Elantec Voltage Mode Feedback to Current Mode Feedback Amplifiers

Current Mode Feedback op amps have inputs similar to voltage mode op amps, but allow control of the bandwidth and offer higher slew rates and video linearity.

Characteristics	Voltage Mode Feedback	Current Mode Feedback
Bandwidth (BW)	Bandwidth generally follows the Gain Bandwidth Product Rule. Bandwidth is defined by internal compensation capacitor. Bandwidth at a Gain of ten is about $\frac{1}{10}$ or 10% of the Gain Bandwidth Product. Amplifiers have a minimum Gain for stable operation.	Bandwidth not defined by gain bandwidth product rule. Bandwidth is defined by the feedback resistor value and internal compensation capacitor. Bandwidth at gain of ten is 50% to 85% of the unity gain bandwidth for a given feedback resistor, which may be reduced to give about the same bandwidth up to a gain of 10.
Slew Rate Small Signal BW Large Signal BW	Slew Rate is defined by compensation capacitor and internal bias currents. Amplifiers with high min. gain have small comp cap's, higher Slew Rate and higher LSBW. Large Signal BW is about 10% to 15% of Small Signal BW. Distortion usually increases for signals ≥20% of slew rate limit.	Slew rate is not limited by internal bias currents and compensation capacitor. Large Signal BW is 25% to 65% of Small Signal BW. Best with input near LSBW and output up to full output volts. Distortion usually increases rapidly for signals ≥35% slew rate limit.
Bias Current IB +Input Current −Input Current	Bias Current Max range is 1 μA to 20 μA on both inputs, which match and cancel.	+Input current max range is 3 μA to 20 μA. −Input current max range is 7 μA to 40 μA quiescent with transient peaks to 20 mA from feedback resistor. Input currents do not match nor cancel.
Input Resistance	R_{IN} differential range is 10 kΩ to 20 MΩ.	$+R_{IN}$ range is 100 kΩ to 36 MΩ. $-R_{IN}$ range is 10Ω to 50Ω and is normally the summing node for feedback currents.
Feedback Resistor	Feedback resistor does not define BW and may be 0Ω for unity gain connected amp.	Feedback resistor defines BW and must be selected for BW even on unity gain connected amp.
Feedback Capacitor	May have feedback capacitors from output to −Input for an integrator, if amplifier is unity-gain stable.	Must not have feedback capacitor from output to −Input. Integrator requires added resistor.
Offset Voltage V_{OS}	V_{OS} Max range is 1.5 mV to 20 mV at 25°C	V_{OS} Max range is 3 mV to 20 mV at 25°C
Settling Time	Settling time to 0.1% is medium speed with similar speed for the remainder. Settling time increases with higher gain.	Settling to about 0.1% is fast with slow settling for the remainder from a long thermal tail for (+) gain. −Gain connections have no thermal tails.
Input Noise	Good for low noise low level input signals.	Noisy at low gains, but quiet for gains ≥5.
RF Amp	Good within 35% of slew rate limit.	Provides lowest distortions.
Video Amp	Flexible, low distortion.	Best for medium to high signals and for low differential gain and phase errors. Best choice for line drivers.
Output Current	Output Current from 50 mA to 75 mA. Use limited by Large Signal BW.	Output Current from 30 mA to 80 mA. May be used over wide BW range. Output current of 600 mA on power amp.
More Help	Tutorial #2 in 1994 Data Book	Application Note #3 in 1995 New Product Supplement Application Note #23 in 1997 Data Book.

Wide Bandwidth/Video Amplifiers

Current Mode Feedback Amplifiers at ±5V and ±15V Supplies.

Listed by decreasing bandwidth.

Part #	Features	# of Amps	Band-width −3 dB A_V +1	I_{CC} at ±5Vs all Amps	Slew Rate A_V +2	A_{VOL} (1/gain error *)	Input Offset Volts	Input Bias Current		Output Current 10Ω Load	Supply Voltage Range		Package P = Pins N = PDIP S = SOIC M = SOL T = TO220 W = SOT23
			Typ	Max	Typ	Min	Max	Max		Min	Min	Max	
								+In	−In				
Up to ±5V													
EL2070C	Disable	1	350 MHz	20 mA	700V/μs	120V/V	5 mV	20 μA	20 μA	50 mA	±4.5V	±7V	8P-N-S
EL400C		1	350 MHz	23 mA	700V/μs	120V/V	5.5 mV	25 μA	25 μA	50 mA	±4.5V	±7V	8P-N-S
EL2180C EL2280C EL2480C	Wide BW Low Power	1 2 4	250 MHz	6 mA 12 mA 24 mA	1200V/μs	200V/V	15 mV	15 μA	30 μA	80 mA 50 mA 50 mA	±1.5V	±6.3V	8P-N-S-W 8P-N-S 14P-N-S
EL2186C EL2286C EL2386C	Disable	1 2 4	250 MHz	6 mA 12 mA 18 mA	1200V/μs	200V/V	15 mV	15 μA	30 μA	80 mA 50 mA 50 mA	±1.5V	±6.3V	8P-N-S 14P-N-S 16P-N-S
EL2071C	Disable A_V +3	1	150 MHz Δ	21 mA	1200 V/μs Δ	167V/V	6 mV	20 μA	30 μA	50 mA	±4.5V	±7V	8P-N-S
EL2171C	Min A_V +3	1	150 MHz Δ	21 mA	1200 V/μs Δ	167V/V	6 mV	20 μA	30 μA	50 mA	±4.5V	±7V	8P-N-S
EL2130C		1	85 MHz	21 mA	600V/μs	97V/V	10 mV	15 μA	40 μA	30 mA	±4.5V	±6V	8P-N-S
EL2170C EL2270C EL2470C	Low Power	1 2 4	70 MHz	2 mA 4 mA 8 mA	800V/μs	200V/V	15 mV	5 μA	10μA	80 mA 50 mA 50 mA	±1.5V	±6.3V	8P-N-S-W 8P-N-S 14P-N-S
EL2176C EL2276C	Disable Low Power	1 2	70 MHz	2 mA 4 mA	800V/μs	200V/V	15 mV	5 μA	10 μA	80 mA 50 mA	±1.5V	±6.3V	8P-N-S 14P-N-S
Up to ±15				**±15V**									
EL2160C EL2260C EL2360C EL2460C	Wide BW Disable	1 2 3 4	180 MHz	11 mA 20 mA 30 mA 40 mA	1500V/μs	890V/V	10 mV	3 μA	15 μA	60 mA	±2V	±16.5V	8P-N-S 8P-N-S 16P-N-S 14P-N-S
EL2175C	Precision	1	142 MHz	10 mA	1000V/μs	6000V/V	3 mV	6 μA	7 μA	80 mA	±4.5V	±16.5V	8P-N-S
EL2030C	Low Distortion	1	120 MHz	21 mA	2000V/μs	1000V/V	20 mV	15 μA	40 μA	60 mA	±4.5V	±18V	8P-N 20P-M

Δ $A_V = +20$

*Derived from: $A_{VOL} \approx R_{OL}/(R_F + (-R_{IN} * A_V))$, for R_F given in AC specs. $-R_{IN}$ is 10Ω to 50Ω.

Wide Bandwidth/Video Amplifiers

Current Mode Feedback Amplifiers at ±5V and ±15V Supplies. — Contd.

Listed by decreasing bandwidth.

Part #	Features	# of Amps	Band-width −3 dB A_V +1	I_{CC} at ±5Vs all Amps	Slew Rate A_V +2	A_{VOL} (1/gain error *)	Input Offset Volts	Input Bias Current		Output Current 10Ω Load	Supply Voltage Range		Package P = Pins N = PDIP S = SOIC M = SOL T = TO220 W = SOT23
			Typ	Max	Typ	Min	Max	Max		Min	Min	Max	
								+In	−In				
EL2166C	Disable	1	115 MHz	10 mA	1500V/μs	890V/V	10 mV	5 μA	20 μA	50 mA	±4.5V	±16.5V	8P-N-S
EL2120C	Disable	1	95 MHz	20 mA	750V/μs	260V/V	25 mV	15 μA	40 μA	50 mA	±2.5V	±16.5V	8P-N-S
EL4393C	Disable	3	90 MHz	27 mA	960V/μs	67V/V	12 mV	5 μA	65 μA	40 mA	±4.5V	±16.5V	16P-N-M
EL2099C	Power	1	50 MHz	45 mA	1000V/μs	167V/V	20 mV	15 μA	35 μA	600 mA	±4.5V	±16.5V	5P-T
EL2020C	Disable	1	50 MHz	12 mA	500V/μs	366V/V	10 mV	15 μA	40 μA	30 mA	±4.5V	±16.5V	8P-N 20P-M
EL2165C	Precision	1	30 MHz	5 mA	500V/μs	14000V/V	3 mV	6 μA	7 μA	55 mA	±4.5V	±16.5V	8P-N-S

Δ $A_V = +20$

*Derived from: $A_{VOL} \approx R_{OL}/(R_F + (-R_{IN} * A_V))$, for R_F given in AC specs. $-R_{IN}$ is 10Ω to 50Ω.

Wide Bandwidth/Video Amplifiers

Voltage Mode Feedback Amplifiers at ±5V and ±15V Supplies.

Listed by decreasing bandwidth.

Part #	Features	# of Amps	Bandwidth −3 dB at Min Gain	I_{CC} at ±5Vs all Amps	Min Stable Gain	Slew Rate at Min Gain	A_{VOL}	Input Offset V_{OS}	Input Bias I_B	Output Current 10Ω Load	Supply Voltage Range		Package P = Pins N = PDIP S = SOIC W = SOT23
			Typ	Max	Min	Typ	Min	Max	Max	Min	Min	Max	
Up to ±5V													
EL2075C	Wide BW	1	400 MHz	23 mA	+10 A_V	800V/μs	500V/V	1 mV	6 μA	50 mA	±3V	±16.5V	8P-N-S
EL2074C		1	400 MHz	23 mA	+2 A_V	400V/μs	500V/V	1.5 mV	6 μA	50 mA	±3V	±6V	8P-N-S
EL2073C		1	400 MHz	23 mA	+1 A_V	250V/μs	500V/V	1.5 mV	6 μA	50 mA	±3V	±7V	8P-N-S
EL2150C	Single Supply	1	125 MHz	6.5 mA	+1 A_V	275V/μs	1778V/V	1.5 mV	10 μA	75 mA	±3V	±12.6V,	8P-N-S-5W
EL2250C		2		13 mA								±6.3V	8P-N-S
EL2450C		4		26 mA									14P-N-S
EL2157C	+ Disable, Clamp	1		6.5 mA									8P-N-S
EL2257C	+ Disable, Clamp	2		13 mA									14P-N-S
EL2357C	+ Disable, Clamp	3		19.5 mA									16P-N-S
EL2211C	Low Cost	2	100 MHz	17 mA	+2 A_V	140V/μs	160V/V	20 mV	15 μA	75 mA	+10V	±9V	8P-N-S
EL2311C	Single Supply	3		25.5 mA									14P-N-S
EL2411C		4		34 mA									14P-N-S
EL2210C	Low Cost	2	110 MHz	17 mA	+1 A_V	130V/μs	160V/V	20 mV	15 μA	75 mA	+10V	±9V	8P-N-S
EL2310C	Single Supply	3		25.5 mA									14P-N-S
EL2410C		4		34 mA									14P-N-S
Up to ±15V				**at ±15V**									
EL2045C	Low Cost	1	100 MHz	6.3 mA	+2 A_V	275V/μs	1500V/V	7 mV	8.2 μA	50 mA	+2.5V	±18V	8P-N-S
EL2245C	V_{IN} to 0.1V	2		12.6 mA				4 mV					8P-N-S
EL2445C	at +5Vs	4		25.2				4 mV					14P-N-S
EL2044C	Low Cost	1	120 MHz	6.3 mA	+1 A_V	325V/μs	750V/V	7 mV	8.2 μA	50 mA	+2.5V	±18V	8P-N-S
EL2244C	V_{IN} to 0.1V	2		12.6 mA				7 mV					8P-N-S
EL2444C	at +5Vs	4		25.2				7 mV					14P-N-S

Output Disable Wide Bandwidth/Video Amplifiers Current Mode Feedback and Voltage Mode Feedback with Clamp at ±5V and ±15V Supplies.

Listed by decreasing bandwidth.

Part #	Features	# of Amps	Band-width −3 dB A_V +1	Turn On Time	Turn Off Time	I_{CC} at ±5V all Amps	I_{CC} at ±5Vs Disable	Slew Rate A_V +2	V_{OS}	Feed-through Cap. *	I_{OUT} into 0Ω Load	Supply Voltage Range		Package P = Pins N = PDIP S = SOIC
			Typ	Typ	Typ	Max	Max	Typ	Max	Typ	Min	Min	Max	
Up to ±5V	Current Mode Feedback													
EL2186C EL2286C EL2286C	Wide BW Low Power	1 2 3	250 MHz	40 ns	500 ns	6 mA 12 mA 18 mA	20 μA 40 μA 60 μA	1200V/μs	15 mV	0.48 pF	80 mA 50 mA 50 mA	±1.5V	±6.3V	8P-N-S 14P-N-S 16P-N-S
EL2070C		1	200 MHz	200 ns	1000 ns	20 mA	7 mA	700V/μs	5 mV	0.18 pF	50 mA	±4.5V	±7V	8P-N-S
EL2071C	$A_V \geq +3$	1	150 MHz Δ	40 ns	70 ns	21 mA	3 mA	1200V/μs Δ	6 mV	0.14 pF	50 mA	±4.5V	±7V	8P-N-S
EL2176C EL2276C	Low Power	1 2	70 MHz	40 ns	500 ns	2 mA 4 mA	20 μA 40 μA	800V/μs	15 mV	0.48 pF	80 mA 50 mA	±1.5V	±6.3V	8P-N-S 14P-N-S
Up to ±15V						**±15V**	**±15V**							
EL2166C		1	115 MHz	70 ns	70 ns	10 mA	10 mA	1500V/μs	10 mV	1.5 pF	50 mA	±4.5V	±16.5V	8P-N-S
EL2120C		1	95 MHz	50 ns	50 ns	20 mA		750V/μs	25 mV	0.2 pF	50 mA	±2.5V	±16.5V	8P-N-S
EL4393C	Triple	3	90 MHz	30 ns	30 ns	27 mA	16 mA	960V/μs	12 mV	2.0 pF	40 mA	±4.5V	±16.5V	16P-N-M
EL2020C		1	50 MHz			12 mA	7.5 mA	500V/μs	10 mV		30 mA	±4.5V	±18V	8P-N 20P-M
Single Supply Up to ±5V	Voltage Mode Feedback										**±5V**			
EL2157C EL2257C EL2357C	$+V_{OUT}$ Clamp	1 2 3	125 MHz	40 ns 25 ns 25 ns	40 ns 50 ns 50 ns	6.5 mA 13 mA 19.5 mA	20 μA 100 μA 150 μA	275V/μs	1.5 mV		75 mA	+3V	±16.5V	8P-N-S 14P-N-S 16P-N-S

*Feedthrough capacitance is the equivalent capacitance from the signal input to the output of a disabled amplifier.

Δ A_V = +10

Video Buffers
Wide Bandwidth/Video/Distribution

Listed by decreasing bandwidth.

Part #	Features	Band-Width −3 dB	Output Current (Peak)	# of Loads * 2 V_{PP}	I_{CC} at V_S	Slew Rate	Input Offset Volts	Input Bias Current	Supply Voltage Range		Package P = Pins N = PDIP S = SOIC M = SOL
		Typ	Min	150Ω Loads	Max	Typ	Max	Max	Min	Max	
EL2072C	Closed Loop	730 MHz	50 mA	4	20 mA	800V/μs	8 mV	50 μA	±4.5V	±7V	8P-N-S
EL2002AC	Low Power Low Cost	180 MHz	100 mA	6	7.5 mA	2000V/μs	15 mV	10 μA	±4.5V	±18V	8P-N 20P-M
EL2003C EL2033C	Video	100 MHz	105 mA	6	15 mA	1200V/μs	40 mV	25 μA	±4.5V	±18V	8P-N 20P-M 8P-N
EL2009C	Power	90 MHz	1.4A	15	65 mA	3000V/μs	60 mV	125 μA	±4.5V	±18V	5P-TO220
EL2001AC	Low Power Low Cost	70 MHz	100 mA		2 mA	2000V/μs	10 mV	3 μA	±4.5V	±18V	8P-N 20P-M
EL2008C	Low Power Low Cost	55 MHz	1.4A	15	22 mA	2500V/μs	40 mV	35 μA	±4.5V	±18V	5P-TO220

*1 V_{PP} out on 75Ω Double Matched Loaded Line.

Power Distribution Amplifiers
Wide Bandwidth/Video/Distribution

Listed by decreasing bandwidth.

Part #	Features	Band-Width −3 dB	Output Current (Peak)	# of Loads * 2 V_{PP}	I_{CC} at ±15 V_S	Slew Rate	Input Offset Volts	Input Bias Current		Supply Voltage Range		Package P = Pins S = SOIC T = TO220
		Typ	Min	150Ω Loads	Max	Typ	Max	Max		Min	Max	
								+In	−In			
EL2009C	Buffer	90 MHz	1.4A	15	65 mA	3000V/μs	60 mV	125 μA	125 μA	±4.5V	±18V	5P-T
EL2008C	Buffer	55 MHz	1.4A	15	22 mA	2500V/μs	40 mV	35 μA	35 μA	±4.5V	±18V	5P-T
EL2099C	Gain Amp	50 MHz	600 mA	6	45 mA	1000V/μs	20 mV	15 μA	35 μA	±4.5V	±16.5V	5P-T
**EL1501C	Dual Driver/ Receiver	63 MHz	2 mA x 75 mA	8	45 mA	1000V/μs	30 mV	10 μA	10 μA	±4.5V	±16.5V	20P-S

*1 V_{PP} out on 75Ω Double Matched Loaded Line.

**For datasheet see Communications Section of Databook.

Instrumentation Wide Bandwidth/Video Amplifiers

Listed by increasing bandwidth.

Part #	Input Offset Volts	Input Bias I_B	Diff. Input Volts	Common Mode Range	Bandwidth −3 dB at Min Gain	Min Stable Gain	Slew Rate at Min Gain	Diff. Gain*	Diff. Phase*	I_{OUT} 10Ω Load	I_{CC} at ±15Vs	Supply Voltage Range		Package P = Pins N = PDIP S = SOIC
Up to ±15V	mV Max	μA Max	V Min	±V Min	MHz Typ	Av Min	V/μs Typ	% Typ	° Typ	mA Min	mA Max	V		
												Min	Max	
EL4431C	8	20	2	12	80	+2	380	0.02	0.02	40	16	±4.5	±16	8P-N-S
EL4430C	8	20	2	12	80	+1	380	0.04	0.08	40	16	±4.5	±16	8P-N-S
Up to ±5V											±5Vs			
EL2142C	−25 +40	20	2	2	150	+1	400	0.2	0.2	50	14	±3	±6	8P-N-N

*R_L = 500Ω for EL4431C, 150Ω for EL4430C, and 100Ω for EL2142C.

Multiplexing Video/Wide Bandwidth Amplifiers

Voltage Feedback Amplifiers listed by decreasing bandwidth.

Part #	Features	Mux Ratio and Gain		Input V_{OS}	Input Bias I_B	A_{VOL}	Bandwidth −3 dB	Slew Rate	Diff Gain	Diff Phase	Mux Delay Time	I_{OUT} 10Ω Load	I_{CC} at V_S	Supply Volts Range		Package P = Pins N = PDIP S = SOIC
Up to ±5V			A_V Min	mV Max	μS Max	V/V Typ	MHz Typ	V/μs Typ	% Typ	° Typ	ns Typ	mA Max	mA Max	V		
														Min	Max	
EL4332C	Triple	2:1	2*	20	30	—	300	650	0.04	0.08	3	30**	60	±5		16P-S
EL4331C	Triple	2:1	1*	25	30	—	300	425	0.04	0.08	3	30**	60	±5		16P-S
Up to ±15V																
EL4421C	Com −IN	2:1	+1	9	12	500	80	200	0.01	0.01	8	40	14	±3	±15	8P-N-S
EL4441C	Com −IN	4:1	+1	9	12	500	80	200	0.01	0.01	12	40	16	±3	±15	14P-N-S
EL4443C	Diff Input	4:1	+1	9	12	500	80	200	0.01	0.01	12	40	16	±3	±15	14P-N-S
EL4422C	Com −IN	2:1	+2	7	12	750	65	400	0.02	0.02	8	40	14	±3	±15	8P-N-S
EL4442C	Com −IN	4:1	+2	7	12	750	65	400	0.02	0.02	12	40	16	±3	±15	14P-N-S
EL4444C	Diff Input	4:1	+2	7	12	750	65	400	0.02	0.02	12	40	16	±3	±15	14P-N-S

*Internally Fixed Gain ** 75Ω Load

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2001C

Low Power, 70 MHz Buffer Amplifier

Features

- 1.3 mA supply current
- 70 MHz bandwidth
- 2000 V/μs slew rate
- Low bias current, 1 μA typical
- 100 mA output current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range ±5V to ±15V
- No thermal runaway

Applications

- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Low standby current systems

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2001ACN	0°C to +75°C	P-DIP	MDP0031
EL2001CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2001CN	0°C to +75°C	P-DIP	MDP0031

General Description

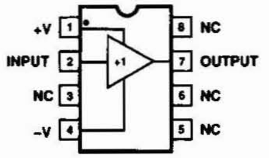
The EL2001 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic Complementary Bipolar process, this patented buffer has a −3 dB bandwidth of 70 MHz, and delivers 100 mA, yet draws only 1.3 mA of supply current. It typically operates from ±15V power supplies but will work with as little as ±5V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. A typical example is a general purpose op amp output current booster where the buffer must have sufficiently high bandwidth and low phase shift at the maximum frequency of the op amp.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagrams

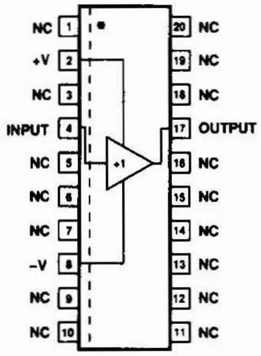
EL2001 DIP Pinout



2001-1

Top View

EL2001 SOL Pinout



2001-2

Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,833,424, 4,827,223 U.K. Patent No. 2217134

EL2001C

Low Power, 70 MHz Buffer Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage (V+ − V−)	±18V or 36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
P_D	Power Dissipation (Note 2)	See Curves
	Output Short Circuit Duration (Note 3)	Continuous

T_A	Operating Temperature Range EL2001AC/EL2001C	 0°C to +75°C
T_J	Operating Junction Temperature	150°C
T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			EL2001AC EL2001C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage EL2001A/EL2001AC	0	∞	25°C	−10	2	I	I	mV
				T_{MIN}, T_{MAX}	−15		+15	III	mV
	EL2001/EL2001C	0	∞	25°C	−30	2	+30	I	mV
				T_{MIN}, T_{MAX}	−40		+40	III	mV
I_{IN}	Input Current EL2001A/EL2001AC	0	∞	25°C	−3	1	+3	I	μA
				T_{MIN}, T_{MAX}	−6		+6	III	μA
	EL2001/EL2001C	0	∞	25°C	−5	1	+5	I	μA
				T_{MIN}, T_{MAX}	−10		+10	III	μA
R_{IN}	Input Resistance	±12V	100Ω	25°	1	8		I	MΩ
				T_{MIN}, T_{MAX}	0.5			III	MΩ

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			EL2001AC EL2001C	Units
		V_{in}	Load	Temp	Min	Typ	Max	Test Level	
A_{V1}	Voltage Gain	±12V	∞	25°C	0.990	0.998		I	V/V
				T_{MIN}, T_{MAX}	0.985			III	V/V
A_{V2}	Voltage Gain	±10V	100Ω	25°C	0.83	0.93		I	V/V
				T_{MIN}, T_{MAX}	0.80			III	V/V
A_{V3}	Voltage Gain with $V_S = \pm 5V$	±3V	100Ω	25°C	0.82	0.89		I	V/V
				T_{MIN}, T_{MAX}	0.79			III	V/V
V_O	Output Voltage Swing	±12V	100Ω	25°C	±10	±11		I	V
				T_{MIN}, T_{MAX}	±9.5			III	V
R_{OUT}	Output Resistance	±2V	100Ω	25°C		10	15	I	Ω
				T_{MIN}, T_{MAX}			18	III	Ω
I_{OUT}	Output Current	±12V	(Note 4)	25°C	±100	±160		I	mA
				T_{MIN}, T_{MAX}	±95			III	mA
I_S	Supply Current	0	∞	25°C		1.3	2.0	I	mA
				T_{MIN}, T_{MAX}			2.5	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	75		I	dB
				T_{MIN}, T_{MAX}	50			III	dB
t_r	Rise Time	0.5V	100Ω	25°C		4.2		V	ns
t_d	Propagation Delay	0.5V	100Ω	25°C		2.0		V	ns
SR	Slew Rate, (Note 6)	±10V	100Ω	25°C	1200	2000		IV	V/μs

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

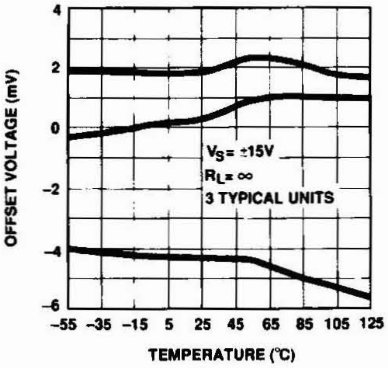
Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12 V_{IN} and −10V on the output.

Note 5: V_{OS} is measured at $V_S+ = +4.5V$, $V_S- = -4.5V$ and at $V_S+ = +18V$, $V_S- = -18V$. Both supplies are changed simultaneously.

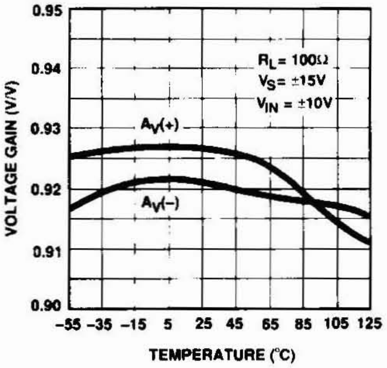
Note 6: Slew rate is measured between $V_{OUT} = +5V$ and $-5V$.

Typical Performance Curves

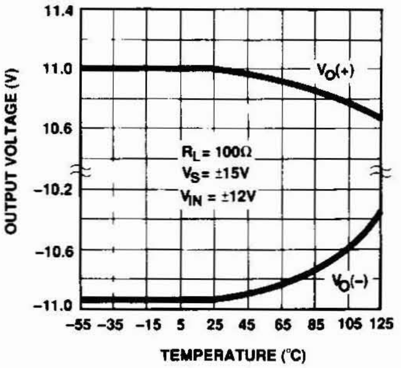
Offset Voltage
vs Temperature



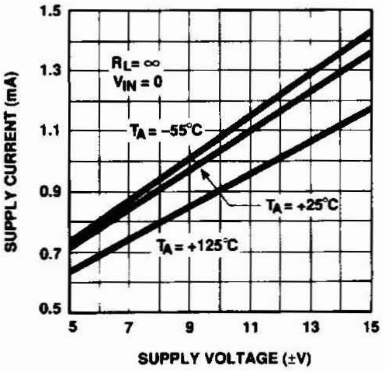
Voltage Gain
vs Temperature



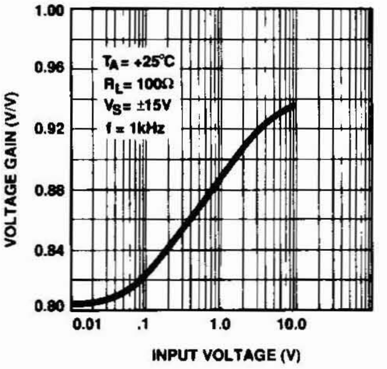
Output Voltage Swing
vs Temperature



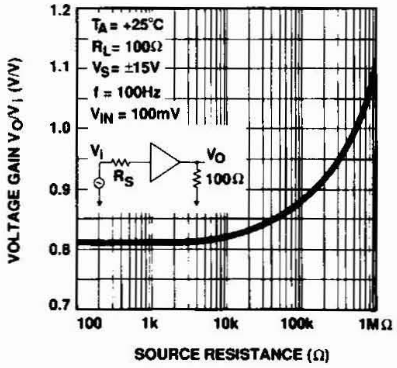
Supply Current
vs Supply Voltage



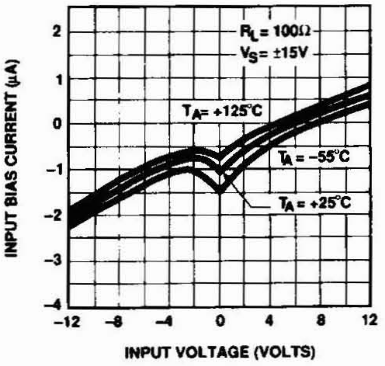
Voltage Gain
vs Input Voltage



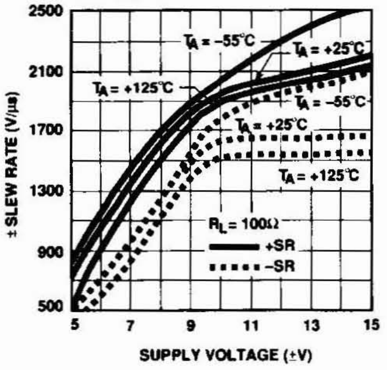
Voltage Gain
vs Source Resistance



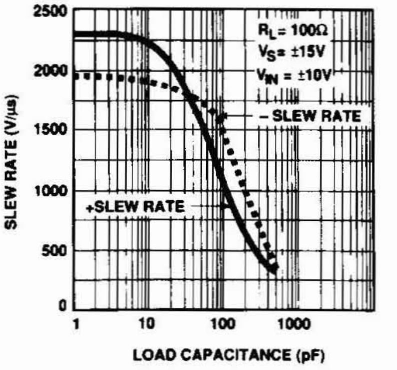
Input Bias Current
vs Input Voltage



± Slew Rate
vs Supply Voltage



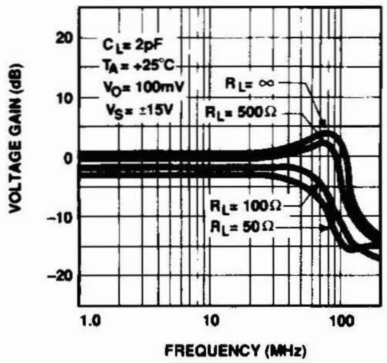
± Slew Rate
vs Capacitive Load



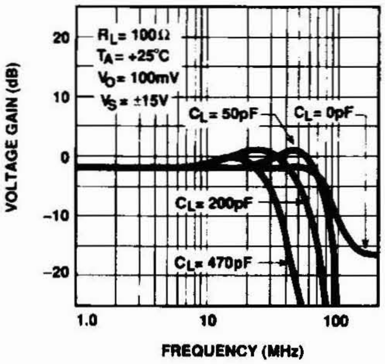
2001-4

Typical Performance Curves — Contd.

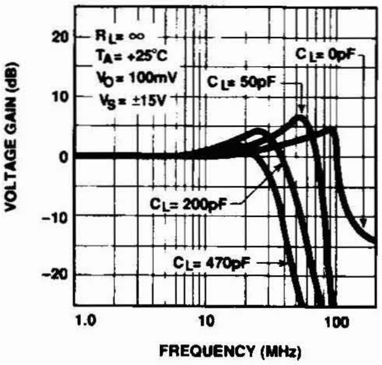
Voltage Gain vs Frequency for Various Resistive Loads



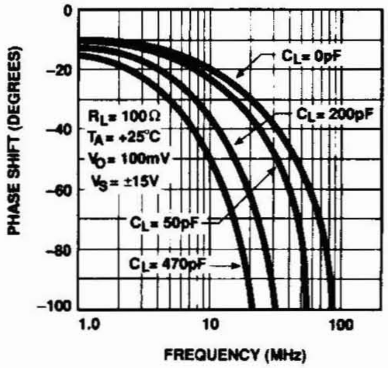
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = 100Ω



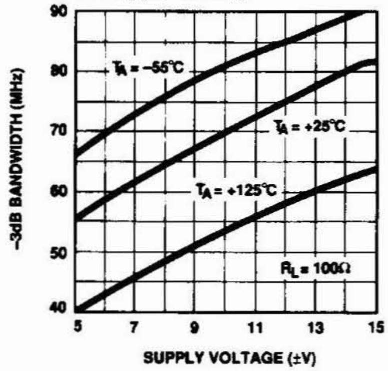
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = ∞



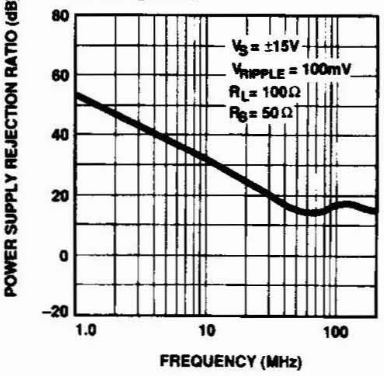
Phase Shift vs Frequency for Various Capacitive Loads



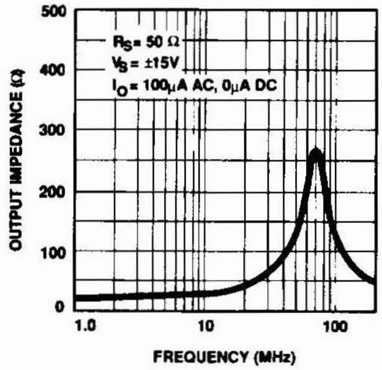
−3 dB Bandwidth vs Supply Voltage



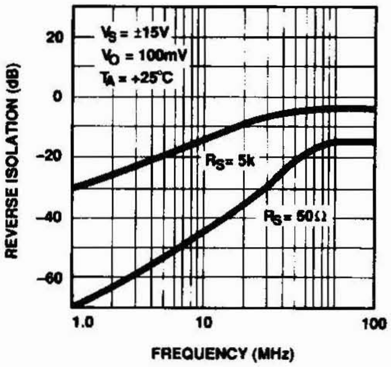
Power Supply Rejection Ratio vs Frequency



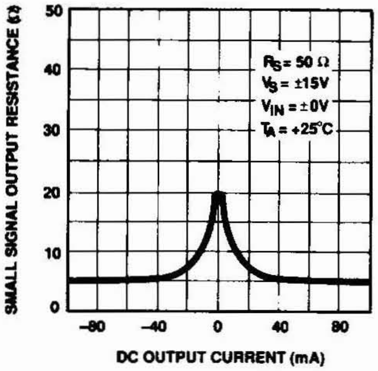
Output Impedance vs Frequency



Reverse Isolation vs Frequency



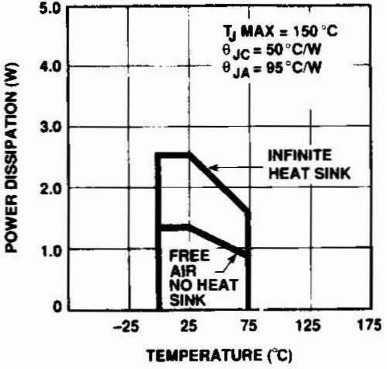
Small Signal Output Resistance vs Output Current



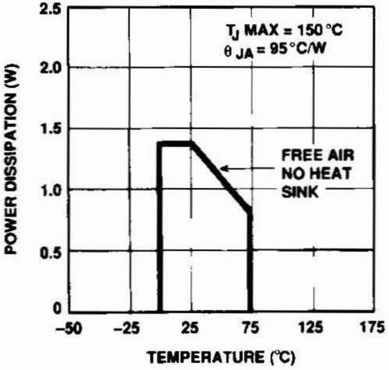
2001-5

Typical Performance Curves — Contd.

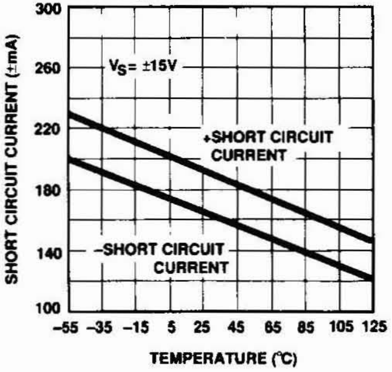
8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature

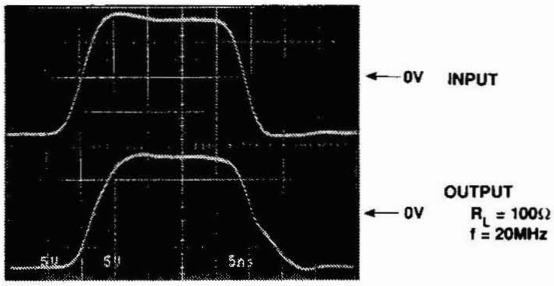


Short Circuit Current
vs Temperature



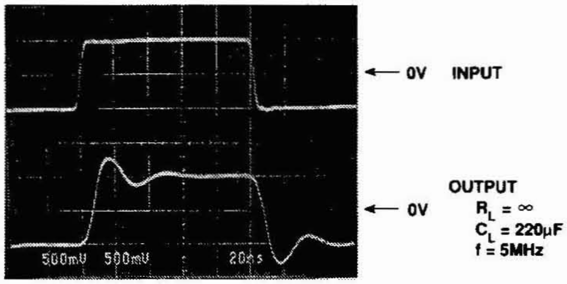
2001-6

Large Signal Response



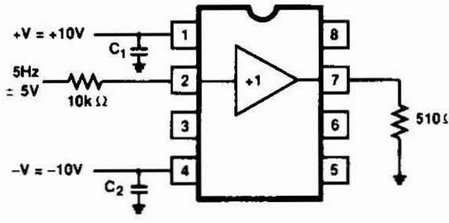
2001-7

Small Signal Response



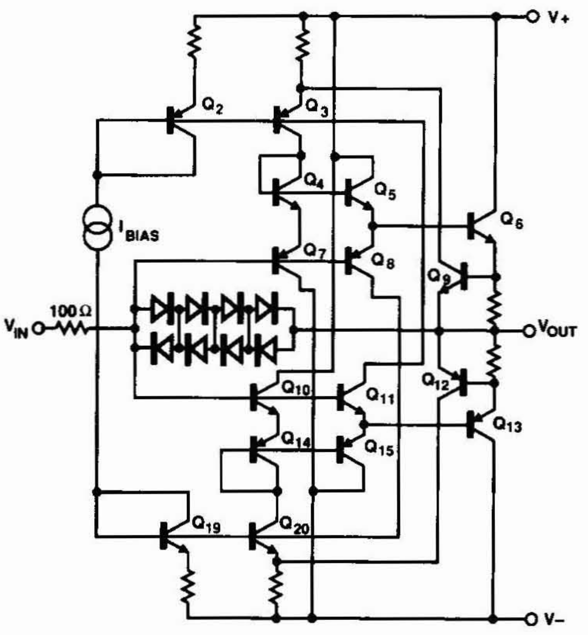
2001-8

Burn-In Circuit



2001-9

Simplified Schematic



2001-10

Application Information

The EL2001 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2001 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2001's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/μs slew rates with 100Ω loads possible with very low supply current.

Power Supplies

The EL2001 may be operated with single or split supplies with total voltage difference between 10V (±5V) and 36V (±18V). It is not necessary to use equal split value supplies. For example −5V and +12V would be excellent for signals from −2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 μF tantalum capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2001 looks like a resistance in parallel with about 3.5 picofarads in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. There is also 100Ω in series with the input that limits input current. Above ±7.5V differential input to output, additional series resistance should be added.

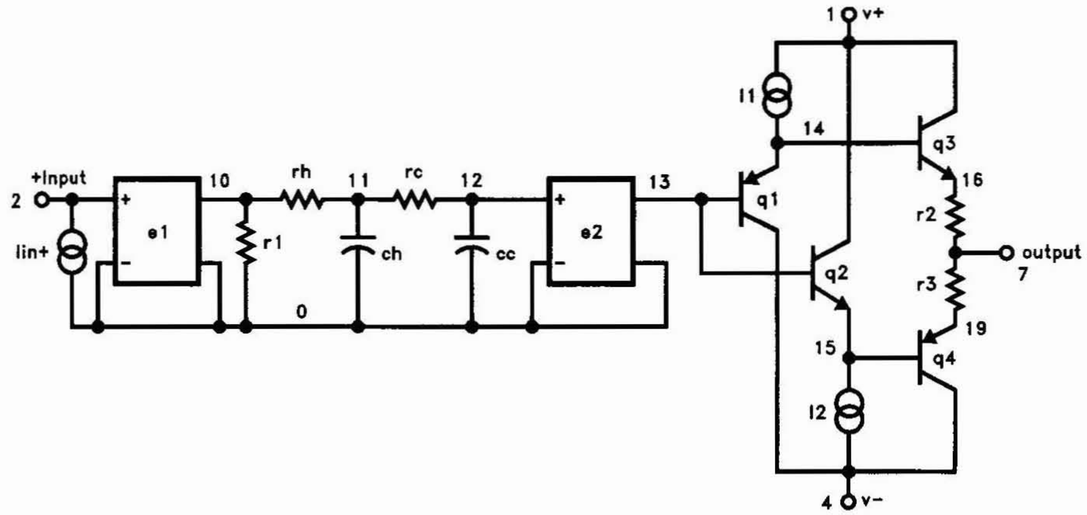
Source Impedance

The EL2001 has good input to output isolation. When the buffer is not used in a feedback loop, capacitive and resistive sources up to 1 Meg present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances (R_S > 100 kΩ), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

EL2001C Macromodel

```
*Connections:    +input
*                 |      +Vsupply
*                 |       |      -Vsupply
*                 |       |       |      output
*                 |       |       |       |
.subckt M2001     2       1       4       7
* Input Stage
e1 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 9pF
rc 11 12 100
cc 12 0 4pF
e2 13 0 12 0 1.0
* Output stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 1
r3 19 7 1
i1 1 14 0.9mA
i2 15 4 0.9mA
* Bias Current
iin+ 2 0 1uA
* Models
.model qn npn(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.model qp pnp(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.ends
```

EL2001C Macromodel — Contd.


1
v+
I1
14
q3
+Input
2
Iin+
+
−
e1
10
r1
rh
11
ch
rc
12
cc
0
+
−
e2
13
q1
q2
16
r2
output
7
r3
19
15
q4
I2
4
v−

2001-11

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2002C
Low Power, 180 MHz Buffer Amplifier

Features
- 180 MHz bandwidth
- 2000 V/μs slew rate
- Low bias current, 3 μA typical
- 100 mA output current
- 5 mA supply current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range ±5V to ±15V
- No thermal runaway

Applications
- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Isolation buffer

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2002ACN	0°C to +75°C	P-DIP	MDP0031
EL2002CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2002CN	0°C to +75°C	P-DIP	MDP0031

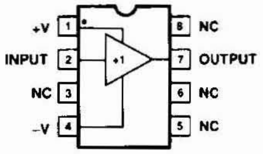
General Description
The EL2002 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic Complementary Bipolar process, this patented buffer has a −3 dB bandwidth of 180 MHz, and delivers 100 mA, yet draws only 5 mA of supply current. It typically operates from ±15V power supplies but will work with as little as ±5V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. Typical examples include fast op-amp output current boosters, coaxial cable drivers and A/D converter input buffers.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

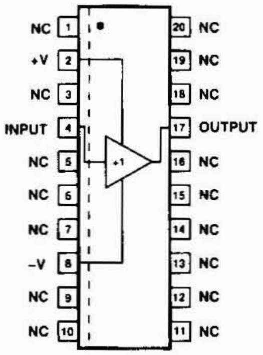
Connection Diagrams

EL2002 DIP Pinout



Top View

EL2002 SOL Pinout



Top View

Manufactured Under U.S. Patent No. 4,833,424 and U.K. Patent No. 2217134.

December 1995 Rev D

EL2002C

Low Power, 180 MHz Buffer Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage ($V^+ - V^-$)	±18V or 36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
P_D	Power Dissipation (Note 2)	See Curves
	Output Short Circuit Duration (Note 3)	Continuous
T_A	Operating Temperature Range: EL2002AC/EL2002C	0°C to +75°C
T_J	Operating Junction Temperature	150°C
T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

Electrical Characteristics $V_S = \pm15V$, $R_S = 50\Omega$, unless otherwise specified

Parameter	Description	Test Conditions			Limits			EL2002AC EL2002C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage EL2002A/EL2002AC	0	∞	25°C	−15	5	+15	I	mV
				T_{MIN}, T_{MAX}	−20		+20	III	mV
	EL2002/EL2002C	0	∞	25°C	−40	10	+40	I	mV
				T_{MIN}, T_{MAX}	−50		+50	III	mV
I_{IN}	Input Current EL2002A/EL2002AC	0	∞	25°C	−10	3	+10	I	μA
				T_{MIN}, T_{MAX}	−15		+15	III	μA
	EL2002/EL2002C	0	∞	25°C	−15	5	+15	I	μA
				T_{MIN}, T_{MAX}	−20		+20	III	μA
R_{IN}	Input Resistance	+12V	100Ω	25°C	1	3		I	MΩ
				T_{MIN}, T_{MAX}	0.1			III	MΩ
A_{V1}	Voltage Gain	±12V	∞	25°C	0.990	0.998		I	V/V
				T_{MIN}, T_{MAX}	0.985			III	V/V
A_{V2}	Voltage Gain	±10V	100Ω	25°C	0.85	0.93		I	V/V
				T_{MIN}, T_{MAX}	0.83			III	V/V

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			EL2002AC EL2002C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	
A_{V3}	Voltage Gain with $V_S = \pm 5V$	±3V	100Ω	25°C	0.83	0.91		I	V/V
				T_{MIN}, T_{MAX}	0.80			III	V/V
V_O	Output Voltage Swing	±12V	100Ω	25°C	±10	±11		I	V
				T_{MIN}, T_{MAX}	±9.5			III	V
R_{OUT}	Output Resistance	±2V	100Ω	25°C		8	13	I	Ω
				T_{MIN}, T_{MAX}			15	III	Ω
I_{OUT}	Output Current	±12V	(Note 4)	25°C	+100	+160		I	mA
				T_{MIN}, T_{MAX}	±95			III	mA
I_S	Supply Current	0	∞	25°C		5	7.5	II	mA
				T_{MIN}, T_{MAX}			10	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	75		I	dB
				T_{MIN}, T_{MAX}	50			III	dB
t_r	Rise Time	0.5V	100Ω	25°C		2.8		V	ns
t_d	Propagation Delay	0.5V	100Ω	25°C		1.5		V	ns
SR	Slew Rate, (Note 6)	±10V	100Ω	25°C	1200	2000		IV	V/μs

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

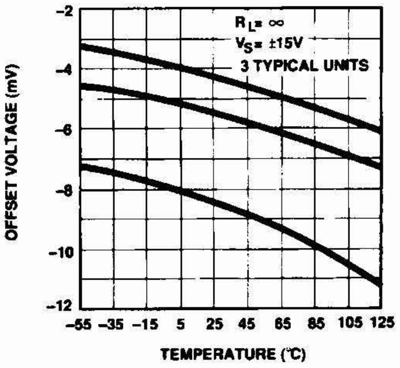
Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12 V_{IN} and −10V on the output.

Note 5: V_{OS} is measured at $V_S+ = +4.5V$, $V_S- = -4.5V$ and $V_S+ = +18V$, $V_S- = 18V$. Both supplies are changed simultaneously.

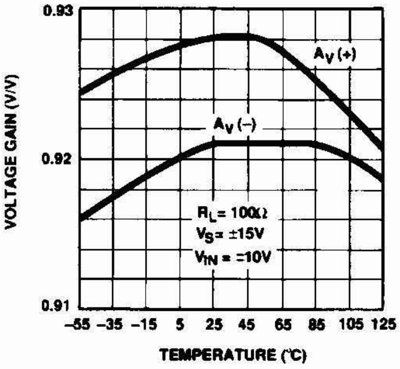
Note 6: Slew rate is measured between $V_{OUT} = +5V$ and $-5V$.

Typical Performance Curves

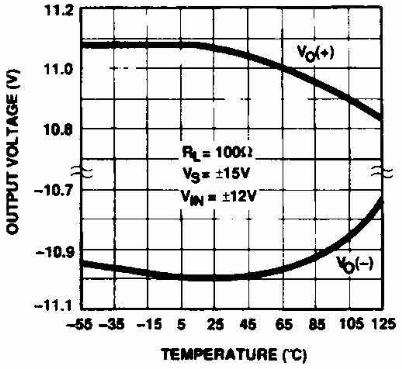
Offset Voltage vs Temperature



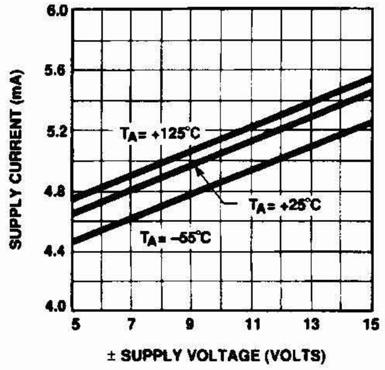
Voltage Gain vs Temperature



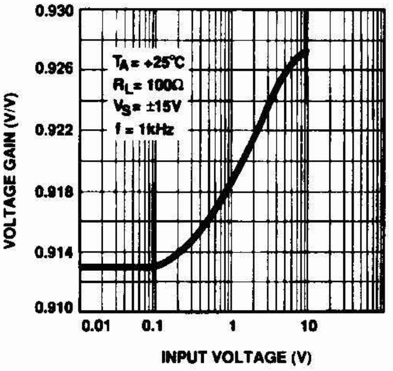
Output Voltage Swing vs Temperature



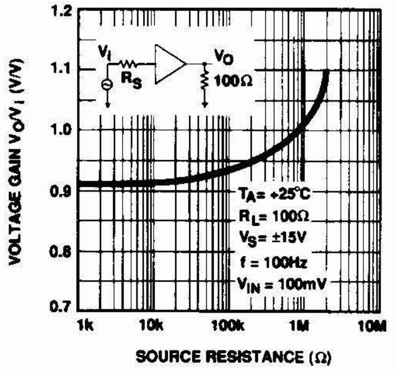
Supply Current vs Supply Voltage



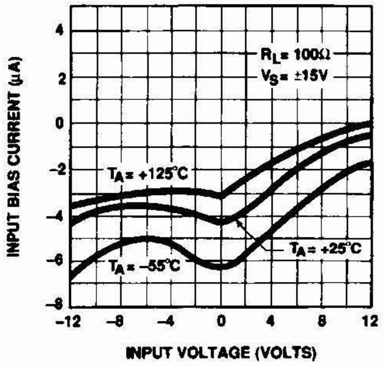
Voltage Gain vs Input Voltage



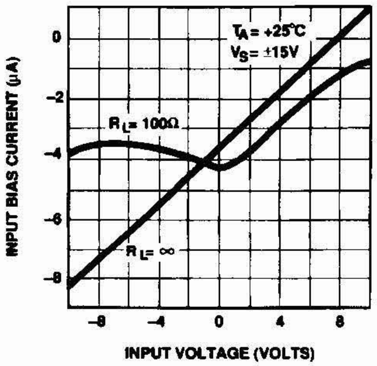
Voltage Gain vs Source Resistance



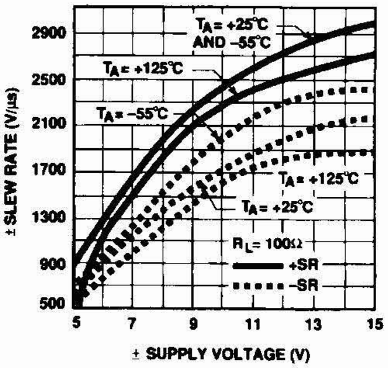
Input Bias Current vs Input Voltage at Various Temperatures



Input Bias Current vs Input Voltage



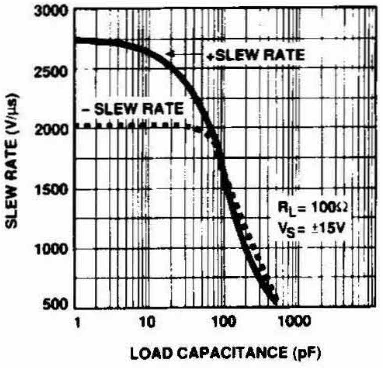
±Slew Rate vs Supply Voltage



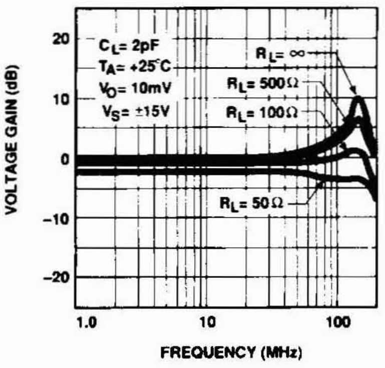
2002-4

Typical Performance Curves — Contd.

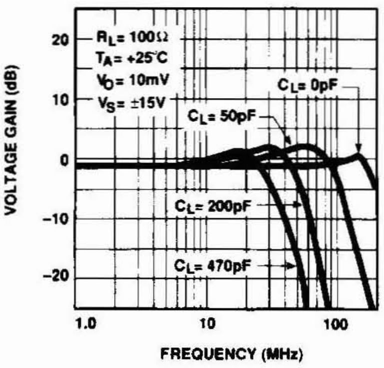
Slew Rate vs Load Capacitance



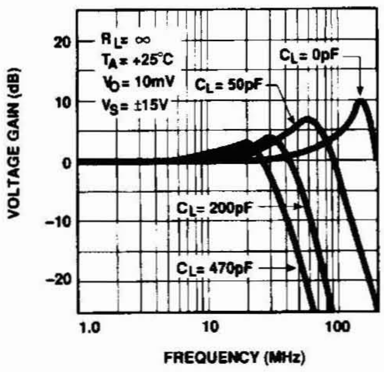
Voltage Gain vs Frequency for Various Resistive Loads



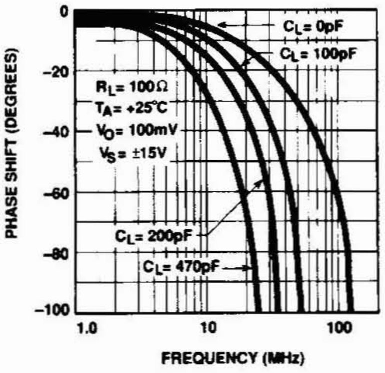
Voltage Gain vs Frequency for Various Capacitive Loads; $R_L = 100\Omega$



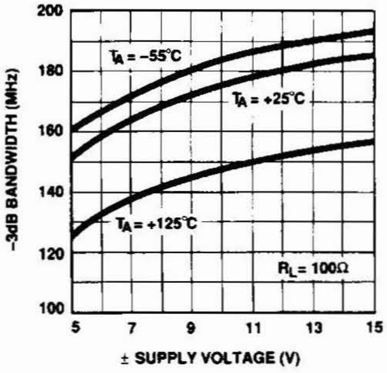
Voltage Gain vs Frequency for Various Capacitive Loads; $R_L = \infty$



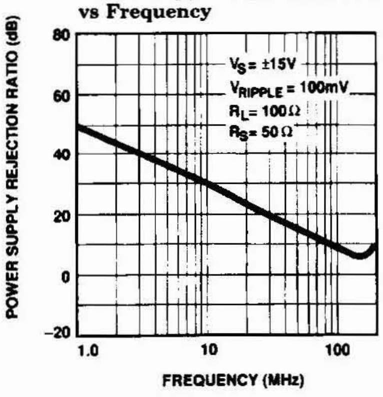
Phase Shift vs Frequency for Various Capacitive Loads



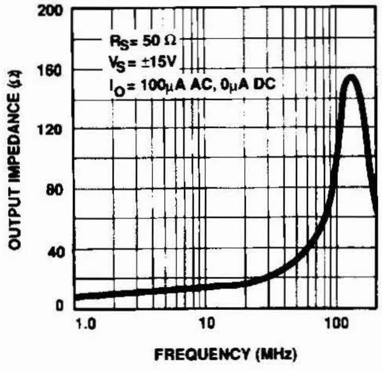
−3 dB Bandwidth vs Supply Voltage



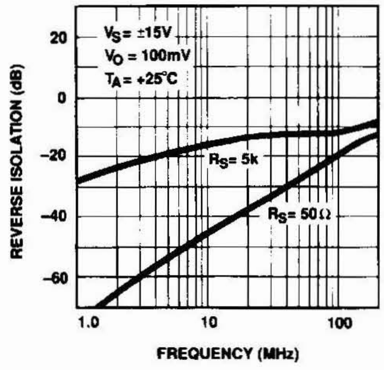
Power Supply Rejection Ratio vs Frequency



Output Impedance vs Frequency



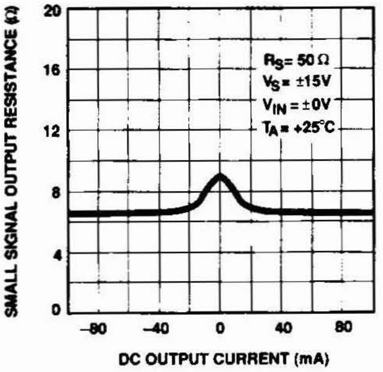
Reverse Isolation vs Frequency



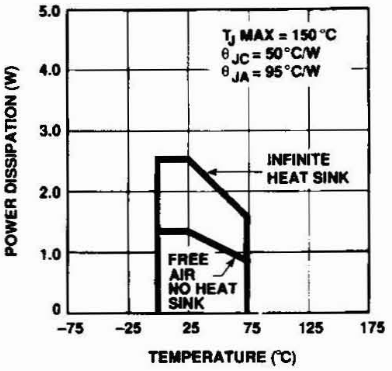
2002-5

Typical Performance Curves — Contd.

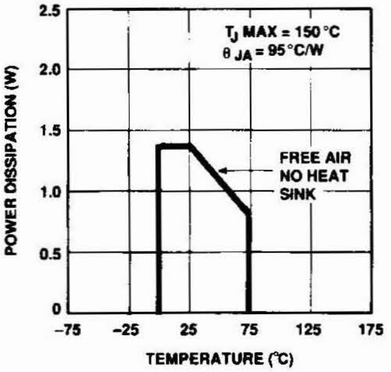
Small Signal Output Resistance vs Output Current



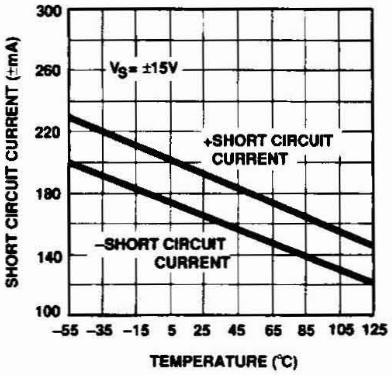
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



Short Circuit Current vs Temperature



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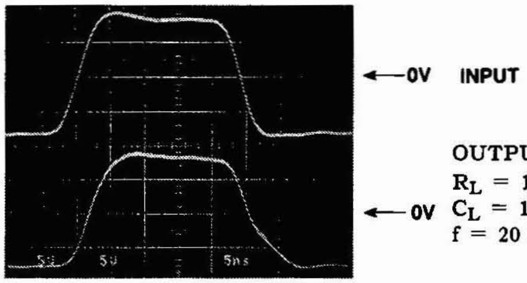
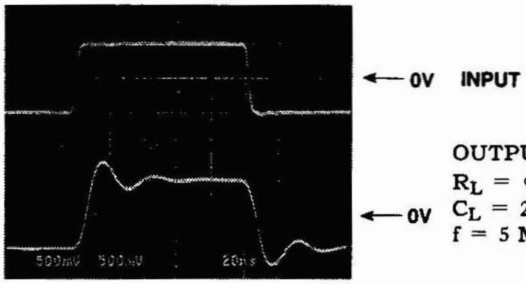
Large Signal Response



OUTPUT
R_L = 100Ω
C_L = 10 pF
f = 20 MHz

2002-8

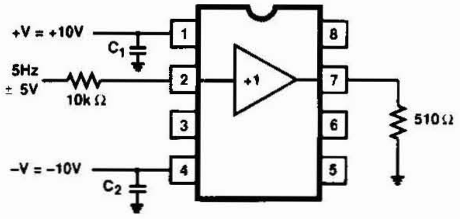
Small Signal Response



OUTPUT
R_L = ∞
C_L = 220 pF
f = 5 MHz

2002-9

Burn-In Circuit



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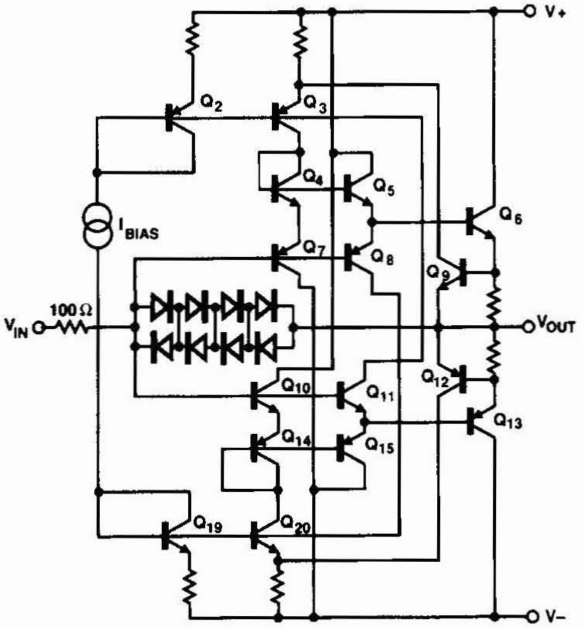
Simplified Schematic



2002-11

Application Information

The EL2002 is a monolithic buffer amplifier built on Elantec's proprietary Complementary Bipolar process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2002 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2002's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/μs slew rates with 100Ω loads possible with very low supply current.

Power Supplies

The EL2002 may be operated with single or split supplies with total voltage difference between 10V (±5V) and 36V (±18V). It is not necessary to use equal split value supplies. For example −5V and +12V would be excellent for signals from −2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 μF tantalum capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2002 looks like a resistance in parallel with about 3.5 pF in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. There is also 100Ω in series with the input that limits input current. Above ±7.5V differential input to output, additional series resistance should be added.

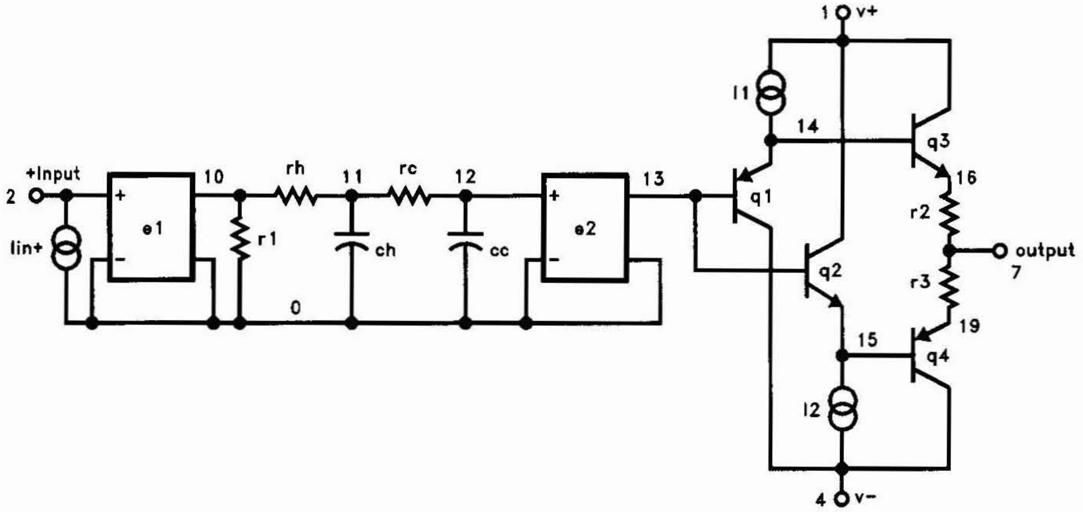
Source Impedance

The EL2002 has good input to output isolation. When the buffer is not used in a feedback loop, capacitive and resisitive sources up to 1 MHz present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances ($R_S > 100$ kΩ), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

EL2002 Macromodel

```
* Connections:   +input
*                 |       +Vsupply
*                 |        |       -Vsupply
*                 |        |        |       output
*                 |        |        |        |
.subckt M2002     2        1        4        7
* Input Stage
e1 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 2pF
rc 11 12 100
cc 12 0 3pF
e2 13 0 12 0 1.0
* Output Stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 1
r3 19 7 1
i1 1 14 2mA
i2 15 4 2mA
* Bias Current
iin+ 2 0 3uA
* Models
.model qn npn(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.model qp pnp(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.ends
```

EL2002 Macromodel — Contd.


1
v+
I1
14
q3
16
+Input
2
Iin+
e1
10
rh
11
rc
12
r1
ch
cc
0
e2
13
q1
q2
r2
output
7
r3
19
15
q4
I2
4
v−

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EL2003C/EL2033C
100 MHz Video Line Driver

Features

- Differential gain 0.1%
- Differential phase 0.1°
- 100 mA continuous output current guaranteed
- Short circuit protected
- Wide bandwidth—100 MHz
- High slew rate—1200 V/μs
- High input impedance—2 MΩ
- Low quiescent current drain
- EL2003—Pin compatible with LH0002CN, LH0002H, HA2-5002
- EL2033—Pin compatible with HA3-5002, HA7-5002, HA3-5033, HA7-5033

Applications

- Co-ax cable driver
- Flash converter driver
- Video DAC buffer
- Op amp booster

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL2003CN	0°C to +75°C	P-DIP	MDP0031
EL2003CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2033CN	0°C to +75°C	P-DIP	MDP0031

General Description

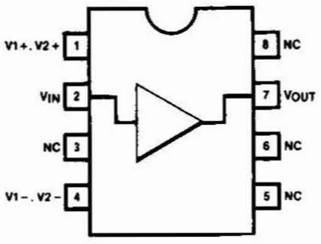
The EL2003/EL2033 are general purpose monolithic unity gain buffers featuring 100 MHz, −3 dB bandwidth and 4 ns small signal rise time. These buffers are capable of delivering a ±100 mA current to a resistive load and are oscillation free into capacitive loads. In addition, the EL2003/EL2033 have internal output short circuit current limiting which will protect the devices under both a DC fault condition and AC operation with reactive loads. The extremely fast slew rate of 1200 V/μs, wide bandwidth, and high output drive make the EL2003/EL2033 ideal choices for closed loop buffer applications with wide band op amps. These same characteristics and excellent DC performance make the EL2003/EL2033 excellent choices for open loop applications such as driving coaxial and twisted pair cables.

The EL2003/EL2033 are constructed using Elantec's proprietary dielectric isolation process that produces PNP and NPN transistors with essentially identical AC and DC characteristics.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, request our brochure: QRA-1: *Elantec's Processing—Monolithic Products.*

Connection Diagrams

EL2003CN



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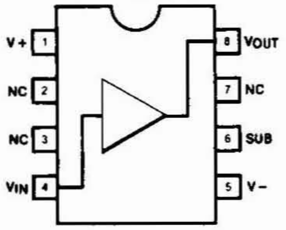
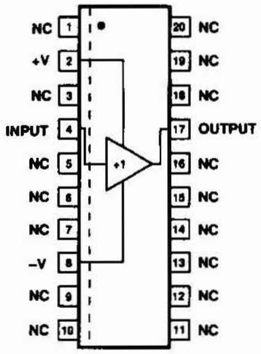
EL2033CN



2003-2

EL2003CM



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January 1996 Rev D

EL2003C/EL2033C

100 MHz Video Line Driver

Absolute Maximum Ratings

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage (Note 1)	±15V or V_S		EL2003C/2033C	0°C to +75°C
I_{IN}	Input Current (Note 1)	±50 mA	T_J	Operating Junction Temperature	
P_D	Power Dissipation (Note 2)	See Curves		Metal Can	175°C
	Output Short Circuit			Plastic	150°C
	Duration (Note 3)	Continuous	T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max	2003C 2033C	
V_{OS}	Output Offset Voltage	0	∞	25°C	−40	5	40	I	mV
				T_{MIN}, T_{MAX}	−50		50	III	mV
I_{IN}	Input Current	0	∞	25°C, T_{MAX}	−25	−5	25	II	μA
				T_{MIN}	−50		50	III	μA
R_{IN}	Input Resistance	±12V	100Ω	25°C, T_{MAX}	0.5	2		II	MΩ
				T_{MIN}	0.05			III	MΩ
A_{V1}	Voltage Gain	±12V	1 kΩ	25°C	0.98	0.99		I	V/V
				T_{MIN}, T_{MAX}	0.97			III	V/V
A_{V2}	Voltage Gain	±6V	50Ω	25°C	0.83	0.90		I	V/V
				T_{MIN}, T_{MAX}	0.80			III	V/V
A_{V3}	Voltage Gain with V_S = ±5V	±3V	50Ω	25°C	0.82	0.89		I	V/V
				T_{MIN}, T_{MAX}	0.79			III	V/V
V_{01}	Output Voltage Swing	±14V	1 kΩ	25°C	±13	±13.5		I	V
				T_{MIN}, T_{MAX}	±12.5			III	V
V_{02}	Output Voltage Swing	±12V	100Ω	25°C	±10.5	±11.3		I	V
				T_{MIN}, T_{MAX}	±10			III	V

Electrical Characteristics V_S = ±15V, R_S = 50Ω — Contd.

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max	2003C 2033C	
R_{OUT}	Output Resistance	±2V	50Ω	25°C		7	10	I	Ω
				T_{MIN}, T_{MAX}			12	III	Ω
I_{OUT}	Output Current	±12V	(Note 4)	25°C	±105	±230		I	mA
				T_{MIN}, T_{MAX}	±100			III	mA
I_S	Supply Current	0	∞	25°C, T_{MAX}		10	15	II	mA
				T_{MIN}			20	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	80		I	dB
				T_{MIN}, T_{MAX}	50			III	dB
SR1	Slew Rate, (Note 6)	±10V	1 kΩ	25°C	600	1200		I	V/µs
SR2	Slew Rate, (Note 7)	±5V	50Ω	25°C	200	400		I	V/µs
THD	Distortion @ 1 kHz	4 V_{rms}	50Ω	25°C		0.2	1	IV	%

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V in and −10V on the output.

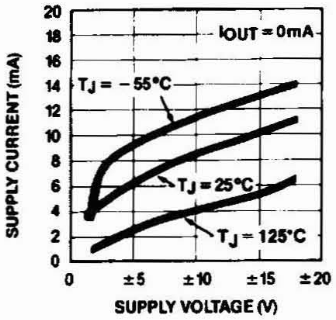
Note 5: V_S = ±4.5V to ±18V.

Note 6: Slew rate is measured between V_{OUT} = +5V and −5V.

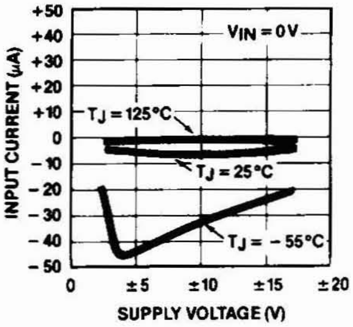
Note 7: Slew rate is measured between V_{OUT} = +2.5V and −2.5V.

Typical Performance Curves

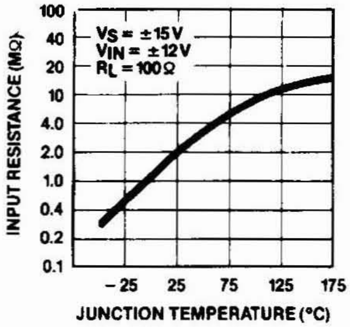
Quiescent Supply Current vs Supply Voltage



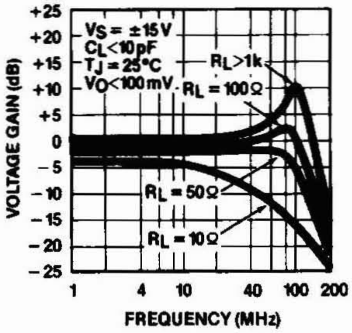
Input Current vs Supply Voltage



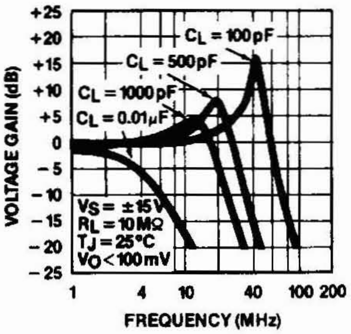
Input Resistance vs Temperature



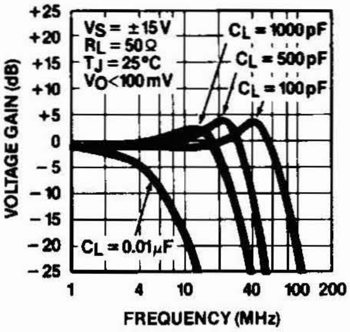
Voltage Gain vs Frequency Various Resistive Loads



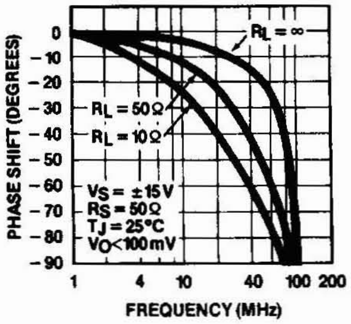
Voltage Gain vs Frequency No Resistive Load Various Capacitive Loads



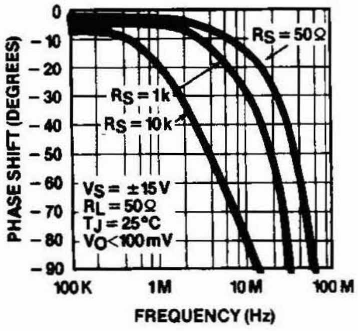
Voltage Gain vs Frequency 50Ω Resistive Load Various Capacitive Loads



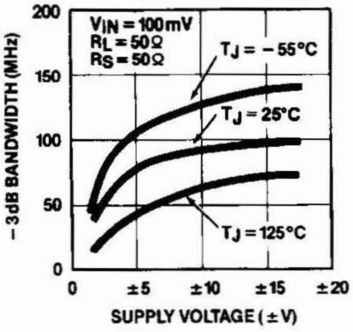
Phase Shift vs Frequency Various Resistive Loads



Phase Shift vs Frequency Various Source Resistors



−3 dB Bandwidth vs Supply Voltage



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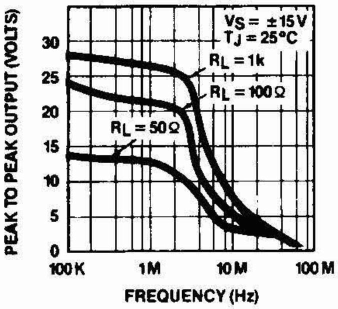
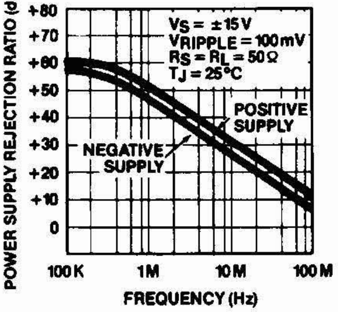
Typical Performance Curves — Contd.

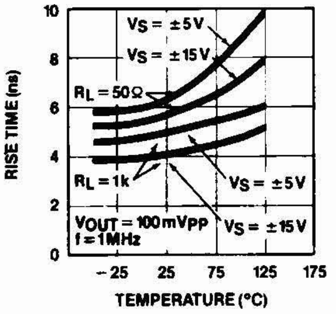
Maximum Undistorted Output Voltage vs Frequency



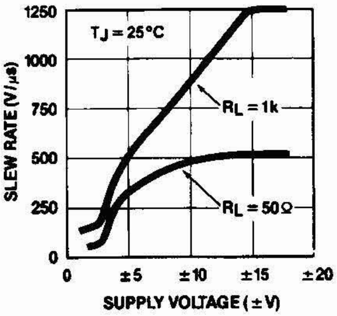
Power Supply Rejection Ratio vs Frequency



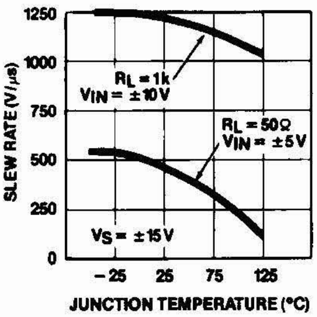
Rise Time vs Temperature



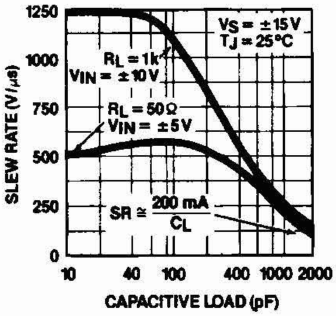
Slew Rate vs Supply Voltage



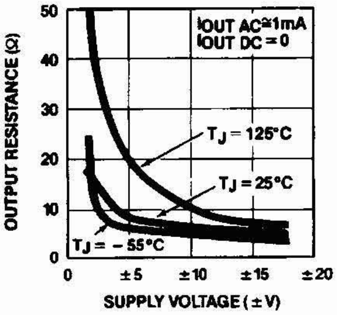
Slew Rate vs Temperature



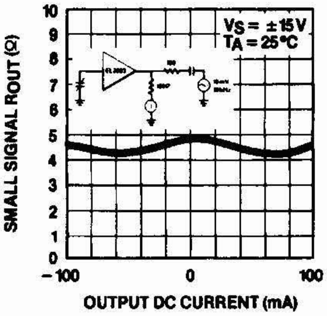
Slew Rate vs Capacitive Load



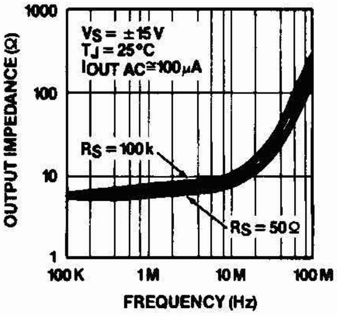
Output Resistance vs Supply Voltage



Small Signal Output Resistance vs DC Output Current



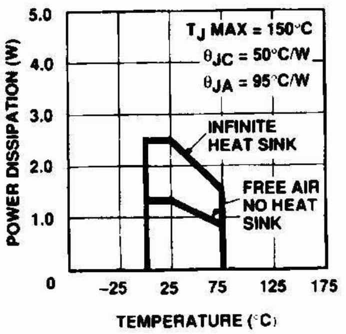
Output Impedance vs Frequency



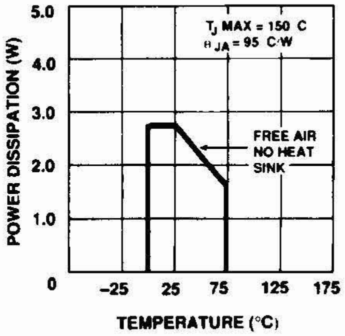
2003-7

Typical Performance Curves — Contd.

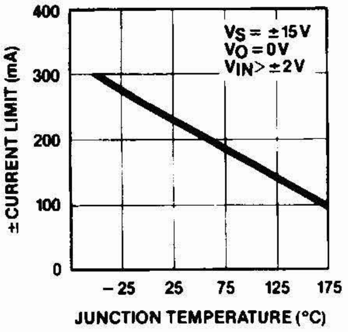
8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



Current Limit
vs Temperature



2003-8

Applications Hints

The EL2003/EL2033 are monolithic buffer amplifiers built with Elantec's proprietary dielectric isolation process that produces NPN and PNP complimentary transistors. The circuits are connection of symmetrical common collector transistors that provide both sink and source current capability independent of output voltage while maintaining constant output and input impedances. The high slew rate and wide bandwidth of the EL2003 and EL2033 make them useful beyond video frequencies.

Power Supplies

The EL2003/EL2033 may be operated with single or split supplies as low as ±2.5V (5V total) to as high as ±18V (36V total). However, the bandwidth, slew rate and output impedance degrade significantly for supply voltages less than ±5V (10V total) as shown in the characteristic curves. It is not necessary to use equal value split supplies, for example −5V and +12V would be excellent for 0V to 1V video signals.

Bypass capacitors from each supply pin to a ground plane are recommended. The EL2003/EL2033 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate a supply ringing and the interference it can cause, a 10 μF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rates and longer settling times.

The EL2003 metal can package has the collectors of the output transistors brought out separately from the input supplies for pin compatibility with the ELH0002H. If the collectors operate on lower supplies than the input stage, the internal power dissipation can be reduced. However, the output transistors can be driven into hard saturation when the input voltage exceeds the collector supply voltage. The recovery time to come out of saturation will be 2 μs or 3 μs and the output may oscillate during this recovery period.

Input Range

The input to the EL2003/EL2033 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit. However, there are clamp diodes from the input to the output that protect the transistor base emitter junctions. These diodes start to conduct at about ±9.5V input to output differential voltage. Of course the input resistance drops dramatically when the diodes start conducting; the diodes are rated at ±50 mA.

The input characteristics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However, if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

Source Impedance

The EL2003/EL2033 have excellent input-output isolation and are very tolerant of variations in source impedances. Capacitive sources cause no problems at all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources can cause oscillations; a 1 kΩ resistor in series with the buffer input lead will usually eliminate problems without sacrificing too much speed. An unterminated cable or other resonant source can also cause oscillations. Again, an isolating resistor will eliminate the problem.

Current Limit

The EL2003/EL2033 have internal current limits that protect the output transistors. The current limit goes down with junction temperature rise as shown in the characteristic curves. At a junction temperature of +175°C the current limits are at about 100 mA. If the EL2003 or EL2033 output is shorted to ground when operating on ±15V supplies, the power dissipation will be greater than 1.5W. A heat sink is required in order for the EL2003 or EL2033 to survive an indefinite short. Recovery time to come out of current limit is about 250 ns.

Applications Hints — Contd.

Heat Sinking

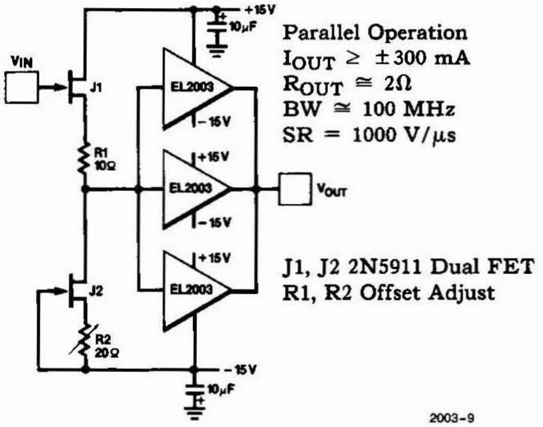
When operating the EL2003/EL2033 in elevated ambient temperatures and/or high supply voltages and low impedance loads, the internal power dissipation can force the junction temperature above the maximum rating (175°C for the metal can package and 150°C for the plastic DIP). Also, an indefinite short of the output to ground will cause excessive power dissipation.

The thermal resistance junction to case is 55°C per Watt for the metal can package and 50°C/W for the plastic DIP. A suitable heat sink will increase the power dissipation capability significantly beyond that of the package alone. Several companies make standard heat sinks for both packages. Aavid and Thermalloy heat sinks have been used successfully.

Parallel Operation

If more than 100 mA output is required or if heat management is a problem, several EL2003s or EL2033s may be paralleled together. The result is as though each device was driving only part of the load. For example, if two units are paralleled then a 50Ω load looks like 100Ω to each EL2003. Parallel operation results in lower input and output impedances, increased bias current but no increase in offset voltage. An example showing three EL2003s in parallel and also the addition of a FET input buffer stage is shown below. By using a dual FET the circuit complexity is minimal and the performance is excellent. Take care to minimize the stray capacitance at the input of the EL2003s for maximum slew rate and bandwidth.

FET Input Buffer with High Output Currents



Parallel Operation
$I_{OUT} \geq \pm 300$ mA
$R_{OUT} \cong 2\Omega$
BW ≅ 100 MHz
SR = 1000 V/μs

J1, J2 2N5911 Dual FET
R1, R2 Offset Adjust

2003-9

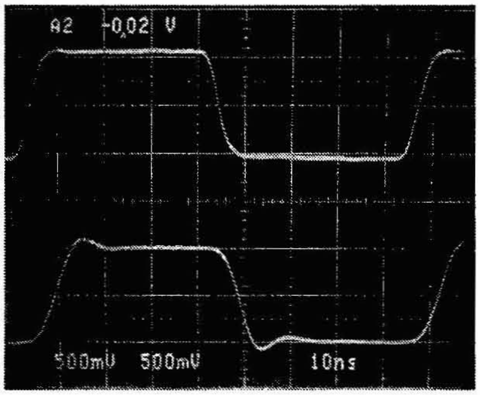
Resistive Loads

The DC gain of the EL2003/EL2033 is the product of the unloaded gain (0.995) and the voltage divider formed by the device output resistance and the load resistance.

$$A_V = 0.995 * R_L/(R_L + R_{OUT})$$

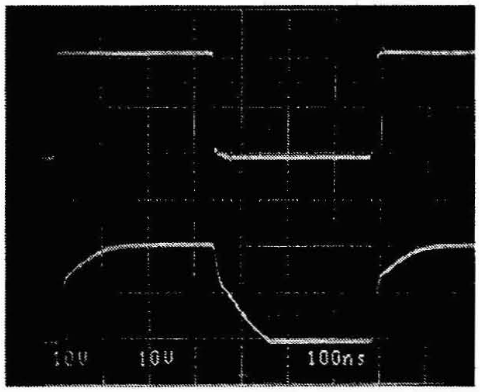
The high frequency response of the EL2003/EL2033 varies with the value of the load resistance as shown in the characteristic curves. If the 100 MHz peaking is undesirable when driving load resistors greater than 50Ω, an RC snubber circuit can be used from the output to ground. The snubber circuit works by presenting a high frequency load resistance of less than 50Ω while having no loading effect at low frequencies.

Small Signal Response



$R_L = 50\Omega$, $C_L = 10$ pF, $V_S = \pm 15V$ 2003-10
Top is V_{IN}, Bottom is V_{OUT}

Large Signal Response



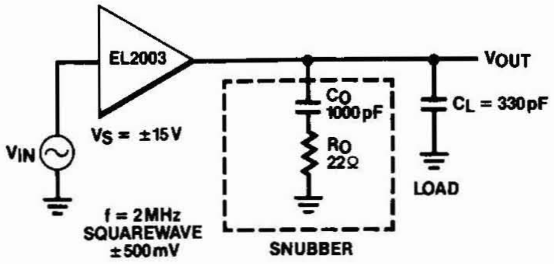
$R_L = 100\Omega$, $C_L = 10$ pF, $V_S = \pm 15V$ 2003-11
Top is V_{IN}, Bottom is V_{OUT}

Applications Hints — Contd.

Capacitive Loads

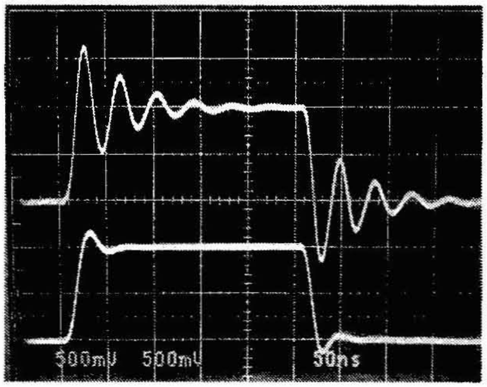
The EL2003/EL2033 are stable driving any type of capacitive load. However, when driving a pure capacitance of less than a thousand picofarads the frequency response has excessive peaking as shown in the characteristic curves. The squarewave response will have large overshoots and will ring for several hundred ns.

If the peaking and ringing cause system problems they can be eliminated with an RC snubber circuit from the output to ground. The values can be found empirically by observing a squarewave or the frequency response. First just put the resistor alone from output to ground until the desired response is obtained. Of course the gain will be reduced due to R_{OUT}. Then put capacitance in series with the resistor to restore the gain at low frequencies. Start with a small capacitor and increase until the response is optimum. Too large a capacitor will roll the gain off prematurely and result in a longer settling time. The figure below shows an example of an EL2003 driving a 330 pF load, which is similar to the input of a flash converter.



2003-12

Driving a Pure Capacitance



Top Trace is without Snubber.
Bottom Trace is with Snubber Circuit.

2003-13

Inductive Loads

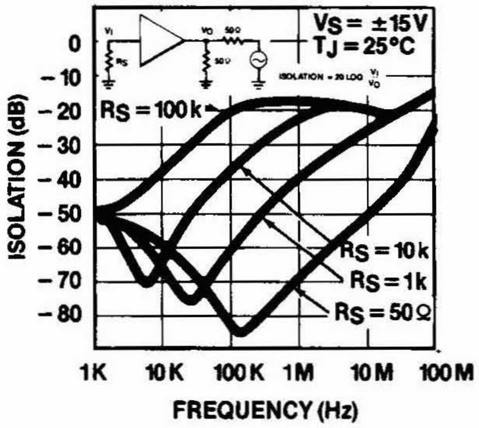
The EL2003/EL2033 can drive small motors, solenoids, LDT's and other inductive loads. Foldback current limiting is NOT used in the EL2003 or EL2033 and current limiting into an inductive load does NOT in and of itself cause spikes or kickbacks. However, if the EL2003 or EL2033 is in current limit and the input voltage is changing quickly (i.e., a squarewave) the inductive load can kick the output beyond the supply voltage. Motors are also able to generate kickbacks when the EL2003 or EL2033 is in current limit.

To prevent damage to the EL2003/EL2033 when the output kicks beyond the supplies it is recommended that catch diodes be placed from each supply to the output.

Reverse Isolation

The EL2003/EL2033 have excellent output to input isolation over a wide frequency range. This characteristic is very important when the buffer is used to drive signals between different equipment over cables. Often the cable is not perfect or the termination is improper and reflections occur that act like a signal source at the output of the buffer. Worst case the cable is connected to a source instead of where it is supposed to go. In both situations the buffer must keep these signals from its input. The following curve shows the reverse isolation of the EL2003/EL2033 verses frequency for various source resistors.

Reverse Isolation vs. Frequency



2003-14

Applications Hints — Contd.

Driving Cables

There are at least three ways to use the EL2003 and EL2033 to drive cables, as shown in the adjacent figure. The most obvious is to directly connect the cable to the output of the buffer. This results in a gain determined by the output resistance of the EL2003 or EL2033 and the characteristic impedance of the cable, assuming it is properly terminated. For RG-58 into 50Ω the gain is about −1 dB, exclusive of cable losses. For optimum response and minimum reflections it is important for the cable to be properly terminated.

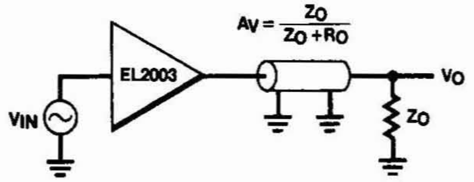
Double termination of a cable is the cleanest way to drive it since reflections are absorbed on both ends of the cable. The cable source resistor is equal to the characteristic impedance of the cable less the output resistance of the EL2003/EL2033. The gain is −6 dB exclusive of the cable attenuation.

Back matching is the last and most interesting way to drive a cable. The cable source resistor is again the characteristic impedance less the output resistance of the EL2003/EL2033; the termination resistance is now much greater than the cable impedance. The gain is 0 dB and DC levels waste no power.

An additional EL2033 or EL2033 make a good receiver at the terminating end. Because an unterminated cable looks like a resonant circuit, the receiving EL2003 or EL2033 should have an isolating resistor in series with its input to prevent oscillations when the cable is not connected to the driver. Of course if the cable is always connected to the back match, no resistor is necessary.

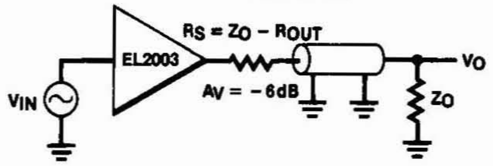
WARNING: ONE END OF A CABLE MUST BE PROPERLY TERMINATED. If neither end is terminated in the cable characteristic impedance, the cable will have standing waves that appear as resonances in the frequency response. The resonant frequencies are a function of the cable length and even relatively short cables can cause problems at frequencies as low as 1 MHz. Longer cables should be terminated on both ends.

Direct Drive



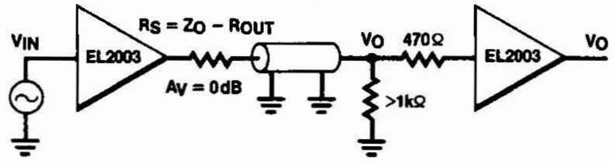
2003-15

Double Matched



2003-16

Back Matched

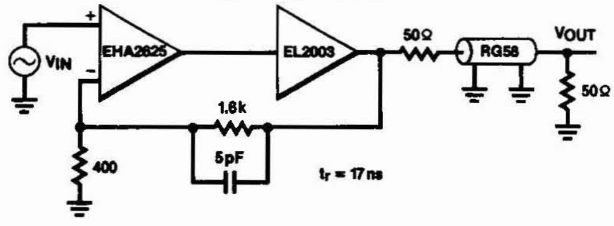


2003-17

Op Amp Booster

The EL2003 or EL2033 can boost the output drive of almost any monolithic op amp. Because the phase shift in the EL2003/EL2033 is low at the op amp's unity gain frequency, no additional compensation is required. By following an op amp with an EL2003 or EL2033, the buffered op amp can drive cables and other low impedance loads directly. Even decompensated high speed op amps can take advantage of the EL2003's or EL2033's 100 mA drive.

Op Amp Booster



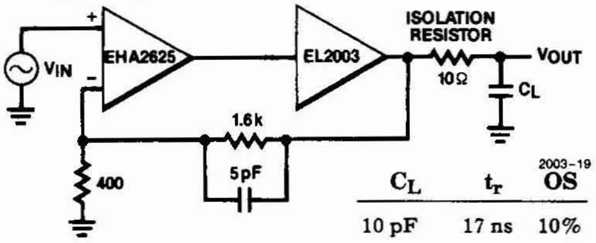
2003-18

Applications Hints — Contd.

Driving capacitive loads with any closed loop amplifier creates special problems. The open loop output impedance works into the load capacitance to generate phase lag which can make the loop unstable. The output impedance of the EL2003 or EL2033 is less than 10Ω from DC to about 10 MHz, but a capacitive load of 1000 pF will generate about 45 degrees phase shift at 10 MHz and make high speed op amps unstable. Obviously more capacitance will cause the same problem but at lower frequencies, and slower op amps as well would become unstable.

The easiest way to drive capacitive loads is to isolate them from the feedback with a series resistor. Ten to twenty ohms is usually enough but the final value depends on the op amp used and the range of load capacitance.

Op Amp Booster with Capacitive Load

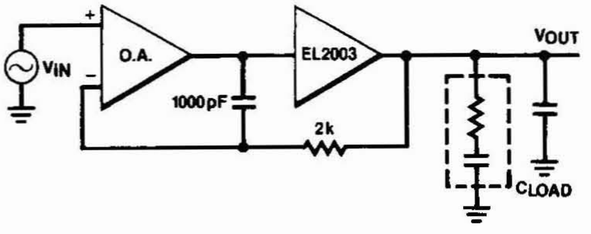

VIN
+
−
EHA2625
EL2003
ISOLATION RESISTOR
10Ω
VOUT
CL
1.6k
5pF
400
2003-19

C_L	t_r	OS
10 pF	17 ns	10%
470 pF	20 ns	50%
0.001 μF	30 ns	35%
0.005 μF	80 ns	0
0.01 μF	220 ns	0
0.05 μF	1.1 μs	0
0.1 μF	2.2 μs	0

10Ω is enough isolation and speed is determined by the isolation resistor and capacitive load time constant.

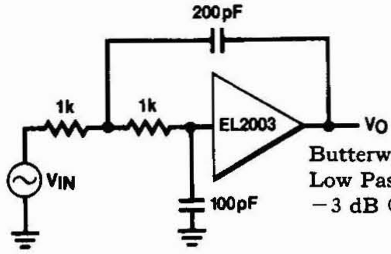
If the system requirements will not tolerate the isolation resistor, then additional high frequency feedback from the op amp output (the buffer input) and an isolating resistor from the buffer output is required. This requires that the op amp be unity gain stable.

Complex Feedback with the Buffer to Drive Capacitive Loads

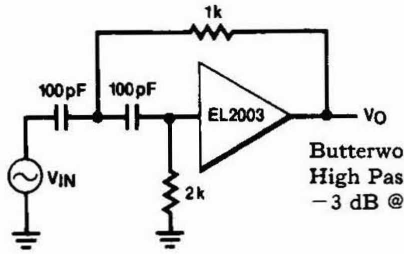

VIN
+
−
O.A.
1000pF
EL2003
2k
VOUT
CLOAD
2003-20

This works with any unity gain stable OA.
Snubber Circuit (51Ω 470 pF) is optional.

Typical Applications

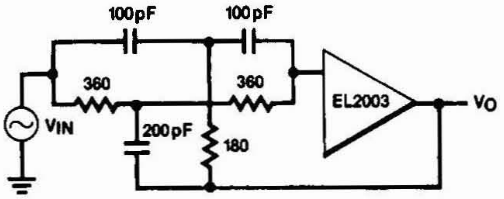

200pF
1k
1k
EL2003
VO
VIN
100pF
2003-21

Butterworth
Low Pass Filter
−3 dB @ 1 MHz


1k
100pF
100pF
EL2003
VO
VIN
2k
2003-22

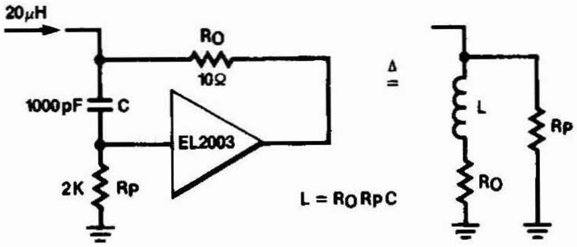
Butterworth
High Pass Filter
−3 dB @ 1 MHz

High Q Notch Filter


100pF
100pF
360
360
EL2003
VO
VIN
200pF
180
2003-23

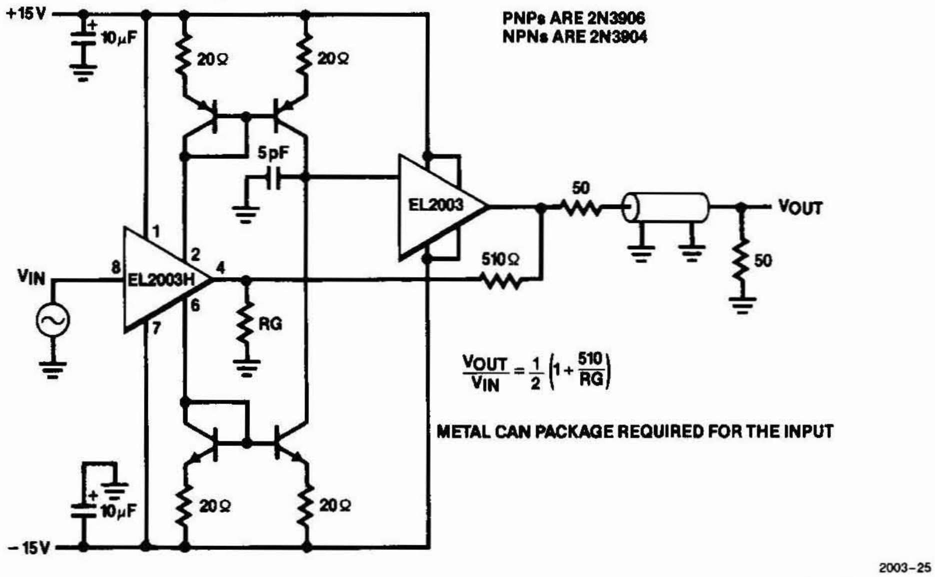
$$f_O = \frac{1}{2\pi\,(100\text{ pF})\,(360)} \approx 4.4\text{ MHz}$$

Simulated Inductor


20μH
RO
10Ω
1000pF
C
EL2003
2K
RP
≙
L
RP
RO
L = RORPC
2003-24

Typical Applications — Contd.

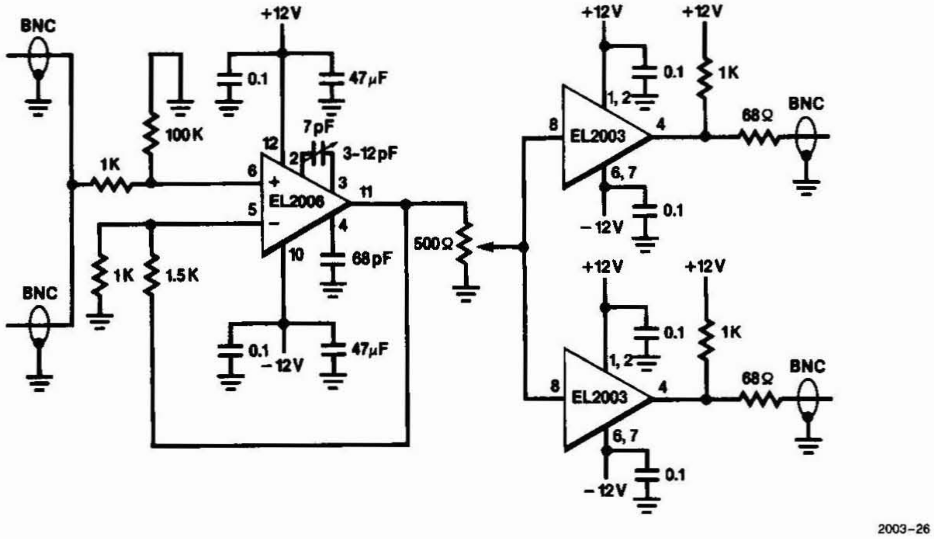
Turbo Amplifier, BW = 30 MHz for Gains from 1 to 5


+15V
10μF
20Ω
20Ω
5pF
EL2003
50
VOUT
50
510Ω
1
2
4
8
6
7
VIN
EL2003H
RG
$\frac{V_{OUT}}{V_{IN}} = \frac{1}{2}\left(1 + \frac{510}{RG}\right)$
METAL CAN PACKAGE REQUIRED FOR THE INPUT
PNPs ARE 2N3906
NPNs ARE 2N3904
10μF
20Ω
20Ω
−15V
2003-25

Video Distribution Amplifier

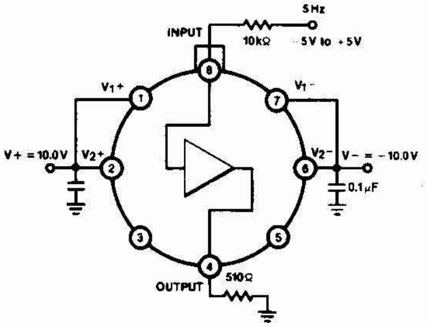
In this broadcast quality circuit, the EL2006 FET input amplifier provides a very high input impedance so that it may be used with a wide variety of signal sources including video DACs, CCD cameras, video switches or 75Ω cables. The EL2006 provides a voltage gain of 2.5 while the potentiometer allows the overall gain to be adjusted to drive the standard signal levels into the back matched 75Ω cables. Back matching prevents multiple reflections in the event that the remote end of the cable is not properly terminated. The 1k pull up resistors reduce the differential gain error from 0.15% to less than 0.1%.

Video Distribution Amplifier


BNC
+12V
0.1
47μF
100K
1K
7pF
3-12pF
12
2
6
3
11
5
4
10
EL2006
68pF
500Ω
1K
1.5K
BNC
0.1
−12V
47μF
+12V
+12V
0.1
1K
1, 2
8
EL2003
4
68Ω
BNC
6, 7
0.1
−12V
+12V
+12V
0.1
1K
1, 2
8
EL2003
4
68Ω
BNC
6, 7
0.1
−12V
2003-26

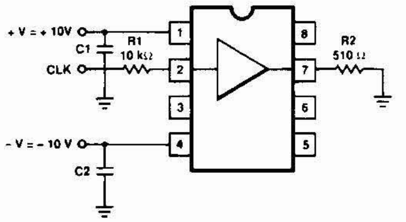
Burn-In Circuits

EL2003 Metal Can


5Hz
INPUT
10kΩ
-5V to +5V
8
V_1+
1
V_1-
7
V+ = 10.0V
V_2+
2
V_2-
V− = −10.0V
6
0.1μF
3
5
4
OUTPUT
510Ω

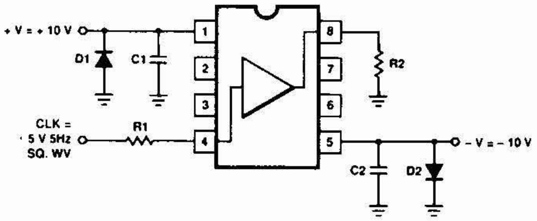
2003-27

EL2003 DIP


+V = +10V
C1
R1
10 kΩ
CLK
1
2
3
4
8
7
6
5
R2
510 Ω
−V = −10 V
C2

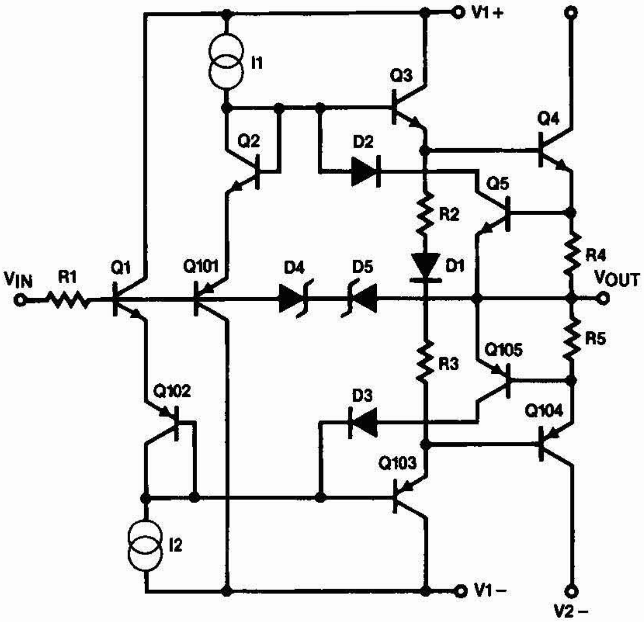
2003-28

EL2033 DIP


+V = +10 V
D1
C1
1
2
3
4
8
7
6
5
R2
CLK =
+5 V 5Hz
SQ. WV
R1
−V = −10 V
C2
D2

2003-29

Simplified Schematic

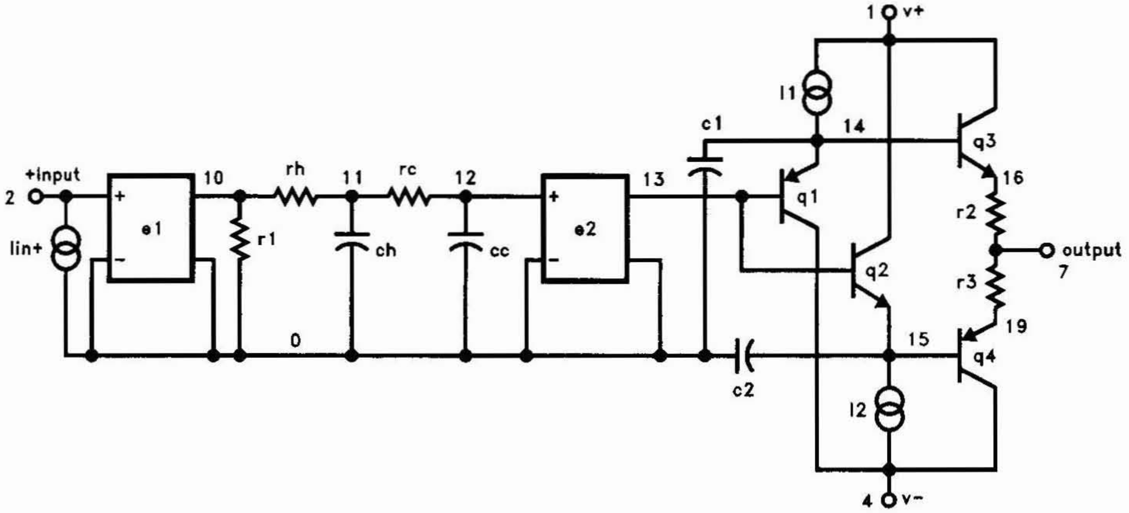

V1+
I1
Q3
Q4
Q2
D2
Q5
R2
R4
V_{IN}
R1
Q1
Q101
D4
D5
D1
V_{OUT}
R5
R3
Q105
Q102
D3
Q104
Q103
I2
V1−
V2−

2003-30

EL2003 Macromodel

```
* Connections:    +input
*                 |     +Vsupply
*                 |     |     -Vsupply
*                 |     |     |     output
*                 |     |     |     |
.subckt M2003     2     1     4     7
* Input Stage
e1 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 10pF
rc 11 12 100
cc 12 0 3pF
e2 13 0 12 0 1.0
* Output Stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 5
r3 19 7 5
c1 14 0 3pF
c2 15 0 3pF
i1 1 14 3mA
i2 15 4 3mA
* Bias Current
iin+ 2 0 5uA
* Models
.model qn npn(is=5e-15 bf=150 rb=350 ptf=45 cjc=2pF tf=0.3nS)
.model qp pnp(is=5e-15 bf=150 rb=350 ptf=45 cjc=2pF tf=0.3nS)
.ends
```

EL2003 Macromodel — Contd.


1 v+
I1
14
c1
q3
+input
2
Iin+
e1
10
r1
rh
11
ch
rc
12
cc
e2
13
q1
q2
16
r2
output
7
r3
19
0
15
q4
c2
I2
4 v-

2003-31

EL2008C

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2008C

55 MHz 1 Amp Buffer Amplifier

Features

- High slew rate—2500 V/μs
- Wide bandwidth—
  100 MHz @ R_L = 50Ω
  55 MHz @ R_L = 10Ω
- Output current—1A continuous
- Output impedance—1Ω
- Quiescent current—13 mA
- Short circuit protected
- Power package with isolated metal tab

Applications

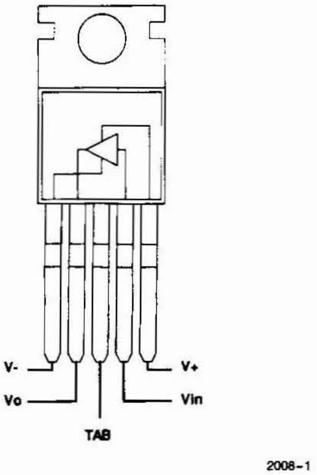
- Video distribution amplifier
- Fast op amp booster
- Flash converter driver
- Motor driver
- Pulse transformer driver
- A.T.E. pin driver

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2008CT	0°C to +75°C	TO-220	MDP0028

Connection Diagram

5-Pin TO-220



Top View

General Description

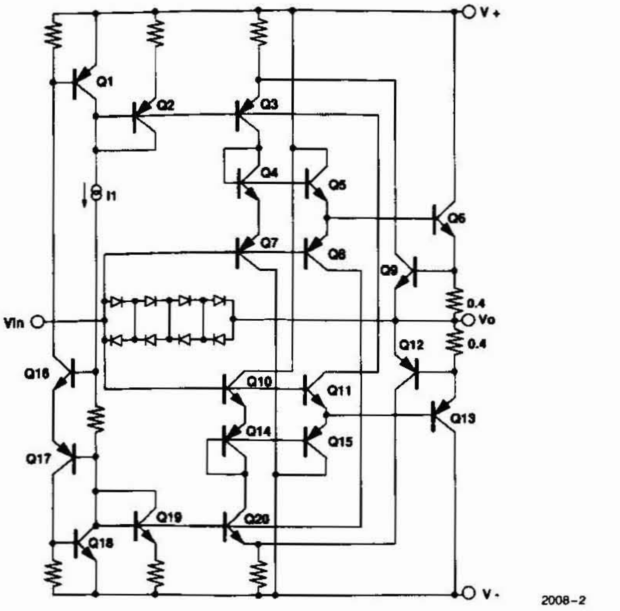
The EL2008 is a patented high speed bipolar monolithic buffer amplifier designed to provide currents over 1 amp at high frequencies, while drawing only 13 mA of quiescent supply current. The EL2008's 1500 V/μs slew rate and 55 MHz bandwidth driving a 10Ω load is second only to the EL2009 and insures stability in fast op amp feedback loops. Elantec has applied for patents on unique circuitry within the EL2008.

Used as an open loop buffer, the EL2008's low output impedance (1Ω) gives a gain of 0.99 when driving a 100Ω load and 0.9 driving a 10Ω load. The EL2008 has output short circuit current limiting which will protect the device under both a DC fault condition and AC operation with reactive loads.

The EL2008 is constructed using Elantec's proprietary Complementary Bipolar process that produces PNP and NPN transistors with essentially identical AC and DC characteristics. In the EL2008, the Complementary Bipolar process also insulates the package's metal heat sink tab from all supply voltages. Therefore the tab may be mounted to an external heat sink or the chassis without an insulator.

The EL2008CT is specified for operation over the 0°C to +75°C temperature range and is provided in a 5-lead TO-220 plastic power package.

Simplified Schematic



Manufactured under U.S. Patent No. 4,833,424 and 4,827,223 and U.K. Patent No. 2217134.

December 1995 Rev. E

EL2008C

55 MHz 1 Amp Buffer Amplifier

Absolute Maximum Ratings (25°C)

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_A	Operating Temperature Range	0°C to +75°C
V_{IN}	Input Voltage (Note 1)	±15 or V_S	T_J	Operating Junction Temp	175°C
I_{IN}	Input Current (Note 1)	±50 mA	T_{ST}	Storage Temp Range	−65°C to +150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{LD}	Lead Solder Temp <10 seconds	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	**Test Procedure**
I	**100% production tested and QA sample tested per QA test plan QCX0002.**
II	**100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.**
III	**QA sample tested per QA test plan QCX0002.**
IV	**Parameter is guaranteed (but not tested) by Design and Characterization Data.**
V	**Parameter is typical value at T_A = 25°C for information purposes only.**

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	25°C	−40	10	+40	I	mV
				T_{MIN}, T_{MAX}	−50		+50	IV	mV
I_{IN}	Input Current	0	∞	25°C	−35	−5	+35	I	μA
				T_{MIN}, T_{MAX}	−50		+50	IV	μA
R_{IN}	Input Impedance	±12V	100Ω	25°C	0.5	2		I	MΩ
A_{V1}	Voltage Gain	±10V	∞	25°C	0.985	0.9995		I	V/V
A_{V2}	Voltage Gain	±10V	10Ω	25°C	0.88	0.91		I	V/V
A_{V3}	Voltage Gain, $V_S = \pm 15V$	±3V	10Ω	25°C	0.87	0.89		I	V/V
V_{01}	Output Voltage Swing	±14V	100Ω	25°C	±13			I	V
V_{02}	Output Voltage Swing	±12V	10Ω	25°C	±10.5	±11		I	V
R_{01}	Output Impedance	±10V	±10 mA	25°C		1.8	2.5	I	Ω
R_{02}	Output Impedance	±10V	±1A	25°C		0.8	1.0	I	Ω
I_O	Output Current	±12V	(Note 3)	25°C	1.4	1.8		I	A
				T_{MIN}, T_{MAX}	1			IV	A
I_S	Supply Current	0	∞	25°C	12	17	26	I	mA
PSRR	Supply Rejection (Note 4)	0	∞	25°C	60			I	dB
V_S+, V_S-	Supply Sensitivity (Note 5)		∞	25°C			2	I	mV/V

EL2008C

55 MHz 1 Amp Buffer Amplifier

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
SR_1	Slew Rate (Note 6)	±10V ±10V	50Ω 10Ω	25°C 25°C		2500 1500		V V	V/µs V/µs
SR_2	Slew Rate (Note 7)	±5V	10Ω	25°C		800		V	V/µs
t_r, t_f	Rise/Fall Time	100 mV	10Ω	25°C		7		V	ns
BW	−3 dB Bandwidth	100 mV	10Ω	25°C		55		V	MHz
C_{IN}	Input Capacitance			25°C		25		V	pF
THD				25°C			1	I	%

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V and −10V on the output.

Note 4: $V_S = \pm 4.5V$ then V_S is changed to ±18V.

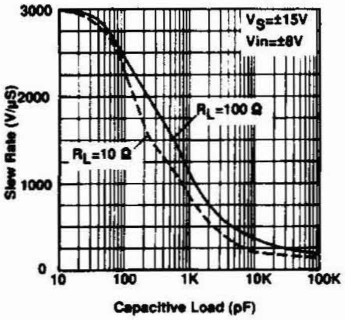
Note 5: $V_S+ = +15V$, $V_S- = -4.5V$ then V_S- is changed to −18V and $V_S- = -15V$, $V_S+ = +4.5V$ then V_S+ is changed to +18V.

Note 6: Slew Rate is measured between $V_{OUT} = +5V$ and −5V.

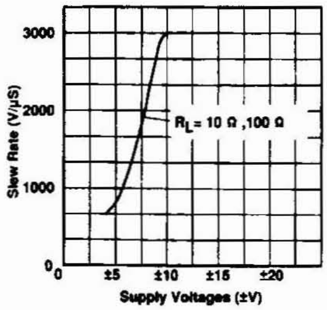
Note 7: Slew Rate is measured between $V_{OUT} = +2.5V$ and −2.5V.

Typical Performance Curves

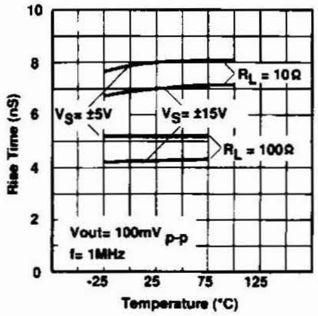
Slew Rate vs Capacitance Load



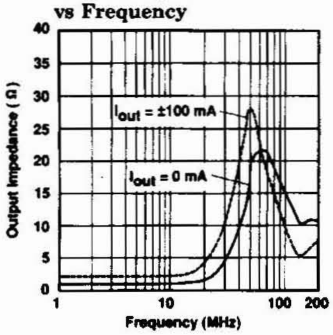
Slew Rate vs Supply Voltage



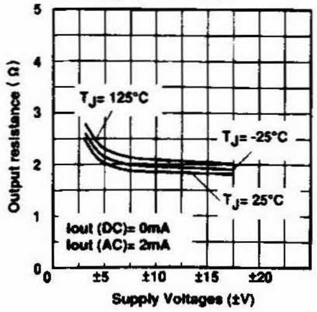
Rise Time vs Temperature



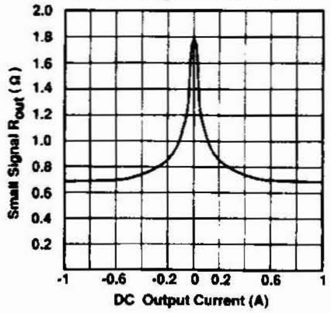
Output Impedance vs Frequency



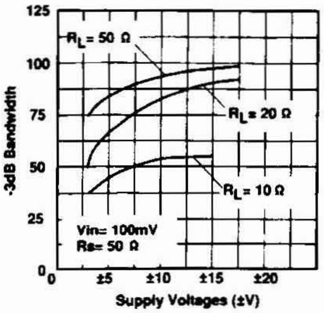
Output Resistance vs Supply Voltage



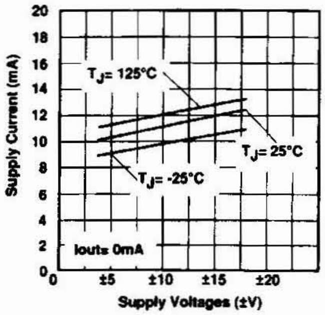
Small Signal Output Resistance vs DC Output Current



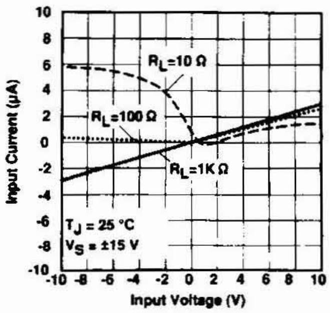
−3 dB Bandwidth vs Supply Voltage



Quiescent Supply Current vs Supply Voltage



Input Current vs Input Voltage



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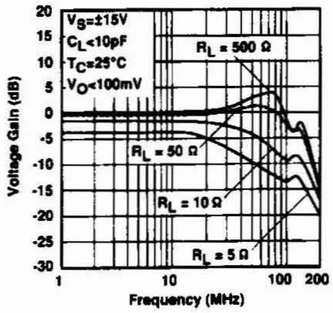
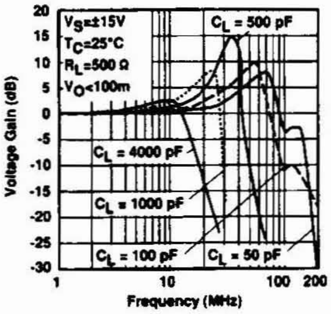
Typical Performance Curves — Contd.

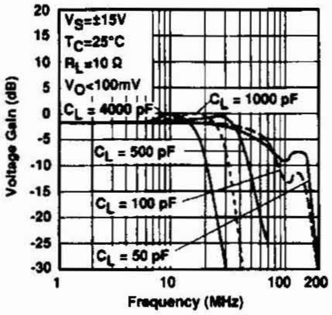
Voltage Gain vs Frequency at Various Resistive Loads



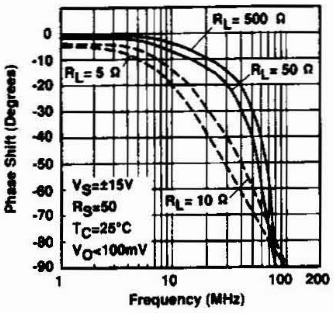
Voltage Gain vs Frequency at Various Capacitive Loads



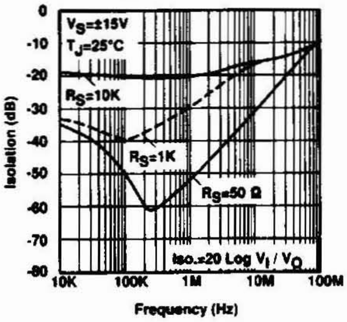
Voltage Gain vs Frequency at Various Capacitive Loads



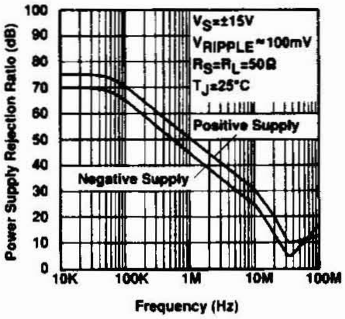
Phase Shift vs Frequency at Various Resistive Loads



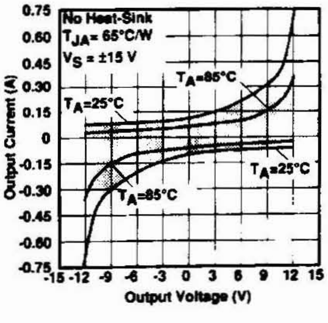
Reverse Isolation vs Frequency



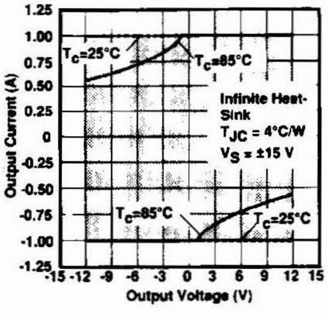
Power Supply Rejection Ratio vs Frequency



Active operating area.



Active operating area.



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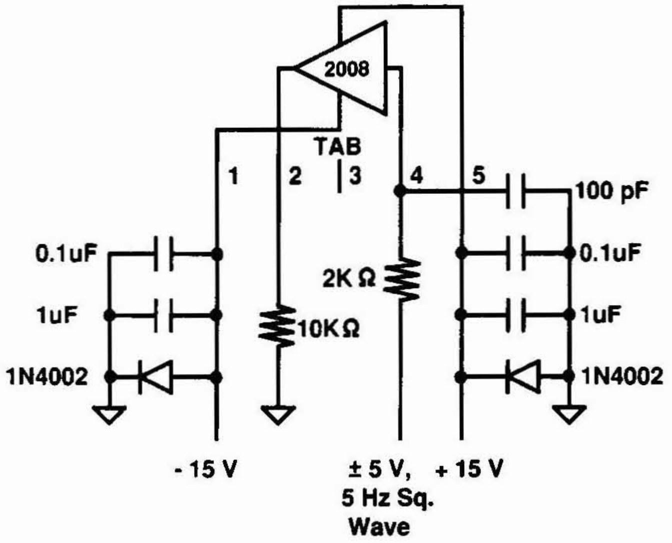
Burn-In Circuit



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Applications Information

The EL2008 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2008 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2008's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 3000 V/μs slew rates with 10Ω load possible with modest supply current.

Power Supplies

The EL2008 may be operated with single or split supplies with total voltage difference between 10V (±5V) and 36V (±18V). However, bandwidth, slew rate and output impedance are affected by total supply voltages below 20V (±10V) as shown by the characteristic curves. It is not necessary to use equal split value supplies. For example −5V and +12V would be excellent for signals from −2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum a 10 μF tantalum capacitor in parallel with a 0.1 μF capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2008 looks like a resistance in parallel with about 25 pF in addition to a DC bias current. The DC bias current is due to the mismatch in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range in some units. A few typical input current (I_{IN}) curves are shown in the characteristic curves.

Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. If the output of the EL2008 is accidentally shorted it is possible that some devices driving the EL2008's input could be damaged or destroyed driving the EL2008's load through the diodes while the EL2008 is unaffected. In such cases a resistor in series with the input of the EL2008 can limit the current.

Applications Information — Contd.

Source Impedance

The EL2008 has good input to output isolation. Open loop, capacitive and resistive sources up to 100 kΩ present no oscillation problem driving resistive loads as long as care is used in board layout to minimize output to input coupling and the supplies are properly bypassed. When driving capacitive loads in the 100 pF to 1000 pF region source resistances above 25Ω can cause peaking and oscillation. Such problems can be eliminated by placing a capacitor from the EL2008's input to ground. The value should be about ¼ the load capacitance. In a feedback loop there is a speed penalty and a possibility of oscillation when the EL2008 is driven with a source impedance of 200Ω or more. Significant phase shift can occur due to the EL2008's 25 pF input capacitance. Inductive sources can cause oscillations. A series resistor of a few hundred ohms to 1 kΩ will usually solve the problem.

Current Limit

The EL2008 has internal current limiting to protect the output transistors. The current limit is about 1.5A at room temperature and decreases with junction temperature. At 150°C junction temperature it is above 1A.

Heat Sinking

A suitable heat sink will be required for most applications. The thermal resistance junction to case for the TO-220 package is 4°C per watt. No voltage appears at the heat sink tab so no precautions need to be taken to avoid shorting the tab to a supply voltage or ground. As there is a small parasitic capacitance between the tab and the buffer circuitry, it is recommended that the tab be connected to AC ground (either supply voltage or DC ground). The center lead is internally connected to the tab so the connection can be made at the tab or the center lead.

Parallel Operation

If more than 1A is required or if heat management is a problem, several EL2008s may be paralleled together. The result is as through each device was driving only part of the load. For example, if two units are paralleled then a 5Ω load looks like 10Ω to each EL2008. Of course, parallel operation reduces both the input and output impedance and increases bias current. But there is no increase in offset voltage. Three units in parallel can drive a 3Ω load ±10V at 2500 V/μs. The output impedance will be about 0.33Ω.

Resistive Loads

The DC gain of the EL2008 is the product of the unloaded gain (0.999) and the voltage divider formed by the device output resistance and the load resistance.

$$A_V = 0.999^* (R_L/R_L + R_{OUT})$$

The high frequency response varies with the load resistance as shown by the characteristic curves. Both gain and phase are shown. If the 80 MHz peaking is undesireable when driving load resistors greater than 50Ω, an RC snubber circuit can be used from output to ground. The capacitive load section discusses snubber usage in more detail.

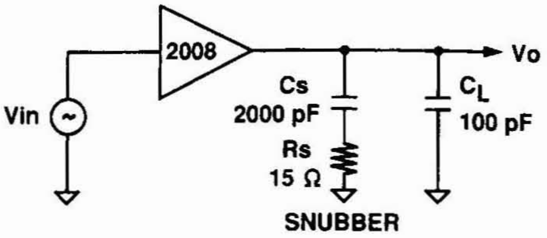
Capacitive Loads

The EL2008 is not stable driving purely capacitive loads between 100 pF and 500 pF. Purely capacitive loads from 500 pF to 1000 pF will also have excessive peaking as shown in the characteristic curves. The squarewave response will have large overshoots and ring for hundreds of nanoseconds.

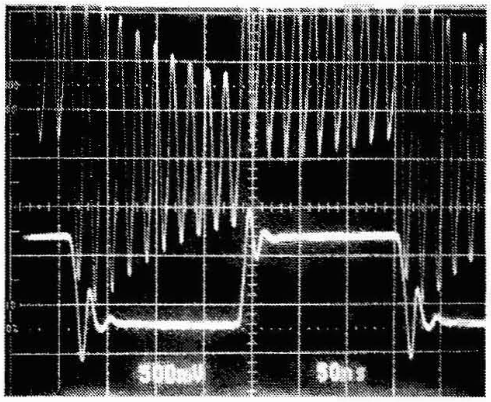
When driving capacitive loads, stability can be achieved and peaking and ringing can be mini-

Applications Information — Contd.

mized either by adding a 50Ω (or less) load in parallel with the capacitive load or by an RC snubber circuit from output to ground. The snubber values can be found empirically by observing a squarewave or the frequency response. First just put a resistor alone from the output to ground until the desired response is achieved. The gain will be reduced due to the output resistance of the EL2008 and power consumption will be high. Then put a capacitor in series with the resistor to restore gain at low frequencies and eliminate the DC current. Start with a small capacitor and increase until the response is optimum. The figure below shows an example of an EL2008 driving a 100 pF load.



2008-6



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Driving a pure capacitive load. Top trace is without a snubber. Bottom trace is with a snubber circuit.

Inductive Loads

The EL2008 with its 1A output current can drive small motors and other inductive loads. The EL2008's current limiting into inductive loads does NOT in and of itself cause spikes and kickbacks. However, if the EL2008 is in current limit and the input voltage is changing very quickly (i.e., a squarewave) the inductive load can kick the output beyond the supply voltages. Motors are also able to generate kickback voltages when the EL2008 is in current limit.

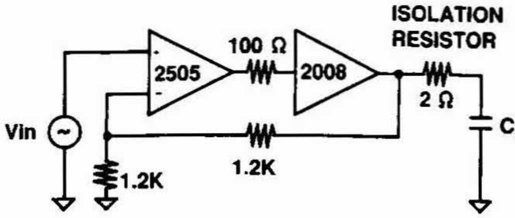
To prevent damage to the EL2008 when the output kicks beyond the supplies it is recommended that catch diodes be placed from each supply to the output.

Op Amp Booster

The EL2008 can boost the output drive of almost any monolithic op amp. If the phase shift in the EL2008 is low at the op amp's unity gain frequency, no additional frequency compensation is required. An op amp followed with the EL2008 can drive loads as low as 10Ω to ±10V.

Driving capacitive loads with any closed loop system creates special problems. The open loop output impedance works into the load capacitance to generate phase lag which can make the loop unstable. The EL2008 output impedance is less than 10Ω from DC to 30 MHz. But a capacitive load of 1000 pF will generate about 45 degrees of phase shift at 30 MHz. More capacitance will cause the problem at lower frequency.

With enough capacitance even slow op amps will become unstable. The simplest way to drive capacitive loads is to isolate them from the feedback with a series resistor. 1Ω to 5Ω is usually enough but the final value will depend on the op amp used and the range of load capacitance.



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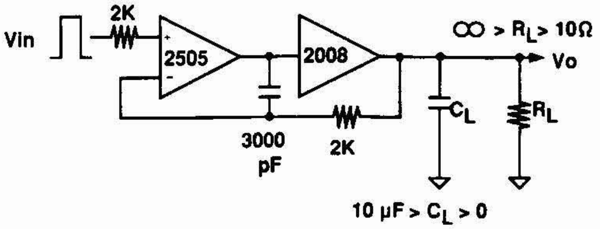
C_L		t_r		O.S.
13	pF	45	ns	20%
470	pF	50	ns	20%
1000	pF	55	ns	30%
3300	pF	60	ns	30%
0.1	μF	350	ns	0%
1	μF	4	μs	0%
5	μF	20	μs	0%

Applications Information — Contd.

Unfortunately the isolation resistor is not inside the op amp feedback loop and cannot be neglected when computing the DC voltage gain into a resistive load. If load dependent DC gain is not tolerable then additional high frequency feedback from the op amp output (the EL2008 input) and an isolation resistor from the buffer output can be used to stabilize the loop. This configuration requires the op amp to be unity gain stable. This feedback method will allow the EL2008 to boost the output of the EHA2505 amplifier below and serve as a variable, bipolar 1A voltage supply with short circuit protection.



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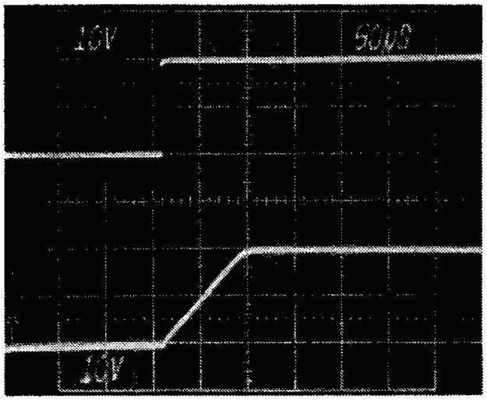
Slew Rate = $1A/C_L$

Video Distribution Amplifier

The EL2008 can drive 15 double matched 75Ω cables. If the EL2008 is used within an op amp feedback loop the output levels are independent of loading. The circuit below accepts 1 of 2 inputs and drives 15 cables. Pin 8 of the EL2020 (Disable) is used to multiplex between the inputs and can be easily expanded to accept more inputs. The circuit as shown when fully loaded has differential phase <0.1° and differential gain <0.1%. The 100Ω resistor at the EL2008 input (R1) is necessary to stabilize the loop. The 100Ω resistor at the EL2008 output (R2) to the −12V supply, insures that the EL2008 sources current even when the output voltage is at 0V. This is necessary to achieve the excellent differential gain and phase values. More information about driving cables can be found in the EL2003 data sheet. See the EL2020 data sheet to learn more about using it as a multiplexer.



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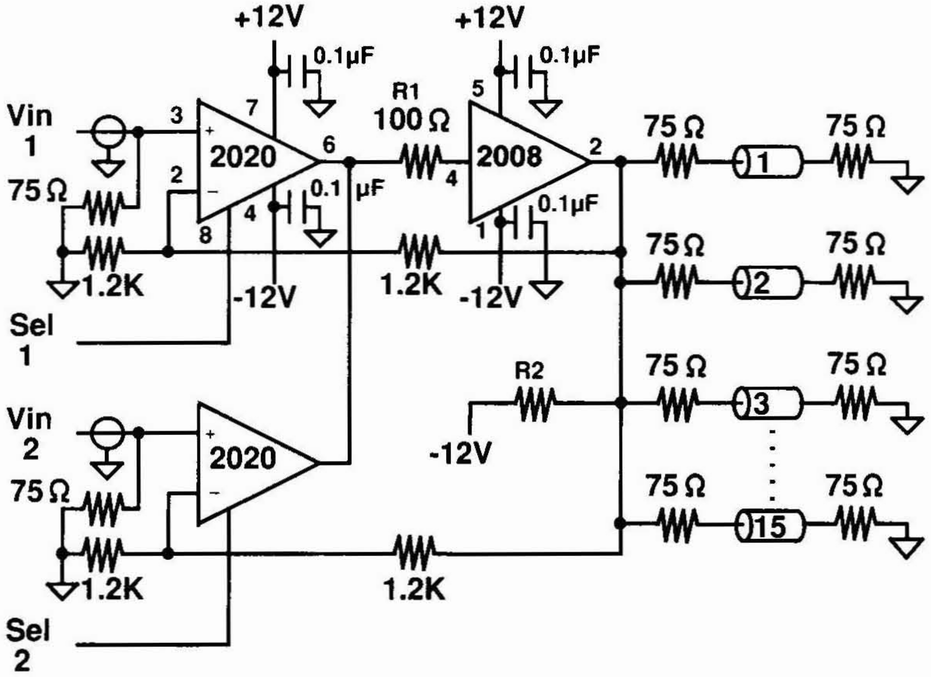
Input (top trace) and output (bottom trace) of EHA2505 op amp boosted by EL2008.

Video Mux and Distribution Amplifier


+12V
0.1μF
+12V
0.1μF
R1
100 Ω
Vin
1
3
7
2020
6
2
5
2008
4
2
75 Ω
75 Ω
75 Ω
1
0.1 μF
0.1μF
8
1
1.2K
-12V
1.2K
-12V
75 Ω
2
75 Ω
Sel
1
R2
75 Ω
3
75 Ω
-12V
Vin
2
2020
75 Ω
75 Ω
15
75 Ω
1.2K
1.2K
Sel
2

2008-11

EL2008 Macromodel

```
* Connections:    +input
*                  |     +Vsupply
*                  |      |     -Vsupply
*                  |      |      |     output
*                  |      |      |      |
.subckt M2008      4      5      1      2
*
* Input Stage
*
e1 10 0 4 0 1.0
r1 10 0 1K
rh 10 11 1K
ch 11 0 2.65pF
rc 11 12 10K
cc 12 0 0.159pF
e2 13 0 12 0 1.0
*
* Output Stage
*
q1 1 13 14 qp
q2 5 13 15 qn
q3 5 14 16 qn 15
q4 1 15 19 qp 15
r2 16 2 0.4
r3 19 2 0.4
c1 14 0 0.6pF
c2 15 0 0.6pF
i1 5 14 1.2mA
i2 15 1 1.2mA
*
* Bias Current
*
iin+ 4 0 5µA
*
* Models
*
.model qn npn (is=5e-15 bf=1500)
.model qp pnp (is=5e-15 bf=1500)
.ends
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2009C

90 MHz 1 Amp Buffer Amplifier

Features

- High slew rate—3000 V/μs
- Wide bandwidth—
  125 MHz @ $R_L = 50\Omega$
  90 MHz @ $R_L = 10\Omega$
- Output current—1A continuous
- Output impedance—1Ω
- Short circuit protected
- Power package with isolated metal tab

Applications

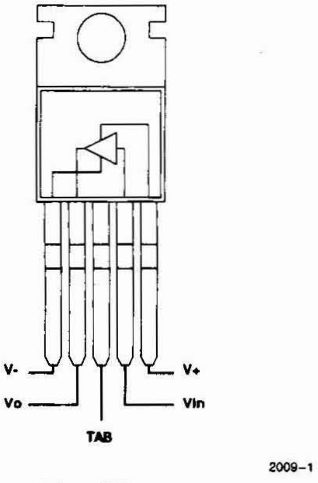
- Video distribution amplifier
- Fast op amp booster
- Flash converter driver
- Motor driver
- Pulse transformer driver
- A.T.E. pin driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2009CT	0°C to +75°C	TO-220	MDP0028

Connection Diagram

5-Pin TO-220



Top View

General Description

The EL2009 is a patented high speed bipolar monolithic buffer amplifier designed to provide currents over 1 amp at high frequencies, while drawing 40 mA of quiescent supply current. The EL2009's 3000 V/μs slew rate and 90 MHz bandwidth driving a 10Ω load insures stability in fast op amp feedback loops. Elantec has applied for patents on unique circuitry within the EL2009.

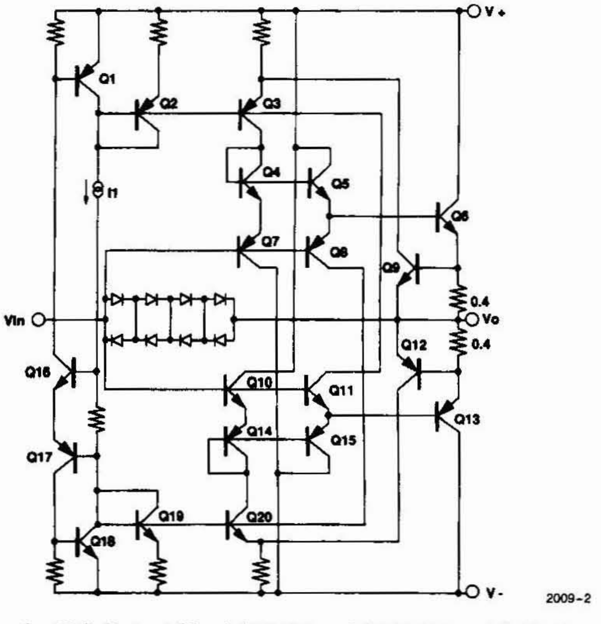
Used as an open loop buffer, the EL2009's low output impedance (1Ω) gives a gain of 0.99 when driving a 100Ω load and 0.9 driving a 10Ω load.

The EL2009 has an output short circuit current limit which will protect the device under both a DC fault condition and AC operation with reactive loads.

The EL2009 is constructed using Elantec's proprietary Complementary Bipolar process that produces PNP and NPN transistors with essentially identical AC and DC characteristics. In the EL2009, the Complementary Bipolar process also insulates the package's metal heat sink tab from all supply voltages. Therefore, the tab may be mounted to an external heat sink or the chassis without an insulator.

The EL2009CT is specified for operation over the 0°C to +75°C temperature range and is provided in a 5-lead TO-220 plastic power package.

Simplified Schematic



Manufactured under U.S. Patent No. 4,833,424 and 4,827,223 and U.K. Patent No. 2217134.

December 1995 Rev C

EL2009C

90 MHz 1 Amp Buffer Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_A	Operating Temperature Range	0°C to +75°C
V_{IN}	Input Voltage (Note 1)	±15V or V_S	T_J	Operating Junction Temp.	175°C
I_{IN}	Input Current (Note 1)	±50 mA	T_{ST}	Storage Temp. Range	−65°C to +150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{LD}	Lead Solder Temp. <10 seconds	300°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	25°C	−60		60	I	mV
				T_{MIN}, T_{MAX}	−80		80	IV	mV
I_{IN}	Input Current	0	∞	25°C	−125	−5	125	I	µA
				T_{MIN}, T_{MAX}	−200		200	IV	µA
R_{IN}	Input Impedance	±12V	100Ω	25°C	250	900		I	kΩ
A_{V1}	Voltage Gain	±10V	∞	25°C	0.985	0.999		I	V/V
A_{V2}	Voltage Gain	±10V	10Ω	25°C	0.88	0.90		I	V/V
A_{V3}	Voltage Gain, V_S = ±5V	±3V	10Ω	25°C	0.87	0.89		I	V/V
V_{O1}	Output Voltage Swing	±14V	100Ω	25°C	±13			I	V
V_{O2}	Output Voltage Swing	±12V	10Ω	25°C	±10.5	±11		I	V
R_{O1}	Output Impedance	±10V	±10 mA	25°C			1.5	I	Ω
R_{O2}	Output Impedance	±10V	±1A	25°C		0.9	1.0	I	Ω
I_O	Output Current	±12V	(Note 3)	25°C	1.4	1.8		I	A
				T_{MIN}, T_{MAX}	1			IV	A
I_S	Supply Current	0	∞	25°C	30	45	65	I	mA
PSRR	Supply Rejection (Note 4)	0	∞	25°C	60			I	dB

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
V_S+, V_S-	Supply Sensitivity (Note 5)		∞	25°C			2	I	mV/V
SR_1	Slew Rate (Note 6)	±10V	50Ω 10Ω	25°C		3000 2500		V	V/μs
SR_2	Slew Rate (Note 7)	±5V	10Ω	25°C		1250		V	V/μs
t_r, t_f	Rise/Fall Time	100 mV	10Ω	25°C		7		V	ns
BW	−3 dB Bandwidth	100 mV	10Ω	25°C		90		V	MHz
C_{IN}	Input Capacitance			25°C		25		V	pF
THD	Total Harmonic Distortion			25°C			1	I	%

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input voltage exceeds ±7.5V then the input current must be limited to ±50 mA.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V input and −10V on the output.

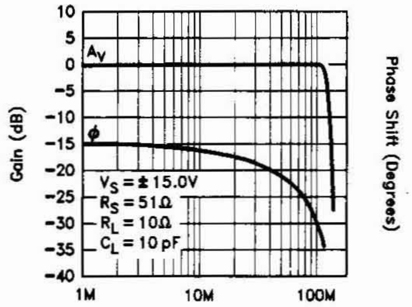
Note 4: $V_S = \pm 4.5V$ then V_S is changed to ±18V.

Note 5: $V_S+ = +15V$, $V_S- = 4.5V$ then V_S- is changed to −18V and $V_S- = -15V$, $V_S+ = +4.5V$ then V_S+ is changed to +18V.

Note 6: Slew Rate is measured between $V_{OUT} = +5V$ and $-5V$.

Note 7: Slew Rate is measured between $V_{OUT} = +2.5V$ and $-2.5V$.

Voltage Gain and Phase vs Frequency



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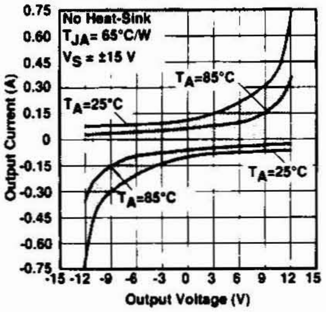
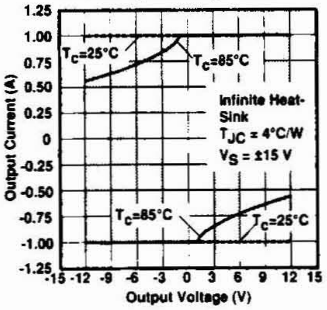
Active operating area



2009-5

Active operating area



2009-6

Applications Information

The EL2009 is a higher bandwidth of the EL2008. It is recommended that you read the EL2008 application section.

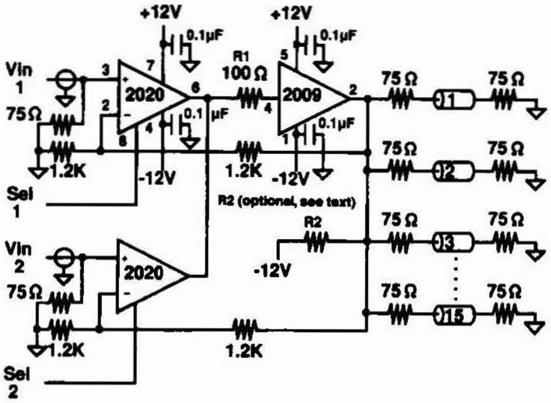
Video Distribution Amplifier

The EL2009 can drive 15 double matched 75Ω cables. If the EL2009 is used within an op amp feedback loop the output levels are independent of loading. The circuit below accepts 1 of 2 inputs and drives 15 cables. Pin 8 of the EL2020 (Disable) is used to multiplex between the inputs and can be easily expanded to accept more inputs. The circuit as shown when fully loaded has differential phase <0.1° and differential gain <0.1%. The 100Ω resistor at the EL2009 input (R1) is necessary to stabilize the loop. The EL2009 operates with a CLASS AB output which exhibits a slight rise in output impedance when-

Applications Information — Contd.

ever the current it sources into the load approaches zero. In those cases, where differential gain and phase are measurably affected, resistor R2 may be added to ensure that the EL2009 output current never reaches zero. This will result in a CLASS A output stage with active pulldown but with the penalty of power dissipation in R2. More information about driving cables can be found in the EL2003 data sheet.

Video Mux and Distribution Amp.


+12V
0.1µF
+12V
0.1µF
R1
100 Ω
5
Vin
1
3
7
2020
6
4
2009
2
75 Ω
1
75 Ω
75Ω
2
0.1 µF
0.1µF
8
4
1
1.2K
-12V
1.2K
-12V
75Ω
2
75 Ω
Sel
1
R2 (optional, see text)
R2
75 Ω
3
75 Ω
Vin
2
2020
-12V
75Ω
75 Ω
15
75Ω
1.2K
1.2K
Sel
2

2009–3

EL2009 Macromodel

```
* Connections:      +input
*                     |     +Vsupply
*                     |       |     -Vsupply
*                     |       |       |     output
*                     |       |       |       |
.subckt M2009         4       5       1       2
*
* Input Stage
*
e1 10 0 4 0 1.0
r1 10 0 1K
rh 10 11 1K
ch 11 0 1pF
rc 11 12 6.3K
cc 12 0 0.159pF
e2 13 0 12 0 1.0
*
* Output Stage
*
q1 1 13 14 qp
q2 5 13 15 qn
q3 5 14 16 qn 10
q4 1 15 19 qp 10
r2 16 2 0.2
r3 19 2 0.2
c1 14 0 1.7pF
c1 15 0 1.7pF
i1 5 14 5mA
i2 15 1 5mA
*
* Bias Current
*
iin+ 4 0 5μA
*
* Models
*
.model qn npn (is=5e-15 bf=500)
.model qp pnp (is=5e-15 bf=500)
*
.ends
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2020C
50 MHz Current Feedback Amplifier

Features

- Slew rate 500 V/μs
- ±33 mA output current
- Drives ±2.4V into 75Ω
- Differential phase <0.1°
- Differential gain <0.1%
- V supply ±5V to ±18V
- Output short circuit protected
- Uses current mode feedback
- 1% settling time of 50 ns for 10V step
- Low cost
- 9 mA supply current
- 8-pin mini-dip

Applications

- Video gain block
- Residue amplifier
- Radar systems
- Current to voltage converter
- Coax cable driver with gain of 2

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2020CN	−40°C to +85°C	P-DIP	MDP0031
EL2020CM	−40°C to +85°C	20-Lead SOL	MDP0027

General Description

The EL2020 is a fast settling, wide bandwidth amplifier optimized for gains between −10 and +10. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain then a conventional voltage feedback operational amplifier.

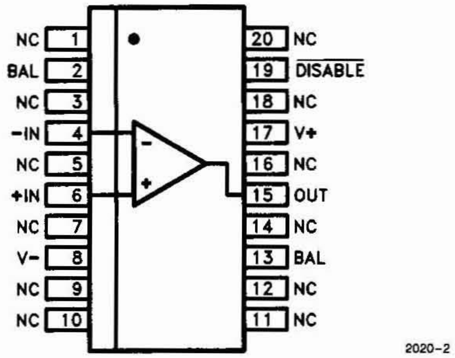
The EL2020 will drive two double terminated 75Ω coax cables to video levels with low distortion. Since it is a closed loop device, the EL2020 provides better gain accuracy and lower distortion than an open loop buffer. The device includes output short circuit protection, and input offset adjust capability.

The bandwidth and slew rate of the EL2020 are relatively independent of the closed loop gain taken. The 50 MHz bandwidth at unity gain only reduces to 30 MHz at a gain of 10. The EL2020 may be used in most applications where a conventional op amp is used, with a big improvement in speed power product.

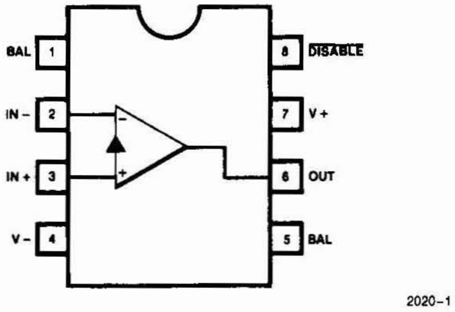
Elantec products and facilities comply with Elantec document, QRA-1: *Processing-Monolithic Products.*

Connection Diagrams

SOL



DIP



Manufactured under U.S. Patent No. 4,893,091.

Absolute Maximum Ratings (25°C)

V_S	Supply Voltage	±18V or 36V
V_{IN}	Input Voltage	±15V or V_S
ΔV_{IN}	Differential Input Voltage	±10V
I_{IN}	Input Current (Pins 2 or 3)	±10 mA
I_{INS}	Input Current (Pins 1, 5, or 8)	±5 mA
P_D	Maximum Power Dissipation (See Curves)	1.25W
I_{OP}	Peak Output Current	Short Circuit Protected
	Output Short Circuit Duration (Note 2)	Continuous

T_A	Operating Temperature Range	−40°C to +85°C
T_J	Operating Junction Temperature Plastic Package, SOL	150°C
T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

Open Loop Characteristics $V_S = \pm 15V$

Parameter	Description	Temp	Limits			Test Level	Units
			Min	Typ	Max		
V_{OS} (Note 1)	Input Offset Voltage	25°C	−10	3	+10	I	mV
		T_{MIN}, T_{MAX}	−15		+15	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			−30		V	μV/°C
CMRR (Note 3)	Common Mode Rejection Ratio	ALL	50	60		II	dB
PSRR (Note 4)	Power Supply Rejection Ratio	25°C	65	75		I	dB
		T_{MIN}, T_{MAX}	60			III	dB
$+I_{IN}$	Non-inverting Input Current	25°C, T_{MAX}	−15	5	+15	II	μA
		T_{MIN}	−25		+25	III	μA
$+R_{IN}$	Non-Inverting Input Resistance	ALL	1	5		II	MΩ
+IPSR (Note 4)	Non-Inverting Input Current Power Supply Rejection	25°C, T_{MAX}		0.05	0.5	II	μA/V
		T_{MIN}			1.0	III	μA/V
$-I_{IN}$ (Note 1)	−Input Current	25°C, T_{MAX}	−40	10	+40	II	μA
		T_{MIN}	−50		+50	III	μA

Open Loop Characteristics $V_S = \pm 15V$ — Contd.

Parameter	Description	Temp	Limits			Test Level	Units
			Min	Typ	Max		
−ICMR (Note 3)	−Input Current Common Mode Rejection	25°C, T_{MAX}		0.5	2.0	II	μA/V
		T_{MIN}			4.0	III	μA/V
−IPSR (Note 4)	−Input Current Power Supply Rejection	25°C, T_{MAX}		0.05	0.5	II	μA/V
		T_{MIN}			1.0	III	μA/V
R_{ol}	Transimpedence ($\Delta V_{OUT}/\Delta(-I_{IN})$) $R_L = 400\Omega$, $V_{OUT} = \pm 10V$	25°C, T_{MAX}	300	1000		II	V/mA
		T_{MIN}	50			III	V/mA
A_{VOL1}	Open Loop DC Voltage Gain $R_L = 400\Omega$, $V_{OUT} = \pm 10V$	25°C, T_{MAX}	70	80		II	dB
		T_{MIN}	60			III	dB
A_{VOL2}	Open Loop DC Voltage Gain $R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	25°C, T_{MAX}	60	70		II	dB
		T_{MIN}	55			III	dB
V_O	Output Voltage Swing $R_L = 400\Omega$	25°C, T_{MAX}	±12	±13		II	V
		T_{MIN}	±11			III	V
I_{OUT}	Output Current $R_L = 400\Omega$	25°C, T_{MAX}	±30	±32.5		II	mA
		T_{MIN}	±27.5			III	mA
I_s	Quiescent Supply Current	25°C		9	12	I	mA
		T_{MIN}, T_{MAX}			15	III	mA
$I_{s\,off}$	Supply Current, Disabled, $V_8 = 0V$	ALL		5.5	7.5	II	mA
I_{logic}	Pin 8 Current, Pin 8 = 0V	ALL		1.1	1.5	II	mA
I_D	Min Pin 8 Current to Disable	ALL		120	250	II	μA
I_e	Max Pin 8 Current to Enable	ALL			30	II	μA

AC Closed Loop Characteristics EL2020C $V_S = \pm 15V, T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level	Units
	Closed Loop Gain of 1 V/V (0 dB), $R_F = 1\ k\Omega$					
SR1	Slew Rate, $R_l = 400\Omega$, $V_O = \pm 10V$, test at $V_O = \pm 5V$	300	500		I	V/µs
FPBW1	Full Power Bandwidth (Note 5)	4.77	7.95		I	MHz
t_r1	Rise Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		6		V	ns
t_f1	Fall Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		6		V	ns
t_p1	Propagation Delay, $R_l = 100\Omega$, $V_{OUT} = 1V$, 50% Points		8		V	ns
	Closed Loop Gain of 1 V/V (0 dB), $R_F = 820\Omega$					
BW	−3 dB Small Signal Bandwidth, $R_l = 100\Omega$, $V_O = 100\ mV$		50		V	MHz
t_s	1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$		50		V	ns
t_s	0.1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$		90		V	ns
	Closed Loop Gain of 10 V/V (20 dB), $R_F = 1\ k\Omega$, $R_G = 111\Omega$					
SR10	Slew Rate, $R_l = 400\Omega$, $V_O = \pm 10V$, Test at $V_O = \pm 5V$	300	500		I	V/µs
FPBW10	Full Power Bandwidth (Note 5)	4.77	7.95		I	MHz
t_r10	Rise Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		25		V	ns
t_f10	Fall Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		25		V	ns
t_p10	Propagation Delay, $R_l = 100\Omega$, $V_{OUT} = 1V$, 50% points		12		V	ns
	Closed Loop Gain of 10 V/V (20 dB), $R_F = 680\Omega$, $R_G = 76\Omega$					
BW	−3 dB Small Signal Bandwidth, $R_l = 100\Omega$, $V_O = 100\ mV$		30		V	MHz
t_s	1% Settling Time, $R_l = 400\ \Omega$, $V_O = 10V$		55		V	ns
t_s	0.1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$		280		V	ns

Note 1: The offset voltage and inverting input current can be adjusted with an external 10 kΩ pot between pins 1 and 5 with the wiper connected to V_{CC} (Pin 7) to make the output offset voltage zero.

Note 2: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

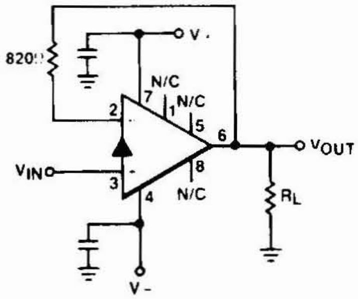
Note 3: $V_{CM} = \pm 10V$.

Note 4: $\pm 4.5V \le V_S \le \pm 18V$.

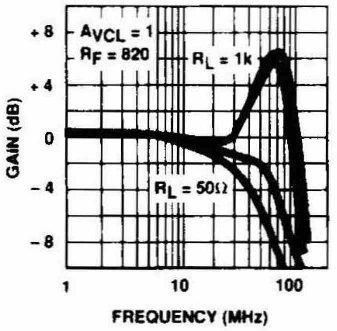
Note 5: Full Power Bandwidth is guaranteed based on Slew Rate measurement. $FPBW = SR/2\pi V_{peak}$.

Typical Performance Curves Non-Inverting Gain of One

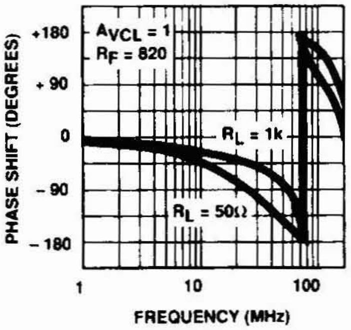
$A_{VCL} = +1$



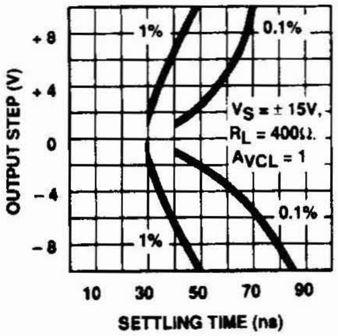
Gain vs Frequency



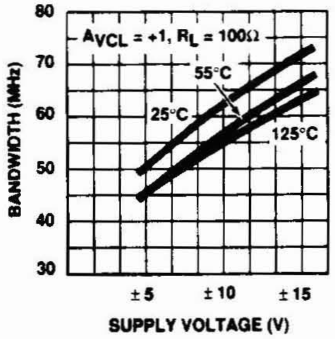
Phase Shift vs Frequency



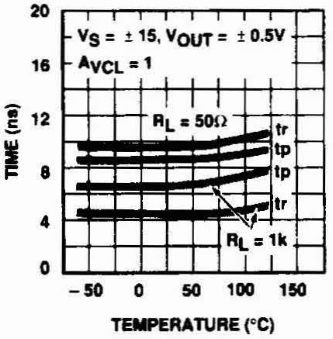
Settling Time vs Output Swing



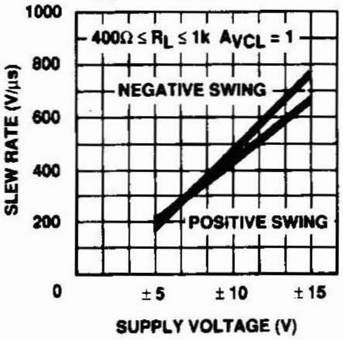
−3 dB Bandwidth vs Supply Voltage



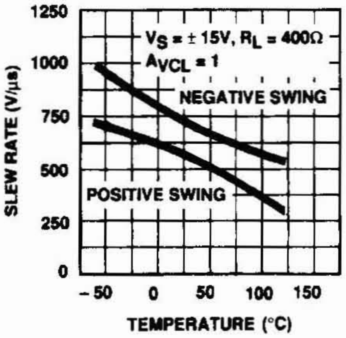
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



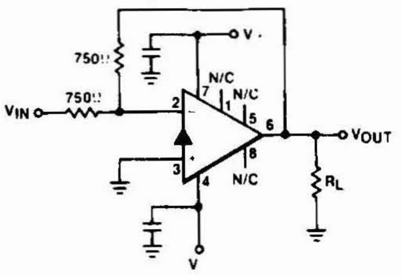
Slew Rate vs Temperature



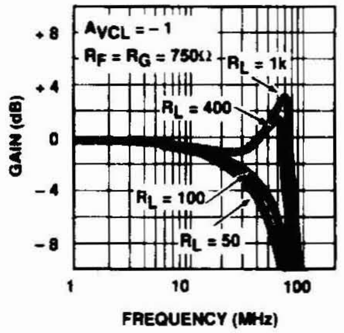
2020-4

Typical Performance Curves — Contd. Inverting Gain of One

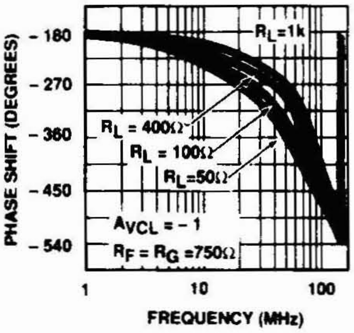
$A_{VCL} = -1$


750Ω
750Ω
VIN
V+
N/C
N/C
N/C
VOUT
RL
V−
2
3
4
5
6
7
8
1

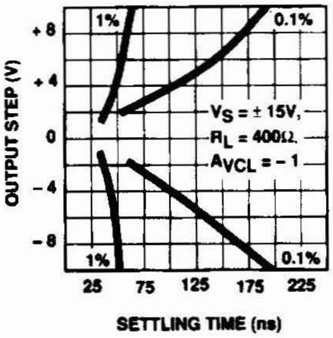
Gain vs Frequency



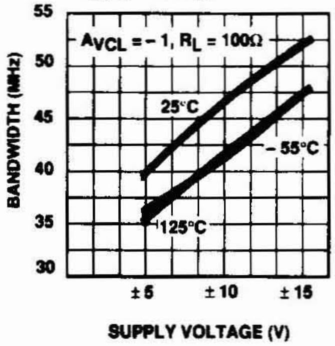
Phase Shift vs Frequency



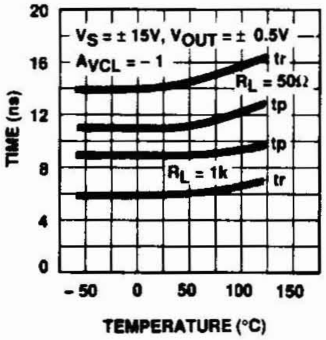
Settling Time vs Output Swing



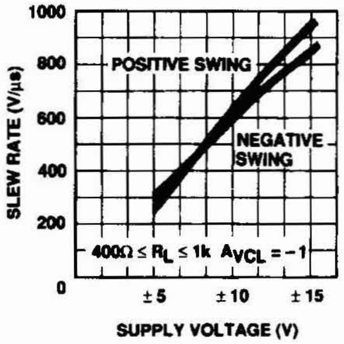
−3 dB Bandwidth vs Supply Voltage



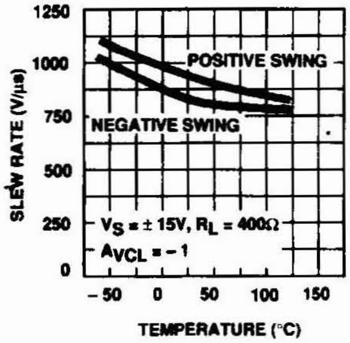
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



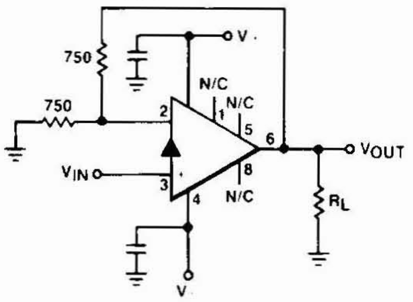
Slew Rate vs Temperature



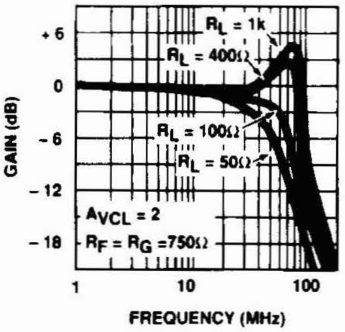
2020-5

Typical Performance Curves — Contd. Non-Inverting Gain of Two

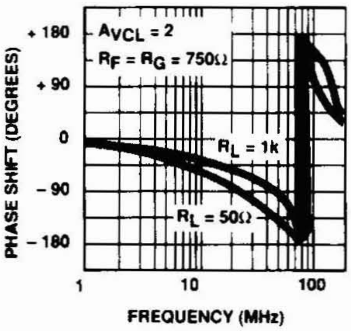
A_{VCL} = +2



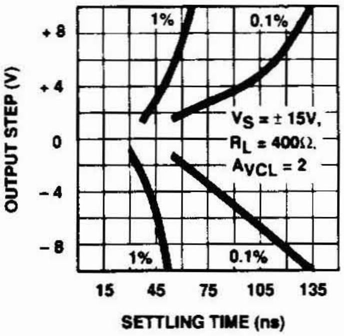
Gain vs Frequency



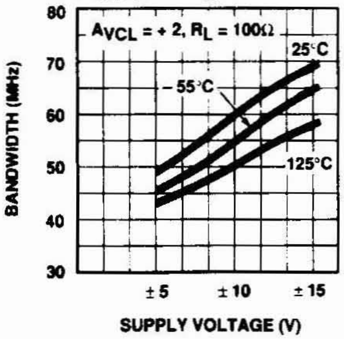
Phase Shift vs Frequency



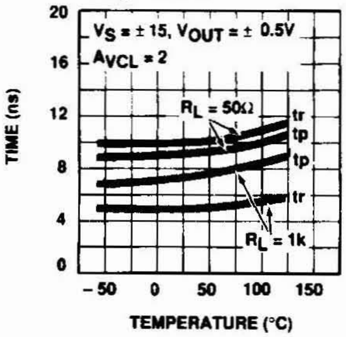
Settling Time vs Output Swing



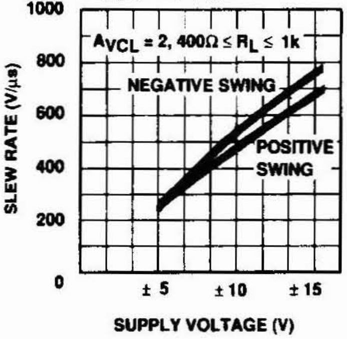
−3 dB Bandwidth vs Supply Voltage



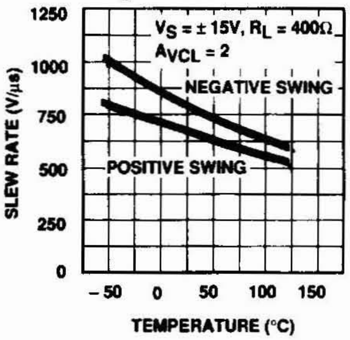
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



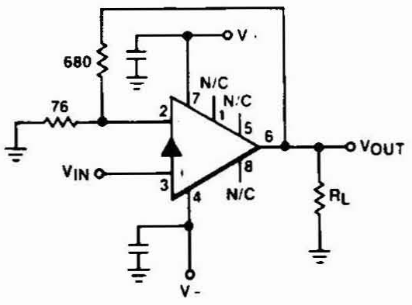
Slew Rate vs Temperature



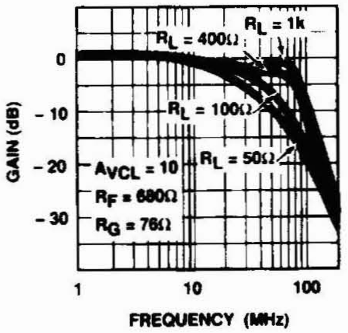
2020-6

Typical Performance Curves — Contd. Non-Inverting Gain of Ten

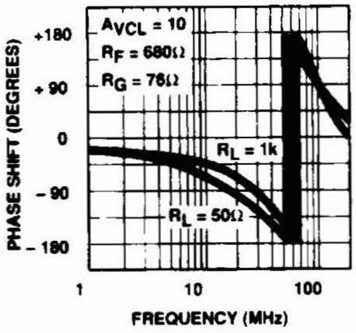
A_{VCL} = +10


680
76
V+
V-
N/C
N/C
N/C
N/C
1
2
3
4
5
6
7
8
VIN
VOUT
RL

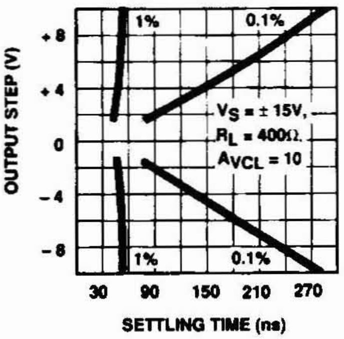
Gain vs Frequency



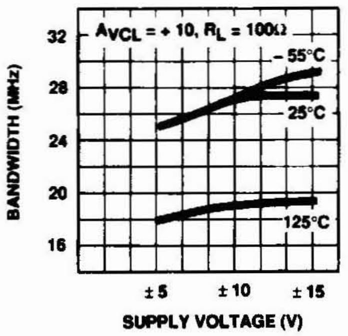
Phase Shift vs Frequency



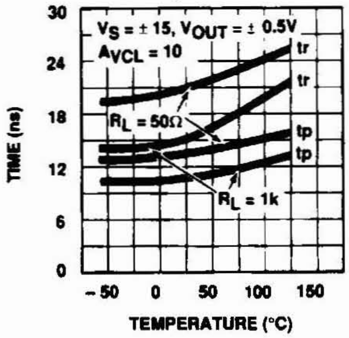
Settling Time vs Output Swing



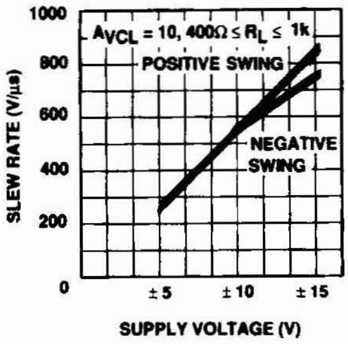
−3 dB Bandwidth vs Supply Voltage



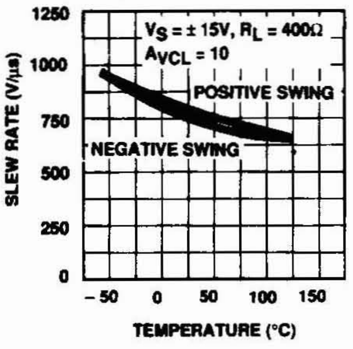
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



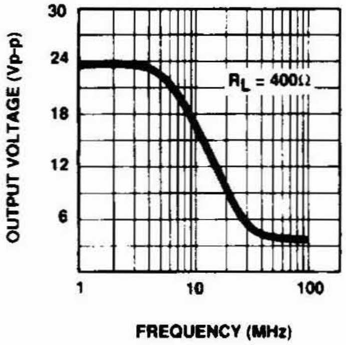
Slew Rate vs Temperature



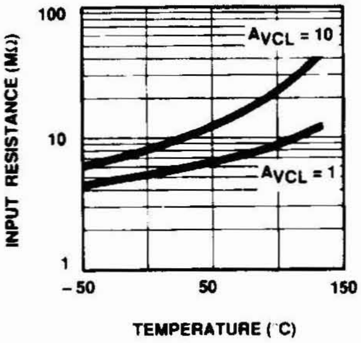
2020-7

Typical Performance Curves — Contd.

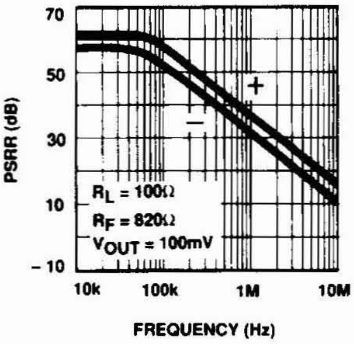
Maximum Undistorted Output Voltage vs Frequency



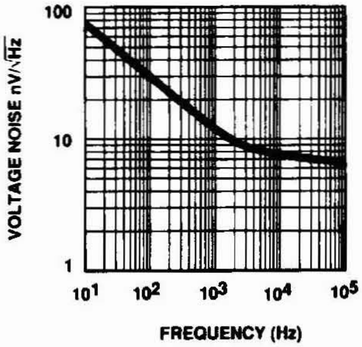
Input Resistance vs Temperature



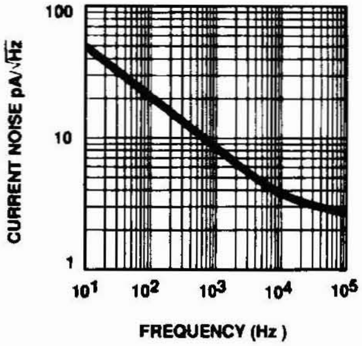
PSRR vs Frequency



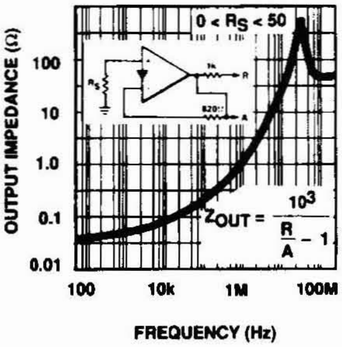
Voltage Noise vs Frequency



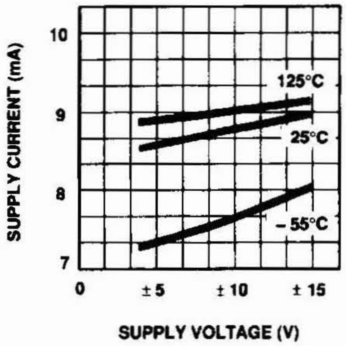
Current Noise vs Frequency



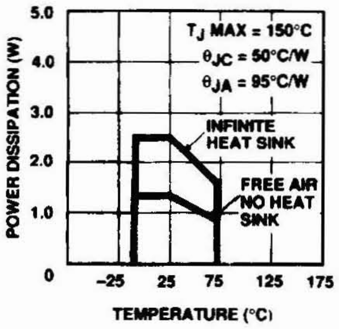
Output Impedance vs Frequency



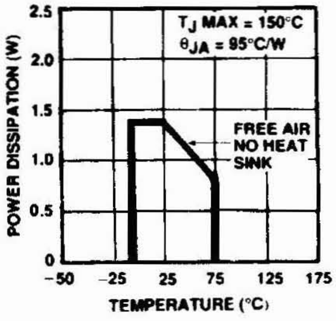
Supply Current vs Supply Voltage



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2020-8

Application Information

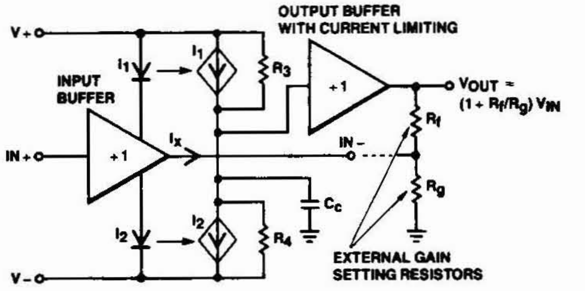
Theory of Operation

The EL2020 has a unity gain buffer similar to the EL2003 from the non-inverting input to the inverting input. The error signal of the EL2020 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is the transresistance (R_{OL}) of the EL2020 [$V_{OUT} = R_{OL} * I_{INV}$]. Since R_{OL} is very large ($\approx 10^6$), the current flowing into the inverting input in the steady state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first order approximation for circuit analysis, namely that...

1. The voltage across the inputs $\approx$ 0 and
2. The current into the inputs is $\approx$ 0

Simplified Block Diagram of EL2020



2020-10

Resistor Value Selection and Optimization

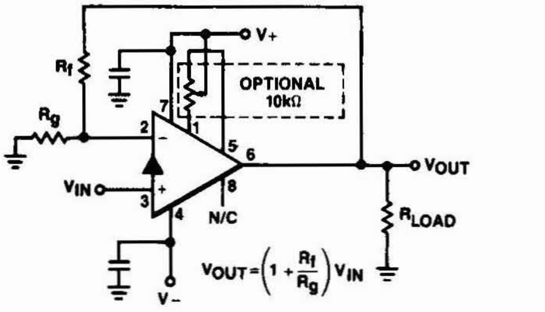
The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2020. A nominal value for the feedback resistor is 1 kΩ, which is the value used for production testing. This value guarantees stability. For a given gain, the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth will be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed loop transfer function which results from stray capacitance between the inverting input and ground.

Power Supplies

The EL2020 may be operated with single or split power supplies as low as ±3V (6V total) to as high as ±18V (36V total). The slew rate degrades significantly for supply voltages less than ±5V (10V total), but the bandwidth only changes 25% for supplies from ±3V to ±18V. It is not necessary to use equal value split power supplies, i.e., −5V and +12V would be excellent for 0V to 1V video signals. Bypass capacitors from each supply pin to a ground plane are recommended. The EL2020 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate supply ringing and the errors it might cause, a 4.7 µF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rate and longer settling times.

Non-Inverting Amplifier



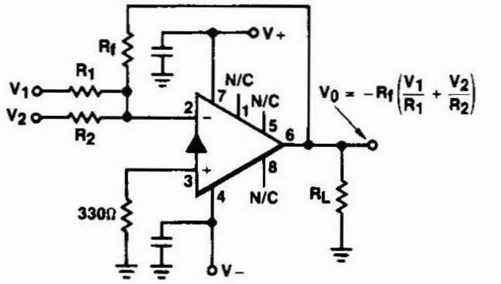
2020-11

EL2020 Typical Non-Inverting Amplifier Characteristics

A_V	R_F	R_G	Bandwidth	10V Settling Time	
				1%	0.1%
+1	820Ω	None	50 MHz	50 ns	90 ns
+2	750Ω	750Ω	50 MHz	50 ns	100 ns
+5	680Ω	170Ω	50 MHz	50 ns	200 ns
+10	680Ω	76Ω	30 MHz	55 ns	280 ns

Application Information — Contd.

Summing Amplifier



2020-12

EL2020 Typical Inverting Amplifier Characteristics

A_V	R_F	R_1, R_2	Bandwidth	10V Settling Time	
				1%	0.1%
−1	750Ω	750Ω	40 MHz	50 ns	130 ns
−2	750Ω	375Ω	40 MHz	55 ns	160 ns
−5	680Ω	130Ω	40 MHz	55 ns	160 ns
−10	680Ω	68Ω	30 MHz	70 ns	170 ns

Input Range

The non-inverting input to the EL2020 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit.

The input charactersitics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that Schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

Source Impedance

The EL2020 is fairly tolerant of variations in source impedances. Capacitive sources cause no problems at all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources may cause oscillations; a 1 kΩ resistor in series with the input lead will usually eliminate problems without sacrificing too much speed.

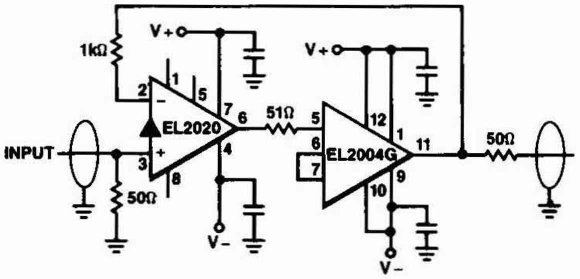
Current Limit

The EL2020 has internal current limits that protect the output transistors. The current limit goes down with junction temperature rise. At a junction temperature of +175°C the current limits are at about 50 mA. If the EL2020 output is shorted to ground when operating on ±15V supplies, the power dissipation could be as great as 1.1W. A heat sink is required in order for the EL2020 to survive an indefinite short. Recovery time to come out of current limit is about 50 ns.

Using the 2020 with Output Buffers

When more output current is required, a wideband buffer amplifier can be included in the feedback loop of the EL2020. With the EL2003 the subsystem overshoots about 10% due to the phase lag of the EL2003. With the EL2004 in the loop, the overshoot is less than 2%. For even more output current, several buffers can be paralleled.

EL2020 Buffered with an EL2004



2020-13

Capacitive Loads

The EL2020 is like most high speed feedback amplifiers in that it does not like capacitive loads between 50 pF and 1000 pF. The output resistance works with the capacitive load to form a second non-dominate pole in the loop. This results in excessive peaking and overshoot and can lead to oscillations. Standard resistive isolation techniques used with other op amps work well to isolate capacitive loads from the EL2020.

Application Information — Contd.

Offset Adjust

To calculate the amplifier system offset voltage from input to output we use the equation:

Output Offset Voltage = $V_{OS}\ (R_F/R_G + 1) \pm I_{BIAS}\ (R_F)$

The EL2020 output offset can be nulled by using a 10 kΩ potentiometer from pins 1 to 5 with the slider tied to pin 7 ($+V_{CC}$). This adjusts both the offset voltage and the inverting input bias current. The typical adjustment range is ±80 mV at the output.

Compensation

The EL2020 is internally compensated to work with external feedback resistors for optimum bandwidth over a wide range of closed loop gain. The part is designed for a nominal 1 kΩ of feedback resistance, although it is possible to get more bandwidth by decreasing the feedback resistance.

The EL2020 becomes *less* stable by adding capacitance in parallel with the feedback resistor, so feedback capacitance is not recommended.

The EL2020 is also sensitive to stray capacitance from the inverting input to ground, so the board should be laid out to keep the physical size of this node small, with ground plane kept away from this node.

Active Filters

The EL2020's low phase lag at high frequencies makes it an excellent choice for high performance active filters. The filter response more closely approaches the theoritical response than with conventional op amps due to the EL2020's smaller propagation delay. Because the internal compensation of the EL2020 depends on resistive feedback, the EL2020 should be set up as a gain block.

Driving Cables

The EL2020 was designed with driving coaxial cables in mind. With 30 mA of output drive and low output impedance, driving one to three 75Ω double terminated coax cables with one EL2020 is practical. Since it is easy to set up a gain of +2, the double matched method is the best way to drive coax cables, because the impedance match on both ends of the cable will suppress reflections. For a discussion on some of the other ways to drive cables, see the section on driving cables in the EL2003 data sheet.

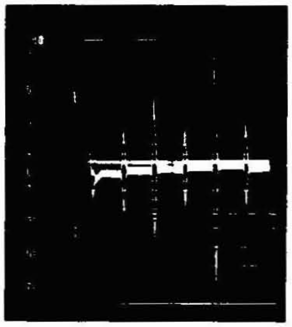
Video Performance Characteristics

The EL2020 makes an excellent gain block for video systems, both RS-170 (NTSC) and faster. It is capable of driving 3 double terminated 75Ω cables with distortion levels acceptable to broadcasters. A common video application is to drive a 75Ω double terminated coax with a gain of 2.

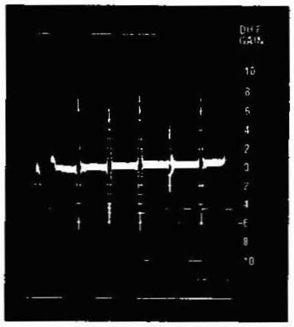
To measure the video performance of the EL2020 in the non-inverting gain of 2 configuration, 5 identical gain-of-two circuits were cascaded (with a divide by two 75Ω attenuator between each stage) to increase the errors.

The results, shown in the photos, indicate the entire system of 5 gain-of-two stages has a differential gain of 0.5% and a differential phase of 0.5°. This implies each device has a differential gain/phase of 0.1% and 0.1°, but these are too small to measure on single devices.

Differential Phase of 5 Cascaded Gain-Of-Two Stages



Differential Gain of 5 Cascaded Gain-Of-Two Stages



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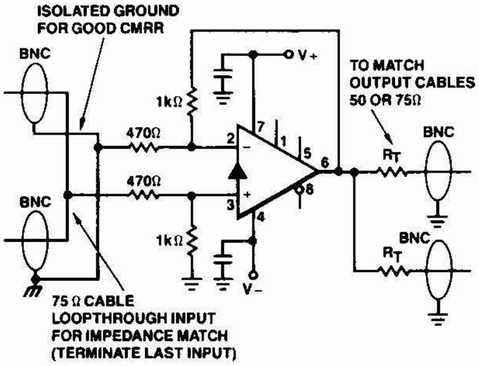
Application Information — Contd.

Video Distribution Amplifier

The distribution amplifier shown below features a difference input to reject common mode signals on the 75Ω coax cable input. Common mode rejection is often necessary to help to eliminate 60 Hz noise found in production environments.

Video Distribution Amplifier with Difference Input


ISOLATED GROUND
FOR GOOD CMRR
BNC
1kΩ
470Ω
470Ω
BNC
1kΩ
V+
V−
2
3
7
1
5
6
8
4
TO MATCH
OUTPUT CABLES
50 OR 75Ω
BNC
R_T
BNC
R_T
75 Ω CABLE
LOOPTHROUGH INPUT
FOR IMPEDANCE MATCH
(TERMINATE LAST INPUT)
2020-15

EL2020 Disable/Enable Operation

The EL2020 has an enable/disable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or returned to pin 7, V_{CC}. When more than 250 μA is pulled from pin 8, the EL2020 is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is halved. To make it easy to use this feature, there is an internal resistor to limit the current to a safe level (~ 1.1 mA) if pin 8 is grounded.

To draw current out of pin 8 an "open collector output" logic gate or a discrete NPN transistor can be used. This logic interface method has the advantage of level shifting the logic signal from 5V supplies to whatever supply the EL2020 is operating on without any additional components.

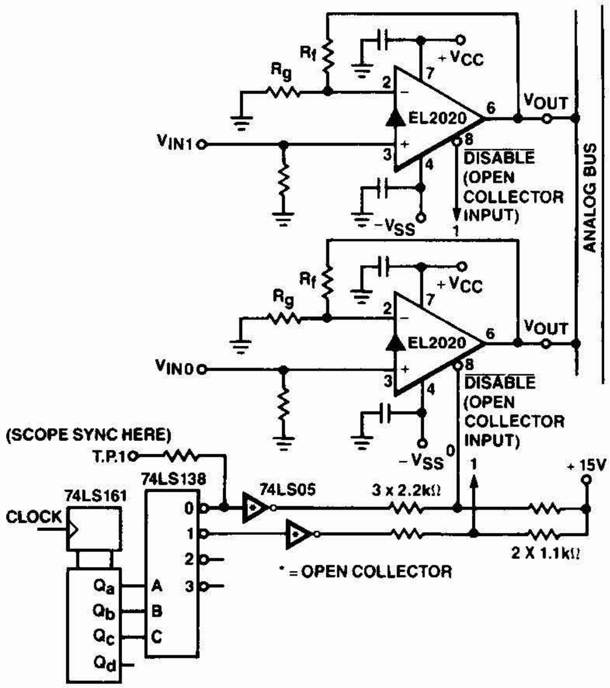
Using the EL2020 as a Multiplexer

An interesting use of the enable feature is to combine several amplifiers in parallel with their outputs common. This combination then acts similar to a MUX in front of an amplifier. A typical circuit is shown.

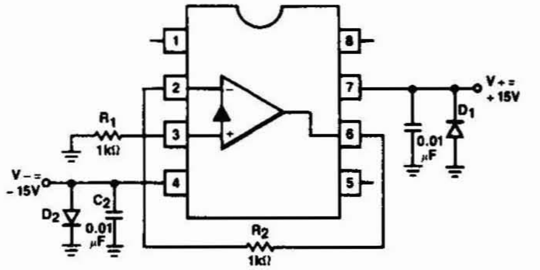
When the EL2020 is disabled, the DC output impedance is very high, over 10 kΩ. However there is also an output capacitance that is non-linear. For signals of less than 5V peak to peak, the output capacitance looks like a simple 15 pF capacitor. However, for larger signals the output capacitance becomes much larger and non-linear.

The example multiplexer will switch between amplifiers in 5 μs for signals of less than ± 2V on the outputs. For full output signals of 20V peak to peak, the selection time becomes 25 μs. The disabled outputs also present a capacitive load and therefore only three amplifiers can have their outputs shorted together. However an unlimited number can sum together if a small resistor (25Ω) is inserted in series with each output to isolate it from the "bus". There will be a small gain loss due to the resistors of course.

Using the EL2020 as a Multiplexer


R_f
R_g
+V_{CC}
EL2020
V_{OUT}
V_{IN1}
$\overline{\text{DISABLE}}$
(OPEN
COLLECTOR
INPUT)
−V_{SS}
1
R_f
R_g
+V_{CC}
EL2020
V_{OUT}
V_{IN0}
$\overline{\text{DISABLE}}$
(OPEN
COLLECTOR
INPUT)
−V_{SS}
0
1
ANALOG BUS
(SCOPE SYNC HERE)
T.P.1
74LS138
74LS161
CLOCK
74LS05
3 x 2.2kΩ
+ 15V
2 X 1.1kΩ
* = OPEN COLLECTOR
Q_a
Q_b
Q_c
Q_d
A
B
C
0
1
2
3
2020-16

Burn-In Circuit


1
2
3
4
5
6
7
8
R1
1kΩ
V− = −15V
D2
C2
0.01 μF
R2
1kΩ
V+ = +15V
D1
0.01 μF

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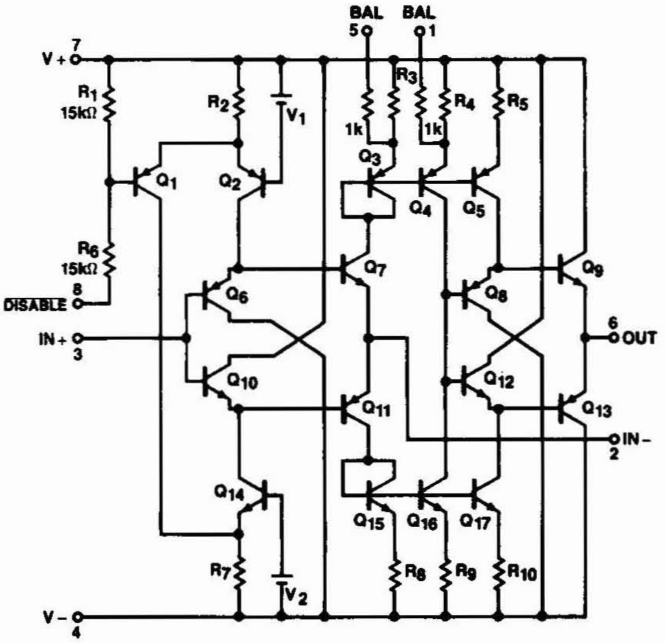
Pin numbers are for DIP Packages.
All Packages Use the Same Schematic.

Equivalent Circuit


BAL
5
BAL
1
V+
7
R1
15kΩ
R2
V1
1k
R3
1k
R4
R5
Q1
Q2
Q3
Q4
Q5
R6
15kΩ
8
DISABLE
Q6
Q7
Q8
Q9
IN+
3
6
OUT
Q10
Q11
Q12
Q13
IN−
2
Q14
Q15
Q16
Q17
R7
V2
R8
R9
R10
V−
4

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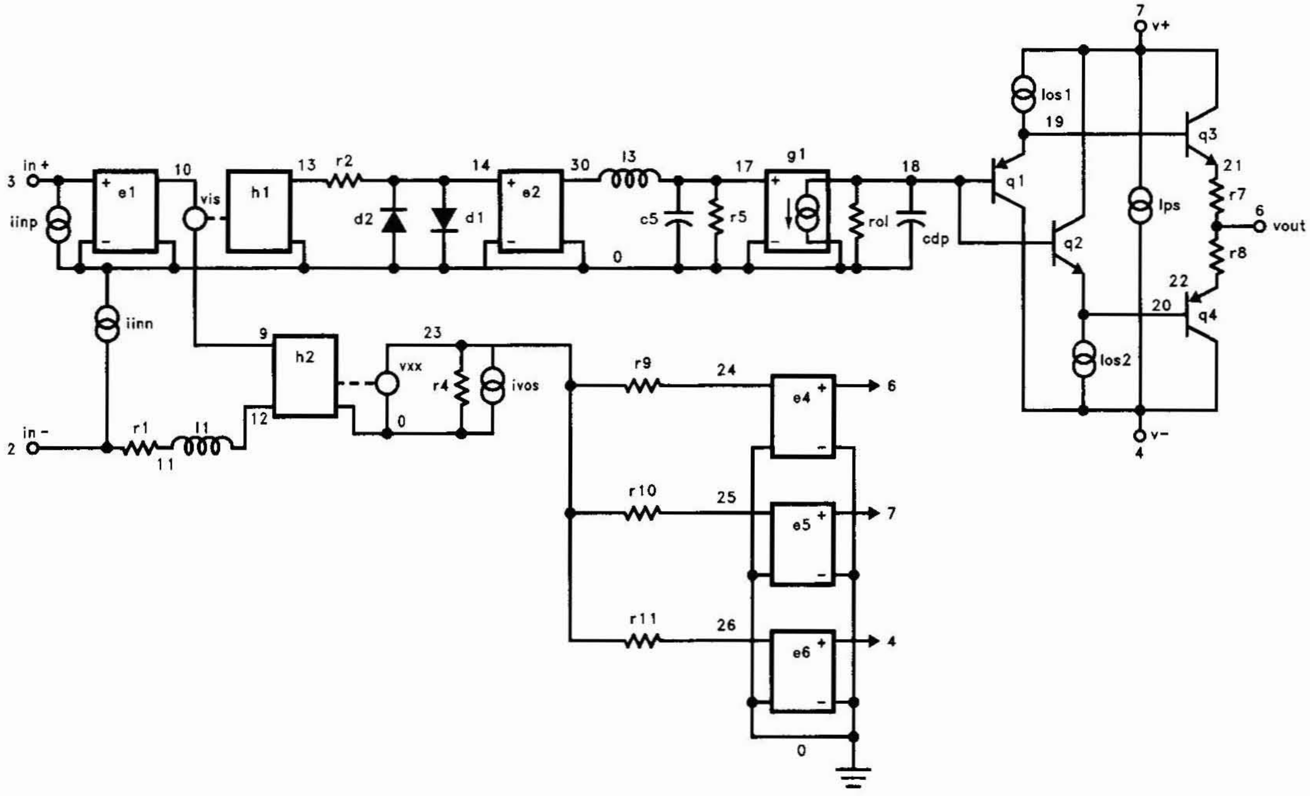
EL2020 Macromodel

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                   |      -input
*                   |      |      +Vsupply
*                   |      |      |      -Vsupply
*                   |      |      |      |      output
*                   |      |      |      |      |
.subckt M2020       3      2      7      4      6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 29nH
iinp 3 0 10μA
iinm 2 0 5μA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
15 30 17 1.5μH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 1Meg
cdp 18 0 5pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
```

EL2020 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply
*
ips 7 4 3mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 6 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 1K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.2nS)
.model qp pnp (is=5e-15 bf=100 tf=0.2nS)
.model dclamp d(is=1e-30 ibv=0.266 bv=1.67 n=4)
.ends
```

EL2020 Macromodel


7
v+
los1
19
q3
21
r7
6
vout
r8
22
20
q4
q1
q2
lps
los2
v−
4
in+
3
iinp
+
e1
−
10
vis
h1
13
r2
d2
d1
14
+
e2
−
30
l3
c5
17
r5
g1
+
−
rol
18
cdp
0
iinn
9
h2
12
23
vxx
r4
ivos
0
in−
2
r1
l1
11
r9
24
e4
+
−
6
r10
25
e5
+
−
7
r11
26
e6
+
−
4
0

2020-22

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2030C
120 MHz Current Feedback Amplifier

Features

- −3 dB bandwidth = 120 MHz, $A_V = 1$
- −3 dB bandwidth = 110 MHz, $A_V = 2$
- 0.01% differential gain and 0.01° differential phase (NTSC, PAL)
- 0.05% differential gain and 0.02° differential phase (HDTV)
- Slew rate 2000 V/µs
- 65 mA output current
- Drives ±10V into 200Ω load
- Characterized at ±5V and ±15V
- Low voltage noise
- Current mode feedback
- Settling time of 40 ns to 0.25% for a 10V step
- Output short circuit protected
- Low cost

Applications

- Video gain block
- Video distribution amplifier
- HDTV amplifier
- Residue amplifiers in ADC
- Current to voltage converter
- Coax cable driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2030CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2030CM	−40°C to +85°C	20-Lead SOL	MDP0027

General Description

The EL2030 is a very fast, wide bandwidth amplifier optimized for gains between −10 and +10. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

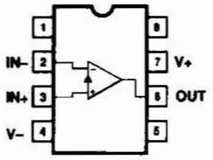
Due to its wide operating supply range (±15V) and extremely high slew rate of 2000 V/µs, the EL2030 drives ±10V into 200Ω at a frequency of 30 MHz, while achieving 110 MHz of small signal bandwidth at $A_V = +2$. This bandwidth is still 95 MHz for a gain of +10. On ±5V supplies the amplifier maintains a 90 MHz bandwidth for $A_V = +2$. When used as a unity gain buffer, the EL2030 has a 120 MHz bandwidth with the gain precision and low distortion of closed loop buffers.

The EL2030 features extremely low differential gain and phase, a low noise topology that reduces noise by a factor of 2 over competing amplifiers, and settling time of 40 ns to 0.25% for a 10V step. The output is short circuit protected. In addition, datasheet limits are guaranteed for ±5V and ±15V supplies.

Elantec's products and facilities comply with applicable quality specifications. See Elantec document, QRA-1: *Processing, Monolithic Integrated Circuits.*

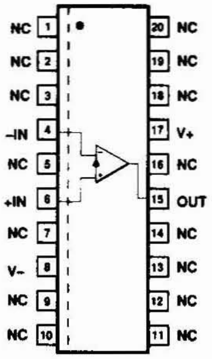
Connection Diagrams

Mini DIP



Top View

SOL



Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,893,091.

EL2030C

120 MHz Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V or 36V
V_{IN}	Input Voltage	±15V or V_S
ΔV_{IN}	Differential Input Voltage	±6V
P_D	Maximum Power Dissipation	See Curves
I_{IN}	Input Current	±10 mA
I_{OP}	Peak Output Current	Short Circuit Protected
	Output Short Circuit Duration (Note 1)	Continuous

T_A	Operating Temperature Range	−40°C to +85°C
T_J	Operating Junction Temperature	
	Plastic Packages	150°C
T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±15V, R_L = 200Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
							EL2030C	
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		10	20	I	mV
			T_{MIN}, T_{MAX}			30	III	mV
		V_S = ±5V	25°C		5	10	I	mV
			T_{MIN}, T_{MAX}			15	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift				25		V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		5	15	I	µA
			T_{MIN}, T_{MAX}			25	III	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		10	40	I	µA
			T_{MIN}, T_{MAX}			50	III	µA
$+R_{IN}$	+Input Resistance		Full	1.1	2.0		II	MΩ
C_{IN}	Input Capacitance		25°C		1		V	pF
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	Full	50	60		II	dB
−ICMR	Input Current Common Mode Rejection (Note 2)		25°C		5	10	I	µA/V
			T_{MIN}, T_{MAX}			20	III	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		Full	60	70		II	dB
+IPSR	+Input Current Power Supply Rejection (Note 3)		25°C		0.1	0.5	II	µA/V
			T_{MIN}, T_{MAX}			1.0	III	µA/V
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.5	5.0	II	µA/V
			T_{MIN}, T_{MAX}			8.0	III	µA/V

Open Loop DC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 200\Omega$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
							EL2030C	
R_{OL}	Transimpedance ($\Delta V_{OUT}/\Delta(-I_{IN})$) $V_{OUT} = \pm 10V$	$V_S = \pm 15V$	25°C	88	150		II	V/mA
			T_{MIN}, T_{MAX}	75			III	V/mA
	$V_{OUT} = \pm 2.5V$ (Note 6)	$V_S = \pm 5V$	25°C	80	120		II	V/mA
			T_{MIN}, T_{MAX}		70		III	V/mA
A_{VOL}	Open Loop DC Voltage Gain $V_{OUT} = \pm 10V$	$V_S = \pm 15V$	Full	60	70		II	dB
	$V_{OUT} = \pm 2.5V$ (Note 6)	$V_S = \pm 5V$	Full	56	65		II	dB
V_O	Output Voltage Swing (Note 6)	$V_S = \pm 15V$	Full	12	13		II	V
		$V_S = \pm 5V$	Full	3	3.5		II	V
I_{OUT}	Output Current (Note 9)	$V_S = \pm 15V$	Full	60	65		II	mA
		$V_S = \pm 5V$	Full	30	35		II	mA
R_{OUT}	Output Resistance		25°C		5		V	Ω
I_S	Quiescent Supply Current		Full		15	21	II	mA
I_{SC}	Short Circuit Current		25°C		85		V	mA

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +2$, $R_F = 820\Omega$, $R_G = 820\Omega$ and $R_L = 200\Omega$

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
							EL2030C	
SR	Slew Rate (Note 7)		25°C	1200	2000		IV	V/μs
FPBW	Full Power Bandwidth (Note 4)		25°C	19	31.8		IV	MHz
t_r, t_f	Rise Time. Fall Time	$V_{pp} = 250\ mV$	25°C		3		V	ns
t_s	Settling Time to 0.25% for 10V step (Note 5)		25°C		40		V	ns
ΔG	Differential Gain (Note 8)		25°C		0.01		V	% p-p
Δϕ	Differential Phase (Note 8)		25°C		0.01		V	° p-p
eN	Input Spot Noise at 1 kHz $R_G = 101$; $R_F = 909$		25°C		4		V	$nV/\sqrt{Hz}$

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 2: $V_{CM} = \pm 10V$ for $V_S = \pm 15V$. For $V_S = \pm 5V$, $V_{CM} = \pm 2.5V$.

Note 3: V_{OS} is measured at $V_S = \pm 4.5V$ and at $V_S = \pm 18V$. Both supplies are changed simultaneously.

Note 4: Full Power Bandwidth is specified based on Slew Rate measurement $FPBW = SR/2\pi V_P$.

Note 5: Settling Time measurement techniques are shown in: "Take The Guesswork Out of Settling Time Measurements", EDN, September 19, 1985. Available from the factory upon request.

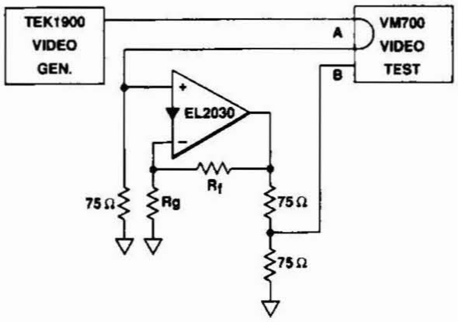
Note 6: $R_L = 100\Omega$.

Note 7: $V_O = \pm 10V$, tested at $V_O = \pm 5$. See test circuit.

Note 8: NTSC (3.58 MHz) and PAL (4.43 MHz).

Note 9: For $V_S = \pm 15V$, $V_{OUT} = \pm 10V$. For V_S $\pm 5V$, $V_{OUT} = \pm 2.5V$.

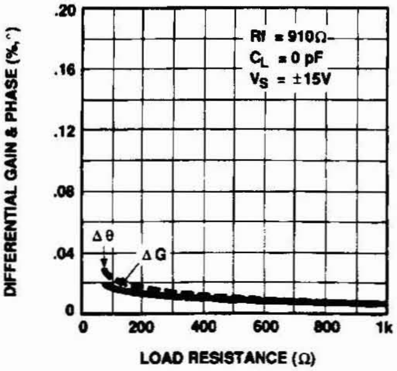
Typical Performance Curves


TEK1900
VIDEO
GEN.
VM700
VIDEO
TEST
A
B
+
−
EL2030
Rf
Rg
75Ω
75Ω
75Ω

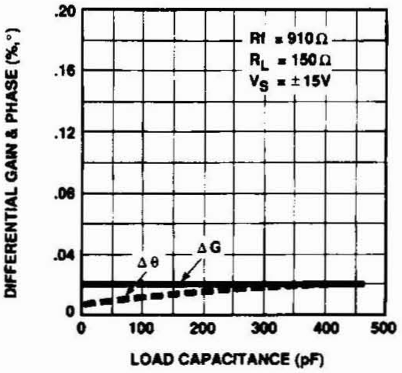
2030-5

Figure 1. NTSC Video Differential Gain and Phase Test Set-Up

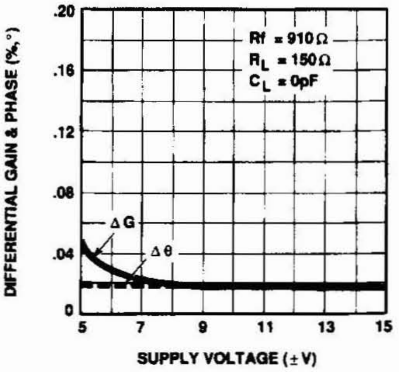
Differential Gain and Phase vs Load Resistance, Gain = +1



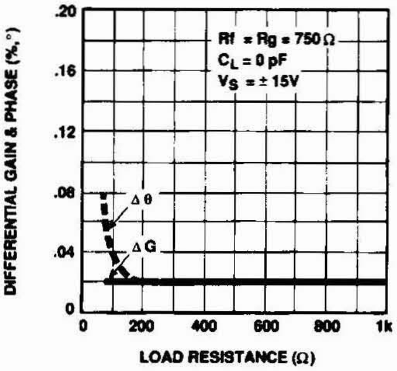
Differential Gain and Phase vs Load Capacitance, Gain = +1



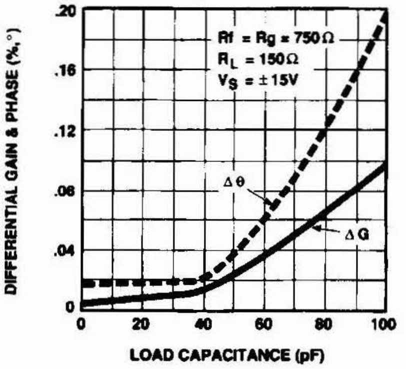
Differential Gain and Phase vs Supply Voltage, Gain = +1



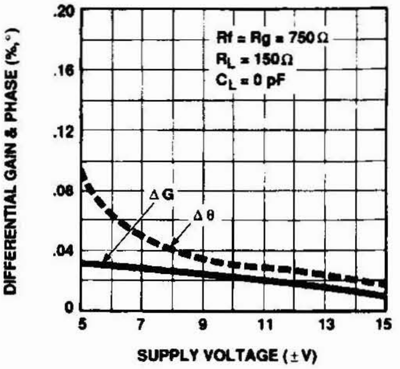
Differential Gain and Phase vs Load Resistance, Gain = +2



Differential Gain and Phase vs Load Capacitance, Gain = +2

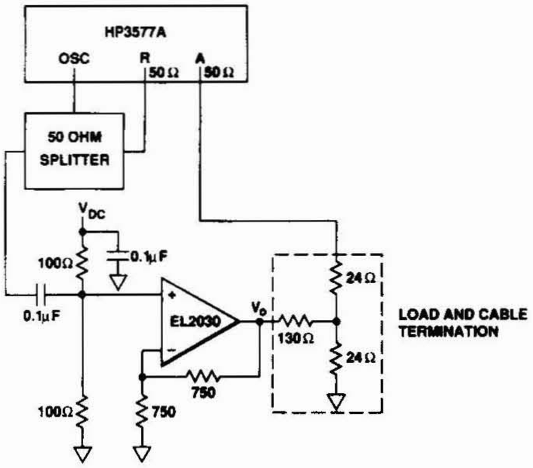


Differential Gain and Phase vs Supply Voltage, Gain = +2



2030-6

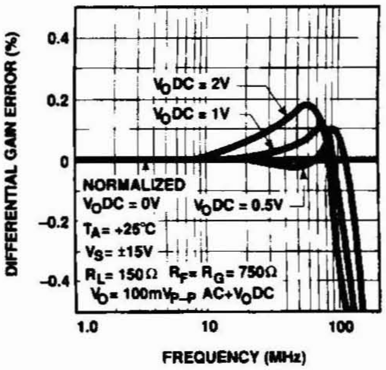
Typical Performance Curves — Contd.


HP3577A
OSC
R
A
50 Ω
50 Ω
50 OHM SPLITTER
V_{DC}
100Ω
0.1μF
0.1μF
EL2030
+
−
V_o
130 Ω
750
750
100Ω
24 Ω
24 Ω
LOAD AND CABLE TERMINATION

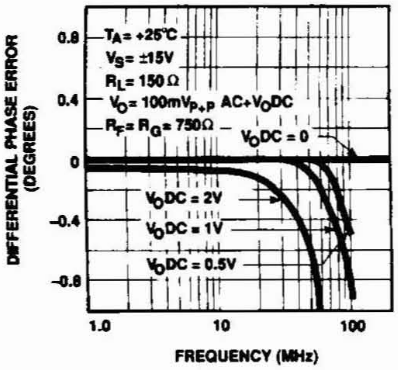
2030-7

Figure 2. HDTV and Wideband Video Differential Gain and Phase Test Set-Up

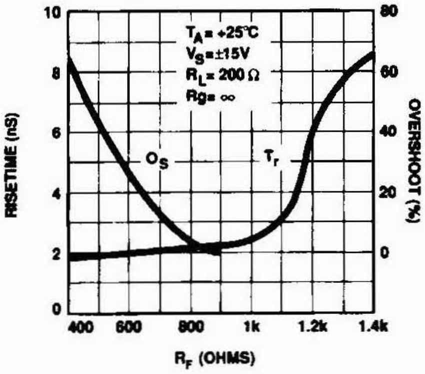
Differential Gain Error vs Frequency for Various DC Output Levels



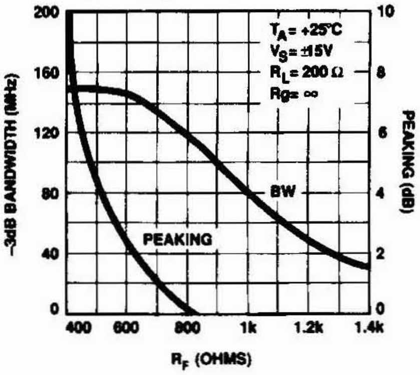
Differential Phase Error vs Frequency for Various DC Output Levels



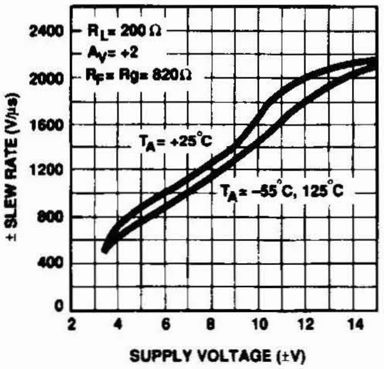
Risetime and Overshoot vs R_F for A_V = +1



Bandwidth and Peaking vs R_F for A_V = +1

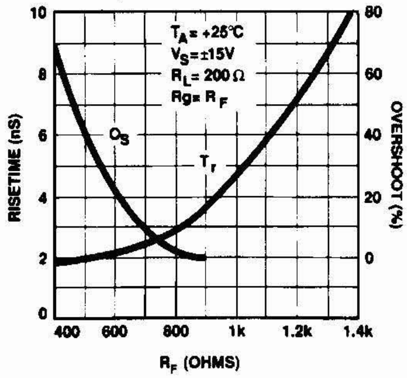


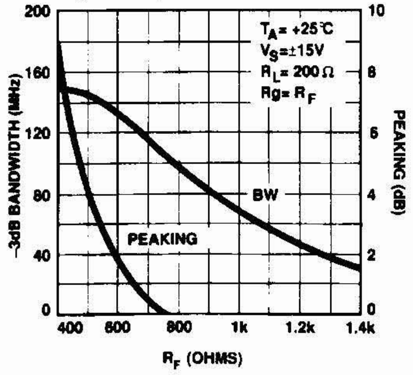
± Slew Rate vs Supply Voltage

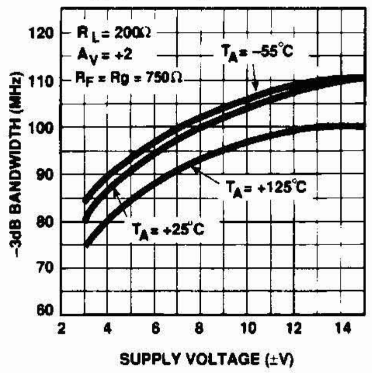


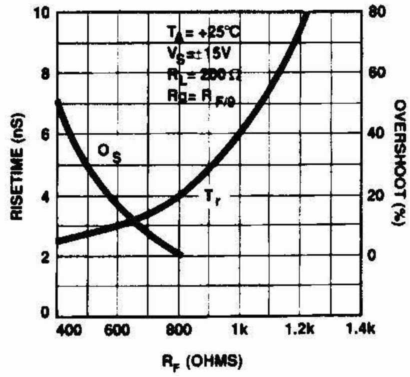
2030-8

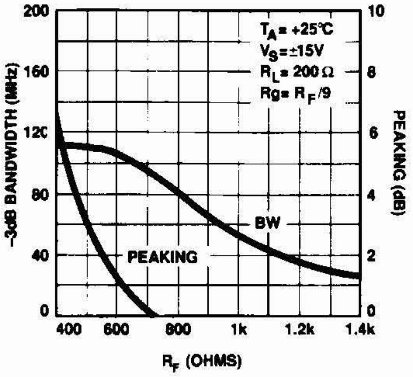
Typical Performance Curves — Contd.

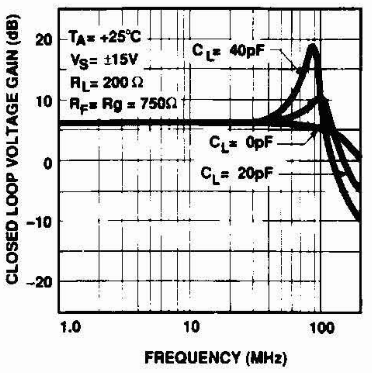

Risetime and Overshoot vs R_F for $A_V = +2$

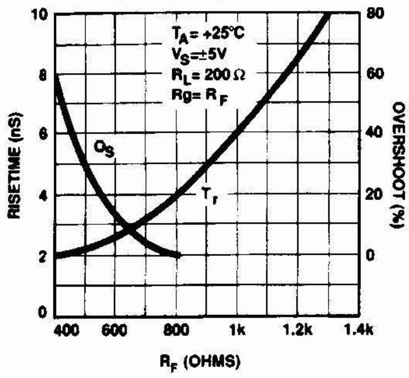

Bandwidth and Peaking vs R_F for $A_V = +2$

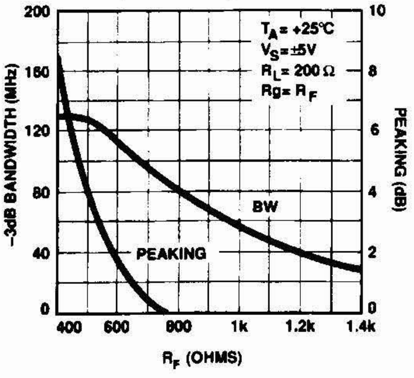

−3 dB Bandwidth vs Supply Voltage

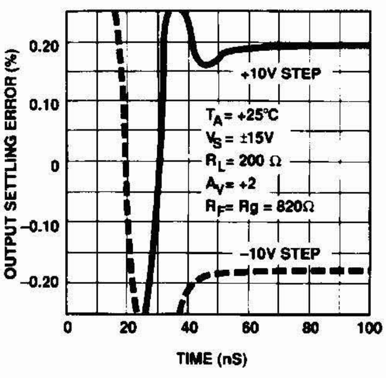

Risetime and Overshoot vs R_F for $A_V = +10$


Bandwidth and Peaking vs R_F for $A_V = +10$


Voltage Gain vs Frequency for $A_V = +2$, various Capacitive Loads


Risetime and Overshoot vs R_F for $A_V = +2$, $V_S = \pm5V$

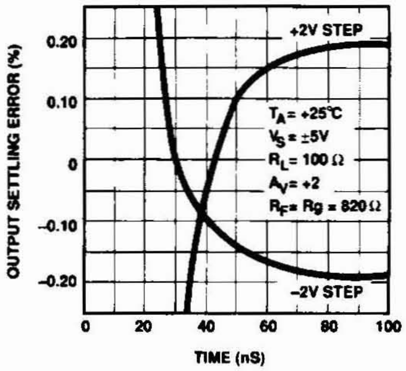

Bandwidth and Peaking vs R_F for $A_V = +2$, $V_S = +5V$


Output Settling Error vs Time

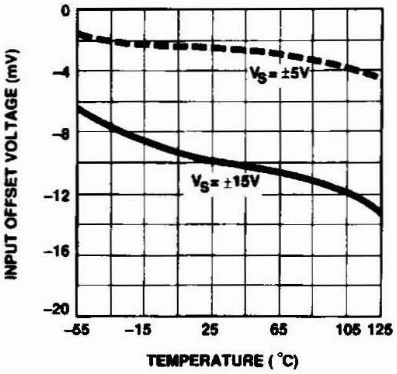
2030-9

Typical Performance Curves — Contd.

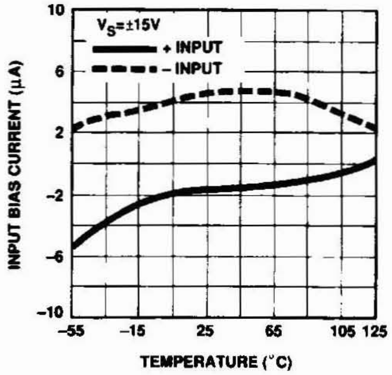
Output Settling Error vs Time, V_S = ±5V



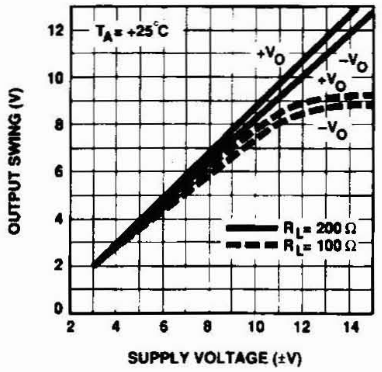
Input Offset Voltage vs Temperature



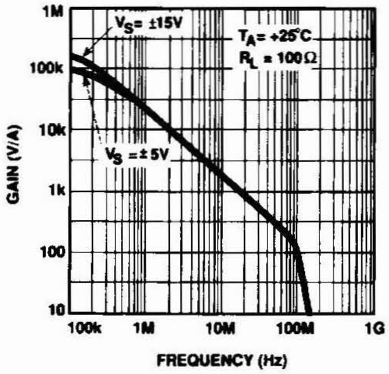
Input Bias Current vs Temperature



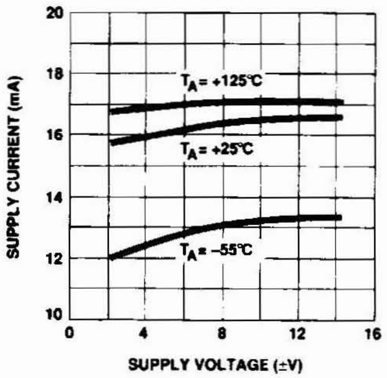
Output Swing vs Supply Voltage



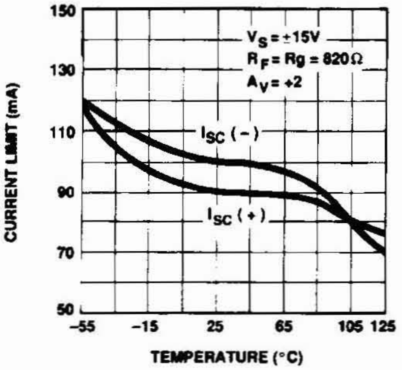
Transimpedance (R_{OL})



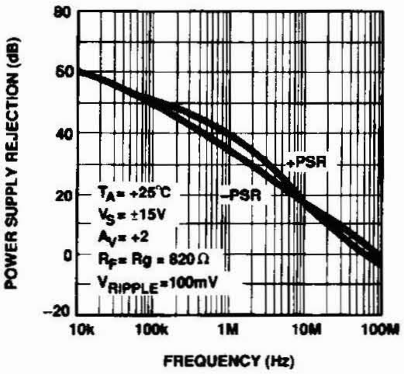
Supply Current vs Supply Voltage



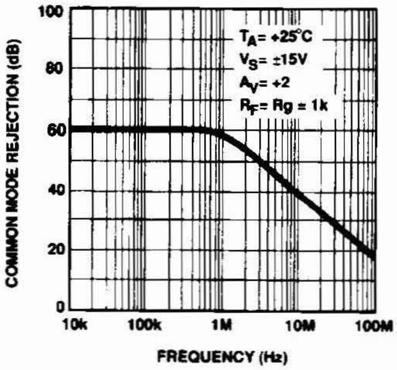
Current Limit vs Temperature



Power Supply Rejection vs Frequency



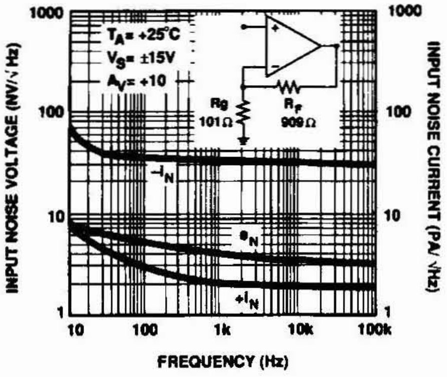
Common Mode Rejection vs Frequency



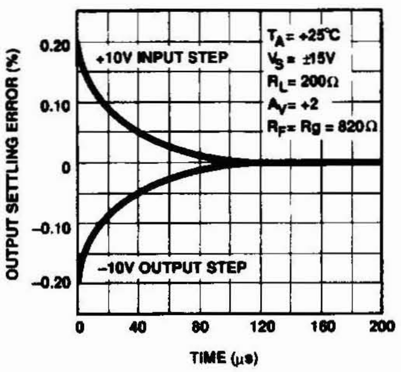
2030-10

Typical Performance Curves — Contd.

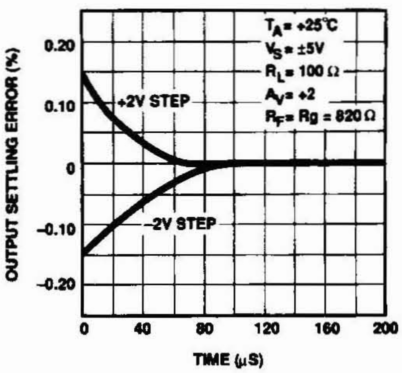
Equivalent Input Noise



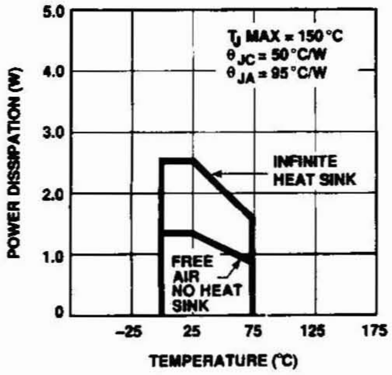
Long-Term Output Settling Error vs Time



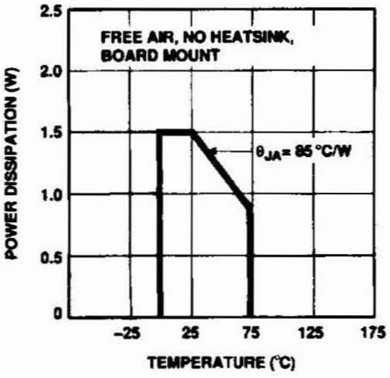
Long-Term Output Settling Error vs Time, V_S = ±5V



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



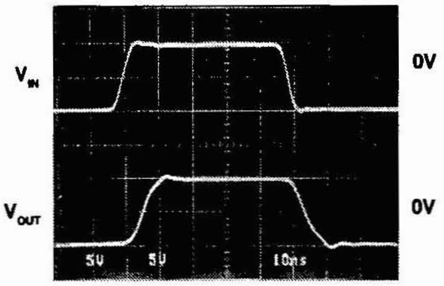
20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2030-11

Typical Performance Curves — Contd.

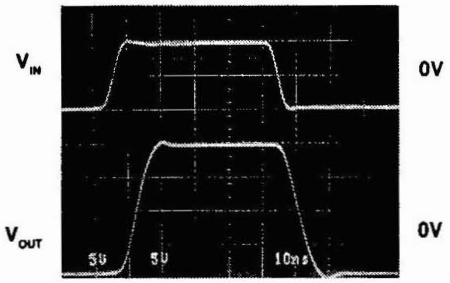
Large Signal Response



$A_V = +1$, $R_F = 1\ k\Omega$,
$R_L = 200\Omega$, $V_S = \pm15V$

2030-12

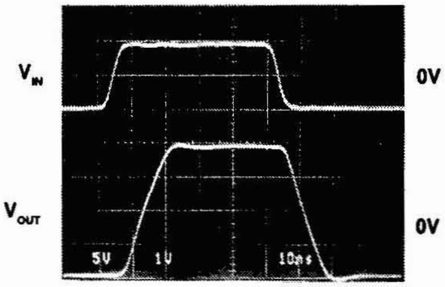
Large Signal Response



$A_V = +2$, $R_F = R_G = 820$,
$R_L = 200\Omega$, $V_S = \pm15V$

2030-13

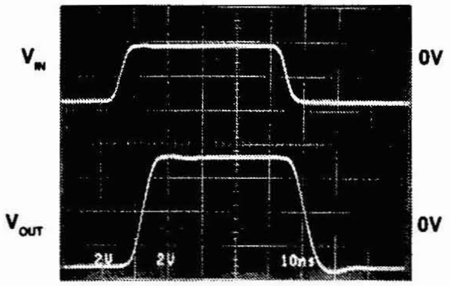
Large Signal Response



$A_V = +10$, $R_F = 750$, $R_G = 82\Omega$,
$R_L = 200\Omega$, $V_S = \pm15V$

2030-14

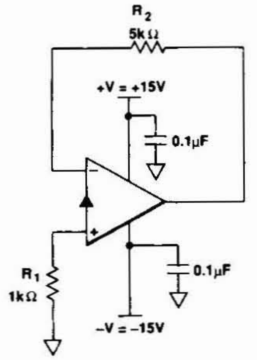
Large Signal Response



$A_V = +2$, $R_F = R_G = 750\Omega$,
$R_L = 200\Omega$, $V_S = \pm15V$

2030-15

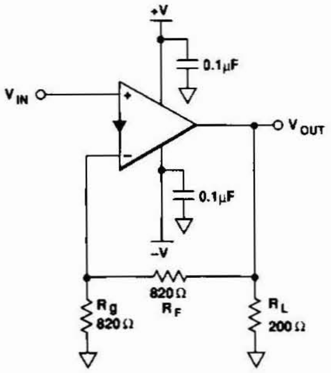
Burn-In Circuit


R_2
5kΩ
+V = +15V
0.1μF
0.1μF
R_1
1kΩ
−V = −15V

2030-16

ALL PACKAGES USE THE SAME SCHEMATIC.

Test Circuit


+V
0.1μF
V_{IN}
V_{OUT}
0.1μF
−V
820Ω
R_F
R_g
820Ω
R_L
200Ω

2030-17

Application Information

Product Description

The EL2030 is a current mode feedback amplifier similar to the industry standard EL2020, but with greatly improved AC characteristics. Most significant among these are the extremely wide bandwidth and very low differential gain and phase. In addition, the EL2030 is fully characterized and tested at ±5V and ±15V supplies.

Power Supply Bypassing/Lead Dressing

It is important to bypass the power supplies of the EL2030 with 0.1 μF ceramic disc capacitors. Although the lead length is not critical, it should not be more the ½ inch from the IC pins. Failure to do this will result in oscillation, and possible destruction of the part. Another important detail is the lead length of the inputs. The inputs should be designed with minimum stray capacitance and short lead lengths to avoid ringing and distortion.

Latch Mode

The EL2030 can be damaged in certain circumstances resulting in catastrophic failure in which destructive supply currents flow in the device. Specifically, an input signal greater than ±5 volts at currents greater than 5 mA is applied to the device when the power supply voltages are zero will result in failure of the device.

In addition, the EL2030 will be destroyed or damaged in the same way for momentary power supply voltage reversals. This could happen, for example, during a power turn on transient, or if the power supply voltages were oscillating and the positive rail were instantaneously negative with respect to the negative rail or vice versa.

Differential Gain and Differential Phase

Composite video signals contain intensity, color, hue, timing and audio information in AM, FM, and Phase Modulation. These video signals pass through many stages during their production, processing, archiving and transmission. It is important that each stage not corrupt these signals to provide a "high fidelity" image to the end viewer.

An industry standard way of measuring the distortion of a video component (or system) is to measure the amount of differential gain and phase error it introduces. A 100 mV peak to peak sine wave at 3.58 MHz for NTSC (4.3 MHz for PAL), with 0V DC component serves as the reference. The reference signal is added to a DC offset, shifting the sine wave from 0V to 0.7V which is then applied to the device under test (DUT). The output signal from the DUT is compared to the reference signal. The Differential Gain is a measure of the change in amplitude of the sine wave and is measured in percent. The Differential Phase is a measure of the change in the phase of the sine wave and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak differential gain and differential phase errors. The test setup in Figure 1 was used to characterize the EL2030. For higher than NTSC and PAL frequencies, an alternate Differential Gain and Phase measurement can be made using an HP3577A Network Analyser and the setup shown in Figure 2. The frequency response is normalized to gain or phase with 0V DC at the input. From the normalized value a DC offset voltage is introduced and the Differential Gain or Phase is the deviation from the normalized value.

Video Applications

The video signals that must be transmitted for modest distances are usually amplified by a device such as the EL2030 and carried via coax cable. There are at least two ways to drive cables, single terminated and double terminated.

When driving a cable, it is important to terminate it properly to avoid unwanted signal reflections. Single termination (75Ω to ground at receive end) may be sufficient for less demanding applications. In general, a double terminated cable (75Ω in series at drive end and 75Ω to ground at receive end) is preferred since the impedance match at both ends of the line will absorb signal reflections. However, when double termination is used (a total impedance of 150Ω), the received signal is reduced by half; therefore, the amplifier is usually set at a gain of 2 or higher to compensate for attenuation.

Video Applications — Contd.

Video signals are 1V peak-peak in amplitude, from sync tip to peak white. There are 100 IRE (0.714V) of picture (from black to peak white of the transmitted signal) and 40 IRE (0.286V) of sync in a composite video signal (140 IRE = 1V).

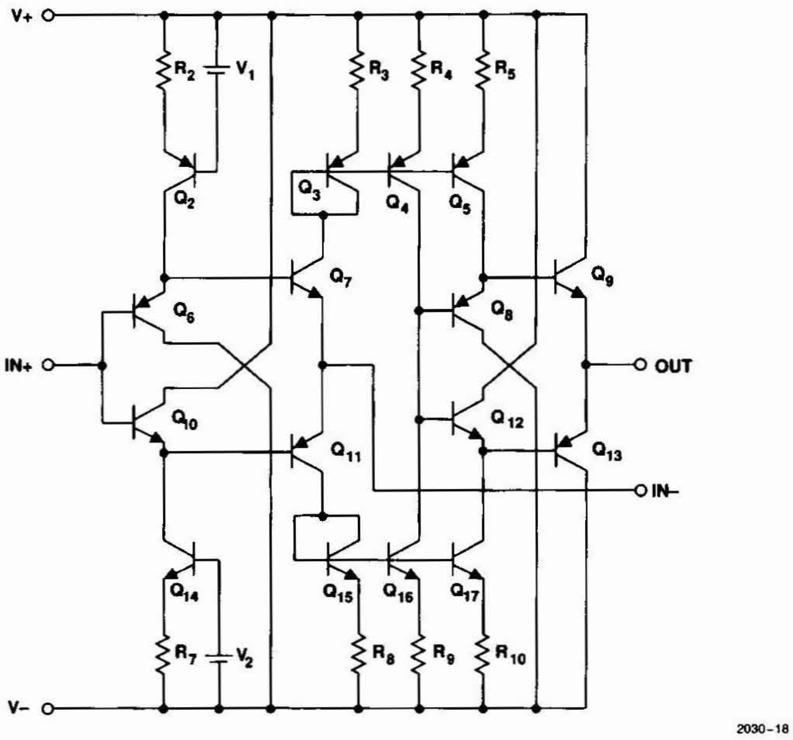
For video applications where a gain of two is used (double termination), the output of the video amplifier will be a maximum of 2V peak-peak. With ±5V power supply, the EL2030 output swing of 3.5V is sufficient to satisfy the video output swing requirements. The EL2030 can drive two double terminated coax cables under these conditions. With ±15V supplies, driving four double terminated cables is feasible.

Although the EL2030's video characteristics (differential gain and phase) are impressive with ±5V supplies at NTSC and PAL frequencies, it can be optimized when the supplies are increased to ±15V, especially at 30 MHz HDTV applications. This is primarily due to a reduction in internal parasitic junction capacitance with increased power supply voltage.

The following table summarizes the behavior of the EL2030 at ±5V and ±15V for NTSC. In addition, 30 MHz HDTV data is included. Refer to the differential gain and phase typical performance curves for more data.

$\pm V_S$	Rload	A_V	ΔGain	ΔPhase	Comments
15V	75Ω	1	0.02%	0.03°	Single terminated
15V	150Ω	1	0.02%	0.02°	Double terminated
5V	150Ω	1	0.05%	0.02°	Double terminated
15V	75Ω	2	0.02%	0.08°	Single terminated
15V	150Ω	2	0.01%	0.02°	Double terminated
5V	150Ω	2	0.03%	0.09°	Double terminated
15V	150Ω	2	0.05%	0.02°	HDTV, Double terminated

Equivalent Circuit



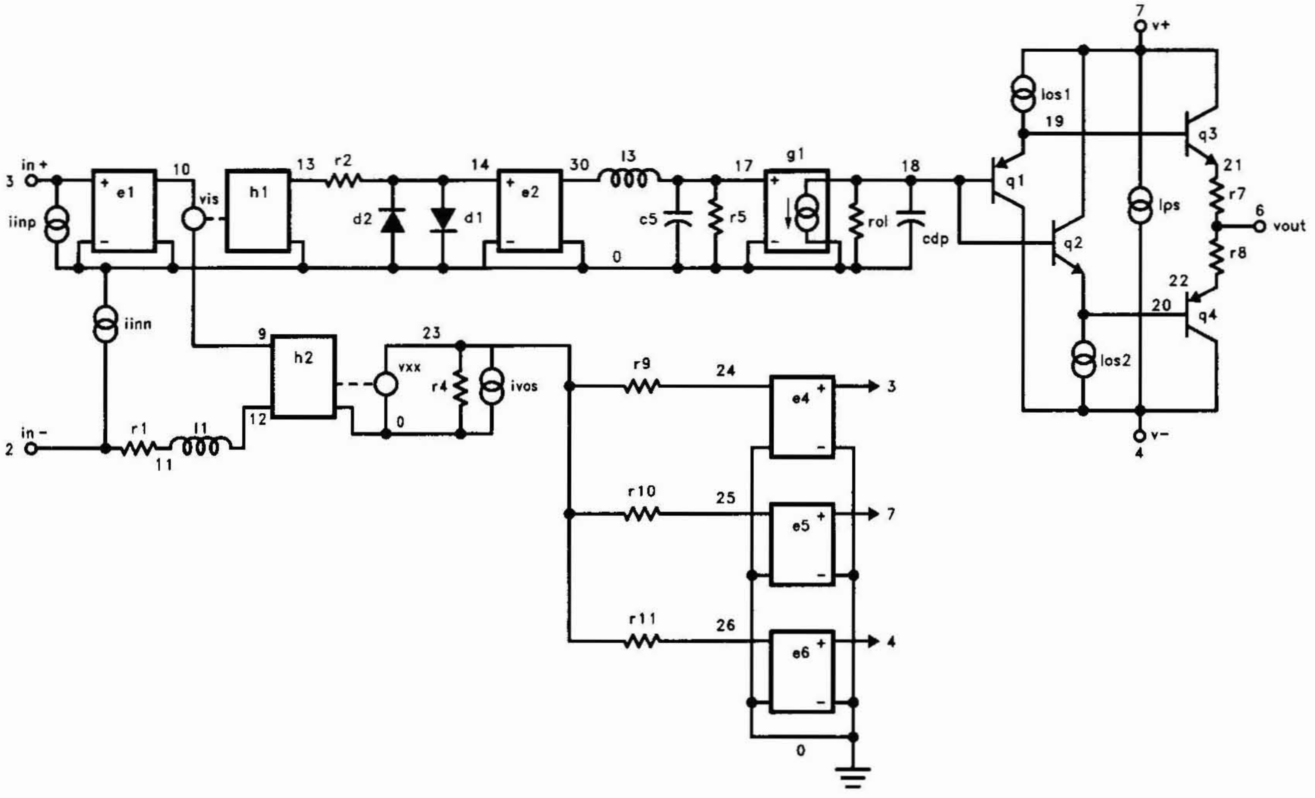
EL2030 Macromodel

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:    +input
*                 |    -input
*                 |    |    +Vsupply
*                 |    |    |    -Vsupply
*                 |    |    |    |    output
*                 |    |    |    |    |
.subckt M2030     3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 48nH
iinp 3 0 5μA
iinm 2 0 10μA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.5μH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 150K
cdp 18 0 2.8pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
```

EL2030 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 3 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.1nS)
.model qp pnp (is=5e-15 bf=100 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.266 bv=3.7 n=4)
.ends
```

EL2030 Macromodel — Contd.


in +
3
iinp
e1
10
vis
h1
13
r2
d2
d1
14
e2
30
l3
c5
17
r5
g1
18
rol
cdp
0
iinn
9
h2
23
vxx
r4
ivos
12
0
in −
2
r1
l1
11
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4
0
7
v+
ios1
19
q1
q3
21
r7
6
vout
Ips
q2
r8
22
20
q4
ios2
v−
4

2030-19

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2044C

Low Power/Low Voltage 120 MHz Unity-Gain Stable Operational Amplifier

Features

- 120 MHz −3 dB bandwidth
- Unity-gain stable
- Low supply current = 5.2 mA at V_S = ±15V
- Wide supply range
  = ±2V to ±18V dual-supply
  = 2.5V to 36V single-supply
- High slew rate = 325 V/µs
- Fast settling = 80 ns to 0.1% for a 10V step
- Low differential gain = 0.04% at $A_V = +2$, $R_L = 150\Omega$
- Low differential phase = 0.15° at $A_V = +2$, $R_L = 150\Omega$
- Stable with unlimited capacitive load
- Wide output voltage swing
  = ±13.6V with V_S = ±15V, $R_L = 1000\Omega$
  = 3.8V/0.3V with V_S = +5V, $R_L = 500\Omega$
- Low cost, enhanced replacement for the AD847 and LM6361

Applications

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2044CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2044CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

The EL2044C is a high speed, low power, low cost monolithic operational amplifier built on Elantec's proprietary complementary bipolar process. The EL2044C is unity-gain stable and features a 325 V/µs slew rate and 120 MHz gain-bandwidth product while requiring only 5.2 mA of supply current.

The power supply operating range of the EL2044C is from ±18V down to as little as ±2V. For single-supply operation, the EL2044C operates from 36V down to as little as 2.5V. The excellent power supply operating range of the EL2044C makes it an obvious choice for applications on a single +5V supply.

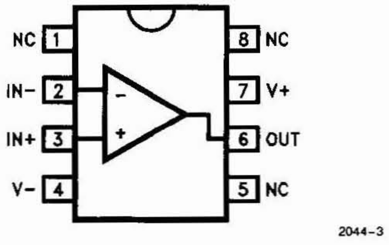
The EL2044C also features an extremely wide output voltage swing of ±13.6V with V_S = ±15V and $R_L = 1000\Omega$. At ±5V, output voltage swing is a wide ±3.8V with $R_L = 500\Omega$ and ±3.2V with $R_L = 150\Omega$. Furthermore, for single-supply operation at +5V, output voltage swing is an excellent 0.3V to 3.8V with $R_L = 500\Omega$.

At a gain of +1, the EL2044C has a −3 dB bandwidth of 120 MHz with a phase margin of 50°. It can drive unlimited load capacitance, and because of its conventional voltage-feedback topology, the EL2044C allows the use of reactive or nonlinear elements in its feedback network. This versatility combined with low cost and 75 mA of output-current drive makes the EL2044C an ideal choice for price-sensitive applications requiring low power and high speed.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



December 1995 Rev D

EL2044C

Low Power/Low Voltage 120 MHz Unity-Gain Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	± 18V or 36V	Power Dissipation (P_D)	See Curves
Peak Output Current (I_{OP})	Short-Circuit Protected	Operating Temperature Range (T_A)	−40°C to +85°C
Output Short-Circuit Duration (Note 1)	Infinite	Operating Junction Temperature (T_J)	150°C
Input Voltage (V_{IN})	± V_S	Storage Temperature (T_{ST})	−65°C to +150°C
Differential Input Voltage (dV_{IN})	± 10V		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1000Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		0.5	7.0	I	mV
			T_{MIN}, T_{MAX}			13.0	IV	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)	All		10.0		V	μV/°C
I_B	Input Bias Current	V_S = ±15V	25°C		2.8	8.2	I	μA
			T_{MIN}, T_{MAX}			11.2	IV	μA
		V_S = ±5V	25°C		2.8		V	μA
I_{OS}	Input Offset Current	V_S = ±15V	25°C		50	300	I	nA
			T_{MIN}, T_{MAX}			500	IV	nA
		V_S = ±5V	25°C		50		V	nA
TCI_{OS}	Average Offset Current Drift	(Note 2)	All		0.3		V	nA/°C
A_{VOL}	Open-Loop Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1000Ω	25°C	800	1500		I	V/V
			T_{MIN}, T_{MAX}	600			IV	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 500Ω	25°C		1200		V	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 150Ω	25°C		1000		V	V/V
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	25°C	65	80		I	dB
			T_{MIN}, T_{MAX}	60			IV	dB

DC Electrical Characteristics V_S = ±15V, R_L = 1000Ω, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V, V_{OUT} = 0V	25°C	70	90		I	dB
			T_{MIN}, T_{MAX}	70			IV	dB
CMIR	Common-Mode Input Range	V_S = ±15V	25°C		±14.0		V	V
		V_S = ±5V	25°C		±4.2		V	V
		V_S = +5V	25°C		4.2/0.1		V	V
V_{OUT}	Output Voltage Swing	V_S = ±15V, R_L = 1000Ω	25°C	±13.4	±13.6		I	V
			T_{MIN}, T_{MAX}	±13.1			IV	V
		V_S = ±15V, R_L = 500Ω	25°C	±12.0	±13.4		I	V
		V_S = ±5V, R_L = 500Ω	25°C	±3.4	±3.8		IV	V
		V_S = ±5V, R_L = 150Ω	25°C		±3.2		V	V
		V_S = +5V, R_L = 500Ω	25°C	3.6/0.4	3.8/0.3		I	V
			T_{MIN}, T_{MAX}	3.5/0.5			IV	V
I_{SC}	Output Short Circuit Current		25°C	40	75		I	mA
			T_{MIN}, T_{MAX}	35			IV	mA
I_S	Supply Current	V_S = ±15V, No Load	25°C		5.2	7	I	mA
			T_{MIN}, T_{MAX}			7.6	IV	mA
		V_S = ±5V, No Load	25°C		5.0		V	mA
R_{IN}	Input Resistance	Differential	25°C		150		V	kΩ
		Common-Mode	25°C		15		V	MΩ
C_{IN}	Input Capacitance	A_V = +1@ 10 MHz	25°C		1.0		V	pF
R_{OUT}	Output Resistance	A_V = +1	25°C		50		V	mΩ
PSOR	Power-Supply Operating Range	Dual-Supply	25°C	±2.0		±18.0	V	V
		Single-Supply	25°C	2.5		36.0	V	V

Closed-Loop AC Electrical Characteristics

V_S = ±15V, A_V = +1, R_L = 1000Ω unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	V_S = ±15V, A_V = +1	25°C		120		V	MHz
		V_S = ±15V, A_V = −1	25°C		60		V	MHz
		V_S = ±15V, A_V = +2	25°C		60		V	MHz
		V_S = ±15V, A_V = +5	25°C		12		V	MHz
		V_S = ±15V, A_V = +10	25°C		6		V	MHz
		V_S = ±5V, A_V = +1	25°C		80		V	MHz
GBWP	Gain-Bandwidth Product	V_S = ±15V	25°C		60		V	MHz
		V_S = ±5V	25°C		45		V	MHz
PM	Phase Margin	R_L = 1 kΩ, C_L = 10 pF	25°C		50		V	°

Closed-Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +1$, $R_L = 1000\Omega$ unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Note 3)	$V_S = \pm 15V$, $R_L = 1000\Omega$	25°C	250	325		I	V/µs
		$V_S = \pm 5V$, $R_L = 500\Omega$	25°C		200		V	V/µs
FPBW	Full-Power Bandwidth (Note 4)	$V_S = \pm 15V$	25°C	4.0	5.2		I	MHz
		$V_S = \pm 5V$	25°C		12.7		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step	25°C		3.0		V	ns
OS	Overshoot	0.1V Step	25°C		20		V	%
t_{PD}	Propagation Delay		25°C		2.5		V	ns
t_s	Settling to +0.1% ($A_V = +1$)	$V_S = \pm 15V$, 10V Step	25°C		80		V	ns
		$V_S = \pm 5V$, 5V Step	25°C		60		V	ns
dG	Differential Gain (Note 5)	NTSC/PAL	25°C		0.04		V	%
dP	Differential Phase (Note 5)	NTSC/PAL	25°C		0.15		V	°
eN	Input Noise Voltage	10 kHz	25°C		15.0		V	nV/$\sqrt{Hz}$
iN	Input Noise Current	10 kHz	25°C		1.50		V	pA/$\sqrt{Hz}$
CI STAB	Load Capacitance Stability	$A_V = +1$	25°C		Infinite		V	pF

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

Note 2: Measured from T_{MIN} to T_{MAX}.

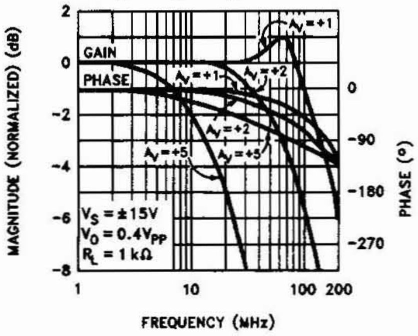
Note 3: Slew rate is measured on rising edge.

Note 4: For $V_S = \pm 15V$, $V_{OUT} = 20\ V_{PP}$. For $V_S = \pm 5V$, $V_{OUT} = 5\ V_{PP}$. Full-power bandwidth is based on slew rate measurement using: FPBW = SR/(2π * Vpeak).

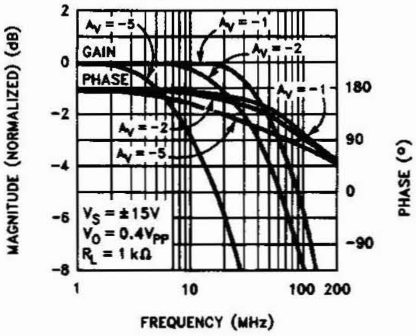
Note 5: Video Performance measured at $V_S = \pm 15V$, $A_V = +2$ with 2 times normal video level across $R_L = 150\Omega$. This corresponds to standard video levels across a back-terminated 75Ω load. For other values of R_L, see curves.

Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified)

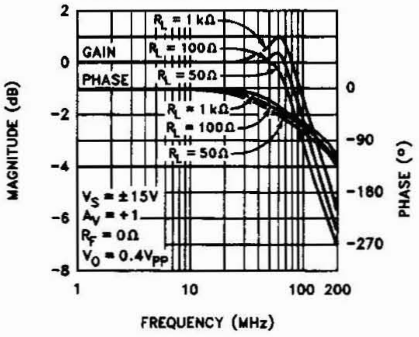
Non-Inverting Frequency Response



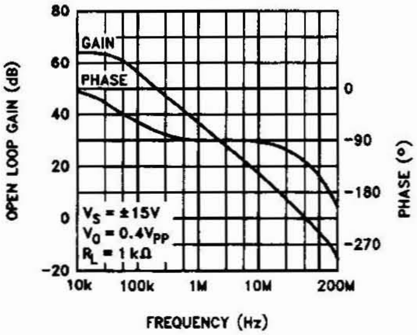
Inverting Frequency Response



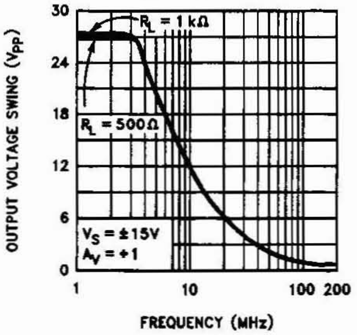
Frequency Response for Various Load Resistances



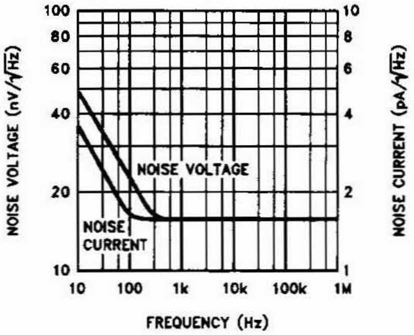
Open-Loop Gain and Phase vs Frequency



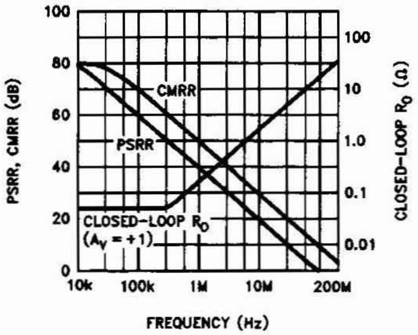
Output Voltage Swing vs Frequency



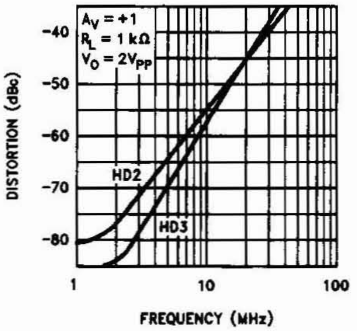
Equivalent Input Noise



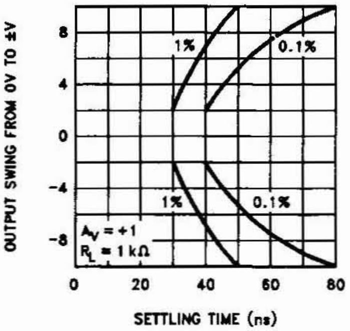
CMRR, PSRR and Closed-Loop Output Resistance vs Frequency



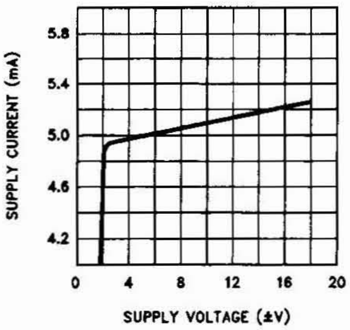
2nd and 3rd Harmonic Distortion vs Frequency



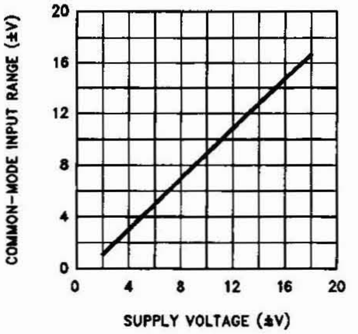
Settling Time vs Output Voltage Change



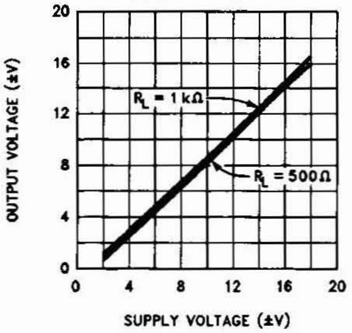
Supply Current vs Supply Voltage



Common-Mode Input Range vs Supply Voltage

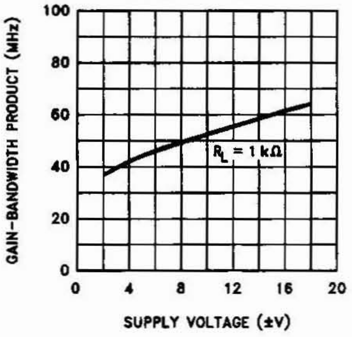


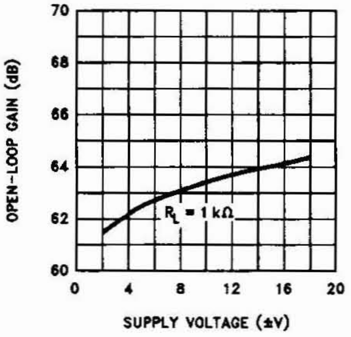
Output Voltage Range vs Supply Voltage

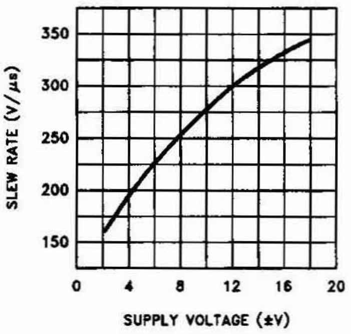


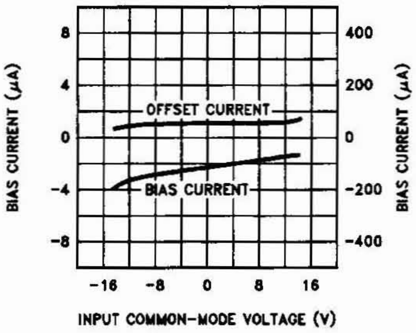
2044-5

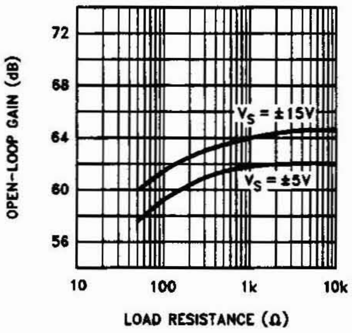
Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.

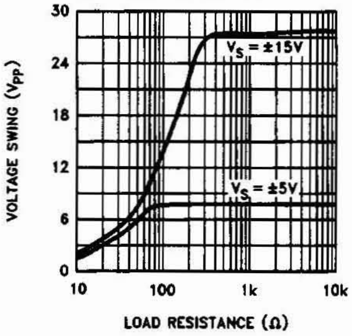

Gain-Bandwidth Product vs Supply Voltage

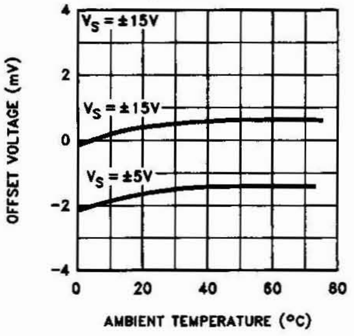

Open-Loop Gain vs Supply Voltage

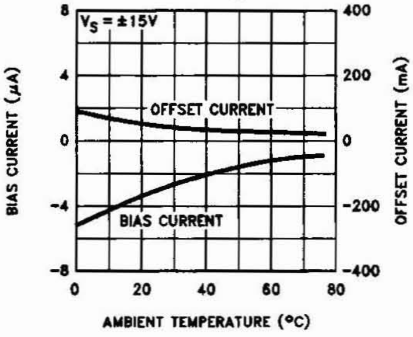

Slew-Rate vs Supply Voltage

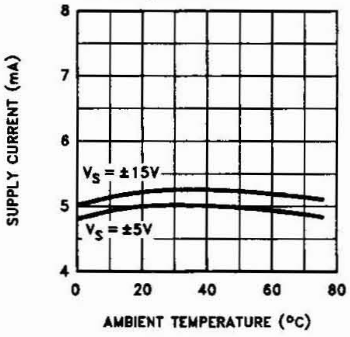

Bias and Offset Current vs Input Common-Mode Voltage

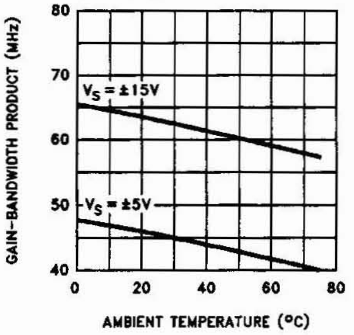

Open-Loop Gain vs Load Resistance

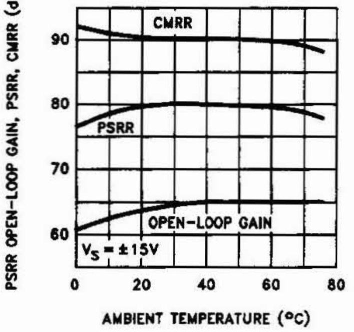

Voltage Swing vs Load Resistance

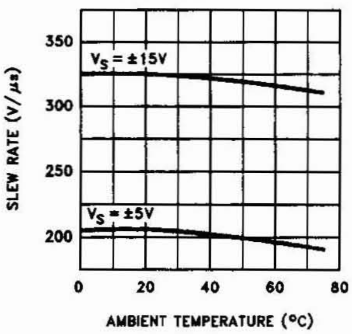

Offset Voltage vs Temperature


Bias and Offset Current vs Temperature


Supply Current vs Temperature


Gain-Bandwidth Product vs Temperature

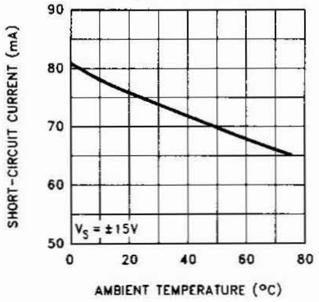

Open-Loop Gain PSRR and CMRR vs Temperature


Slew Rate vs Temperature

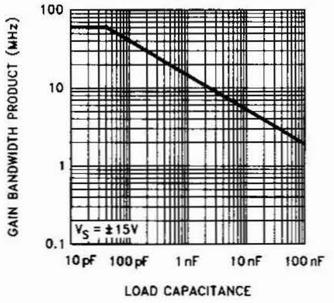
2044-6

Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.

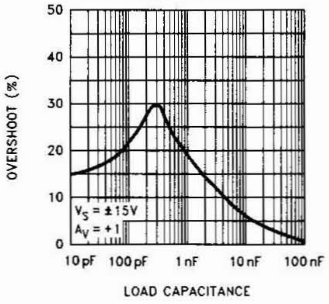
Short-Circuit Current vs Temperature



Gain-Bandwidth Product vs Load Capacitance

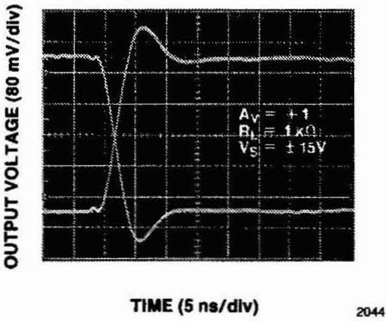


Overshoot vs Load Capacitance



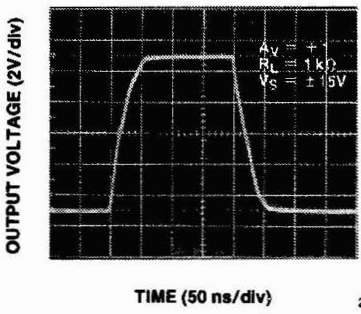
2044-7

Small-Signal Step Response



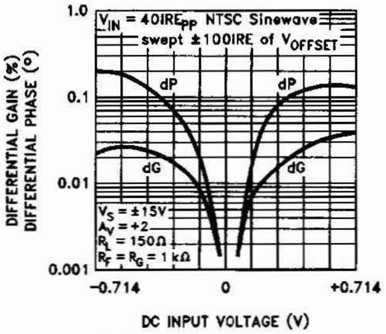
2044-8

Large-Signal Step Response

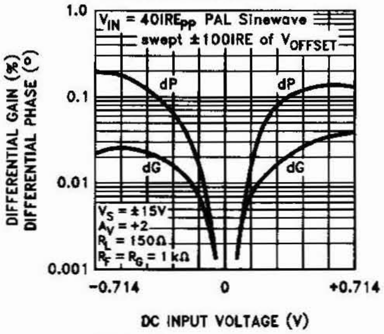


2044-9

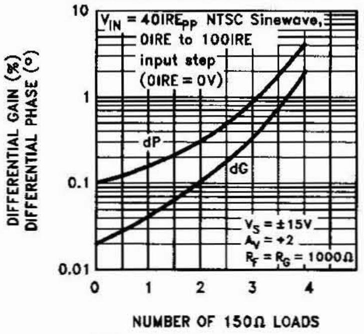
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



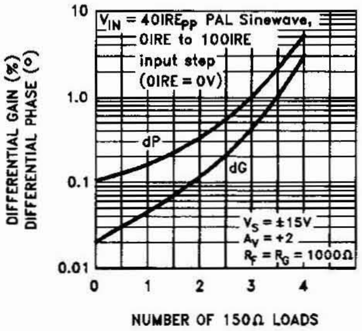
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



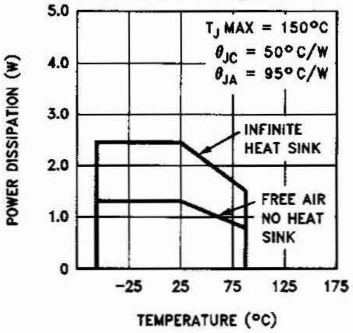
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



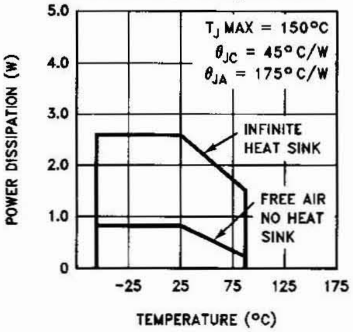
Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature

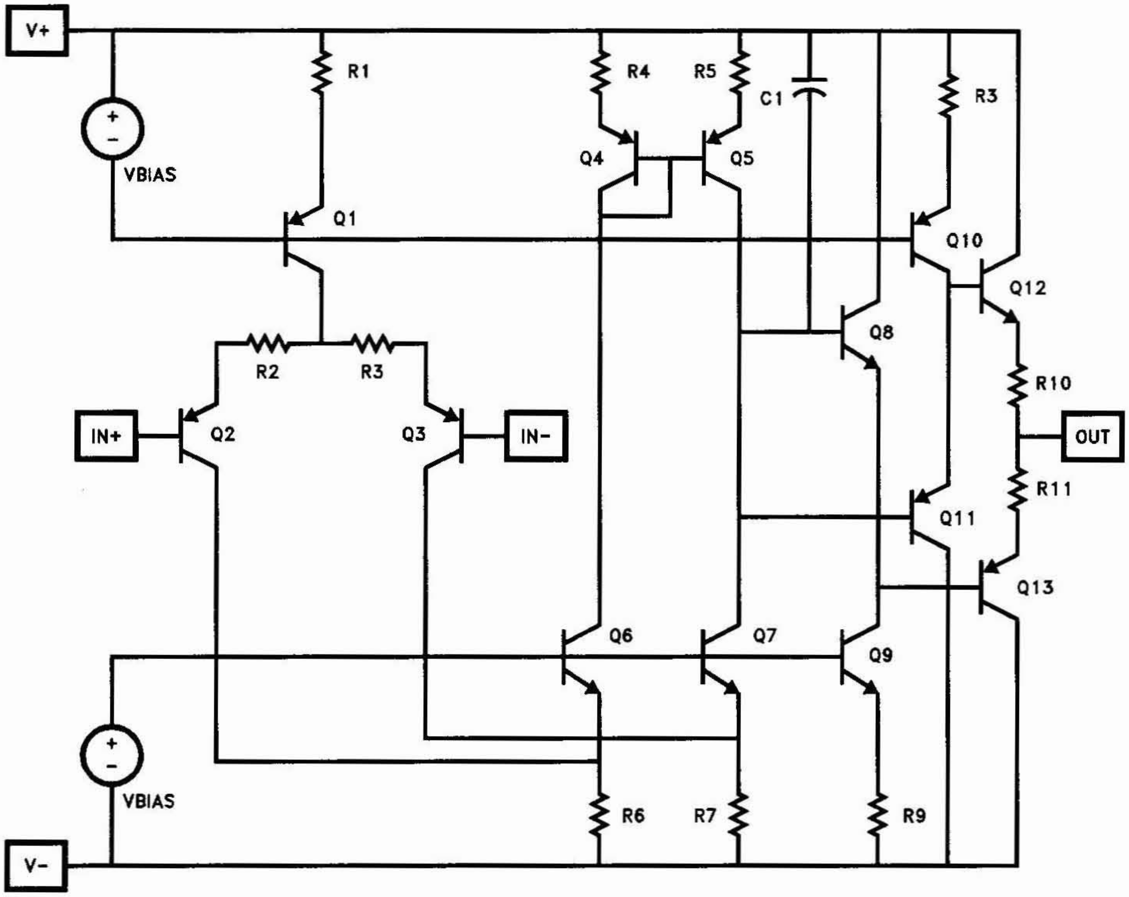


8-Lead SO Maximum Power Dissipation vs Ambient Temperature



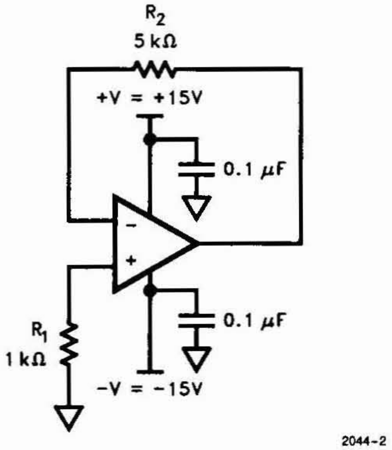
2044-10

Simplified Schematic


V+
VBIAS
R1
Q1
R2
R3
IN+
Q2
Q3
IN-
R4
R5
C1
Q4
Q5
R3
Q10
Q12
Q8
R10
OUT
R11
Q11
Q13
Q6
Q7
Q9
VBIAS
R6
R7
R9
V-

2044-1

Burn-In Circuit



All Packages Use the Same Schematic

Applications Information

Product Description

The EL2044C is a low-power wideband monolithic operational amplifier built on Elantec's proprietary high-speed complementary bipolar process. The EL2044C uses a classical voltage-feedback topology which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2044C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2044C is an excellent choice for applications such as fast log amplifiers.

Single-Supply Operation

The EL2044C has been designed to have a wide input and output voltage range. This design also makes the EL2044C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground ($R_L = 500\Omega$), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and $R_L = 500\Omega$. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2044C still has 1V of output swing.

Gain-Bandwidth Product and the −3 dB Bandwidth

The EL2044C has a gain-bandwidth product of 60 MHz while using only 5.2 mA of supply current. For gains greater than 4, its closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2044C has a −3 dB bandwidth of 120 MHz at a gain of +1, dropping to 60 MHz at a gain of +2. It is important to note that the EL2044C has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2044C in a gain of +1 only exhibits 1.0 dB of peaking with a 1000Ω load.

Video Performance

An industry-standard method of measuring the video distortion of a component such as the EL2044C is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2044C has been designed as an economical solution for applications requiring low video distortion. It has been thoroughly characterized

Applications Information — Contd.

for video performance in the topology described above, and the results have been included as typical dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2044C exhibits dG and dP of only 0.04% and 0.15° at NTSC and PAL. Because dG and dP can vary with different DC offsets, the video performance of the EL2044C has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The output drive capability of the EL2044C allows it to drive up to 2 back-terminated loads with good video performance. For more demanding applications such as greater output drive or better video distortion, a number of alternatives such as the EL2120, EL400, or EL2073 should be considered.

Output Drive Capability

The EL2044C has been designed to drive low impedance loads. It can easily drive 6 V_{PP} into a 150Ω load. This high output drive capability makes the EL2044C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2044C remains a minimum of 35 mA at low temperatures. The EL2044C is current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2044C has been designed to drive any capacitive load. However, the EL2044C remains stable by automatically reducing its gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (Rs). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2044C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2044C is well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2044C Macromodel

This macromodel has been developed to assist the user in simulating the EL2044C with surrounding circuitry. It has been developed for the PSPICE simulator (copywritten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

The model does not simulate these characteristics accurately:

noise
settling-time
CMRR
PSRR

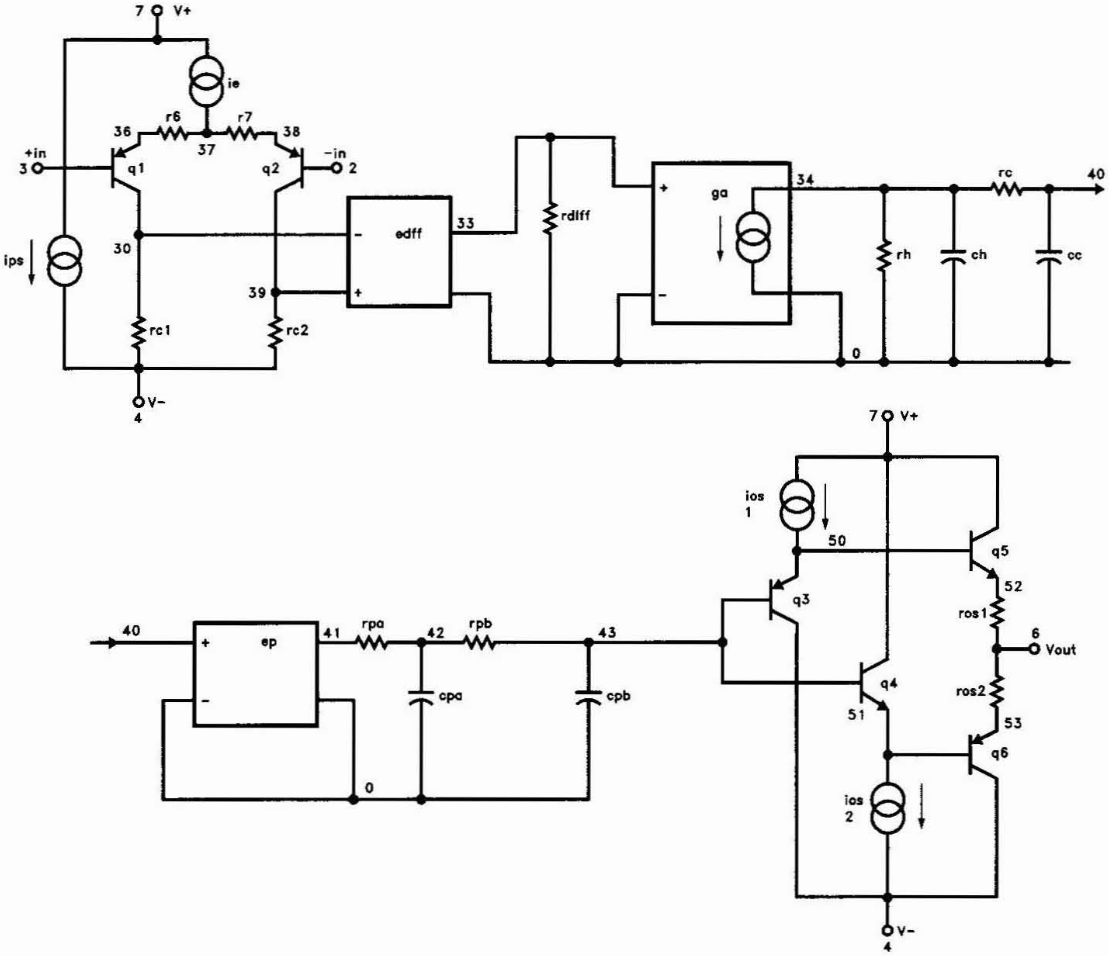
non-linearities
temperature effects
manufacturing variations

EL2044C Macromodel — Contd.

```
* Connections:  +input
*                 |   -input
*                 |     |   +Vsupply
*                 |     |     |   -Vsupply
*                 |     |     |     |   output
*                 |     |     |     |     |
.subckt M2044     3     2     7     4     6
*
* Input stage
*
ie 7 37 1mA
r6 36 37 800
r7 38 37 800
rc1 4 30 850
rc2 4 39 850
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 1m
rh 34 0 2Meg
ch 34 0 1.3pF
rc 34 40 1K
cc 40 0 1pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 200
cpa 42 0 1pF
rpb 42 43 200
cpb 43 0 1pF
*
* Output Stage
*
ios1 7 50 1.0mA
ios2 51 4 1.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
*
* Power Supply Current
*
ips 7 4 2.7mA
*
```

```
* Models
*
.model qn npn(is=800E-18 bf=200 tf=0.2nS)
.model qpa pnp(is=864E-18 bf=100 tf=0.2nS)
.model qp pnp(is=800E-18 bf=125 tf=0.2nS)
.ends
```

EL2044C Macromodel — Contd.


7 V+
ie
r6
r7
36
37
38
+in
3
q1
q2
−in
2
ips
30
39
rc1
rc2
V−
4
edff
33
rdiff
ga
34
rh
ch
rc
40
cc
0
7 V+
ios
1
50
q5
52
q3
ros1
6
Vout
40
ep
41
rpa
42
rpb
43
cpa
cpb
q4
51
ros2
53
q6
0
ios
2
V−
4

2044-4

EL2044C Model

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2244C/EL2444C

Dual/Quad Low-Power 60 MHz Unity-Gain Stable Op Amp

Features

- 60 MHz gain-bandwidth product
- Unity-gain stable
- Low supply current (per Amplifier) = 5.2 mA at V_S = ±15V
- Wide supply range
  = ±2V to ±18V dual-supply
  = 2.5V to 36V single-supply
- High slew rate = 325 V/μs
- Fast settling = 80 ns to 0.1% for a 10V step
- Low differential gain = 0.04% at A_V = +2, R_L = 150Ω
- Low differential phase = 0.15° at A_V = +2, R_L = 150Ω
- Stable with unlimited capacitive load
- Wide output voltage swing
  = ±13.6V with V_S = ±15V, R_L = 1000Ω
  = 3.8V/0.3V with V_S = +5V, R_L = 500Ω
- Low cost, enhanced replacement for the AD827 and LT1229/LT1230

Applications

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
Duals			
EL2244CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2244CS	−40°C to +85°C	8-Lead SO	MDP0027
Quads			
EL2444CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL2444CS	−40°C to +85°C	14-Lead SO	MDP0027

General Description

The EL2244C/EL2444C are dual and quad versions of the popular EL2044C. They are high speed, low power, low cost monolithic operational amplifiers built on Elantec's proprietary complementary bipolar process. The EL2244C/EL2444C are unity-gain stable and feature a 325 V/μs slew rate and 60 MHz gain-bandwidth product while requiring only 5.2 mA of supply current per amplifier.

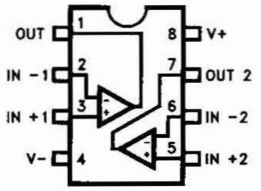
The power supply operating range of the EL2244C/EL2444C is from ±18V down to as little as ±2V. For single-supply operation, the EL2244C/EL2444C operate from 36V down to as little as 2.5V. The excellent power supply operating range of the EL2244C/EL2444C makes them an obvious choice for applications on a single +5V or +3V supply.

The EL2244C/EL2444C also feature an extremely wide output voltage swing of ±13.6V with V_S = ±15V and R_L = 1000Ω. At ±5V, output voltage swing is a wide ±3.8V with R_L = 500Ω and ±3.2V with R_L = 150Ω. Furthermore, for single-supply operation at +5V, output voltage swing is an excellent 0.3V to 3.8V with R_L = 500Ω.

At a gain of +1, the EL2244C/EL2444C have a −3 dB bandwidth of 120 MHz with a phase margin of 50°. They can drive unlimited load capacitance, and because of their conventional voltage-feedback topology, the EL2244C/EL2444C allow the use of reactive or non-linear elements in their feedback network. This versatility combined with low cost and 75 mA of output-current drive make the EL2244C/EL2444C an ideal choice for price-sensitive applications requiring low power and high speed.

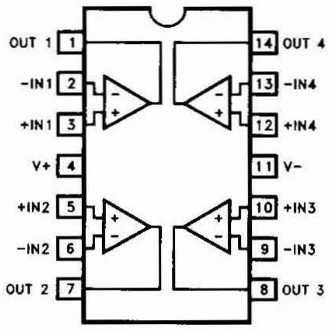
Connection Diagrams

EL2244CN/CS
Dual



2244-1

EL2444CN/CS
Quad



2244-2

December 1995 Rev C

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	± 18V or 36V	Power Dissipation (P_D)	See Curves
Peak Output Current (I_{OP})	Short-Circuit Protected	Operating Temperature Range (T_A)	−40°C to +85°C
Output Short-Circuit Duration (Note 1)	Infinite	Operating Junction Temperature (T_J)	150°C
Input Voltage (V_{IN})	$\pm V_S$	Storage Temperature (T_{ST})	−65°C to +150°C
Differential Input Voltage (dV_{IN})	± 10V		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1000Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		0.5	4.0	I	mV
			T_{MIN}, T_{MAX}			9.0	IV	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)	All		10.0		V	μV/°C
I_B	Input Bias Current	V_S = ±15V	25°C		2.8	8.2	I	μA
			T_{MIN}, T_{MAX}			11.2	IV	μA
		V_S = ±5V	25°C		2.8		V	μA
I_{OS}	Input Offset Current	V_S = ±15V	25°C		50	300	I	nA
			T_{MIN}, T_{MAX}			500	IV	nA
		V_S = ±5V	25°C		50		V	nA
TCI_{OS}	Average Offset Current Drift	(Note 2)	All		0.3		V	nA/°C
A_{VOL}	Open-Loop Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1000Ω	25°C	800	1500		I	V/V
			T_{MIN}, T_{MAX}	600			IV	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 500Ω	25°C		1200		V	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 150Ω	25°C		1000		V	V/V
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	25°C	65	80		I	dB
			T_{MIN}, T_{MAX}	60			IV	dB

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1000\Omega$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12V$, $V_{OUT} = 0V$	25°C	70	90		I	dB
			T_{MIN}, T_{MAX}	70			IV	dB
CMIR	Common-Mode Input Range	$V_S = \pm 15V$	25°C		±14.0		V	V
		$V_S = \pm 5V$	25°C		±4.2		V	V
		$V_S = +5V$	25°C		4.2/0.1		V	V
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 1000\Omega$	25°C	±13.4	±13.6		I	V
			T_{MIN}, T_{MAX}	±13.1			IV	V
		$V_S = \pm 15V$, $R_L = 500\Omega$	25°C	±12.0	±13.4		I	V
		$V_S = \pm 5V$, $R_L = 500\Omega$	25°C	±3.4	±3.8		IV	V
		$V_S = \pm 5V$, $R_L = 150\Omega$	25°C		±3.2		V	V
		$V_S = +5V$, $R_L = 500\Omega$	25°C	3.6/0.4	3.8/0.3		I	V
			T_{MIN}, T_{MAX}	3.5/0.5			IV	V
I_{SC}	Output Short Circuit Current		25°C	40	75		I	mA
			T_{MIN}, T_{MAX}	35			IV	mA
I_S	Supply Current (Per Amplifier)	$V_S = \pm 15V$, No Load	25°C		5.2	7	I	mA
			T_{MIN}			7.6	IV	mA
			T_{MAX}			7.6	IV	mA
		$V_S = \pm 5V$, No Load	25°C		5.0		V	mA
R_{IN}	Input Resistance	Differential	25°C		150		V	kΩ
		Common-Mode	25°C		15		V	MΩ
C_{IN}	Input Capacitance	$A_V = +1$@ 10 MHz	25°C		1.0		V	pF
R_{OUT}	Output Resistance	$A_V = +1$	25°C		50		V	mΩ
PSOR	Power-Supply Operating Range	Dual-Supply	25°C	±2.0		±18.0	V	V
		Single-Supply	25°C	2.5		36.0	V	V

Closed-Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +1$, $R_L = 1000\Omega$ unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth ($V_{OUT} = 0.4\ V_{PP}$)	$V_S = \pm 15V$, $A_V = +1$	25°C		120		V	MHz
		$V_S = \pm 15V$, $A_V = -1$	25°C		60		V	MHz
		$V_S = \pm 15V$, $A_V = +2$	25°C		60		V	MHz
		$V_S = \pm 15V$, $A_V = +5$	25°C		12		V	MHz
		$V_S = \pm 15V$, $A_V = +10$	25°C		6		V	MHz
		$V_S = \pm 5V$, $A_V = +1$	25°C		80		V	MHz
GBWP	Gain-Bandwidth Product	$V_S = \pm 15V$	25°C		60		V	MHz
		$V_S = \pm 5V$	25°C		45		V	MHz

Closed-Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +1$, $R_L = 1000\Omega$ unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
PM	Phase Margin	$R_L = 1\ k\Omega$, $C_L = 10\ pF$	25°C		50		V	°
CS	Channel Separation	f = 5 MHz	25°C		85		V	dB
SR	Slew Rate (Note 3)	$V_S = \pm 15V$, $R_L = 1000\Omega$	25°C	250	325		I	V/µs
		$V_S = \pm 5V$, $R_L = 500\Omega$	25°C		200		V	V/µs
FPBW	Full-Power Bandwidth (Note 4)	$V_S = \pm 15V$	25°C	4.0	5.2		I	MHz
		$V_S = \pm 5V$	25°C		12.7		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step	25°C		3.0		V	ns
OS	Overshoot	0.1V Step	25°C		20		V	%
t_{PD}	Propagation Delay		25°C		2.5		V	ns
t_s	Settling to +0.1% ($A_V = +1$)	$V_S = \pm 15V$, 10V Step	25°C		80		V	ns
		$V_S = \pm 5V$, 5V Step	25°C		60		V	ns
dG	Differential Gain (Note 5)	NTSC/PAL	25°C		0.04		V	%
dP	Differential Phase (Note 5)	NTSC/PAL	25°C		0.15		V	°
eN	Input Noise Voltage	10 kHz	25°C		15.0		V	$nV/\sqrt{Hz}$
iN	Input Noise Current	10 kHz	25°C		1.50		V	$pA/\sqrt{Hz}$
CI STAB	Load Capacitance Stability	$A_V = +1$	25°C		Infinite		V	pF

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

Note 2: Measured from T_{MIN} to T_{MAX}.

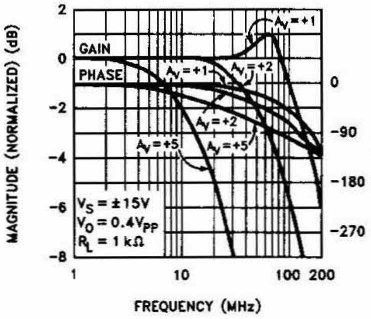
Note 3: Slew rate is measured on rising edge.

Note 4: For $V_S = \pm 15V$, $V_{OUT} = 20\ V_{PP}$. For $V_S = \pm 5V$, $V_{OUT} = 5\ V_{PP}$. Full-power bandwidth is based on slew rate measurement using: FPBW = SR/(2π * Vpeak).

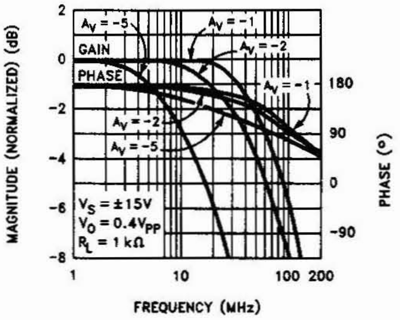
Note 5: Video Performance measured at $V_S = \pm 15V$, $A_V = +2$ with 2 times normal video level across $R_L = 150\Omega$. This corresponds to standard video levels across a back-terminated 75Ω load. For other values of R_L, see curves.

Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified)

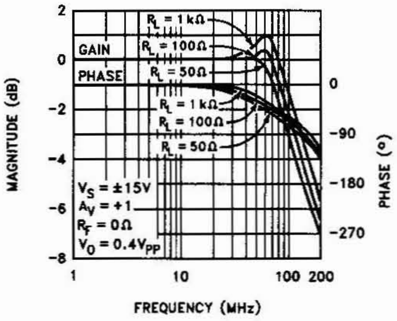
Non-Inverting Frequency Response



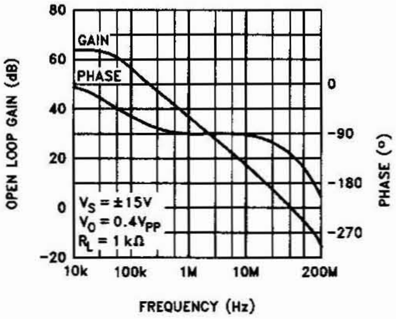
Inverting Frequency Response



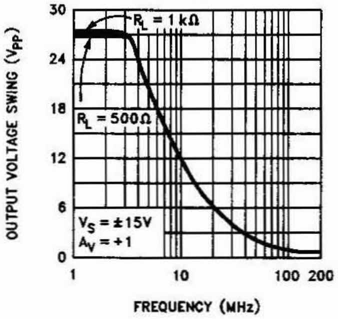
Frequency Response for Various Load Resistances



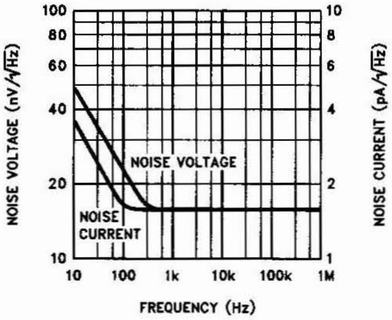
Open-Loop Gain and Phase vs Frequency



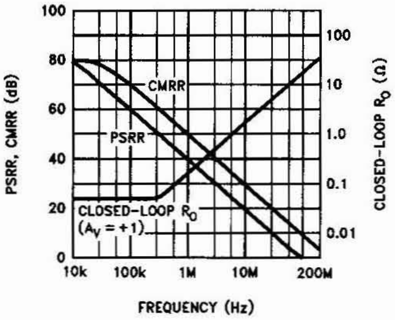
Output Voltage Swing vs Frequency



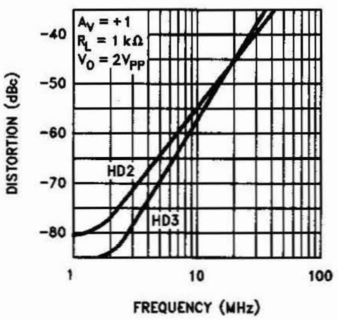
Equivalent Input Noise



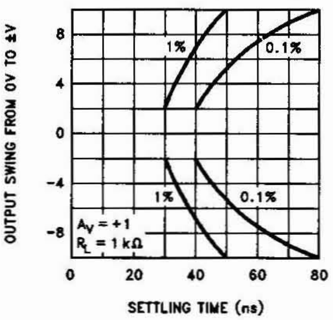
CMRR, PSRR and Closed-Loop Output Resistance vs Frequency



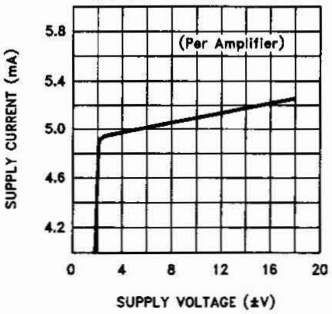
2nd and 3rd Harmonic Distortion vs Frequency



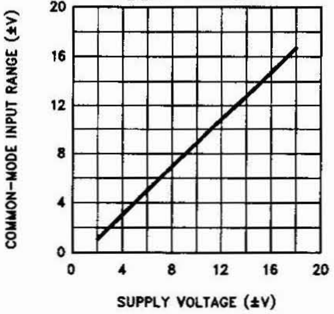
Settling Time vs Output Voltage Change



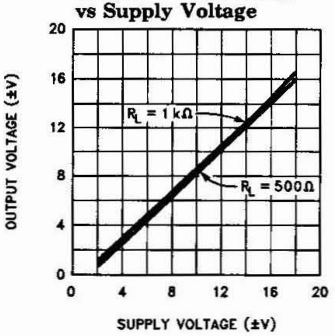
Supply Current vs Supply Voltage



Common-Mode Input Range vs Supply Voltage

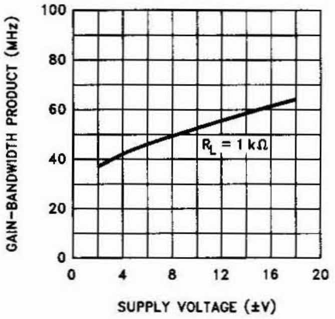


Output Voltage Range vs Supply Voltage

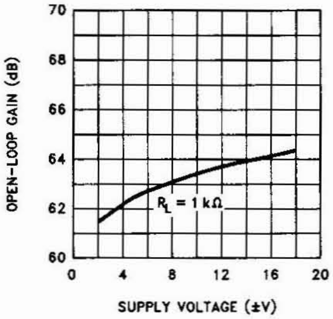


2244-3

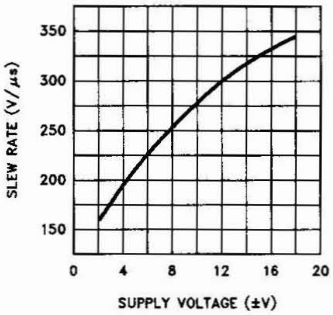
Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.



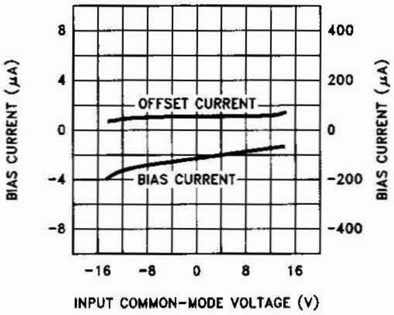
Gain-Bandwidth Product vs Supply Voltage



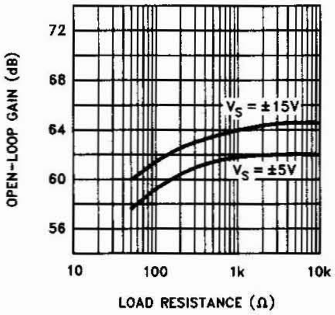
Open-Loop Gain vs Supply Voltage



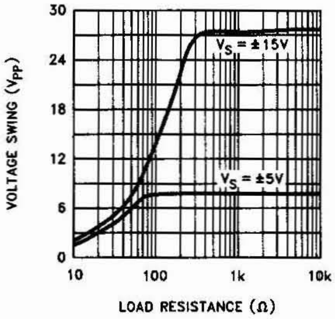
Slew-Rate vs Supply Voltage



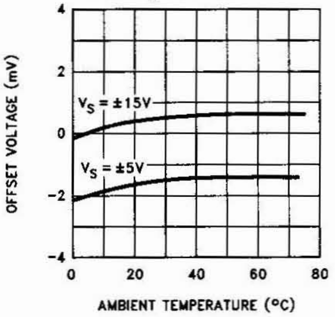
Bias and Offset Current vs Input Common-Mode Voltage



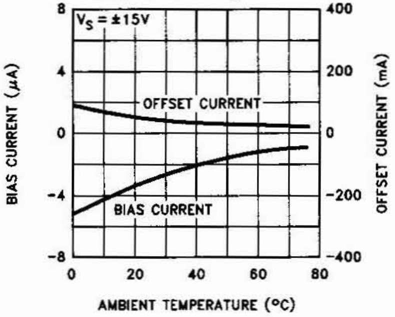
Open-Loop Gain vs Load Resistance



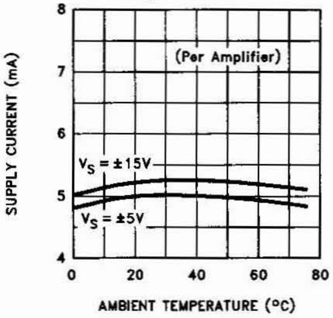
Voltage Swing vs Load Resistance



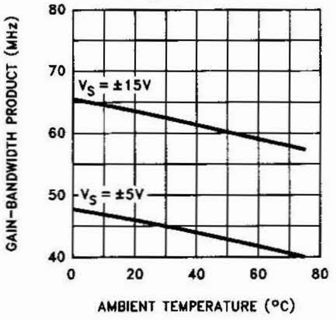
Offset Voltage vs Temperature



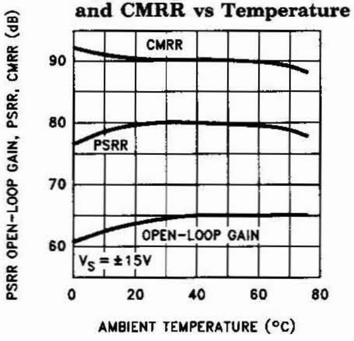
Bias and Offset Current vs Temperature



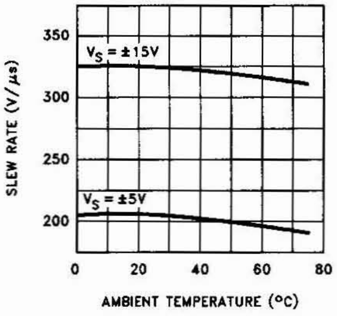
Supply Current vs Temperature



Gain-Bandwidth Product vs Temperature



Open-Loop Gain, PSRR and CMRR vs Temperature

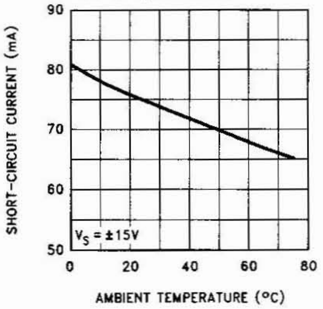


Slew Rate vs Temperature

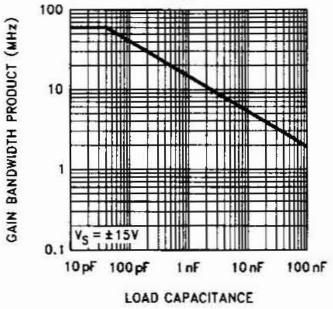
2244-4

Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.

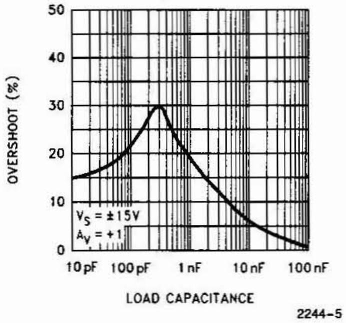
Short-Circuit Current vs Temperature



Gain-Bandwidth Product vs Load Capacitance

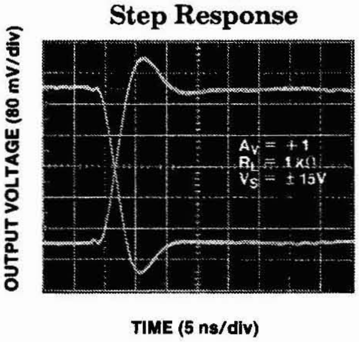


Overshoot vs Load Capacitance



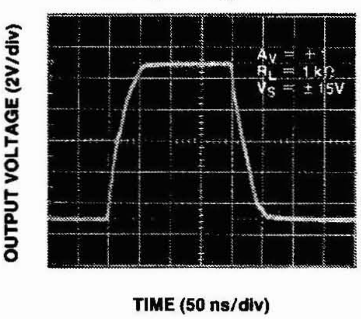
2244-5

Small-Signal Step Response



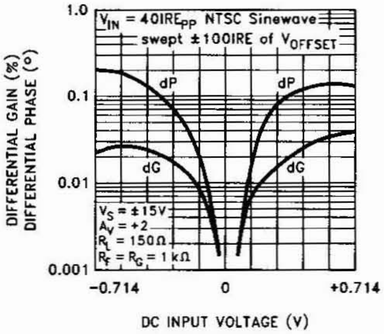
2244-6

Large-Signal Step Response

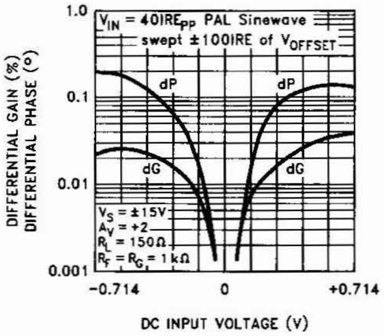


2244-7

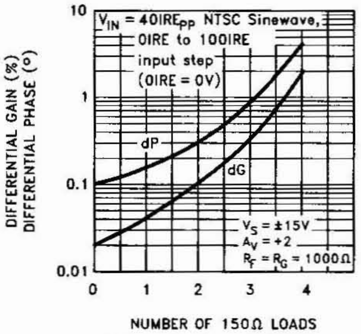
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



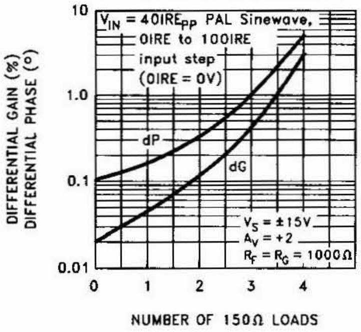
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



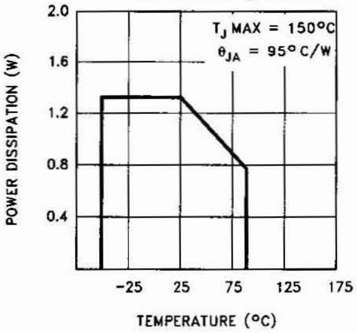
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



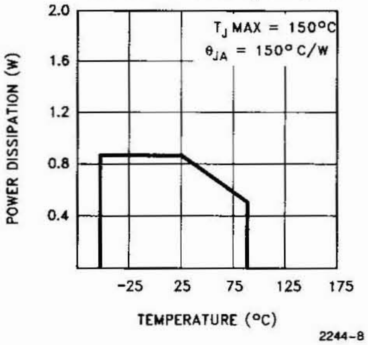
Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



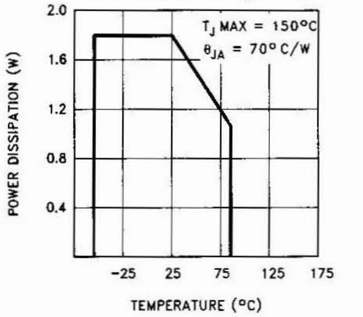
8-Lead SO Maximum Power Dissipation vs Ambient Temperature



2244-8

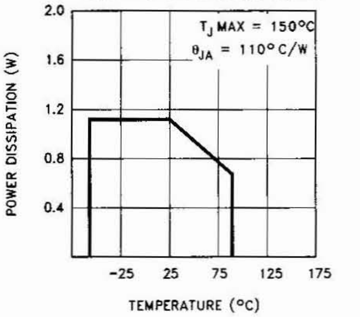
Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.

14-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



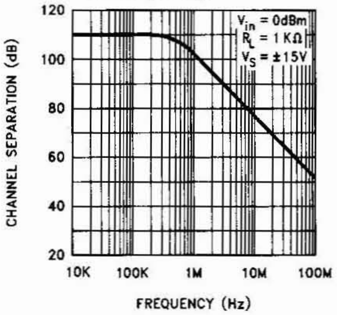
2244-9

14-Lead SO Maximum Power Dissipation vs Ambient Temperature



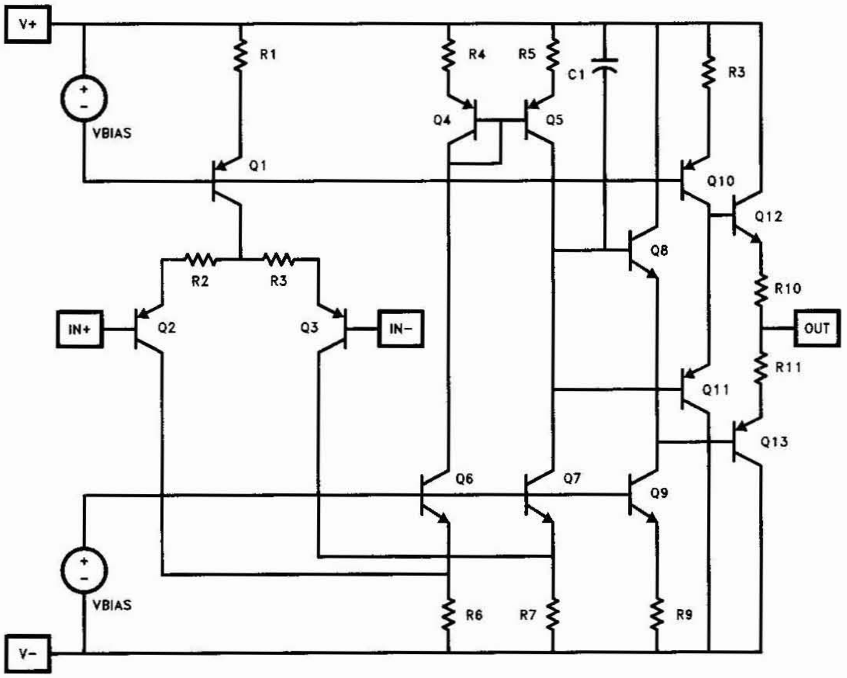
2244-10

Channel Separation vs Frequency



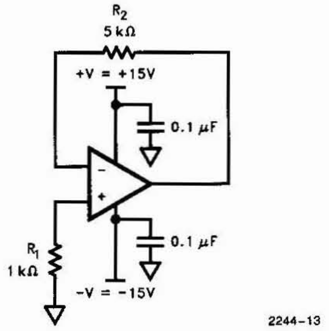
2244-11

Simplified Schematic (Per Amplifier)


V+
VBIAS
R1
Q1
R2
R3
IN+
Q2
Q3
IN−
R4
R5
C1
Q4
Q5
R3
Q10
Q12
Q8
R10
OUT
R11
Q11
Q13
Q6
Q7
Q9
VBIAS
R6
R7
R9
V−

2244-12

Burn-In Circuit (Per Amplifier)


R_2
5 kΩ
+V = +15V
0.1 µF
−
+
0.1 µF
R_1
1 kΩ
−V = −15V

2244-13

All Packages Use the Same Schematic

Applications Information

Product Description

The EL2244C/EL2444C are low-power wideband monolithic operational amplifiers built on Elantec's proprietary high-speed complementary bipolar process. The EL2244C/EL2444C use a classical voltage-feedback topology which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2244C/EL2444C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2244C/EL2444C are an excellent choice for applications such as fast log amplifiers.

Power Dissipation

With the wide power supply range and large output drive capability of the EL2244C/EL2444C, it is possible to exceed the 150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{Jmax}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified for the EL2244C/EL2444C to remain in the safe operating area. These parameters are related as follows:

$$T_{Jmax} = T_{max} + (\theta_{JA} * (\text{PDmaxtotal}))$$

where PDmaxtotal is the sum of the maximum power dissipation of each amplifier in the package (PDmax). PDmax for each amplifier can be calculated as follows:

$$\text{PDmax} = (2 * V_S * I_{Smax} + (V_S - V_{outmax}) * (V_{outmax}/R_L))$$

where:

T_{max} = Maximum Ambient Temperature

θ_{JA} = Thermal Resistance of the Package

PDmax = Maximum Power Dissipation of 1 Amplifier

V_S = Supply Voltage

I_{Smax} = Maximum Supply Current of 1 Amplifier

V_{outmax} = Maximum Output Voltage Swing of the Application

R_L = Load Resistance

To serve as a guide for the user, we can calculate maximum allowable supply voltages for the example of the video cable-driver below since we know that T_{Jmax} = 150°C, T_{max} = 75°C, I_{Smax} = 7.6 mA, and the package θ_{JA}s are shown in Table 1. If we assume (for this example) that we are driving a back-terminated video cable, then the maximum average value (over duty-cycle) of V_{outmax} is 1.4V, and R_L = 150Ω, giving the results seen in Table 1.

Table 1

Duals	Package	θ_{JA}	Max PDiss @ T_{max}	Max V_S
EL2244CN	PDIP8	95°C/W	0.789W @ 75°C	±16.6V
EL2244CS	SO8	150°C/W	0.500W @ 75°C	±10.7V
QUADS				
EL2444CN	PDIP14	70°C/W	1.071W @ 75°C	±11.5V
EL2444CS	SO14	110°C/W	0.682W @ 75°C	±7.5V

Single-Supply Operation

The EL2244C/EL2444C have been designed to have a wide input and output voltage range. This design also makes the EL2244C/EL2444C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground (R_L = 500Ω), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and R_L = 500Ω. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2244C/EL2444C still have 1V of output swing.

Gain-Bandwidth Product and the −3 dB Bandwidth

The EL2244C/EL2444C have a gain-bandwidth product of 60 MHz while using only 5.2 mA of supply current per amplifier. For gains greater

Applications Information — Contd.

than 4, their closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifiers' transfer function contribute to even higher closed loop bandwidths. For example, the EL2244C/EL2444C have a −3 dB bandwidth of 120 MHz at a gain of +1, dropping to 60 MHz at a gain of +2. It is important to note that the EL2244C/EL2444C have been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2244C/EL2444C in a gain of +1 only exhibit 1.0 dB of peaking with a 1000Ω load.

Video Performance

An industry-standard method of measuring the video distortion of components such as the EL2244C/EL2444C is to measure the amount of differential gain (dG) and differential phase (dP) that they introduce. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2244C/EL2444C have been designed as an economical solution for applications requiring low video distortion. They have been thoroughly characterized for video performance in the topology described above, and the results have been included as typical dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2244C/EL2444C exhibit dG and dP of only 0.04% and 0.15° at NTSC and PAL. Because dG and dP can vary with different DC offsets, the video performance of the EL2244C/EL2444C has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

Output Drive Capability

The EL2244C/EL2444C have been designed to drive low impedance loads. They can easily drive 6 V_{PP} into a 150Ω load. This high output drive capability makes the EL2244C/EL2444C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2244C/EL2444C remains a minimum of 35 mA at low temperatures. The EL2244C/EL2444C are current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2244C/EL2444C have been designed to drive any capacitive load. However, the EL2244C/EL2444C remain stable by automatically reducing their gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (Rs). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2244C/EL2444C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2244C/EL2444C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum

Applications Information — Contd.

performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2244C/EL2444C Macromodel

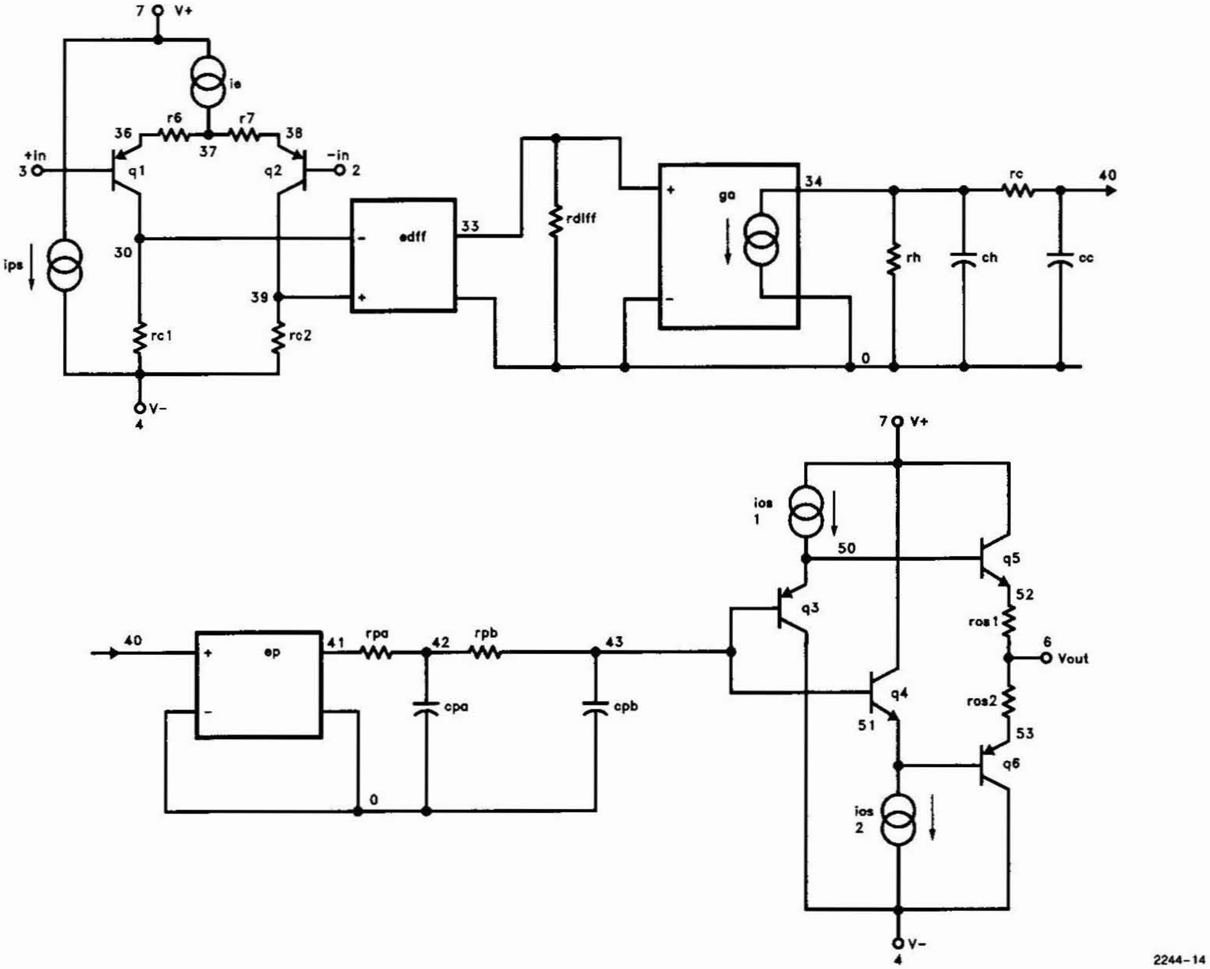
This macromodel has been developed to assist the user in simulating the EL2244C/EL2444C with surrounding circuitry. It has been developed for the PSPICE simulator (copywritten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

The model does not simulate these characteristics accurately:

noise
settling-time
CMRR
PSRR
non-linearities
temperature effects
manufacturing variations

```
* Connections:  +input
*               |    -input
*               |    |    +Vsupply
*               |    |    |    -Vsupply
*               |    |    |    |    output
*               |    |    |    |    |
.subckt M2244   3    2    7    4    6
*
* Input stage
*
ie 7 37 1mA
r6 36 37 800
r7 38 37 800
rc1 4 30 850
rc2 4 39 850
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 1m
rh 34 0 2Meg
ch 34 0 1.3pF
rc 34 40 1K
cc 40 0 1pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 200
cpa 42 0 1pF
rpb 42 43 200
cpb 43 0 1pF
*
* Output Stage
*
ios1 7 50 1.0mA
ios2 51 4 1.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
*
* Power Supply Current
*
ips 7 4 2.7mA
*
* Models
*
.model qn npn(is=800E-18 bf=200 tf=0.2nS)
.model qpa pnp(is=864E-18 bf=100 tf=0.2nS)
.model qp pnp(is=800E-18 bf=125 tf=0.2nS)
.ends
```

EL2244C/EL2444C Macromodel — Contd.


7 V+
ie
r6
r7
36
37
38
+in
3
q1
q2
-in
2
ips
30
39
rc1
rc2
V-
4
ediff
33
rdiff
ga
34
rh
ch
rc
cc
40
0
7 V+
ios
1
50
q5
q3
52
ros1
6
Vout
40
ep
41
rpa
42
rpb
43
cpa
cpb
q4
ros2
51
53
q6
0
ios
2
V-
4
2244-14

EL2244C/EL2444C Model

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2045C

Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

Features

- 100 MHz gain-bandwidth product
- Gain-of-2 stable
- Low supply current = 5.2 mA at V_S = ±15V
- Wide supply range = ±2V to ±18V dual-supply = 2.5V to 36V single-supply
- High slew rate = 275 V/µs
- Fast settling = 80 ns to 0.1% for a 10V step
- Low differential gain = 0.02% at $A_V = +2, R_L = 150\Omega$
- Low differential phase = 0.07° at $A_V = +2, R_L = 150\Omega$
- Stable with unlimited capacitive load
- Wide output voltage swing = ±13.6V with V_S = ±15V, $R_L = 1000\Omega$ = 3.8V/0.3V with V_S = +5V, $R_L = 500\Omega$

Applications

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2045CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2045CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

The EL2045C is a high speed, low power, low cost monolithic operational amplifier built on Elantec's proprietary complementary bipolar process. The EL2045C is gain-of-2 stable and features a 275 V/µs slew rate and 100 MHz gain-bandwidth product while requiring only 5.2 mA of supply current.

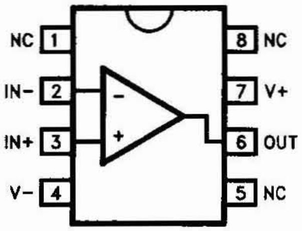
The power supply operating range of the EL2045C is from ±18V down to as little as ±2V. For single-supply operation, the EL2045C operates from 36V down to as little as 2.5V. The excellent power supply operating range of the EL2045C makes it an obvious choice for applications on a single +5V or +3V supply.

The EL2045C also features an extremely wide output voltage swing of ±13.6V with V_S = ±15V and $R_L = 1000\Omega$. At ±5V, output voltage swing is a wide ±3.8V with $R_L = 500\Omega$ and ±3.2V with $R_L = 150\Omega$. Furthermore, for single-supply operation at +5V, output voltage swing is an excellent 0.3V to 3.8V with $R_L = 500\Omega$.

At a gain of +2, the EL2045C has a −3 dB bandwidth of 100 MHz with a phase margin of 50°. It can drive unlimited load capacitance, and because of its conventional voltage-feedback topology, the EL2045C allows the use of reactive or nonlinear elements in its feedback network. This versatility combined with low cost and 75 mA of output-current drive makes the EL2045C an ideal choice for price-sensitive applications requiring low power and high speed.

Connection Diagram

DIP and SO Package



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EL2045C

Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±18V or 36V
Peak Output Current (I_{OP})	Short-Circuit Protected
Output Short-Circuit Duration (Note 1)	Infinite
Input Voltage (V_{IN})	±V_S
Differential Input Voltage (dV_{IN})	±10V
Power Dissipation (P_D)	See Curves
Operating Temperature Range (T_A)	0°C to +75°C
Operating Junction Temperature (T_J)	150°C
Storage Temperature (T_{ST})	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1000Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		0.5	7.0	I	mV
			T_{MIN}, T_{MAX}			9.0	III	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)	All		10.0		V	μV/°C
I_B	Input Bias Current	V_S = ±15V	25°C		2.8	8.2	I	μA
			T_{MIN}, T_{MAX}			9.2	III	μA
		V_S = ±5V	25°C		2.8		V	μA
I_{OS}	Input Offset Current	V_S = ±15V	25°C		50	300	I	nA
			T_{MIN}, T_{MAX}			400	III	nA
		V_S = ±5V	25°C		50		V	nA
TCI_{OS}	Average Offset Current Drift	(Note 2)	All		0.3		V	nA/°C
A_{VOL}	Open-Loop Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1000Ω	25°C	1500	3000		I	V/V
			T_{MIN}, T_{MAX}	1500			III	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 500Ω	25°C		2500		V	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 150Ω	25°C		1750		V	V/V
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	25°C	65	85		I	dB
			T_{MIN}, T_{MAX}	60			III	dB

DC Electrical Characteristics $V_S = \pm15V, R_L = 1000\Omega$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm12V, V_{OUT} = 0V$	25°C	70	95		I	dB
			T_{MIN}, T_{MAX}	70			III	dB
CMIR	Common-Mode Input Range	$V_S = \pm15V$	25°C		±14.0		V	V
		$V_S = \pm5V$	25°C		±4.2		V	V
		$V_S = +5V$	25°C		4.2/0.1		V	V
V_{OUT}	Output Voltage Swing	$V_S = \pm15V, R_L = 1000\Omega$	25°C	±13.4	±13.6		I	V
			T_{MIN}, T_{MAX}	±13.1			III	V
		$V_S = \pm15V, R_L = 500\Omega$	25°C	±12.0	±13.4		I	V
		$V_S = \pm5V, R_L = 500\Omega$	25°C	±3.4	±3.8		IV	V
		$V_S = \pm5V, R_L = 150\Omega$	25°C		±3.2		V	V
		$V_S = +5V, R_L = 500\Omega$	25°C	3.6/0.4	3.8/0.3		I	V
			T_{MIN}, T_{MAX}	3.5/0.5			III	V
I_{SC}	Output Short Circuit Current		25°C	40	75		I	mA
			T_{MIN}, T_{MAX}	35			III	mA
I_S	Supply Current	$V_S = \pm15V$, No Load	25°C		5.2	7	I	mA
			T_{MIN}, T_{MAX}			7.6	III	mA
		$V_S = \pm5V$, No Load	25°C		5.0		V	mA
R_{IN}	Input Resistance	Differential	25°C		150		V	kΩ
		Common-Mode	25°C		15		V	MΩ
C_{IN}	Input Capacitance	$A_V = +2$ @ 10 MHz	25°C		1.0		V	pF
R_{OUT}	Output Resistance	$A_V = +2$	25°C		50		V	mΩ
PSOR	Power-Supply Operating Range	Dual-Supply	25°C	±2.0		±18.0	V	V
		Single-Supply	25°C	2.5		36.0	V	V

Closed-Loop AC Electrical Characteristics

$V_S = \pm15V, A_V = +2, R_f = R_g = 1\,k\Omega, C_f = 3\,pF, R_L = 1000\Omega$ unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth ($V_{OUT} = 0.4\,V_{PP}$)	$V_S = \pm15V, A_V = +2$	25°C		100		V	MHz
		$V_S = \pm15V, A_V = -1$	25°C		75		V	MHz
		$V_S = \pm15V, A_V = +5$	25°C		20		V	MHz
		$V_S = \pm15V, A_V = +10$	25°C		10		V	MHz
		$V_S = \pm15V, A_V = +20$	25°C		5		V	MHz
		$V_S = \pm5V, A_V = +2$	25°C		75		V	MHz
GBWP	Gain-Bandwidth Product	$V_S = \pm15V$	25°C		100		V	MHz
		$V_S = \pm5V$	25°C		75		V	MHz
PM	Phase Margin	$R_L = 1\,k\Omega, C_L = 10\,pF$	25°C		50		V	°

Closed-Loop AC Electrical Characteristics

$V_S = \pm 15V, A_V = +2, R_f = R_g = 1\ k\Omega, C_f = 3\ pF, R_L = 1000\Omega$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Note 3)	$V_S = \pm 15V, R_L = 1000\Omega$	25°C	200	275		I	V/µs
		$V_S = \pm 5V, R_L = 500\Omega$	25°C		200		V	V/µs
FPBW	Full-Power Bandwidth (Note 4)	$V_S = \pm 15V$	25°C	3.2	4.4		I	MHz
		$V_S = \pm 5V$	25°C		12.7		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Output Step	25°C		3.0		V	ns
OS	Overshoot	0.1V Output Step	25°C		20		V	%
t_{PD}	Propagation Delay		25°C		2.5		V	ns
t_s	Settling to +0.1% ($A_V = +2$)	$V_S = \pm 15V$, 10V Step	25°C		80		V	ns
		$V_S = \pm 5V$, 5V Step	25°C		60		V	ns
dG	Differential Gain (Note 5)	NTSC/PAL	25°C		0.02		V	%
dP	Differential Phase (Note 5)	NTSC/PAL	25°C		0.07		V	°
eN	Input Noise Voltage	10 kHz	25°C		15.0		V	$nV/\sqrt{Hz}$
iN	Input Noise Current	10 kHz	25°C		1.50		V	$pA/\sqrt{Hz}$
CI STAB	Load Capacitance Stability	$A_V = +2$	25°C		Infinite		V	pF

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

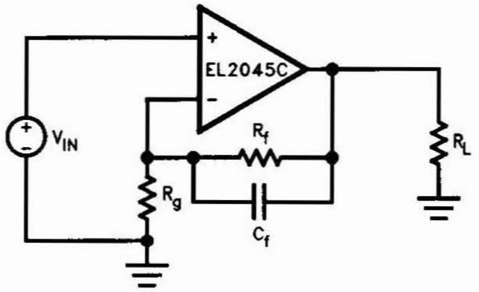
Note 2: Measured from T_{MIN} to T_{MAX}.

Note 3: Slew rate is measured on rising edge.

Note 4: For $V_S = \pm 15V$, $V_{OUT} = 20\ V_{PP}$. For $V_S = \pm 5V$, $V_{OUT} = 5\ V_{PP}$. Full-power bandwidth is based on slew rate measurement using: FPBW = SR/(2π * Vpeak).

Note 5: Video Performance measured at $V_S = \pm 15V$, $A_V = +2$ with 2 times normal video level across $R_L = 150\Omega$. This corresponds to standard video levels across a back-terminated 75Ω load. For other values of R_L, see curves.

EL2045C Test Circuit

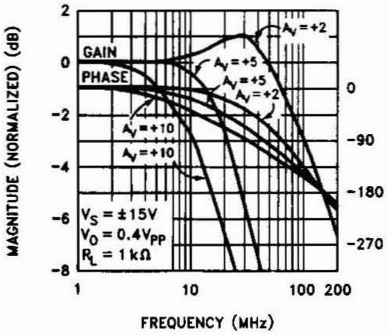


2045-2

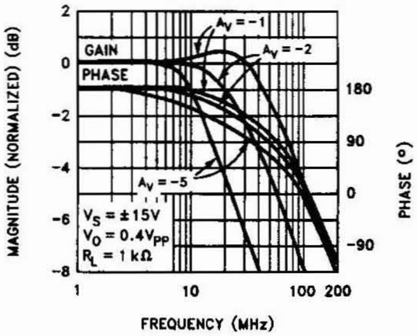
Typical Performance Curves

($T_A = 25°C, R_f = 1\ k\Omega, C_f = 3\ pF, R_L = 1000\Omega, A_V = +2$ unless otherwise specified)

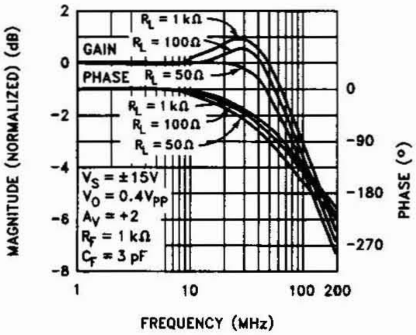
Non-Inverting Frequency Response



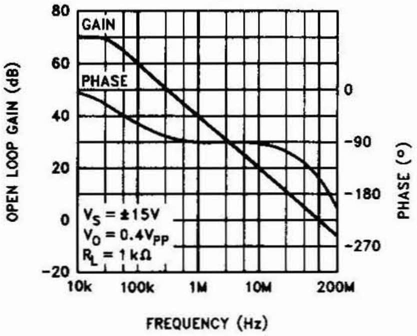
Inverting Frequency Response



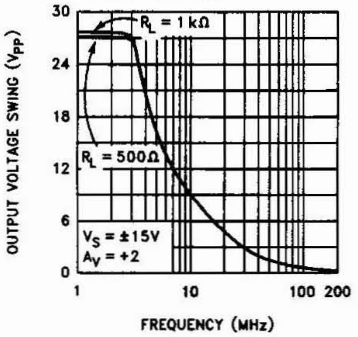
Frequency Response for Various Load Resistances



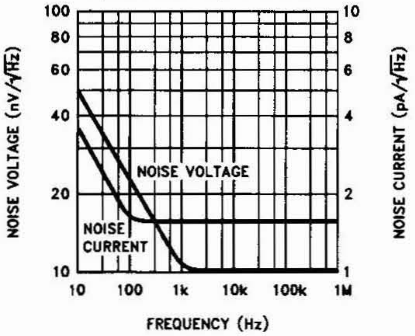
Open-Loop Gain and Phase vs Frequency



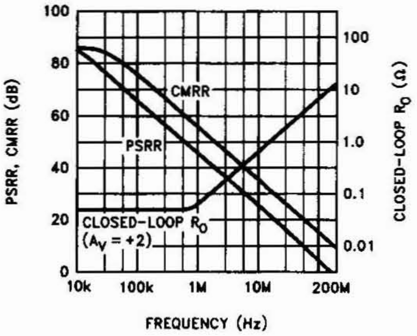
Output Voltage Swing vs Frequency



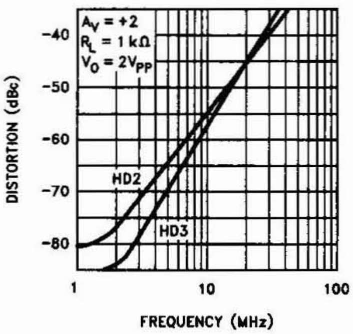
Equivalent Input Noise



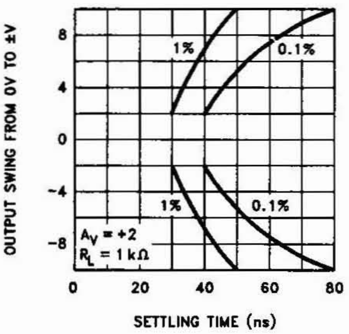
CMRR, PSRR and Closed-Loop Output Resistance vs Frequency



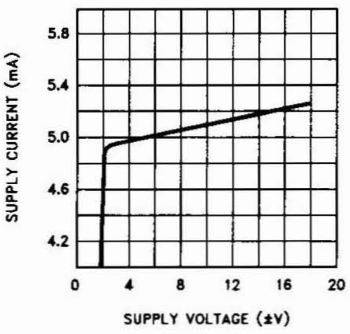
2nd and 3rd Harmonic Distortion vs Frequency



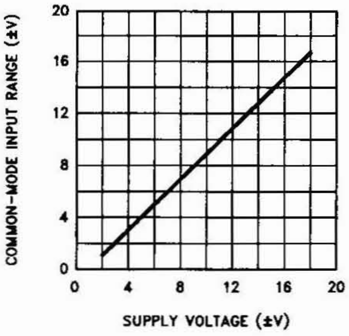
Settling Time vs Output Voltage Change



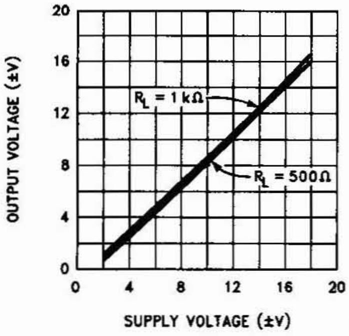
Supply Current vs Supply Voltage



Common-Mode Input Range vs Supply Voltage



Output Voltage Range vs Supply Voltage

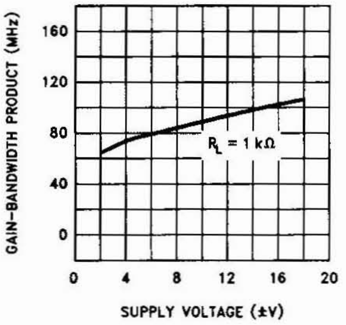


2045-3

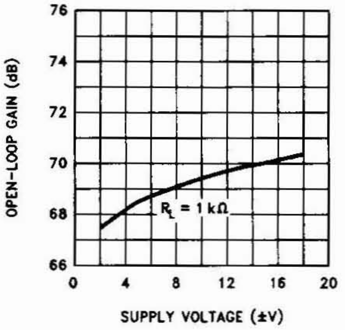
Typical Performance Curves

(T_A = 25°C, R_f = 1 kΩ, C_f = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified) — Contd.

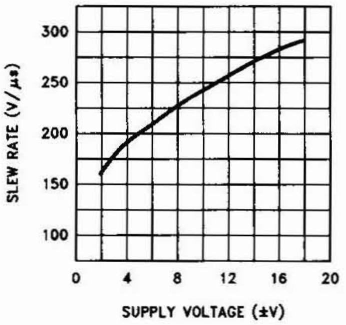
Gain-Bandwidth Product vs Supply Voltage



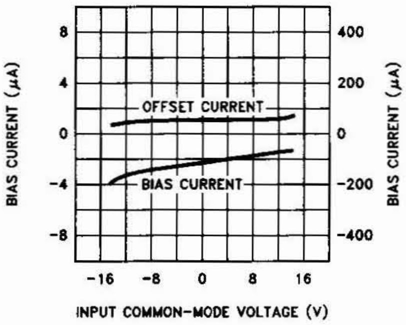
Open-Loop Gain vs Supply Voltage



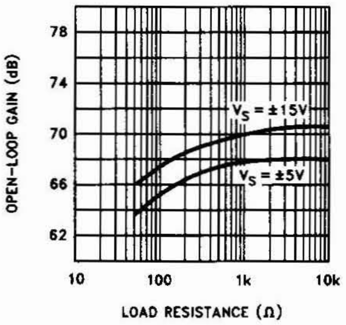
Slew-Rate vs Supply Voltage



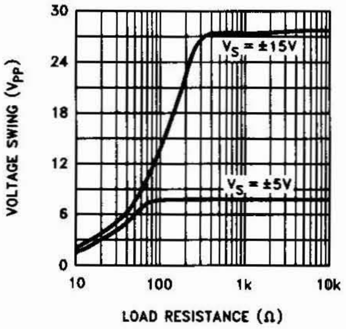
Bias and Offset Current vs Input Common-Mode Voltage



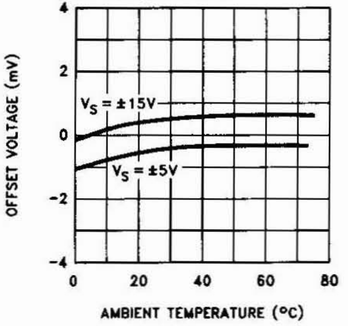
Open-Loop Gain vs Load Resistance



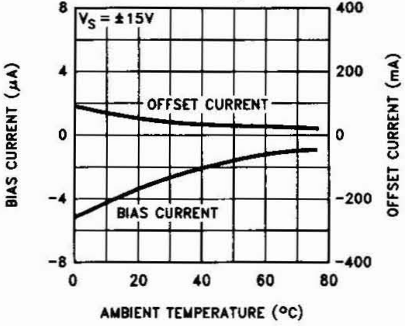
Voltage Swing vs Load Resistance



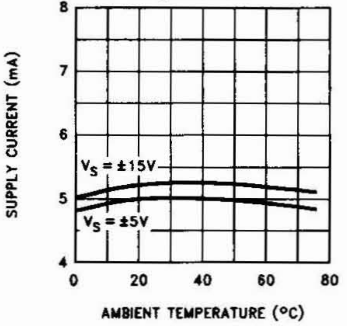
Offset Voltage vs Temperature



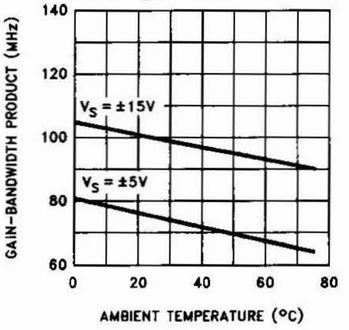
Bias and Offset Current vs Temperature



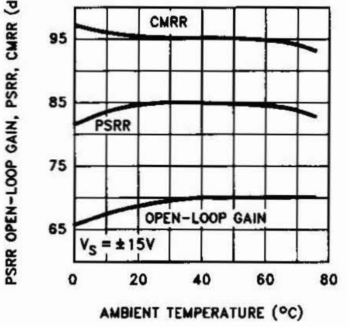
Supply Current vs Temperature



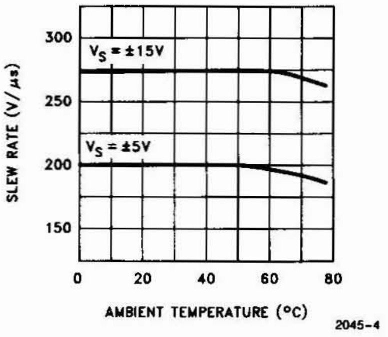
Gain-Bandwidth Product vs Temperature



Open-Loop Gain PSRR and CMRR vs Temperature



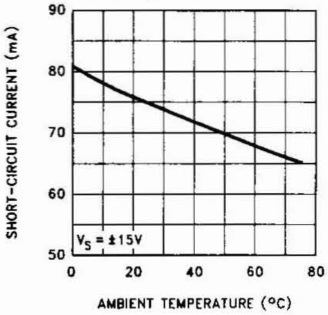
Slew Rate vs Temperature



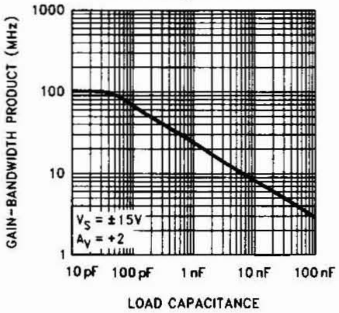
Typical Performance Curves

($T_A = 25°C$, $R_f = 1\ k\Omega$, $C_f = 3\ pF$, $R_L = 1000\Omega$, $A_V = +2$ unless otherwise specified) — Contd.

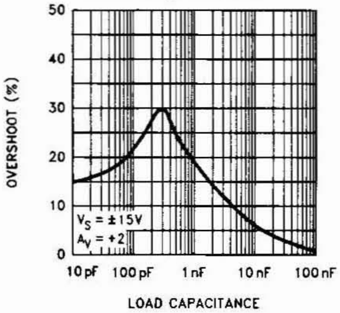
Short-Circuit Current vs Temperature



Gain-Bandwidth Product vs Load Capacitance

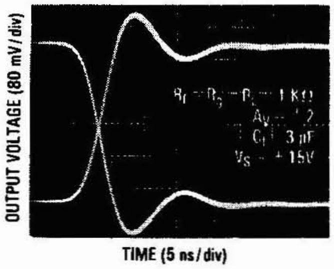


Overshoot vs Load Capacitance



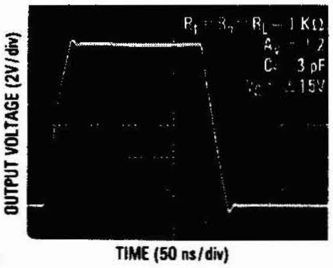
2045-5

Small-Signal Step Response



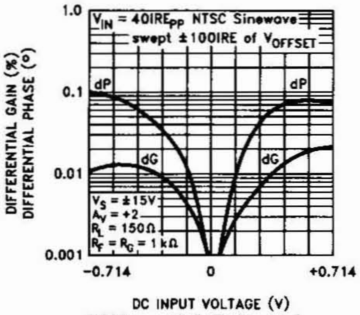
2045-6

Large-Signal Step Response

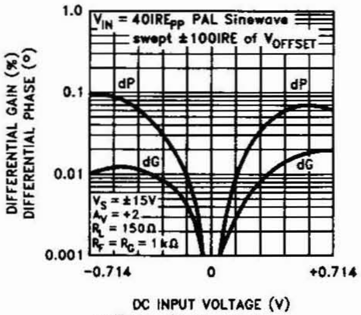


2045-7

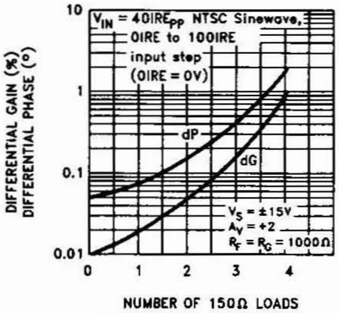
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



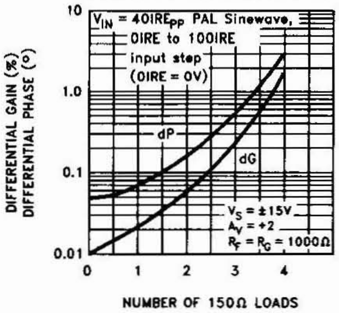
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



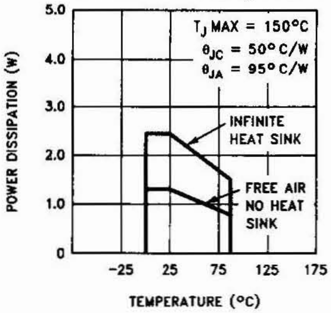
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



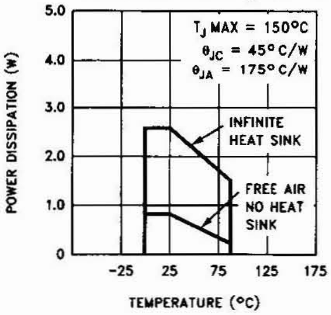
Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead SO Maximum Power Dissipation vs Ambient Temperature

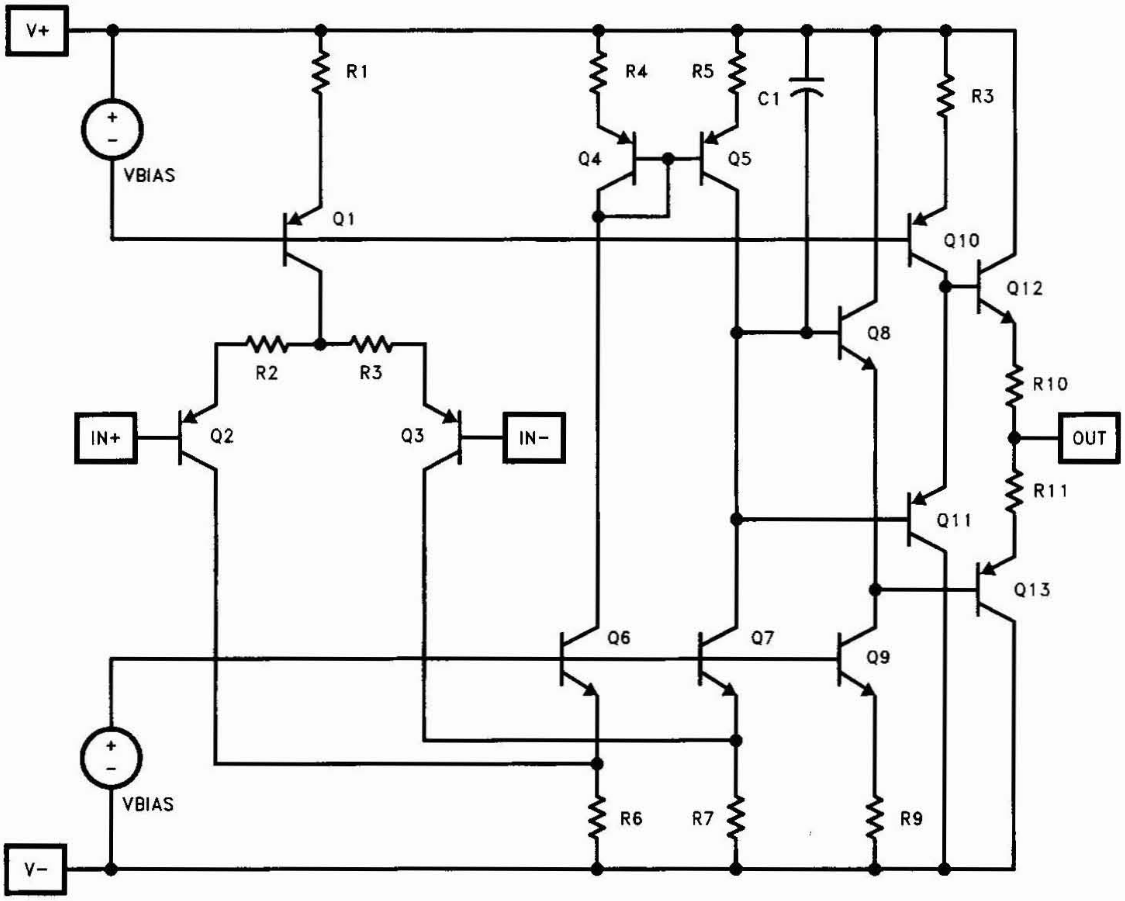


2045-8

EL2045C

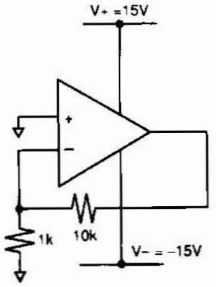
Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

Simplified Schematic


V+
VBIAS
R1
Q1
R2
R3
IN+
Q2
Q3
IN-
R4
R5
C1
Q4
Q5
Q6
Q7
Q8
Q9
R3
Q10
Q11
Q12
Q13
R10
R11
OUT
VBIAS
R6
R7
R9
V-

2045-9

Burn-In Circuit



2045-10

All Packages Use the Same Schematic

Applications Information

Product Description

The EL2045C is a low-power wideband, gain-of-2 stable monolithic operational amplifier built on Elantec's proprietary high-speed complementary bipolar process. The EL2045C uses a classical voltage-feedback topology which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2045C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2045C is an excellent choice for applications such as fast log amplifiers.

Single-Supply Operation

The EL2045C has been designed to have a wide input and output voltage range. This design also makes the EL2045C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground (R_L = 500Ω), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and R_L = 500Ω. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2045C still has 1V of output swing.

Gain-Bandwidth Product and the −3 dB Bandwidth

The EL2045C has a gain-bandwidth product of 100 MHz while using only 5.2 mA of supply current. For gains greater than 4, its closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2045C has a −3 dB bandwidth of 100 MHz at a gain of +2, dropping to 20 MHz at a gain of +5. It is important to note that the EL2045C has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2045C in a gain of +2 only exhibits 1.0 dB of peaking with a 1000Ω load.

Video Performance

An industry-standard method of measuring the video distortion of a component such as the EL2045C is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2045C has been designed as an economical solution for applications requiring low video distortion. It has been thoroughly characterized

Applications Information — Contd.

for video performance in the topology described above, and the results have been included as typical dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2045C exhibits dG and dP of only 0.02% and 0.07° at NTSC and PAL. Because dG and dP can vary with different DC offsets, the video performance of the EL2045C has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The output drive capability of the EL2045C allows it to drive up to 2 back-terminated loads with good video performance. For more demanding applications such as greater output drive or better video distortion, a number of alternatives such as the EL2120, EL400, or EL2074 should be considered.

Output Drive Capability

The EL2045C has been designed to drive low impedance loads. It can easily drive 6 V_{PP} into a 150Ω load. This high output drive capability makes the EL2045C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2045C remains a minimum of 35 mA at low temperatures. The EL2045C is current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2045C has been designed to drive any capacitive load. However, the EL2045C remains stable by automatically reducing its gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (Rs). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2045C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2045C is well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2045C Macromodel

This macromodel has been developed to assist the user in simulating the EL2045C with surrounding circuitry. It has been developed for the PSPICE simulator (copywritten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

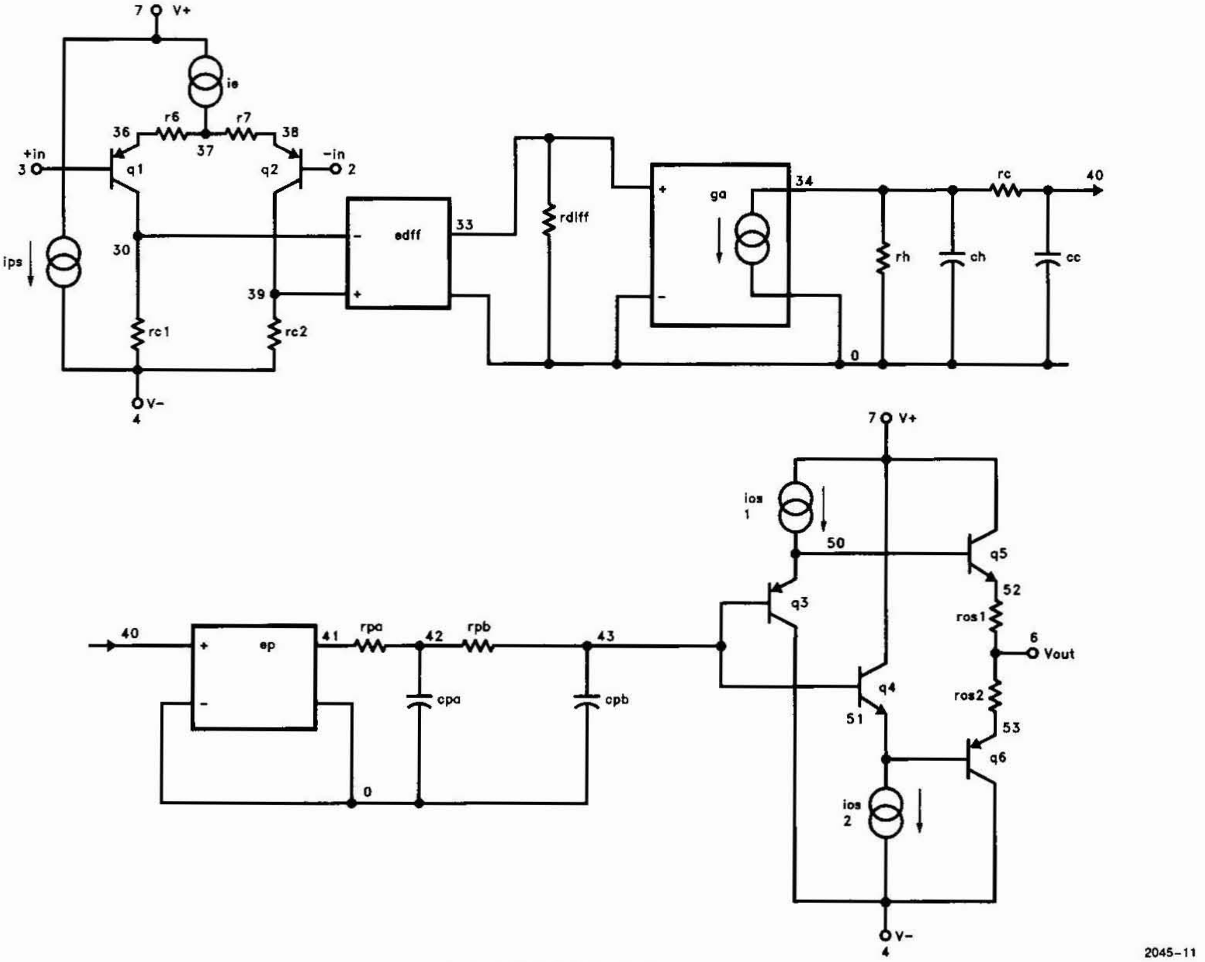
The model does not simulate these characteristics accurately:

noise
settling-time
CMRR
PSRR
non-linearities
temperature effects
manufacturing variations

EL2045C Macromodel — Contd.

```
* Connections:  +input
*               |    -input
*               |    |    +Vsupply
*               |    |    |    -Vsupply
*               |    |    |    |    output
*               |    |    |    |    |
.subckt M2045   3    2    7    4    6
*
* Input stage
*
ie 7 37 0.9mA
r6 36 37 400
r7 38 37 400
rc1 4 30 850
rc2 4 39 850
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 1m
rh 34 0 2Meg
ch 34 0 1.5pF
rc 34 40 1K
cc 40 0 1pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 200
cpa 42 0 2pF
rpb 42 43 200
cpb 43 0 2pF
*
* Output Stage
*
ios1 7 50 1.0mA
ios2 51 4 1.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
*
* Power Supply Current
*
ips 7 4 2.7mA
*
* Models
*
.model qn npn(is=800E-18 bf=200 tf=0.2nS)
.model qpa pnp(is=864E-18 bf=100 tf=0.2nS)
.model qp pnp(is=800E-18 bf=125 tf=0.2nS)
.ends
```

EL2045C Macromodel — Contd.


7 V+
ie
r6
r7
36
37
38
+in
3
q1
q2
-in
2
ips
30
39
rc1
rc2
V-
4
edff
33
rdiff
ga
34
rh
ch
rc
40
cc
0
7 V+
ios 1
50
q5
q3
52
ros1
6 Vout
ros2
q4
51
53
q6
ios 2
V-
4
40
ep
41
rpa
42
rpb
43
cpa
cpb
0
2045-11

EL2045C Model

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2245C/EL2445C

Dual/Quad Low-Power 100 MHz Gain-of-2 Stable Op Amp

Features

- 100 MHz gain-bandwidth product
- Gain-of-2 stable
- Low supply current (per Amplifier) = 5.2 mA at $V_S = \pm 15V$
- Wide supply range
  = ±2V to ±18V dual-supply
  = 2.5V to 36V single-supply
- High slew rate = 275 V/µs
- Fast settling = 80 ns to 0.1% for a 10V step
- Low differential gain = 0.02% at $A_V = +2, R_L = 150\Omega$
- Low differential phase = 0.07° at $A_V = +2, R_L = 150\Omega$
- Stable with unlimited capacitive load
- Wide output voltage swing
  = $\pm 13.6V$ with $V_S = \pm 15V$, $R_L = 1000\Omega$
  = 3.8V/0.3V with $V_S = +5V$, $R_L = 500\Omega$

Applications

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
Duals			
EL2245CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2245CS	0°C to +75°C	8-Lead SO	MDP0027
Quads			
EL2445CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2445CS	0°C to +75°C	14-Lead SO	MDP0027

General Description

The EL2245C/EL2445C are dual and quad versions of the popular EL2045C. They are high speed, low power, low cost monolithic operational amplifiers built on Elantec's proprietary complementary bipolar process. The EL2245C/EL2445C are unity-gain stable and feature a 275 V/µs slew rate and 100 MHz gain-bandwidth product while requiring only 5.2 mA of supply current per amplifier.

The power supply operating range of the EL2245C/EL2445C is from ±18V down to as little as ±2V. For single-supply operation, the EL2245C/EL2445C operate from 36V down to as little as 2.5V. The excellent power supply operating range of the EL2245C/EL2445C makes them an obvious choice for applications on a single +5V or +3V supply.

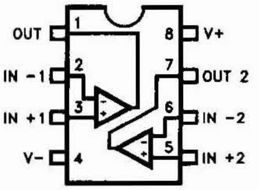
The EL2245C/EL2445C also feature an extremely wide output voltage swing of $\pm 13.6V$ with $V_S = \pm 15V$ and $R_L = 1000\Omega$. At ±5V, output voltage swing is a wide ±3.8V with $R_L = 500\Omega$ and ±3.2V with $R_L = 150\Omega$. Furthermore, for single-supply operation at +5V, output voltage swing is an excellent 0.3V to 3.8V with $R_L = 500\Omega$.

At a gain of +2, the EL2245C/EL2445C have a −3 dB bandwidth of 100 MHz with a phase margin of 50°. They can drive unlimited load capacitance, and because of their conventional voltage-feedback topology, the EL2245C/EL2445C allow the use of reactive or non-linear elements in their feedback network. This versatility combined with low cost and 75 mA of output-current drive make the EL2245C/EL2445C an ideal choice for price-sensitive applications requiring low power and high speed.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

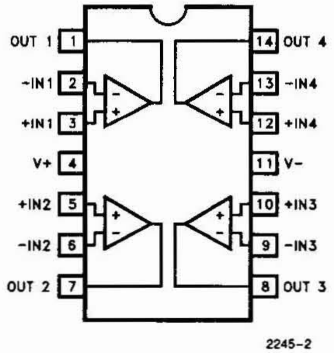
Connection Diagrams

EL2245CN/CS
Dual



2245-1

EL2445CN/CS
Quad



2245-2

December 1995 Rev C

Absolute Maximum Ratings ($T_A = 25°C$)

Supply Voltage (V_S)	±18V or 36V	Power Dissipation (P_D)	See Curves
Peak Output Current (I_{OP})	Short-Circuit Protected	Operating Temperature Range (T_A)	0°C to +75°C
Output Short-Circuit Duration (Note 1)	Infinite	Operating Junction Temperature (T_J)	150°C
Input Voltage (V_{IN})	$\pm V_S$	Storage Temperature (T_{ST})	−65°C to +150°C
Differential Input Voltage (dV_{IN})	±10V		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1000\Omega$, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	$V_S = \pm 15V$	25°C		0.5	4.0	I	mV
			T_{MIN}, T_{MAX}			6.0	III	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)	All		10.0		V	µV/°C
I_B	Input Bias Current	$V_S = \pm 15V$	25°C		2.8	8.2	I	µA
			T_{MIN}, T_{MAX}			9.2	III	µA
		$V_S = \pm 5V$	25°C		2.8		V	µA
I_{OS}	Input Offset Current	$V_S = \pm 15V$	25°C		50	300	I	nA
			T_{MIN}, T_{MAX}			400	III	nA
		$V_S = \pm 5V$	25°C		50		V	nA
TCI_{OS}	Average Offset Current Drift	(Note 2)	All		0.3		V	nA/°C
A_{VOL}	Open-Loop Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 1000\Omega$	25°C	1500	3000		I	V/V
			T_{MIN}, T_{MAX}	1500			III	V/V
		$V_S = \pm 5V$, $V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$	25°C		2500		V	V/V
		$V_S = \pm 5V$, $V_{OUT} = \pm 2.5V$, $R_L = 150\Omega$	25°C		1750		V	V/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	25°C	65	80		I	dB
			T_{MIN}, T_{MAX}	60			III	dB

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1000\Omega$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12V$, $V_{OUT} = 0V$	25°C	70	90		I	dB
			T_{MIN}, T_{MAX}	70			III	dB
CMIR	Common-Mode Input Range	$V_S = \pm 15V$	25°C		±14.0		V	V
		$V_S = \pm 5V$	25°C		±4.2		V	V
		$V_S = +5V$	25°C		4.2/0.1		V	V
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 1000\Omega$	25°C	±13.4	±13.6		I	V
			T_{MIN}, T_{MAX}	±13.1			III	V
		$V_S = \pm 15V$, $R_L = 500\Omega$	25°C	±12.0	±13.4		I	V
		$V_S = \pm 5V$, $R_L = 500\Omega$	25°C	±3.4	±3.8		IV	V
		$V_S = \pm 5V$, $R_L = 150\Omega$	25°C		±3.2		V	V
		$V_S = +5V$, $R_L = 500\Omega$	25°C	3.6/0.4	3.8/0.3		I	V
			T_{MIN}, T_{MAX}	3.5/0.5			III	V
I_{SC}	Output Short Circuit Current		25°C	40	75		I	mA
			T_{MIN}, T_{MAX}	35			III	mA
I_S	Supply Current (Per Amplifier)	$V_S = \pm 15V$, No Load	25°C		5.2	7	I	mA
			T_{MIN}			7.6	III	mA
			T_{MAX}			7.6	III	mA
		$V_S = \pm 5V$, No Load	25°C		5.0		V	mA
R_{IN}	Input Resistance	Differential	25°C		150		V	kΩ
		Common-Mode	25°C		15		V	MΩ
C_{IN}	Input Capacitance	$A_V = +1$@ 10 MHz	25°C		1.0		V	pF
R_{OUT}	Output Resistance	$A_V = +1$	25°C		50		V	mΩ
PSOR	Power-Supply Operating Range	Dual-Supply	25°C	±2.0		±18.0	V	V
		Single-Supply	25°C	2.5		36.0	V	V

Closed-Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +1$, $R_L = 1000\Omega$ unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth ($V_{OUT} = 0.4\ V_{PP}$)	$V_S = \pm 15V$, $A_V = +2$	25°C		100		V	MHz
		$V_S = \pm 15V$, $A_V = -1$	25°C		75		V	MHz
		$V_S = \pm 15V$, $A_V = +5$	25°C		20		V	MHz
		$V_S = \pm 15V$, $A_V = +10$	25°C		10		V	MHz
		$V_S = \pm 15V$, $A_V = +20$	25°C		5		V	MHz
		$V_S = \pm 5V$, $A_V = +2$	25°C		75		V	MHz
GBWP	Gain-Bandwidth Product	$V_S = \pm 15V$	25°C		100		V	MHz
		$V_S = \pm 5V$	25°C		75		V	MHz

Closed-Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +2$, $R_L = 1000\Omega$ unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
PM	Phase Margin	$R_L = 1\ k\Omega$, $C_L = 10\ pF$	25°C		50		V	°
CS	Channel Separation	f = 5 MHz	25°C		85		V	dB
SR	Slew Rate (Note 3)	$V_S = \pm 15V$, $R_L = 1000\Omega$	25°C	200	275		I	V/µs
		$V_S = \pm 5V$, $R_L = 500\Omega$	25°C		200		V	V/µs
FPBW	Full-Power Bandwidth (Note 4)	$V_S = \pm 15V$	25°C	3.2	4.4		I	MHz
		$V_S = \pm 5V$	25°C		12.7		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step	25°C		3.0		V	ns
OS	Overshoot	0.1V Step	25°C		20		V	%
t_{PD}	Propagation Delay		25°C		2.5		V	ns
t_s	Settling to +0.1% ($A_V = +1$)	$V_S = \pm 15V$, 10V Step	25°C		80		V	ns
		$V_S = \pm 5V$, 5V Step	25°C		60		V	ns
dG	Differential Gain (Note 5)	NTSC/PAL	25°C		0.02		V	%
dP	Differential Phase (Note 5)	NTSC/PAL	25°C		0.07		V	°
eN	Input Noise Voltage	10 kHz	25°C		15.0		V	nV/√Hz
iN	Input Noise Current	10 kHz	25°C		1.50		V	pA/√Hz
CI STAB	Load Capacitance Stability	$A_V = +1$	25°C		Infinite		V	pF

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

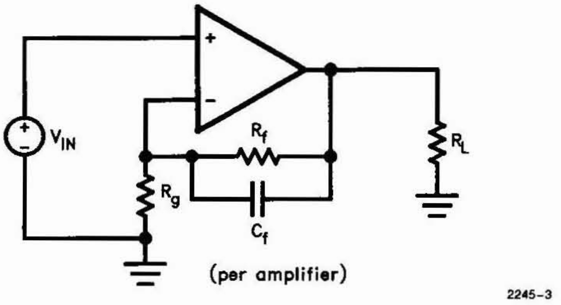
Note 2: Measured from T_{MIN} to T_{MAX}.

Note 3: Slew rate is measured on rising edge.

Note 4: For $V_S = \pm 15V$, $V_{OUT} = 20\ V_{PP}$. For $V_S = \pm 5V$, $V_{OUT} = 5\ V_{PP}$. Full-power bandwidth is based on slew rate measurement using: FPBW = SR/(2π * Vpeak).

Note 5: Video Performance measured at $V_S = \pm 15V$, $A_V = +2$ with 2 times normal video level across $R_L = 150\Omega$. This corresponds to standard video levels across a back-terminated 75Ω load. For other values of R_L, see curves.

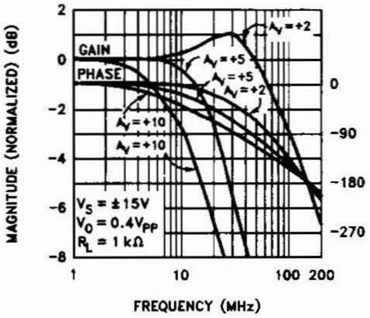
EL2245C/EL2445C Test Circuit



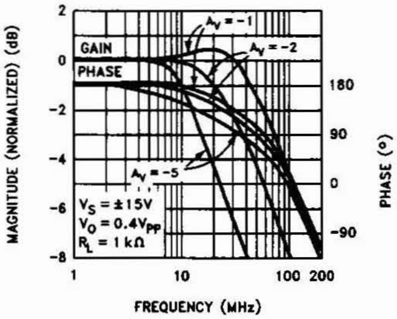
Typical Performance Curves

(T_A = 25°C, R_F = 1 kΩ, C_F = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified)

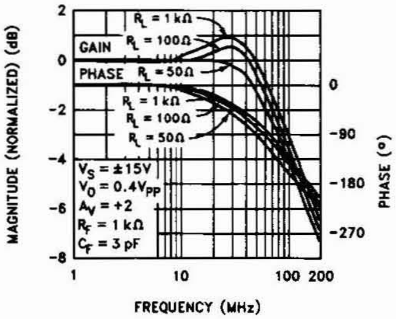
Non-Inverting Frequency Response



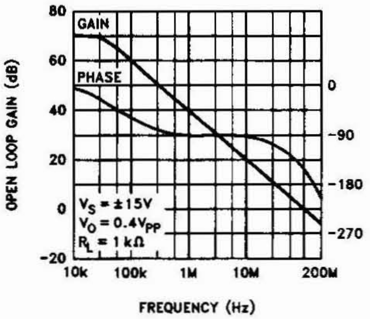
Inverting Frequency Response



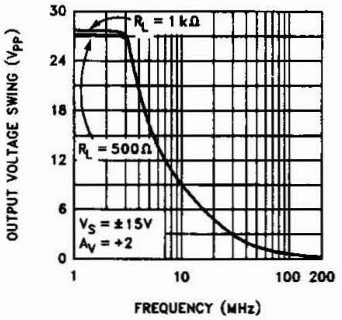
Frequency Response for Various Load Resistances



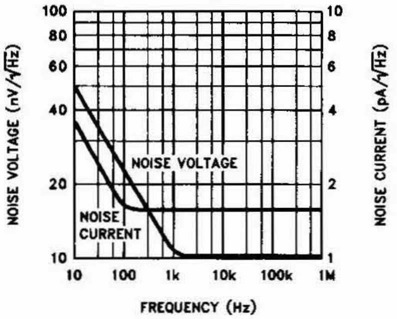
Open-Loop Gain and Phase vs Frequency



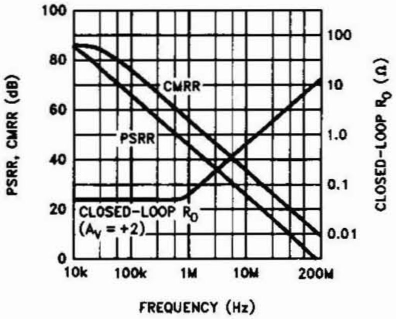
Output Voltage Swing vs Frequency



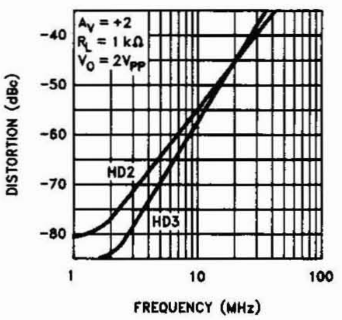
Equivalent Input Noise



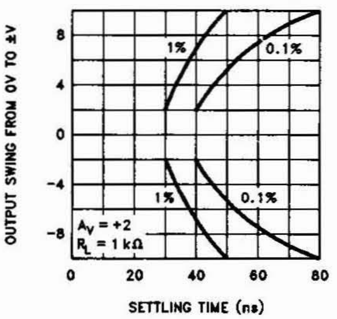
CMRR, PSRR and Closed-Loop Output Resistance vs Frequency



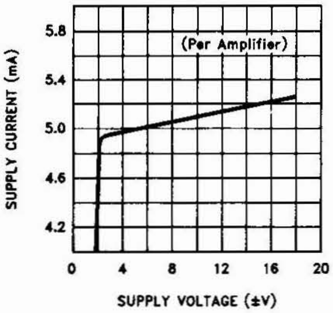
2nd and 3rd Harmonic Distortion vs Frequency



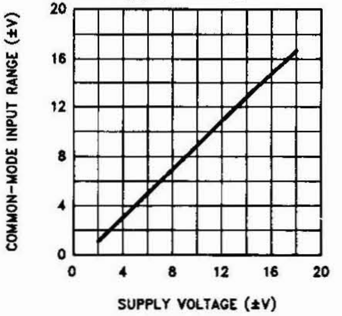
Settling Time vs Output Voltage Change



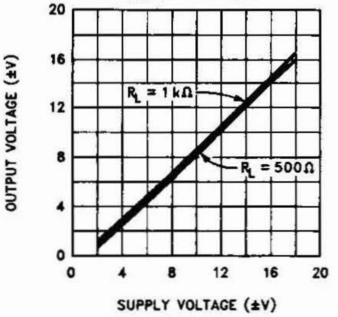
Supply Current vs Supply Voltage



Common-Mode Input Range vs Supply Voltage



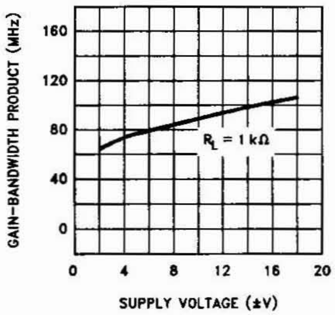
Output Voltage Range vs Supply Voltage

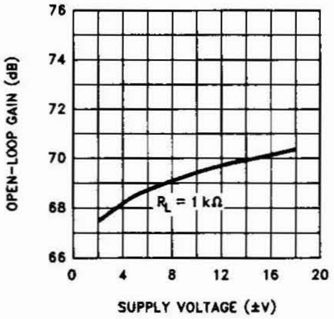


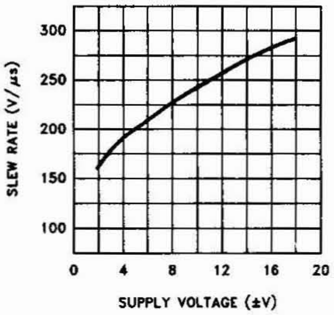
2245-4

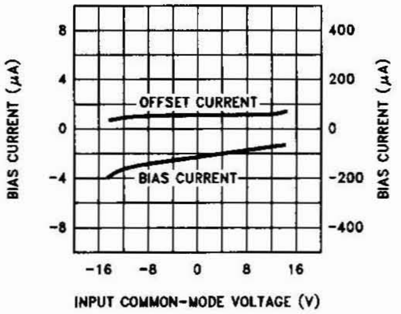
Typical Performance Curves

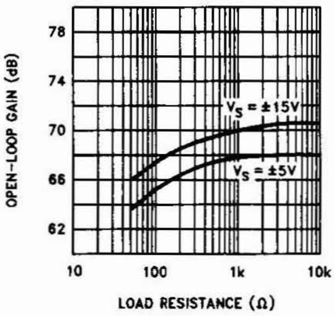
(T_A = 25°C, R_F = 1 kΩ, C_F = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified) — Contd.

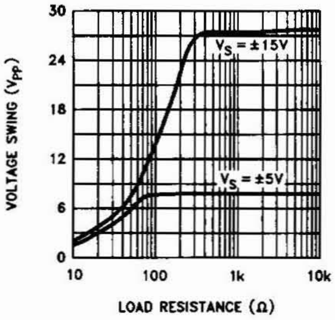

Gain-Bandwidth Product vs Supply Voltage

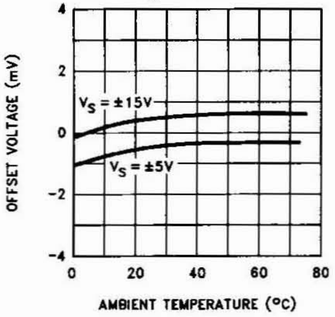

Open-Loop Gain vs Supply Voltage

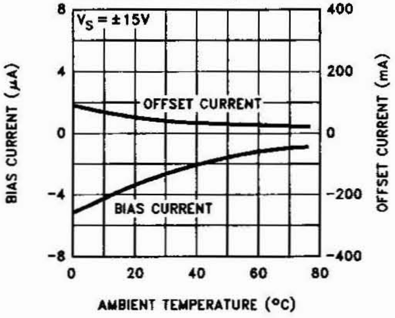

Slew-Rate vs Supply Voltage

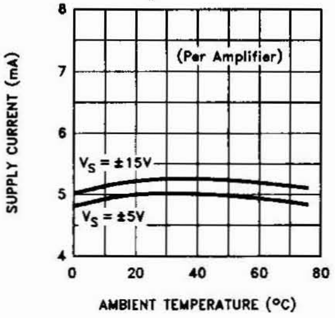

Bias and Offset Current vs Input Common-Mode Voltage

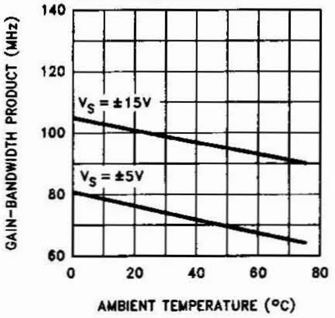

Open-Loop Gain vs Load Resistance

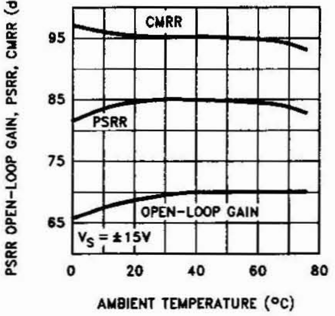

Voltage Swing vs Load Resistance

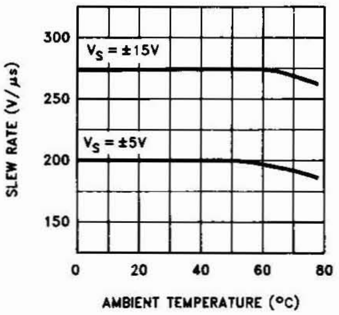

Offset Voltage vs Temperature


Bias and Offset Current vs Temperature


Supply Current vs Temperature


Gain-Bandwidth Product vs Temperature


Open-Loop Gain PSRR and CMRR vs Temperature

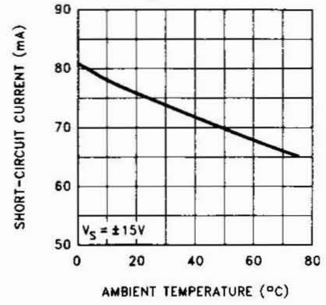

Slew Rate vs Temperature

2245-5

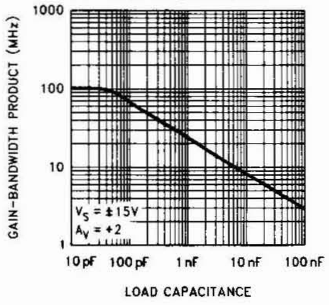
Typical Performance Curves

($T_A = 25°C, R_F = 1\ k\Omega, C_F = 3\ pF, R_L = 1000\Omega, A_V = +2$ unless otherwise specified) — Contd.

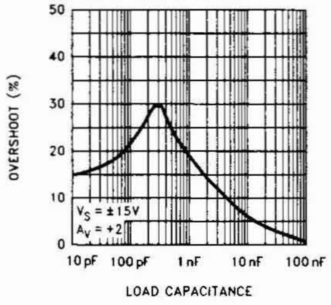
Short-Circuit Current vs Temperature



Gain-Bandwidth Product vs Load Capacitance

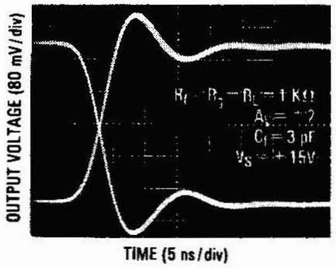


Overshoot vs Load Capacitance



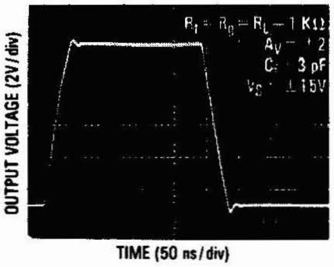
2245-6

Small-Signal Step Response



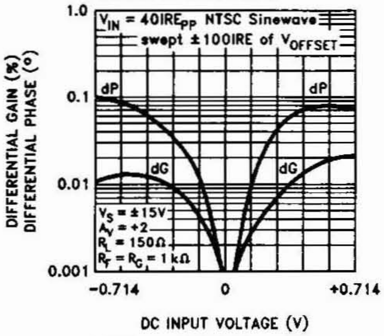
2245-7

Large-Signal Step Response

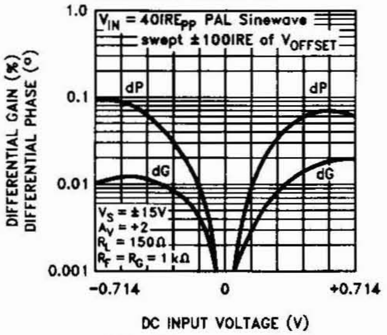


2245-8

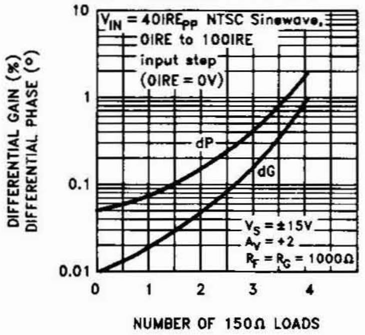
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



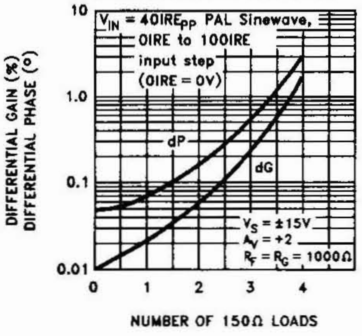
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



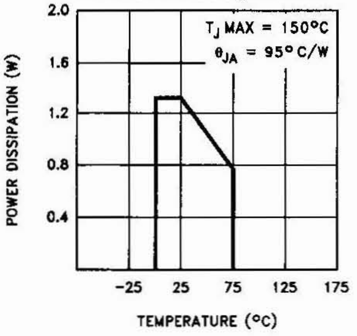
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



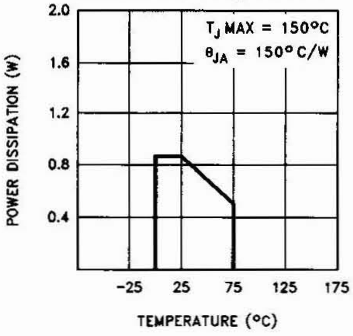
Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



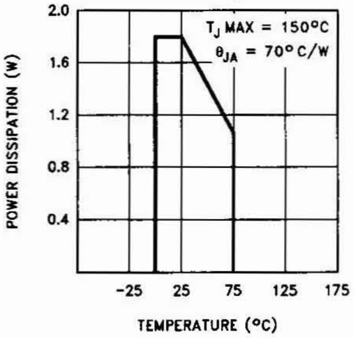
8-Lead SO Maximum Power Dissipation vs Ambient Temperature



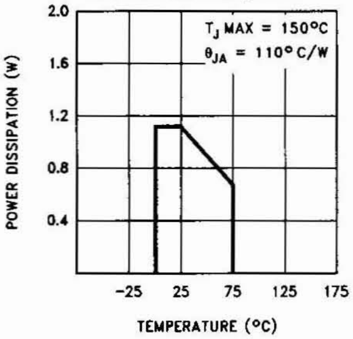
2245-9

Typical Performance Curves

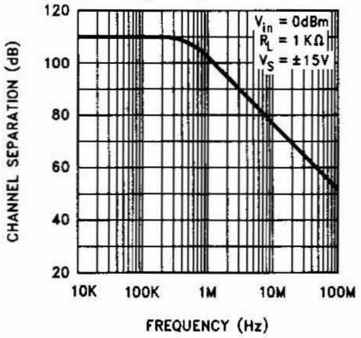
(T_A = 25°C, R_F = 1 kΩ, C_F = 3 pF, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.



14-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



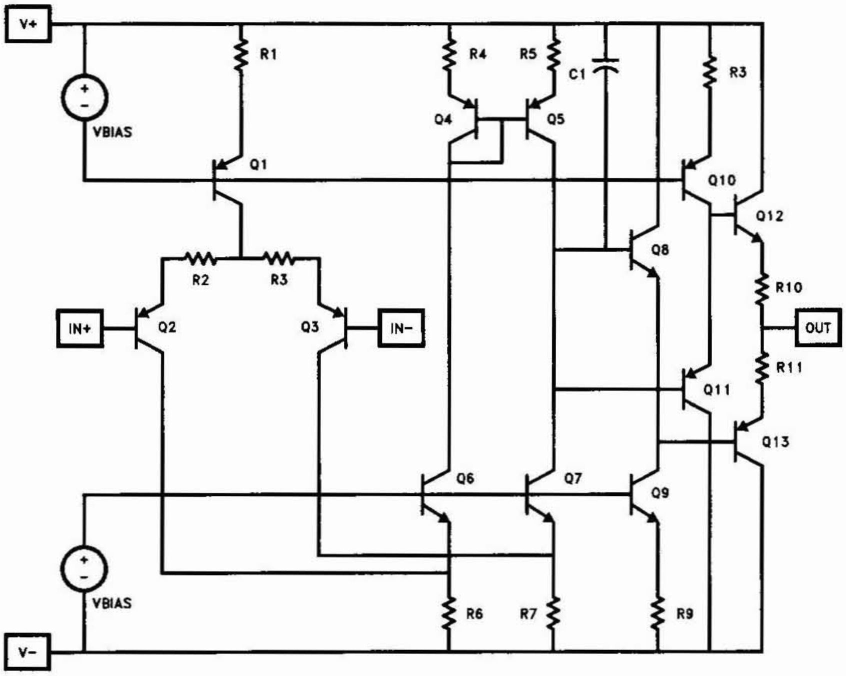
14-Lead SO Maximum Power Dissipation vs Ambient Temperature



Channel Separation vs Frequency

2245-10

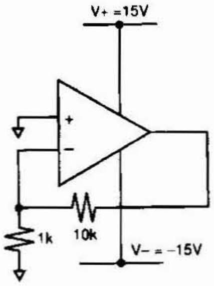
Simplified Schematic (Per Amplifier)



V+
VBIAS
R1
Q1
R2
R3
IN+
Q2
Q3
IN−
R4
R5
C1
Q4
Q5
R3
Q10
Q12
Q8
R10
OUT
R11
Q11
Q13
Q6
Q7
Q9
VBIAS
R6
R7
R9
V−

2245-11

Burn-In Circuit (Per Amplifier)



V+ = 15V
+
−
1k
10k
V− = −15V

2245-12

All Packages Use the Same Schematic

Applications Information

Product Description

The EL2245C/EL2445C are dual and quad low-power wideband monolithic operational amplifiers built on Elantec's proprietary high-speed complementary bipolar process. The EL2245C/EL2445C use a classical voltage-feedback topology which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2245C/EL2445C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2245C/EL2445C are an excellent choice for applications such as fast log amplifiers.

Power Dissipation

With the wide power supply range and large output drive capability of the EL2245C/EL2445C, it is possible to exceed the 150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{Jmax}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified for the EL2245C/EL2445C to remain in the safe operating area. These parameters are related as follows:

$$T_{Jmax} = T_{max} + (\theta_{JA} * (PDmaxtotal))$$

where PDmaxtotal is the sum of the maximum power dissipation of each amplifier in the package (PDmax). PDmax for each amplifier can be calculated as follows:

$$PDmax = (2 * V_S * I_{Smax} + (V_S - V_{outmax}) * (V_{outmax}/R_L))$$

where:

T_{max} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
PDmax = Maximum Power Dissipation of 1 Amplifier
V_S = Supply Voltage
I_{Smax} = Maximum Supply Current of 1 Amplifier
V_{outmax} = Maximum Output Voltage Swing of the Application
R_L = Load Resistance

To serve as a guide for the user, we can calculate maximum allowable supply voltages for the example of the video cable-driver below since we know that T_{Jmax} = 150°C, T_{max} = 75°C, I_{Smax} = 7.6 mA, and the package θ_{JA}s are shown in Table 1. If we assume (for this example) that we are driving a back-terminated video cable, then the maximum average value (over duty-cycle) of V_{outmax} is 1.4V, and R_L = 150Ω, giving the results seen in Table 1.

Table 1

Duals	Package	θ_{JA}	Max PDiss @ T_{max}	Max V_S
EL2245CN	PDIP8	95°C/W	0.789W @ 75°C	±16.6V
EL2245CS	SO8	150°C/W	0.500W @ 75°C	±10.7V
QUADS				
EL2445CN	PDIP14	70°C/W	1.071W @ 75°C	±11.5V
EL2445CS	SO14	110°C/W	0.682W @ 75°C	±7.5V

Single-Supply Operation

The EL2245C/EL2445C have been designed to have a wide input and output voltage range. This design also makes the EL2245C/EL2445C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground (R_L = 500Ω), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and R_L = 500Ω. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2245C/EL2445C still have 1V of output swing.

Gain-Bandwidth Product and the −3 dB Bandwidth

The EL2245C/EL2445C have a gain-bandwidth product of 100 MHz while using only 5.2 mA of supply current per amplifier. For gains greater

Applications Information — Contd.

than 4, their closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifiers' transfer function contribute to even higher closed loop bandwidths. For example, the EL2245C/EL2445C have a −3 dB bandwidth of 100 MHz at a gain of +2, dropping to 20 MHz at a gain of +5. It is important to note that the EL2245C/EL2445C have been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2245C/EL2445C in a gain of +2 only exhibit 1.0 dB of peaking with a 1000Ω load.

Video Performance

An industry-standard method of measuring the video distortion of components such as the EL2245C/EL2445C is to measure the amount of differential gain (dG) and differential phase (dP) that they introduce. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2245C/EL2445C have been designed as an economical solution for applications requiring low video distortion. They have been thoroughly characterized for video performance in the topology described above, and the results have been included as typical dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2245C/EL2445C exhibit dG and dP of only 0.02% and 0.07° at NTSC and PAL. Because dG and dP can vary with different DC offsets, the video performance of the EL2245C/EL2445C has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

Output Drive Capability

The EL2245C/EL2445C have been designed to drive low impedance loads. They can easily drive 6 V_{PP} into a 150Ω load. This high output drive capability makes the EL2245C/EL2445C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2245C/EL2445C remains a minimum of 35 mA at low temperatures. The EL2245C/EL2445C are current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2245C/EL2445C have been designed to drive any capacitive load. However, the EL2245C/EL2445C remain stable by automatically reducing their gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (Rs). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2245C/EL2445C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2245C/EL2445C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum

Applications Information — Contd.

performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2245C/EL2445C Macromodel

This macromodel has been developed to assist the user in simulating the EL2245C/EL2445C with surrounding circuitry. It has been developed for the PSPICE simulator (copywritten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

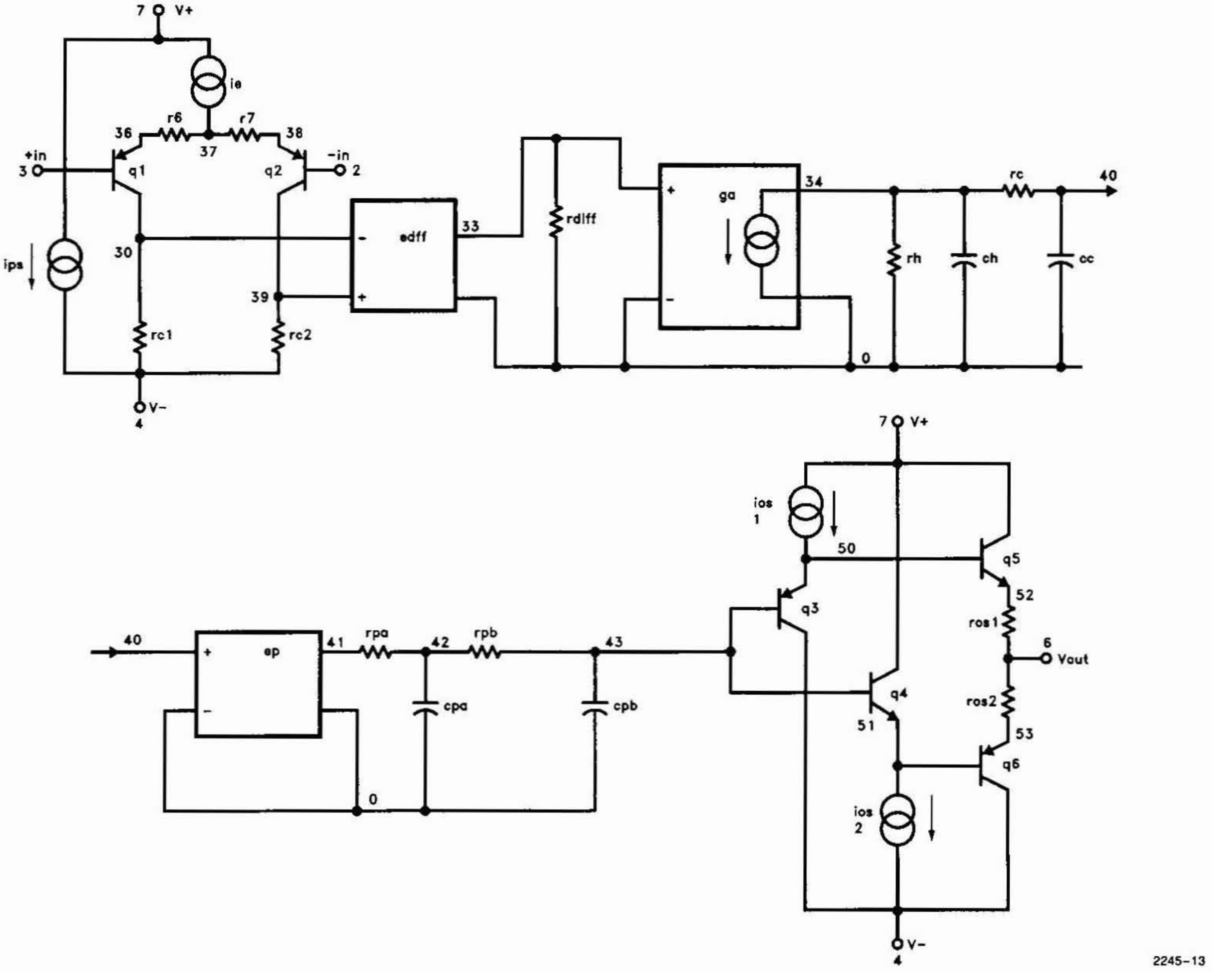
The model does not simulate these characteristics accurately:

noise
settling-time
CMRR
PSRR

non-linearities
temperature effects
manufacturing variations

```
* Connections:   +input
*                |     -input
*                |     |     +Vsupply
*                |     |     |     -Vsupply
*                |     |     |     |     output
*                |     |     |     |     |
.subckt M2245    3     2     7     4     6
*
* Input stage
*
ie 7 37 1mA
r6 36 37 400
r7 38 37 400
rc1 4 30 850
rc2 4 39 850
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 1m
rh 34 0 2Meg
ch 34 0 1.3pF
rc 34 40 1K
cc 40 0 1pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 200
cpa 42 0 1pF
rpb 42 43 200
cpb 43 0 1pF
*
* Output Stage
*
ios1 7 50 1.0mA
ios2 51 4 1.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
*
* Power Supply Current
*
ips 7 4 2.7mA
*
* Models
*
.model qn npn(is=800E-18 bf=200 tf=0.2nS)
.model qpa pnp(is=864E-18 bf=100 tf=0.2nS)
.model qp pnp(is=800E-18 bf=125 tf=0.2nS)
.ends
```

EL2245C/EL2445C Macromodel — Contd.


7 V+
ie
r6
r7
36
37
38
+in
3
q1
q2
-in
2
ips
30
39
rc1
rc2
V-
4
edff
33
rdiff
ga
34
rh
ch
rc
cc
40
0
7 V+
ios 1
50
q5
q3
52
ros1
6
Vout
40
ep
41
rpa
42
rpb
43
cpa
cpb
0
q4
51
ros2
53
q6
ios 2
V-
4
2245-13

EL2245C/EL2445C Model

EL2070C
200 MHz Current Feedback Amplifier

Features

- 200 MHz −3 dB bandwidth, $A_V = 2$
- Disable/enable
- 12 ns settling to 0.05%
- $V_S = \pm 5V$ @ 15 mA
- Low distortion: HD2, HD3 @ −60 dBc at 20 MHz
- Differential gain 0.02% at NTSC, PAL
- Differential phase 0.01° at NTSC, PAL
- Overload/short-circuit protected
- ±1 to ±8 closed-loop gain range
- Low cost

Applications

- Video gain block
- Video distribution
- HDTV amplifier
- Analog multiplexing (using disable)
- Power-down mode (using disable)
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2070CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2070CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

The EL2070 is a wide bandwidth, fast settling monolithic amplifier incorporating a disable/enable feature. Built using an advanced complementary bipolar process, this amplifier uses current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of ±1 to ±8, the EL2070 has a 200 MHz −3 dB bandwidth ($A_V = +2$), and 12 ns settling to 0.05% while consuming only 15 mA of supply current. Furthermore, the fast disable/enable times of 200 ns/100 ns allow rapid analog multiplexing.

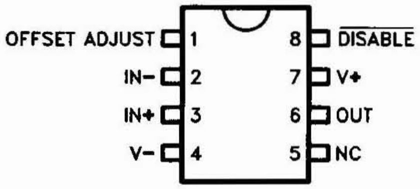
The EL2070 is an obvious high-performance solution for video distribution and line-driving applications, especially when its disable feature can be used for fast analog multiplexing. Furthermore, the low 15 mA supply current, and the very low 5 mA of supply current when disabled suggest use in systems where power is critical. With differential gain/phase of 0.02%/0.01°, guaranteed video specifications, and a minimum 50 mA output drive, performance in these areas is assured.

The EL2070's settling to 0.05% in 12 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 200 MHz bandwidth and extremely linear phase allow unmatched signal fidelity. D/A systems can also benefit from the EL2070, especially if linearity and drive levels are important.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



2070-1

Top View

Manufactured under U.S. Patent No. 4,893,091

EL2070C

200 MHz Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	5V
Disable Input Voltage	$+V_S$, $-1V$
Thermal Resistance θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO-8	
Applied Output Voltage (Disabled)	$\pm V_S$
Power Dissipation	See Curves
Operating Temperature EL2070C	−40C to +85C
Lead Temperature (Soldering, 5 Seconds)	300°C
Junction Temperature	175°C
Storage Temperature	−60°C to +150°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±5V, R_L = 100Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		25°C		2	5.5	I	mV
			T_{MIN}			8.2	III	mV
			T_{MAX}			9.0	III	mV
$d(V_{OS})/dT$	Average Offset Voltage Drift	(Note 1)	All		10.0	40.0	IV	µV/°C
$+I_{IN}$	+Input Current		25°C, T_{MAX}		10	25.0	II	µA
			T_{MIN}			36.0	III	µA
$d(+I_{IN})/dT$	Average +Input Current Drift	(Note 1)	All		50.0	200.0	IV	nA/°C
$-I_{IN}$	−Input Current		25.0°C		10	30	I	µA
			T_{MIN}, T_{MAX}			46	III	µA
$d(-I_{IN})/dT$	Average −Input Current Drift	(Note 1)	All		50.0	200.0	IV	nA/°C

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 5V, R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
PSRR	Power Supply Rejection Ratio		All	45.0	50.0		II	dB
CMRR	Common-Mode Rejection Ratio		All	40.0	50.0		II	dB
I_S	Supply Current—Quiescent	No Load	All		16.0	20.0	II	mA
IS_{OFF}	Supply Current—Disabled	(Note 2)	All		4.0	7.0	II	mA
$+R_{IN}$	+ Input Resistance		25°C, T_{MAX}	100.0	200.0		II	kΩ
			T_{MIN}	50.0			III	kΩ
C_{IN}	Input Capacitance		All		0.5	2.0	IV	pF
R_{OUT}	Output Impedance (DC)		All		0.1	0.2	IV	Ω
$R_{OUT}D$	Output Resistance (DC)	Disabled	All	100.0	200.0		IV	kΩ
$C_{OUT}D$	Output Capacitance (DC)	Disabled	All		0.5	2.0	IV	pF
CMIR	Common-Mode Input Range	(Note 3)	25°C, T_{MAX}	2.0	2.1		IV	V
			T_{MIN}	1.2			IV	V
I_{OUT}	Output Current		25°C, T_{MAX}	50.0	70.0		II	mA
			T_{MIN}	35.0			III	mA
V_{OUT}	Output Voltage Swing	No Load	All	3.3	3.5		II	V
$V_{OUT}L$	Output Voltage Swing	100Ω	25°C	3.0	3.4		I	V
−ICMR	Input Current Common Mode Rejection		25°C		8.0	33.0	I	μA/V
+IPSR	+ Input Current Power Supply Rejection		25°C		1.0	3.6	I	μA/V
−IPSR	− Input Current Power Supply Rejection		25°C		20	24	I	μA/V
R_{OL}	Transimpedance		25°C	30.0	125.0		II	V/mA
			T_{MIN}		80.0		V	V/mA
			T_{MAX}		140.0		V	V/mA
I_{LOGIC}	Pin 8 Current @ 0V		All		0.8	1.2	II	mA
V_{DIS}	Maximum Pin 8 V to Disable		All			0.5	II	V
V_{EN}	Minimum Pin 8 V to Enable		All	3.5			II	V
I_{DIS}	Minimum Pin 8 I to Disable		All	350.0			II	μA
I_{EN}	Maximum Pin 8 I to Enable		All			60.0	II	μA

Closed-Loop AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = 250\Omega$, $A_V = +2$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
FREQUENCY RESPONSE								
SSBW	−3 dB Bandwidth ($V_{OUT} < 0.5\ V_{PP}$)		25°C	150.0	200.0		V	MHz
			T_{MIN}	150.0			V	MHz
			T_{MAX}	120.0			V	MHz
LSBW	−3 dB Bandwidth ($V_{OUT} < 5.0\ V_{PP}$)	$A_V = +5$	All	35.0	50.0		IV	MHz
GAIN FLATNESS								
GFPL	Peaking $V_{OUT} < 0.5\ V_{PP}$	<40 MHz	25°C		0.0	0.3	V	dB
			T_{MIN}, T_{MAX}			0.4	V	dB
GFPH	Peaking $V_{OUT} < 0.5\ V_{PP}$	>40 MHz	25°C		0.0	0.5	V	dB
			T_{MIN}, T_{MAX}			0.7	V	dB
GFR	Rolloff $V_{OUT} < 0.5\ V_{PP}$	<75 MHz	25°C		0.6	1.0	V	dB
			T_{MIN}			1.0	V	dB
			T_{MAX}			1.3	V	dB
LPD	Linear Phase Deviation $V_{OUT} < 0.5\ V_{PP}$	<75 MHz	25°C, T_{MIN}		0.2	1.0	IV	°
			T_{MAX}			1.2	IV	°
TIME-DOMAIN RESPONSE								
t_{r1}, t_{f1}	Rise Time, Fall Time	0.5V Step	All		1.6	2.4	IV	ns
t_{r2}, t_{f2}	Rise Time, Fall Time	5.0V Step	All		6.5	10.0	IV	ns
t_{s1}	Settling Time to 0.1%	2.0V Step	All		10.0	13.0	IV	ns
t_{s2}	Settling Time to 0.05%	2.0V Step	All		12.0	15.0	IV	ns
OS	Overshoot	0.5V Step	25°C, T_{MAX}		0.0	10.0	IV	%
			T_{MIN}			15.0	IV	%
SR	Slew Rate	$A_V = +2$	All	430.0	700.0		IV	V/µs
		$A_V = -2$	All		1600.0		V	V/µs
DISTORTION								
HD2	2nd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−60.0	−45.0	V	dBc
			T_{MIN}			−40.0	V	dBc
			T_{MAX}			−45.0	V	dBc
HD3	3rd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−60.0	−50.0	V	dBc
			T_{MIN}, T_{MAX}			−50.0	V	dBc

Closed-Loop AC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_F = 250\Omega$, $A_V = +2$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
EQUIVALENT INPUT NOISE								
NF	Noise Floor >100 kHz	(Note 4)	25°C		−157.0	−154.0	IV	dBm (1 Hz)
			T_{MIN}			−154.0	IV	dBm (1Hz)
			T_{MAX}			−153.0IV	IV	dBm (1Hz)
INV	Integrated Noise 100 kHz to 200 MHz	(Note 4)	25°C		40.0	57.0	IV	μV
			T_{MIN}			57.0	IV	μV
			T_{MAX}			63.0	IV	μV
DISABLE/ENABLE PERFORMANCE								
T_{OFF}	Disable Time to >50 dB	10 MHz	All		1000.0	IV	V	ns
T_{ON}	Enable Time		All		200.0		V	ns
OFFIso	Off Isolation	10 MHz	All	55.0	59.0		IV	dB
VIDEO PERFORMANCE								
d_G	Differential Gain (Note 5)	NTSC/PAL	25°C		0.02	0.08	V	% pp
d_P	Differential Phase (Note 5)	NTSC/PAL	25°C		0.01	0.08	V	° pp
d_G	Differential Gain (Note 5)	30 MHz	25°C		0.05	0.18	IV	% pp
d_P	Differential Phase (Note 5)	30 MHz	25°C		0.05	0.18	IV	° pp
VBW	−0.1 dB Bandwidth (Note 5)		25°C	30.0	60.0		V	MHz

Note 1: Measured from T_{MIN} to T_{MAX}.

Note 2: Supply current when disabled is measured at the negative supply.

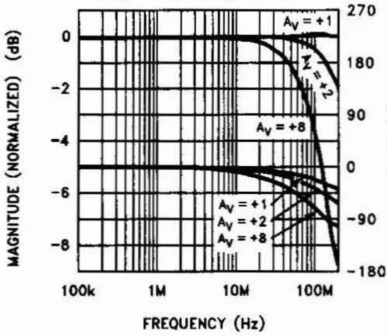
Note 3: Common-mode input range for rated performance.

Note 4: Noise Tests are performed from 5 MHz to 200 MHz.

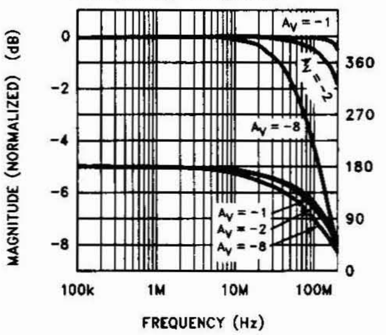
Note 5: Differential gain/phase tests are with $R_L = 100\Omega$. For other values of R_L, see curves.

Typical Performance Curves

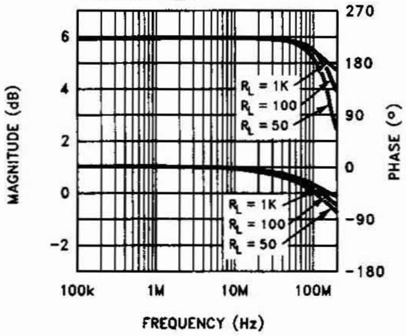
Non-Inverting Frequency Response



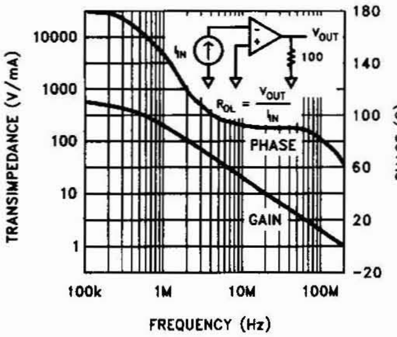
Inverting Frequency Response



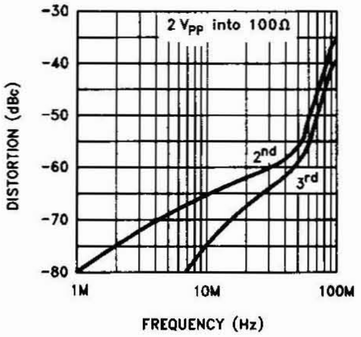
Frequency Response for Various R_Ls



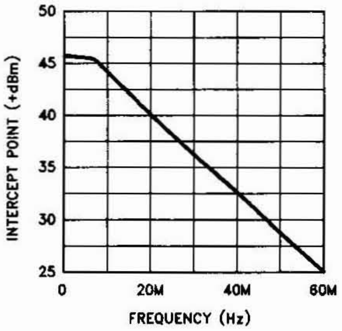
Open-Loop Transimpedance Gain and Phase



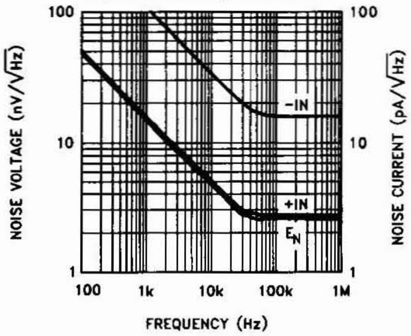
2nd and 3rd Harmonic Distortion



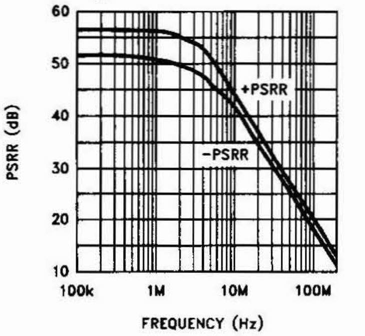
2-Tone 3rd Order Intermodulation Intercept



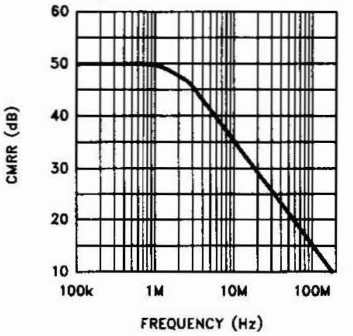
Equivalent Input Noise



Power-Supply Rejection Ratio

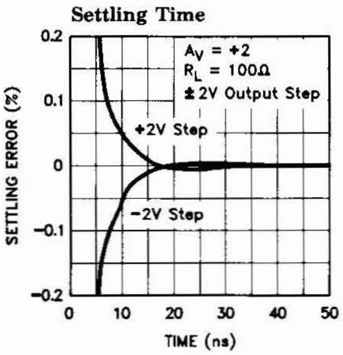


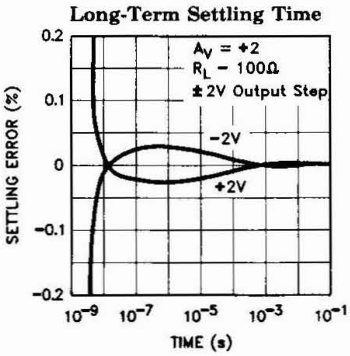
Common-Mode Rejection Ratio

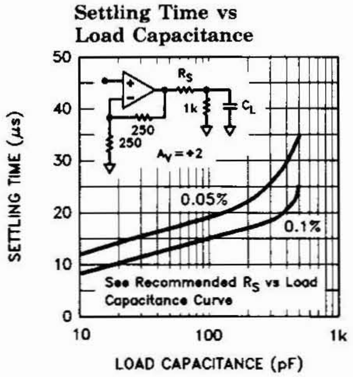


2070-2

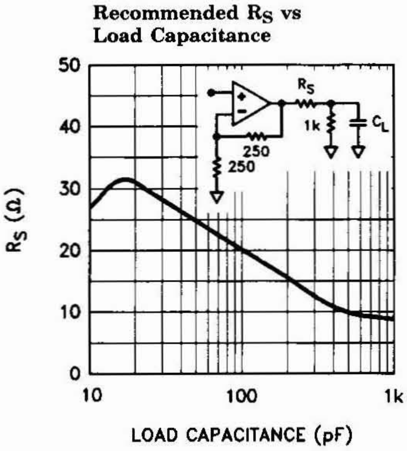
Typical Performance Curves — Contd.


Settling Time

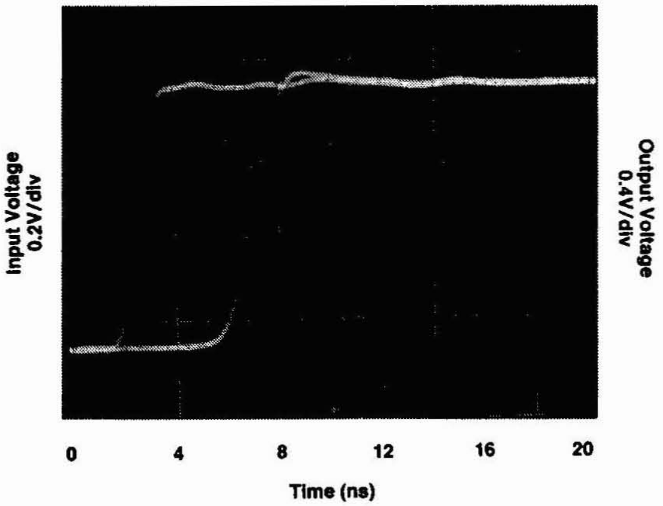

Long-Term Settling Time


Settling Time vs Load Capacitance

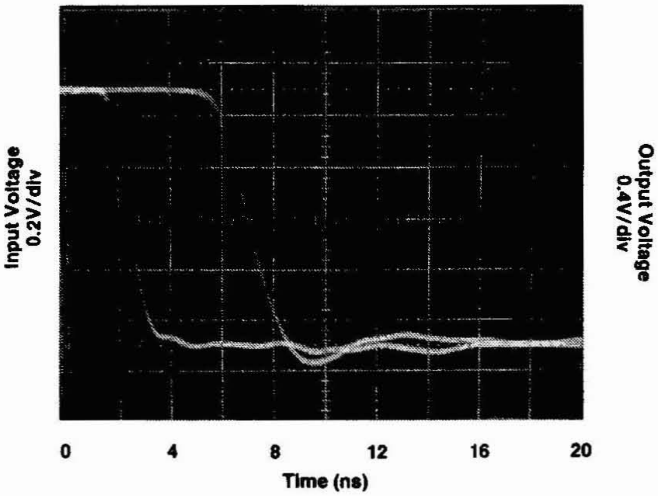
2070-3


Recommended RS vs Load Capacitance

2070-4


Pulse Response AV = +2

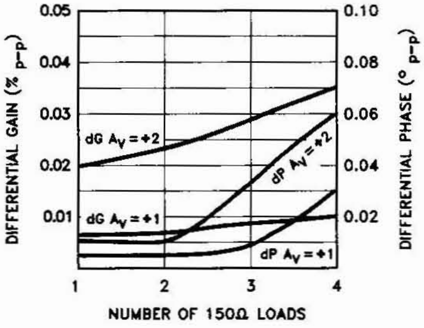
2070-5


Pulse Response AV = +2

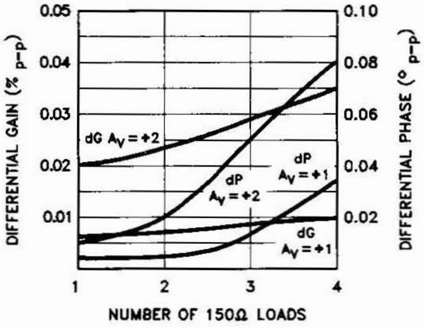
2070-6

Typical Performance Curves — Contd.

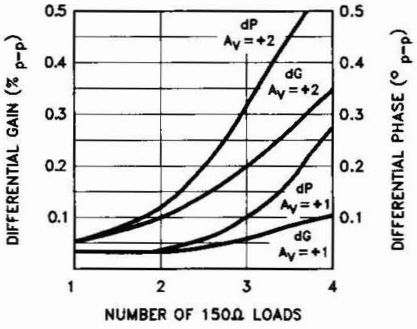
Differential Gain and Phase (3.58 MHz)



Differential Gain and Phase (4.43 MHz)

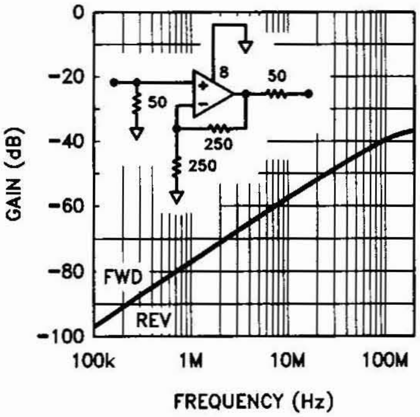


Differential Gain and Phase (30 MHz)



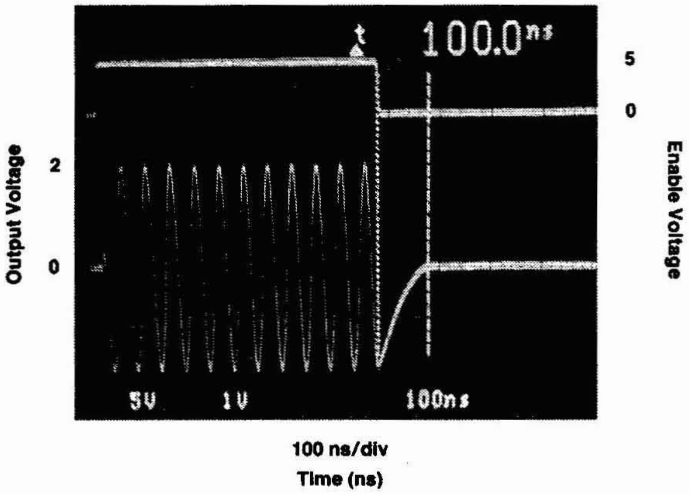
2070-7

Forward and Reverse Gain during Disable



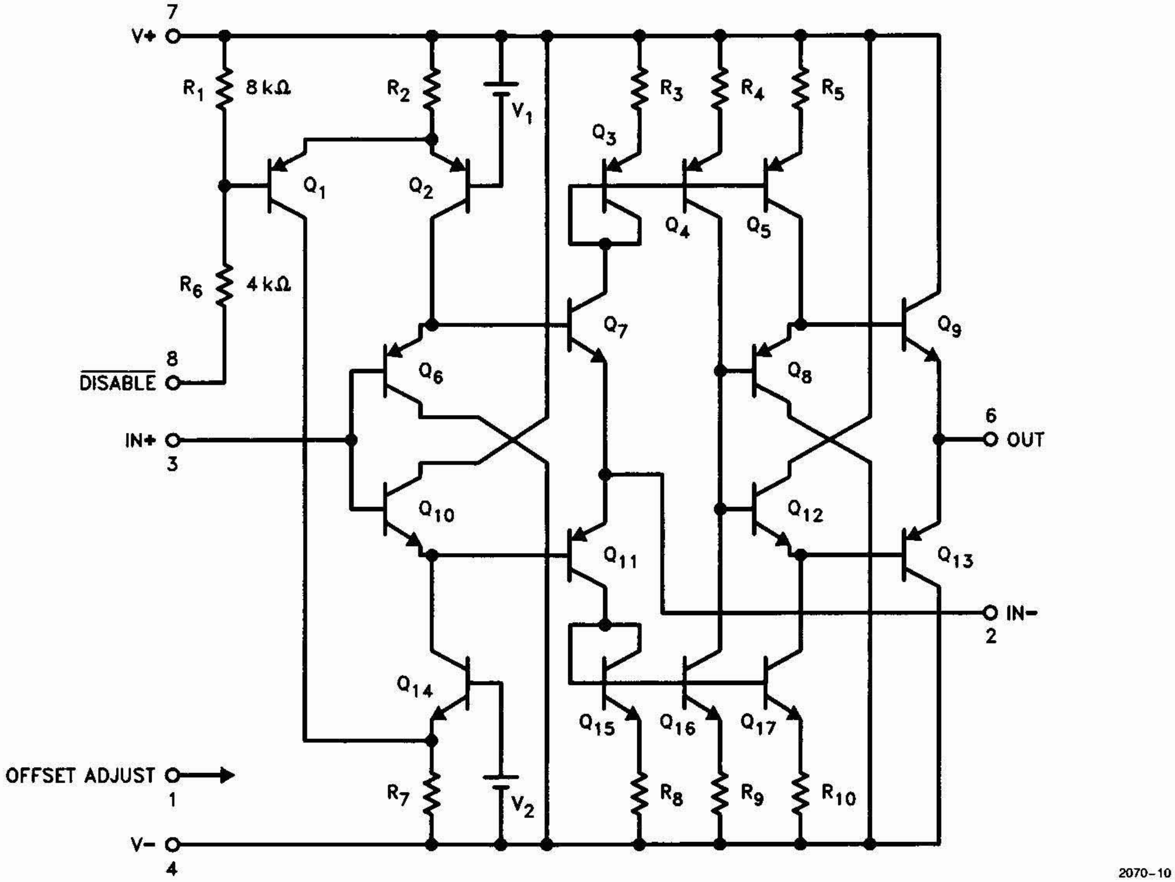
2070-8

Enable/Disable Response

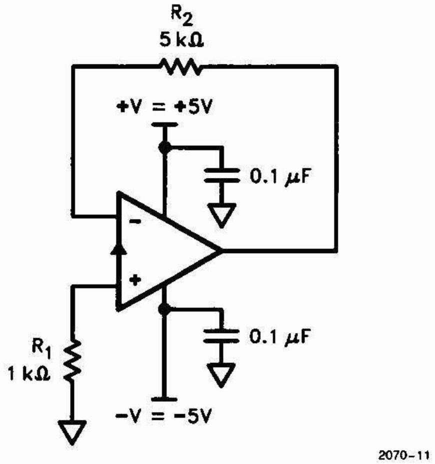


2070-9

Equivalent Circuit


7
V+
R1
8 kΩ
R2
V1
R3
R4
R5
Q1
Q2
Q3
Q4
Q5
R6
4 kΩ
Q7
Q9
8
DISABLE
Q6
Q8
IN+
3
6
OUT
Q10
Q12
Q11
Q13
IN−
2
Q14
Q15
Q16
Q17
OFFSET ADJUST
1
R7
V2
R8
R9
R10
V−
4
2070-10

Burn-In Circuit


R2
5 kΩ
+V = +5V
0.1 μF
−
+
0.1 μF
R1
1 kΩ
−V = −5V
2070-11

ALL PACKAGES USE THE SAME SCHEMATIC.

Applications Information

Theory of Operation

The EL2070 has a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL2070 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transimpedance (R_{OL}) of the EL2070 [$V_{OUT} = (R_{OL}) * (-I_{IN})$]. Since R_{OL} is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:

1. The voltage across the inputs is approximately 0V.
2. The current into the inputs is approximately 0 mA.

Resistor Value Selection and Optimization

The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2070. The nominal value for the feedback resistor is 250Ω, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Differential Gain/Phase

An industry-standard method of measuring the distortion of a video component is to measure the amount of differential gain and phase error it introduces. To measure these, a 40 IRE_{PP} reference signal is applied to the device with 0V DC offset (0 IRE) at 3.58 MHz for NTSC, 4.43 MHz for PAL, and 30 MHz for HDTV. A second measurement is then made with a 0.714V DC offset (100 IRE). Differential Gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential Phase is a measure of the change in phase, and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak values.

In general, a back terminated cable (75Ω in series at the drive end and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double-termination is used, the received signal is reduced by half; therefore a gain of 2 configuration is typically used to compensate for the attenuation. In a gain of 2 configuration, with output swing of 2 V_{PP}, with each back-terminated load at 150Ω. The EL2070 is capable of driving up to 4 back-terminated loads with excellent video performance. Please refer to the typical curves for more information on video performance with respect to frequency, gain, and loading.

Capacitive Feedback

The EL2070 relies on its feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.

Applications Information — Contd.

Offset Adjustment Pin

Output offset voltage of the EL2070 can be nulled by tying a 10k potentiometer between $+V_S$ and $-V_S$ with the slider attached to pin 1. A full-range variation of the voltage at pin 1 to ±5V results in an offset voltage adjustment of at least ±10 mV. For best settling performance pin 1 should be bypassed to ground with a ceramic capacitor located near to the package, even if the offset voltage adjustment feature is not being used.

Printed Circuit Layout

As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply and Offset Adjust bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling to the ground plane as possible.

Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL2070 allows a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

Disable/Enable Operation

The EL2070 has a disable/enable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or tied to pin 7. When more than 350 μA is pulled from pin 8, the EL2070 is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is reduced by ⅔. To make it easy to use this feature, there is an internal resistor to limit the current to a safe level (0.8 mA) if pin 8 is grounded.

To draw current out of pin 8 an open-collector TTL output, a 5V CMOS output, or an NPN transistor can be used.

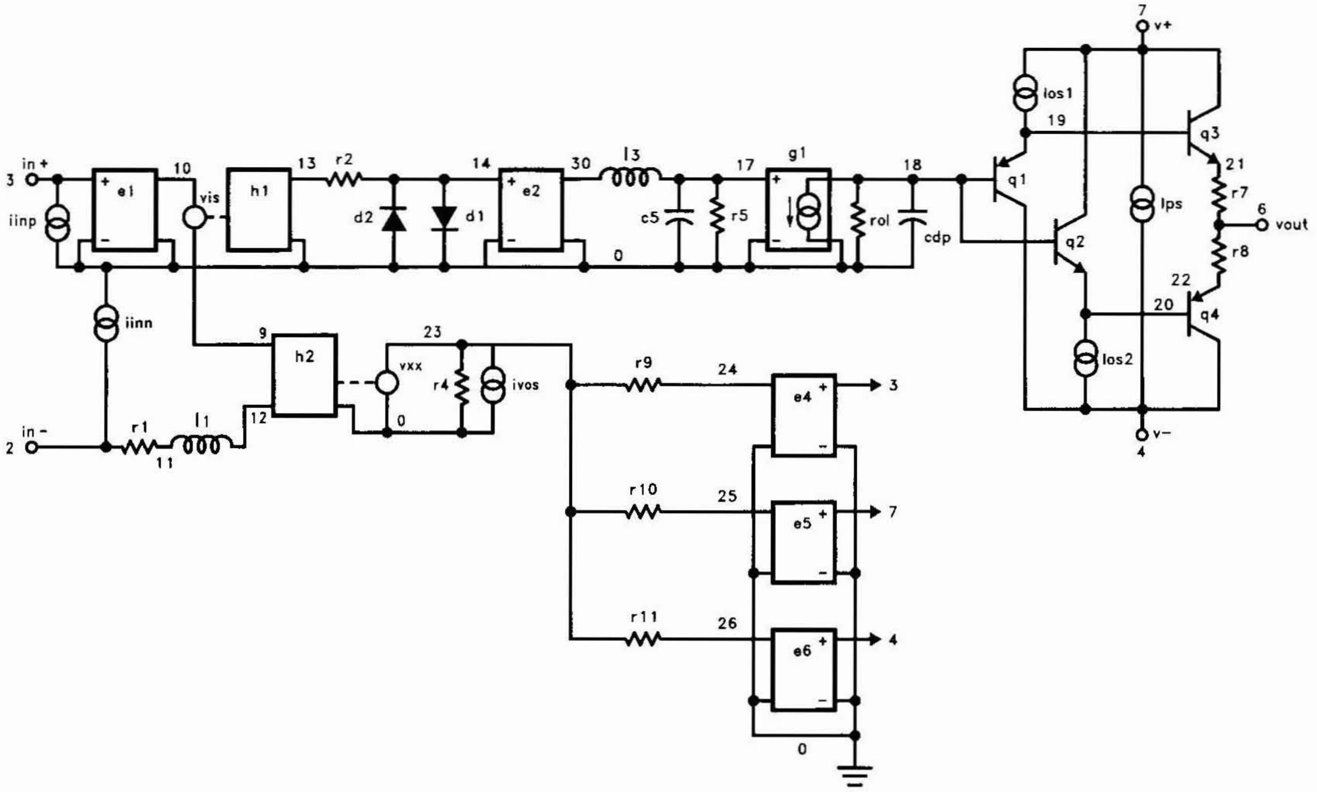
EL2070 Macromodel

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                    |      -input
*                    |        |      +Vsupply
*                    |        |        |      -Vsupply
*                    |        |        |        |      output
*                    |        |        |        |        |
.subckt M2070        3        2        7        4        6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 48nH
iinp 3 0 8µA
iinm 2 0 8µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 0.1µH
c5 17 0 0.1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 150K
cdp 18 0 2.8pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 2
r8 22 6 2
```

EL2070 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=200 tf=0.05nS)
.model qp pnp (is=5e-15 bf=200 tf=0.05nS)
.model dclamp d(is=1e-30 ibv=0.266 bv=1.3 n=4)
.ends
```

EL2070 Macromodel — Contd.


in +
3
iinp
e1
10
vis
h1
13
r2
d2
d1
14
e2
30
l3
c5
r5
17
g1
rol
18
cdp
0
iinn
9
h2
23
vxx
r4
ivos
0
12
in -
2
r1
11
l1
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4
0
7
v+
los1
19
q3
q1
21
r7
lps
6
vout
q2
r8
22
20
q4
los2
v-
4

2070-12

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL400C
200 MHz Current Feedback Amplifier

Features

- 200 MHz −3 dB bandwidth, $A_V = 2$
- 12 ns settling to 0.05%
- $V_S = \pm 5V$ @ 15 mA
- Low distortion: HD2, HD3 @ −60 dBc at 20 MHz
- Differential gain 0.02% at NTSC, PAL
- Differential phase 0.01° at NTSC, PAL
- Overload/short-circuit protected
- ±1 to ±8 closed-loop gain range
- Low cost
- Direct replacement for CLC400

Applications

- Video gain block
- Video distribution
- HDTV amplifier
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL400CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL400CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

The EL400 is a wide bandwidth, fast settling monolithic amplifier built using an advanced complementary bipolar process. This amplifier uses current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of ±1 to ±8, the EL400 has a 200 MHz −3 dB bandwidth ($A_V = +2$), and 12 ns settling to 0.05% while consuming only 15 mA of supply current.

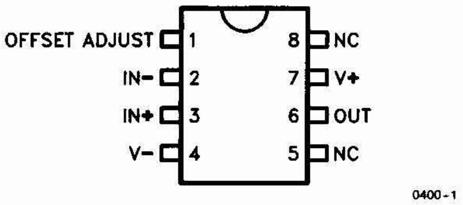
The EL400 is an obvious high-performance solution for video distribution and line-driving applications. With low 15 mA supply current, differential gain/phase of 0.02%/0.01°, and a minimum 50 mA output drive, performance in these areas is assured.

The EL400's settling to 0.05% in 12 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 200 MHz bandwidth and extremely linear phase allow unmatched signal fidelity. D/A systems can also benefit from the EL400, especially if linearity and drive levels are important.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, *QRA-1: Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



Top View

Manufactured under U.S. Patent No. 4,893,091

EL400C

200 MHz Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	5V
Power Dissipation	See Curves
Operating Temperature	−40°C to +85°C

Lead Temperature (Soldering, 5 Seconds)	300°C
Junction Temperature	175°C
Storage Temperature	−60°C to +150°C
Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO-8

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	**Test Procedure**
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±5V, R_L = 100Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
							EL400C	
V_{OS}	Input Offset Voltage		25°C		2.0	5.5	I	mV
			T_{MIN}			8.7	III	mV
			T_{MAX}			9.5	III	mV
$d(V_{OS})/dT$	Average Offset Voltage Drift	(Note 1)	All		10.0	40.0	IV	μV/°C
$+I_{IN}$	+Input Current		25°C, T_{MAX}		10.0	25.0	II	μA
			T_{MIN}			41.0	III	μA
$d(+I_{IN})/dT$	Average +Input Current Drift	(Note 1)	All		50.0	200.0	IV	nA/°C
$-I_{IN}$	−Input Current		25°C		10.0	25.0	I	μA
			T_{MIN}			41.0	III	μA
			T_{MAX}			35.0	III	μA
$d(-I_{IN})/dT$	Average −Input Current Drift	(Note 1)	All		100.0	200.0	IV	nA/°C
PSRR	Power Supply Rejection Ratio		All	40.0	50.0		II	dB
CMRR	Common-Mode Rejection Ratio		All	40.0	50.0		II	dB
I_S	Supply Current—Quiescent	No Load	All		15.0	23.0	II	mA

Open Loop DC Electrical Characteristics

$V_S = \pm 5V$, $R_L = 100\Omega$ unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL400C	Units
$+R_{IN}$	+ Input Resistance		25°C, T_{MAX}	100.0	200.0		II	kΩ
			T_{MIN}	50.0			III	kΩ
C_{IN}	Input Capacitance		All		0.5	2.0	IV	pF
R_{OUT}	Output Impedance (DC)		All		0.1	0.2	IV	Ω
CMIR	Common-Mode Input Range	(Note 2)	25°C, T_{MAX}	2.0	2.1		IV	V
			T_{MIN}	1.2			IV	V
I_{OUT}	Output Current		25°C, T_{MAX}	50.0	70.0		II	mA
			T_{MIN}	35.0			III	mA
V_{OUT}	Output Voltage Swing	No Load	All	3.2	3.5		II	V
$V_{OUT}L$	Output Voltage Swing	100Ω	25°C	3.0	3.4		I	V
R_{OL}	Transimpedance		25°C	30.0	125.0		II	V/mA
			T_{MIN}		80.0		V	V/mA
			T_{MAX}		140.0		V	V/mA

Closed-Loop AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = 250\Omega$, $A_V = +2$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL400C	Units
FREQUENCY RESPONSE								
SSBW	−3 dB Bandwidth ($V_{OUT} < 0.5\ V_{PP}$)		25°C	150.0	200.0		V	MHz
			T_{MIN}	150.0			V	MHz
			T_{MAX}	120.0			V	MHz
LSBW	−3 dB Bandwidth ($V_{OUT} < 5.0\ V_{PP}$)	$A_V = +5$	All	35.0	50.0		IV	MHz
GAIN FLATNESS								
GFPL	Peaking $V_{OUT} < 0.5\ V_{PP}$	<40 MHz	25°C		0.0	0.3	V	dB
			T_{MIN}, T_{MAX}			0.4	V	dB
GFPH	Peaking $V_{OUT} < 0.5\ V_{PP}$	>40 MHz	25°C		0.0	0.5	V	dB
			T_{MIN}, T_{MAX}			0.7	V	dB
GFR	Rolloff $V_{OUT} < 0.5\ V_{PP}$	<75 MHz	25°C		0.6	1.0	V	dB
			T_{MIN}			1.0	V	dB
			T_{MAX}			1.3	V	dB
LPD	Linear Phase Deviation $V_{OUT} < 0.5\ V_{PP}$	<75 MHz	25°C, T_{MIN}		0.2	1.0	IV	°
			T_{MAX}			1.2	IV	°

Closed-Loop AC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_F = 250\Omega$, $A_V = +2$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL400C	Units
TIME-DOMAIN RESPONSE								
t_{r1}, t_{f1}	Rise Time, Fall Time	0.5V Step	25°C, T_{MIN}		1.6	2.4	IV	ns
			T_{MAX}			2.9	IV	ns
t_{r2}, t_{f2}	Rise Time, Fall Time	5.0V Step	All		6.5	10.0	IV	ns
t_{s1}	Settling Time to 0.1%	2.0V Step	All		10.0	13.0	IV	ns
t_{s2}	Settling Time to 0.05%	2.0V Step	All		12.0	15.0	IV	ns
OS	Overshoot	0.5V Step	25°C		0.0	10.0	IV	%
			T_{MIN}, T_{MAX}			15.0	IV	%
SR	Slew Rate	$A_V = +2$	All	430.0	700.0		IV	V/µs
		$A_V = -2$	All		1600.0		V	V/µs
DISTORTION								
HD2	2nd Harmonic Distortion at 20 MHz	$2\ V_{PP}$	25°C		−60.0	−45.0	V	dBc
			T_{MIN}			−40.0	V	dBc
			T_{MAX}			−45.0	V	dBc
HD3	3rd Harmonic Distortion at 20 MHz	$2\ V_{PP}$	25°C		−60.0	−50.0	V	dBc
			T_{MIN}, T_{MAX}			−50.0	V	dBc
EQUIVALENT INPUT NOISE								
NF	Noise Floor >100 kHz	(Note 3)	25°C		−157.0	−154.0	IV	dBm (1 Hz)
			T_{MIN}			−154.0	IV	dBm (1Hz)
			T_{MAX}			−153.0	IV	dBm (1Hz)
INV	Integrated Noise 100 kHz to 200 MHz	(Note 3)	25°C		40.0	57.0	IV	µV
			T_{MIN}			57.0	IV	µV
			T_{MAX}			63.0	IV	µV
VIDEO PERFORMANCE								
d_G	Differential Gain (Note 4)	NTSC/PAL	25°C		0.02		V	% pp
d_P	Differential Phase (Note 4)	NTSC/PAL	25°C		0.01		V	° pp
d_G	Differential Gain (Note 4)	30 MHz	25°C		0.05		V	% pp
d_P	Differential Phase (Note 4)	30 MHz	25°C		0.05		V	° pp
VBW	−0.1 dB Bandwidth (Note 4)		25°C		60.0		V	MHz

Note 1: Measured from T_{MIN} to T_{MAX}.

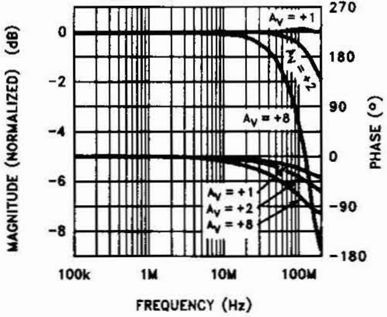
Note 2: Common-Mode Input Range for Rated Performance.

Note 3: Noise Tests are Performed from 5 MHz to 200 MHz.

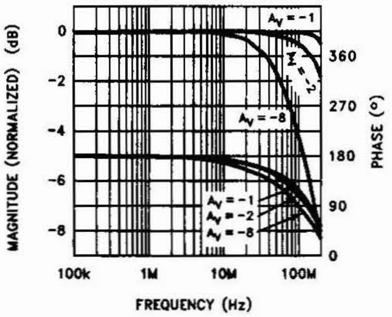
Note 4: Differential Gain/Phase Tests are $R_L = 100\Omega$. For other values of R_L, see curves.

Typical Performance Curves

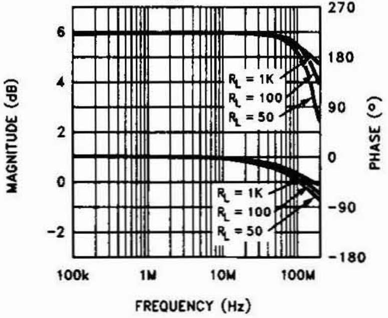
Non-Inverting Frequency Response



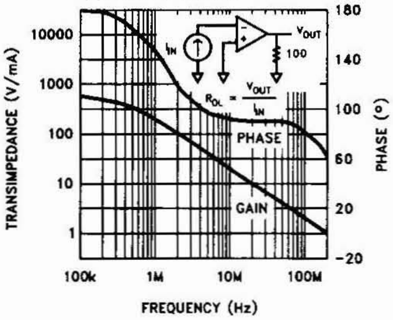
Inverting Frequency Response



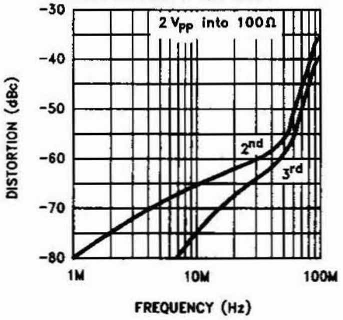
Frequency Response for Various R_Ls



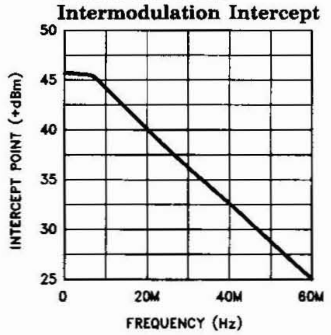
Open-Loop Transimpedance Gain and Phase



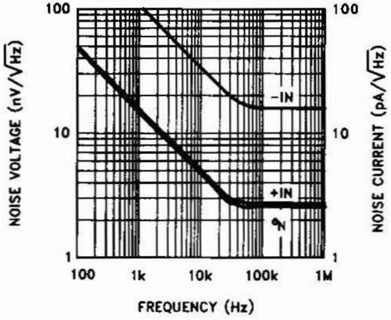
2nd and 3rd Harmonic Distortion



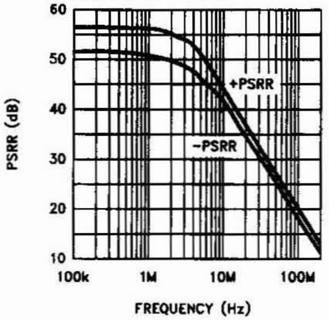
2-Tone 3rd Order Intermodulation Intercept



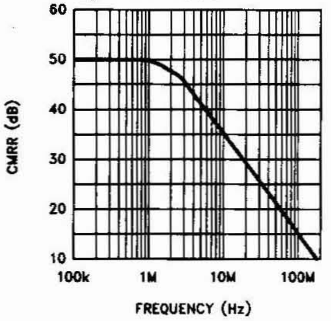
Equivalent Input Noise



Power-Supply Rejection Ratio

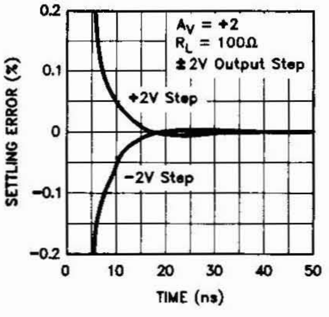


Common-Mode Rejection Ratio

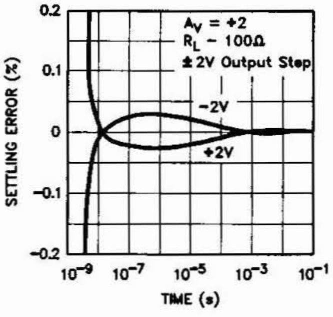


0400-2

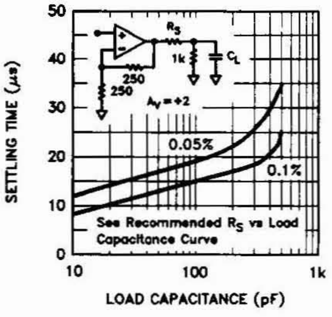
Settling Time



Long-Term Settling Time



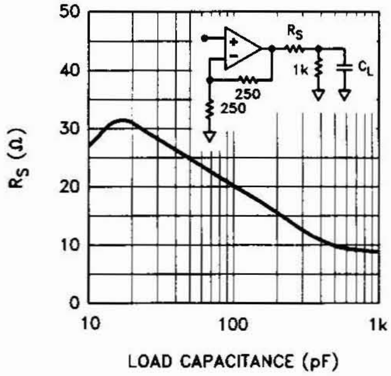
Settling Time vs Load Capacitance



0400-3

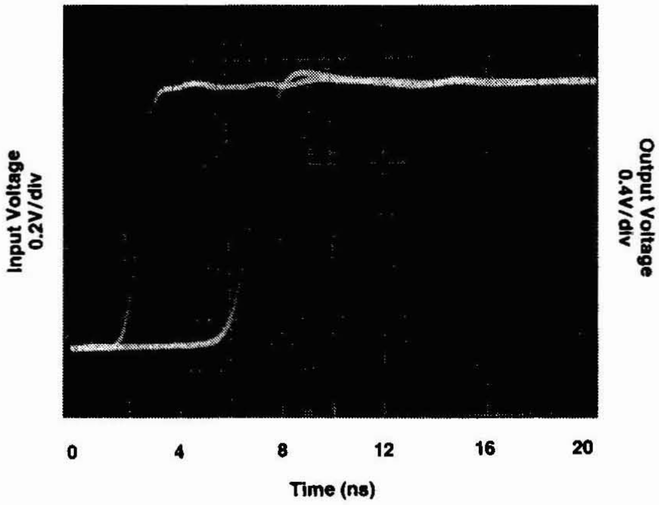
Typical Performance Curves — Contd.

Recommended R_S vs Load Capacitance



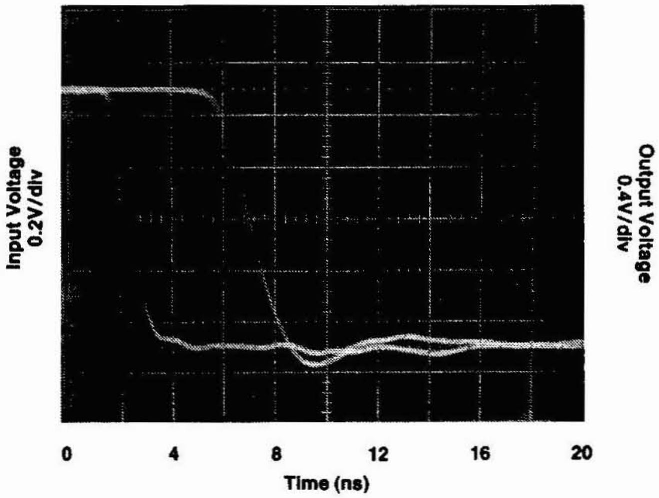
0400-4

Pulse Response A_V = +2



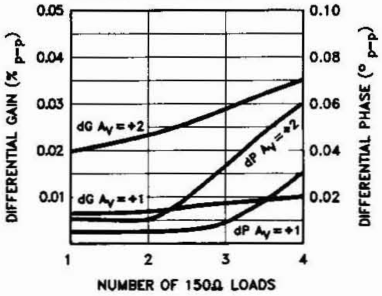
0400-5

Pulse Response A_V = +2

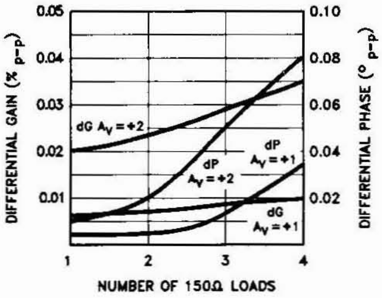


0400-6

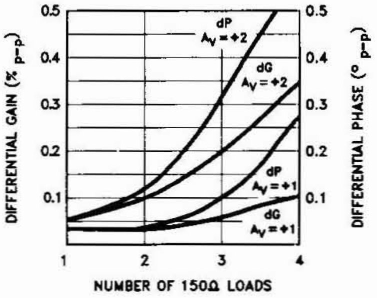
Differential Gain and Phase (3.58 MHz)



Differential Gain and Phase (4.43 MHz)

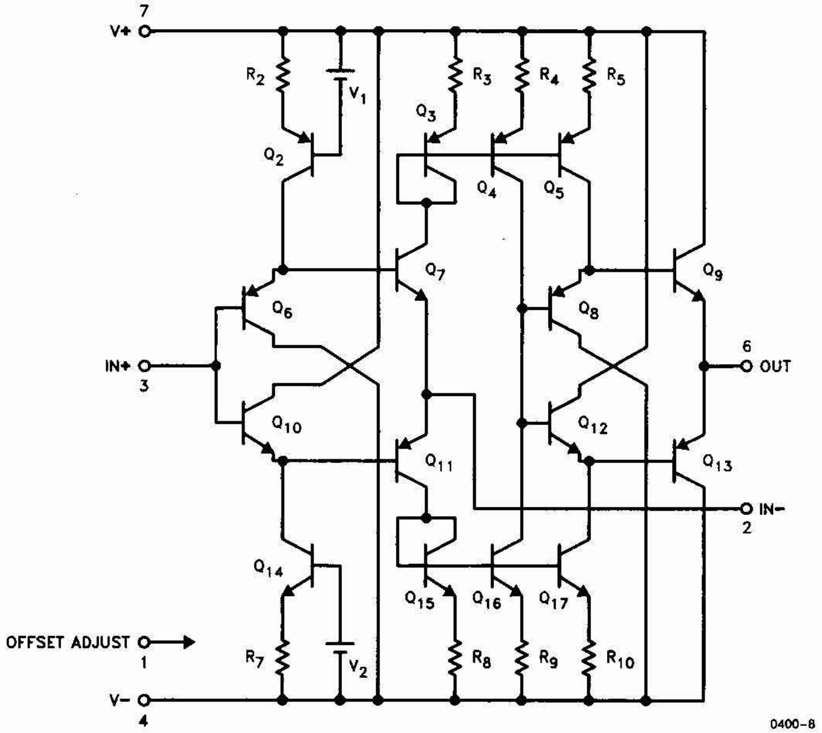


Differential Gain and Phase (30 MHz)

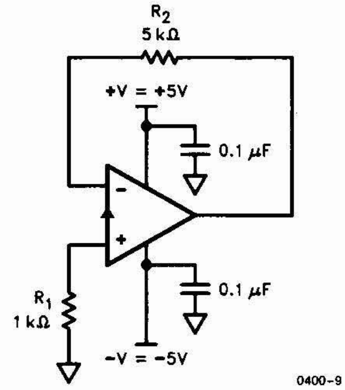


0400-7

Equivalent Circuit



Burn-In Circuit



ALL PACKAGES USE THE SAME SCHEMATIC.

Applications Information

Theory of Operation

The EL400 has a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL400 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transimpedance (R_{OL}) of the EL400 [$V_{OUT} = (R_{OL}) * (-I_{IN})$]. Since R_{OL} is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:

1. The voltage across the inputs is approximately 0V.
2. The current into the inputs is approximately 0 mA.

Resistor Value Selection and Optimization

The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL400. The nominal value for the feedback resistor is 250Ω, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Differential Gain/Phase

An industry-standard method of measuring the distortion of a video component is to measure the amount of differential gain and phase error it introduces. To measure these, a 40 IRE_{PP} reference signal is applied to the device with 0V DC offset (0IRE) at 3.58 MHz for NTSC, 4.43 MHz for

Applications Information — Contd.

PAL, and 30 MHz for HDTV. A second measurement is then made with a 0.714V DC offset (100IRE). Differential Gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential Phase is a measure of the change in phase, and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak values.

In general, a back terminated cable (75Ω in series at the drive end and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double-termination is used, the received signal is reduced by half; therefore a gain of 2 configuration is typically used to compensate for the attenuation. In a gain of 2 configuration, with output swing of 2 V_{PP}, with each back-terminated load at 150Ω. The EL400 is capable of driving up to 4 back-terminated loads with excellent video performance. Please refer to the typical curves for more information on video performance with respect to frequency, gain, and loading.

Capacitive Feedback

The EL400 relies on its feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.

Offset Adjustment Pin

Output offset voltage of the EL400 can be nulled by tying a 10k potentiometer between $+V_S$ and $-V_S$ with the slider attached to pin 1. A full-range variation of the voltage at pin 1 to ±5V results in an offset voltage adjustment of at least ±10 mV. For best settling performance pin 1 should be bypassed to ground with a ceramic capacitor located near to the package, even if the offset voltage adjustment feature is not being used.

Printed Circuit Layout

As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply and Offset Adjust bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling the ground plane as possible.

Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL400 allows a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

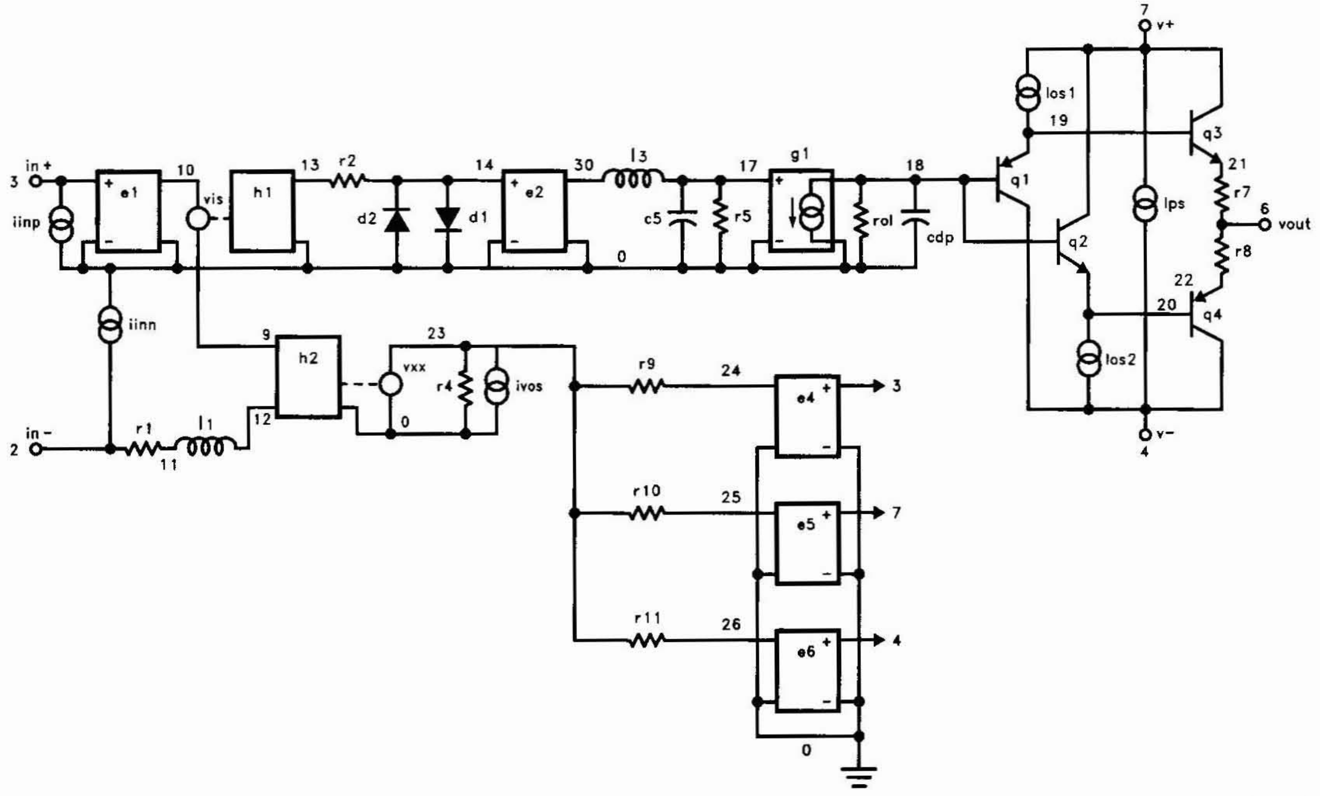
EL400 Macromodel

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:    +input
*                 |      -input
*                 |      |      +Vsupply
*                 |      |      |      -Vsupply
*                 |      |      |      |      output
*                 |      |      |      |      |
.subckt M400      3      2      7      4      6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 48nH
iinp 3 0 8µA
iinm 2 0 8µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.1µH
c5 17 0 0.1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 150K
cdp 18 0 2.8pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 2
r8 22 6 2
```

EL400 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=200 tf=0.5nS)
.model qp pnp (is=5e-15 bf=200 tf=0.5nS)
.model dclamp d(is=1e-30 ibv=0.266 bv=1.3 n=4)
.ends
```

EL400 Macromodel — Contd.


7
v+
los1
19
q3
21
r7
6
vout
r8
22
20
q4
lps
q1
q2
los2
v-
4
in+
3
iinp
e1
10
vis
h1
13
r2
d2
d1
14
e2
30
l3
17
g1
18
c5
r5
rol
cdp
0
iinn
9
h2
23
vxx
r4
ivos
0
in-
2
r1
11
l1
12
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4
0

0400-10

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2071C/EL2171C
150 MHz Current Feedback Amplifier

Features

- 150 MHz − 3 dB bandwidth, $A_V = 20$
- 10 ns settling to 0.1%
- $V_S = \pm 5V$ @ 15 mA
- 2.5 ns rise/fall times (2V step)
- Overload/short-circuit protected
- ±7 to ±50 closed-loop gain range
- Low cost
- EL2171 is direct replacement for CLC401
- Disable capability on EL2071

Applications

- Line drivers
- DC-coupled log amplifiers
- High-speed modems, radios
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications
- Analog multiplexing (using disable—EL2071)
- Power down mode (using disable—EL2071)

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2171CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2171CS	−40°C to +85°C	8-Lead SO	MDP0027
EL2071CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2071CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

The EL2071 and EL2171 are wide bandwidth, fast settling monolithic amplifiers built using an advanced complementary bipolar process. The EL2071 has a disable/enable feature which allows power down and analog multiplexing. These amplifiers use current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of ±7 to ±50, the EL2071 and EL2171 have a 150 MHz − 3 dB bandwidth ($A_V = +20$), and 2.5 ns rise/fall time, while consuming only 15 mA of supply current. The EL2071 consumes only 1.5 mA when disabled.

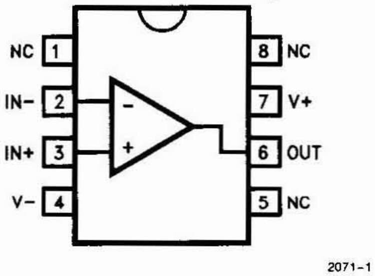
The wide 150 MHz bandwidth and extremely linear phase (0.2 dB deviation from linear at 50 MHz) allow superior signal fidelity. These features make the EL2071 and EL2171 especially suited for many digital communication system applications.

The EL2071's and EL2171's settling to 0.1% in 10 ns and ability to drive capacitive loads make them ideal in flash A/D applications. D/A systems can also benefit from the EL2071 and EL2171, especially if linearity and drive levels are important.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, *QRA-1: Elantec's Processing, Monolithic Integrated Circuits.*

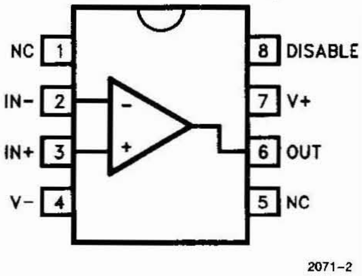
Connection Diagrams

EL2171
DIP and SO Package



Top View

EL2071
DIP and SO Package



Top View

Manufactured under U.S. Patent No. 4,893,091

EL2071C/EL2171C

150 MHz Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Common Mode Input Voltage	$\pm V_S$
Differential Input Voltage	5V

Power Dissipation	See Curves
Operating Temperature	−40°C to +85°C
Operating Junction Temperature	
Ceramic Packages	175°C
Plastic Packages	150°C
Storage Temperature	−60°C to +150°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		25°C		3	6	I	mV
			T_{MIN}, T_{MAX}			10	III	mV
TC V_{OS}	Average Offset Voltage Drift	(Note 1)	All		20	50	IV	μV/°C
$+I_{IN}$	+ Input Current		25°C, T_{MAX}		10	20	II	μA
			T_{MIN}			36	III	μA
TC ($+I_{IN}$)	Average + Input Current Drift	(Note 1)	All		100	200	IV	nA/°C
$-I_{IN}$	− Input Current		25°C		10	30	I	μA
			T_{MIN}			46	III	μA
			T_{MAX}			40	III	μA
TC ($-I_{IN}$)	Average − Input Current Drift	(Note 1)	All		100	200	IV	nA/°C

Open Loop DC Electrical Characteristics

$V_S = \pm 5V$, $R_L = 100\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
PSRR	Power Supply Rejection Ratio	(Note 2)	All	50	55		II	dB
CMRR	Common-Mode Rejection Ratio		All	40	50		II	dB
I_S	Supply Current—Quiescent	No Load	All		15	21	II	mA
$I_{S_{OFF}}$	Supply Current—Disabled	EL2071C (Note 3)	All		1.5	3.0	II	mA
$+R_{IN}$	+Input Resistance		25°C, T_{MAX}	100	200		II	kΩ
			T_{MIN}	50			III	kΩ
C_{IN}	Input Capacitance		All		0.5	2.5	IV	pF
R_{OUT}	Output Resistance (DC)		All		0.2	0.3	IV	Ω
R_{OUT_D}	Output Resistance (DC)	EL2071C Disabled	All	100	200		IV	kΩ
C_{OUT_D}	Output Capacitance (DC)	EL2071C Disabled	All		0.5	2.0	IV	pF
CMIR	Common-Mode Input Range	(Note 4)	25°C, T_{MAX}	±2.5	±2.8		IV	V
			T_{MIN}	±2			IV	V
I_{OUT}	Output Current		25°C, T_{MAX}	50	70		II	mA
			T_{MIN}	35			III	mA
V_{OUT}	Output Voltage Swing	No Load	25°C, T_{MAX}	3.2	3.5		II	V
			T_{MIN}	3			II	V
V_{OUT_L}	Output Voltage Swing	$R_L = 100\Omega$	25°C	3.2	3.4		I	V
R_{OL}	Transimpedance		25°C	250	1000		I	V/mA
I_{LOGIC}	Pin 8 Current @ +5V	EL2071C	All		500	750	II	μA
V_{DIS}	Minimum Pin 8 V to Disable	EL2071C	25°C	4.3			II	V
			T_{MIN}	4.0				
			T_{MAX}	4.6				
V_{EN}	Maximum Pin 8 V to Enable	EL2071C	All			0.7	II	V
I_{DIS}	Minimum Pin 8 I to Disable	EL2071C	All	750			II	μA
I_{EN}	Maximum Pin 8 I to Enable	EL2071C	All			35	II	μA

Closed Loop AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = 1.5\ k\Omega$, $A_V = +20$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
FREQUENCY RESPONSE								
SSBW	−3 dB Bandwidth (V_{OUT} <2.0 V_{PP})		25°C	100	150		V	MHz
			T_{MIN}	100			V	MHZ
			T_{MAX}	70			V	MHz
LSBW	−3 dB Bandwidth (V_{OUT} < 5.0 V_{PP})		25°C, T_{MIN}	65	100		IV	MHz
			T_{MAX}	55			IV	MHz
GAIN FLATNESS								
GFPL	Peaking V_{OUT} < 2.0 V_{PP}	<25 MHz	25°C		0.0	0.1	V	dB
			T_{MIN}, T_{MAX}			0.1	V	dB
GFPH	Peaking V_{OUT} < 2.0 V_{PP}	>25 MHz	25°C		0.0	0.2	V	dB
			T_{MIN}, T_{MAX}			0.2	V	dB
GFR	Rolloff V_{OUT} < 2.0 V_{PP}	<50 MHz	25°C		0.2	1.0	V	dB
			T_{MIN}			1.0	V	dB
			T_{MAX}			1.3	V	dB
LPD	Linear Phase Deviation V_{OUT} < 2.0 V_{PP}	<50 MHz	25°C, T_{MIN}		0.2	1.0	IV	°
			T_{MAX}			1.5	IV	°
TIME-DOMAIN RESPONSE								
t_{r1}, t_{f1}	Rise Time, Fall Time	2.0V Step	25°C, T_{MIN}		2.5	3.5	IV	ns
			T_{MAX}			5	IV	ns
t_{r2}, t_{f2}	Rise Time, Fall Time	5.0V Step	25°C, T_{MIN}		5	7	IV	ns
			T_{MAX}			8	IV	ns
t_s	Settling Time to 0.1%	2.0V Step	All		10	15	IV	ns
OS	Overshoot	2.0V Step	All		0	10	IV	%
SR	Slew Rate		25°C, T_{MIN}	800	1200		IV	V/µs
			T_{MAX}	700			IV	V/µs
DISTORTION								
HD2	2nd Harmonic Distortion @20 MHz	2 V_{PP}	25°C		−45	−35	V	dBc
			T_{MIN}, T_{MAX}			−35	V	dBc
HD3	3rd Harmonic Distortion @20 MHz	2 V_{PP}	25°C		−60	−50	V	dBc
			T_{MIN}			−50	V	dBc
			T_{MAX}			−45	V	dBc

Closed Loop AC Electrical Characteristics

V_S = ±5V, R_F = 1.5 kΩ, A_V = +20, R_L = 100Ω unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
EQUIVALENT INPUT NOISE								
NF	Noise Floor >100 kHz		25°C		−158	−155	IV	dBm (1 Hz)
			T_{MIN}			−155	IV	dBm (1 Hz)
			T_{MAX}			−154	IV	dBm (1 Hz)
INV	Integrated Noise 100 kHz to 200 MHz		25°C		35	50	IV	μV
			T_{MIN}			50	IV	μV
			T_{MAX}			55	IV	μV
DISABLE/ENABLE PERFORMANCE—EL2071C								
T_{OFF}	V_{OUT} = 2 V_{PP} Disable Time to >40 dB	20 MHz	All		70	200	IV	ns
T_{ON}	Enable Time		All		40	100	IV	ns
ISO	Off Isolation	20 MHz	All	50	55		IV	dB

Note 1: Measured from T_{MIN} to T_{MAX}.

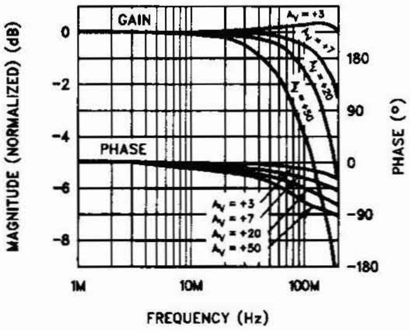
Note 2: PSRR is measured at V_S = ±4.5V and V_S = ±5.5V. Both supplies are changed simultaneously.

Note 3: Supply current when disabled is measured at the negative supply.

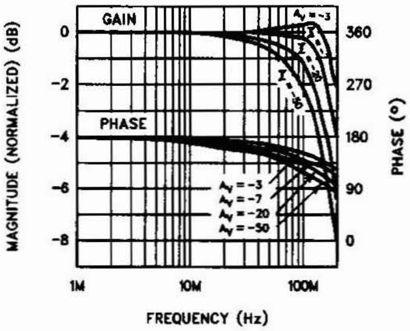
Note 4: Common-Mode Input Range for Rated Performance.

Typical Performance Curves

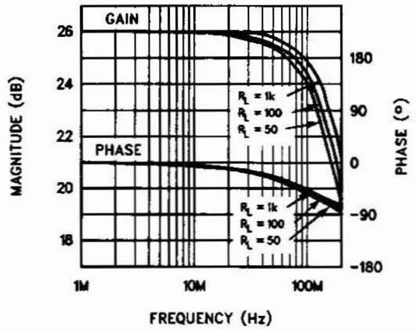
Non-Inverting Frequency Response



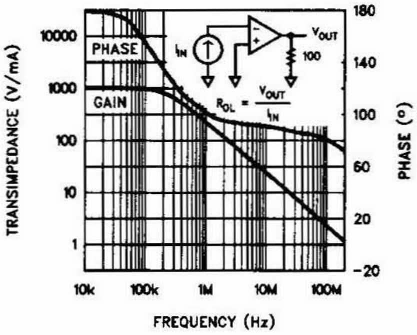
Inverting Frequency Response



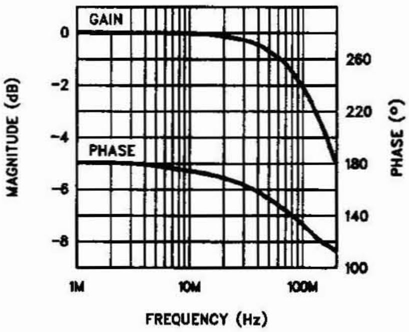
Frequency Response for Various R_Ls



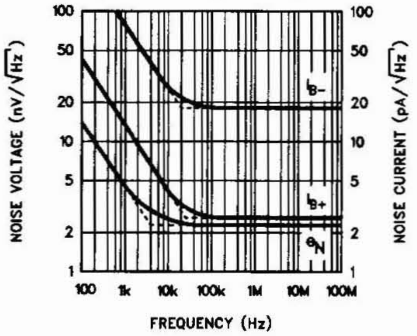
Open-Loop Transimpedance Gain and Phase



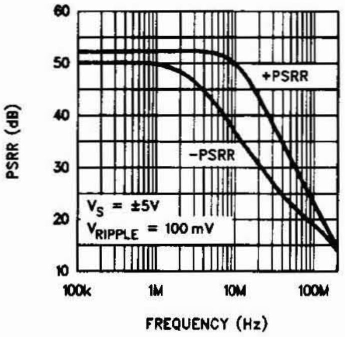
Frequency Response, $A_V = -1$, $R_F = 2.5\ k\Omega$



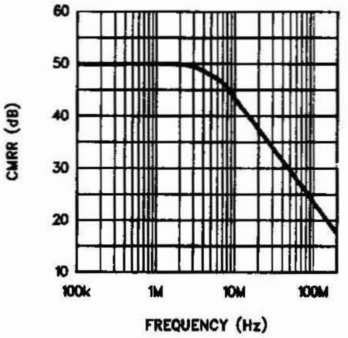
Equivalent Input Noise



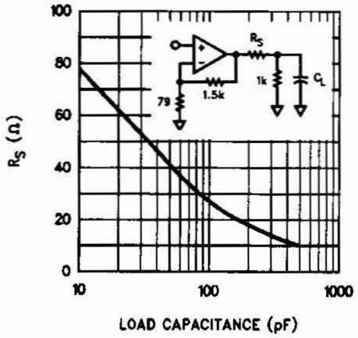
Single Power Supply Rejection Ratio



Common Mode Rejection Ratio ($A_V = +20$)



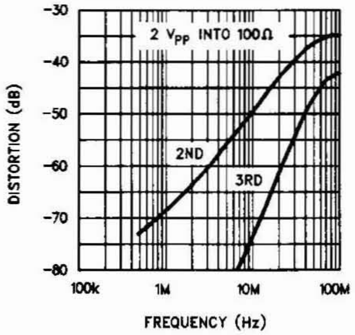
Recommended R_S vs Load Capacitance



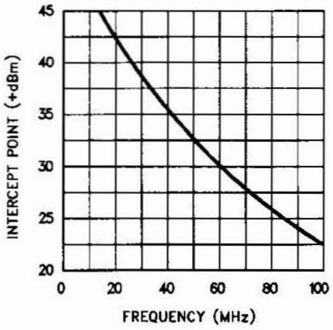
2071-3

Typical Performance Curves — Contd.

2nd and 3rd
Harmonic Distortion

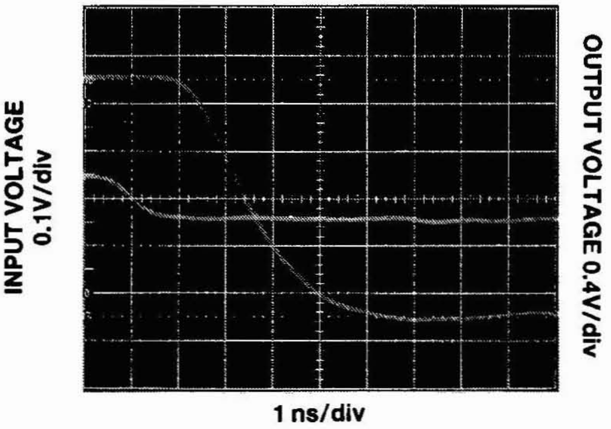


2-Tone 3rd Order
Intermodulation Intercept



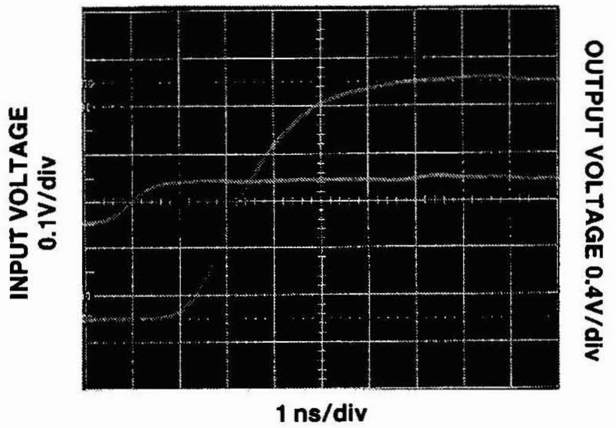
2071-4

Pulse Response $A_V = +20$



2071-5

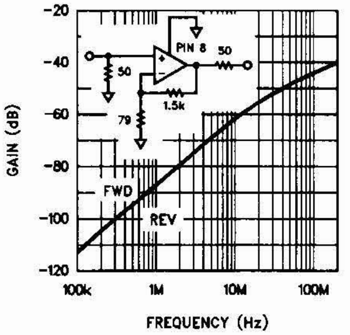
Pulse Response $A_V = +20$



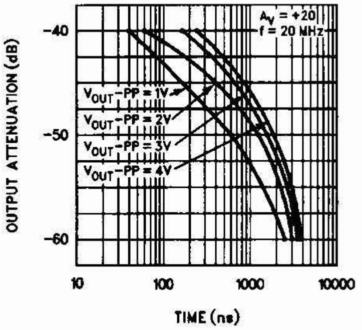
2071-6

Typical Performance Curves — Contd.

Forward and Reverse Gain during Disable—EL2071C

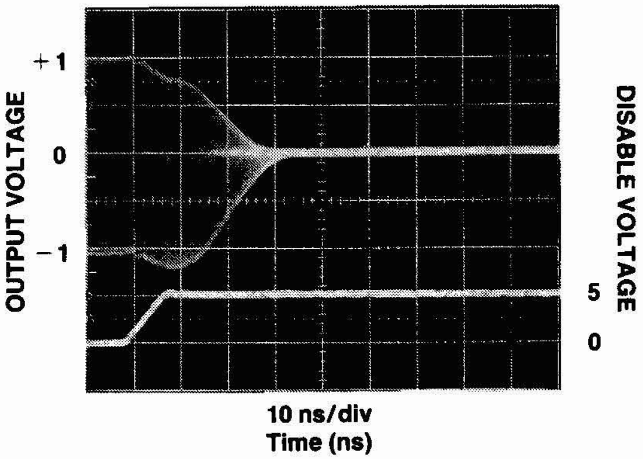


Disabled Attenuation vs Time for Various Output Levels—EL2071C



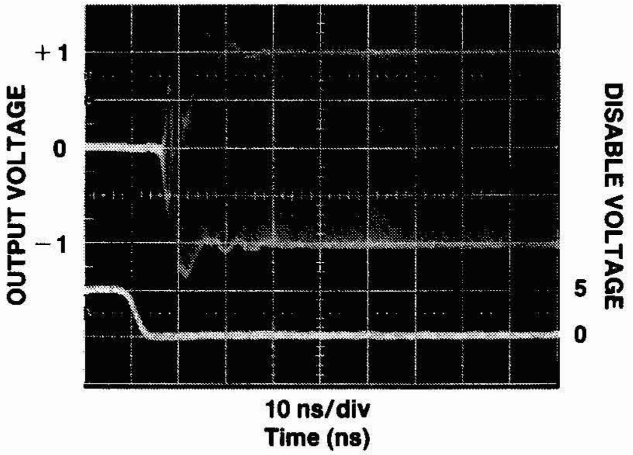
2071-7

Disable Response—EL2071C



2071-8

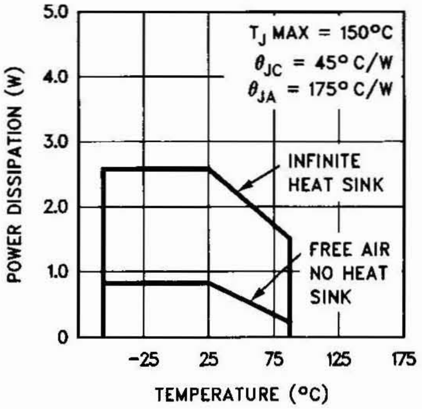
Enable Response—EL2071C



2071-9

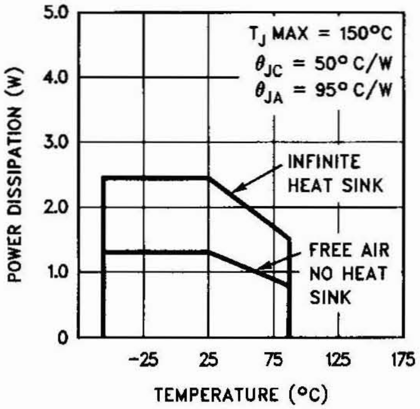
Typical Performance Curves — Contd.

8-Lead SO Maximum Power Dissipation vs Ambient Temperature



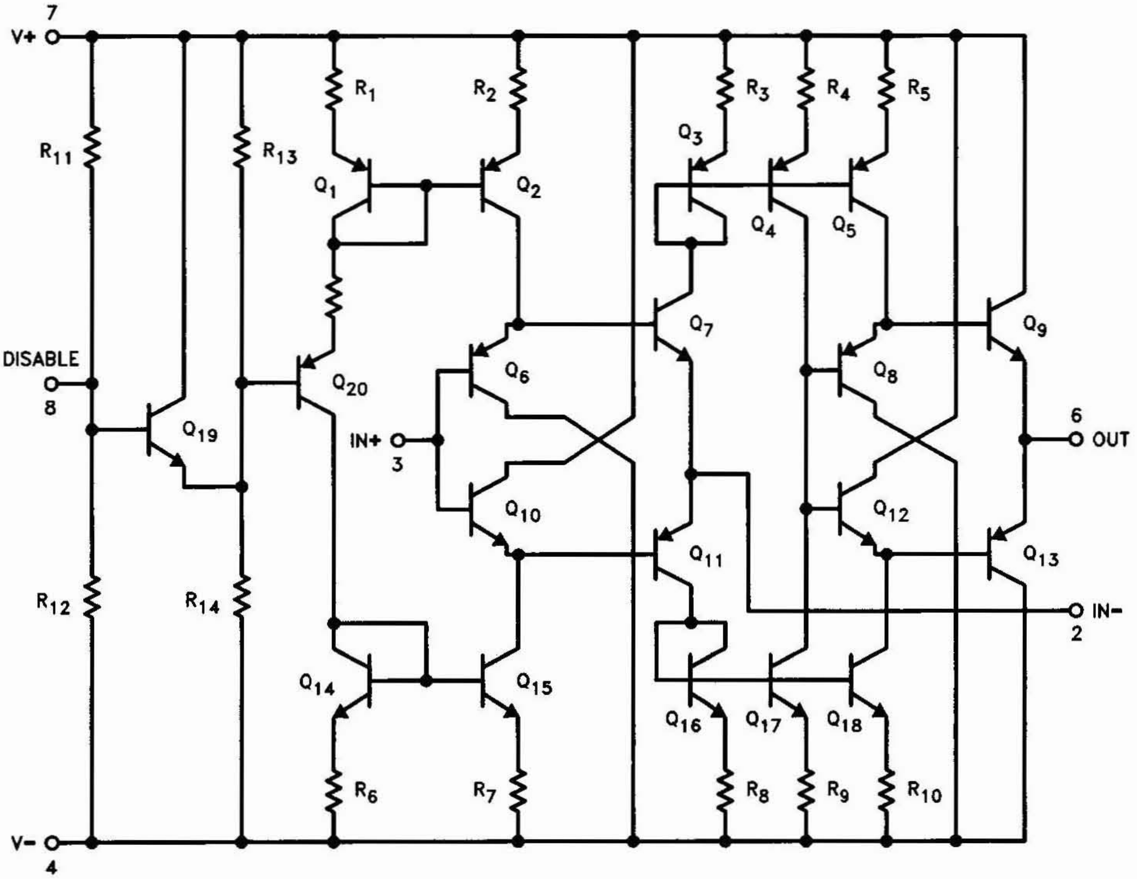
2071-10

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



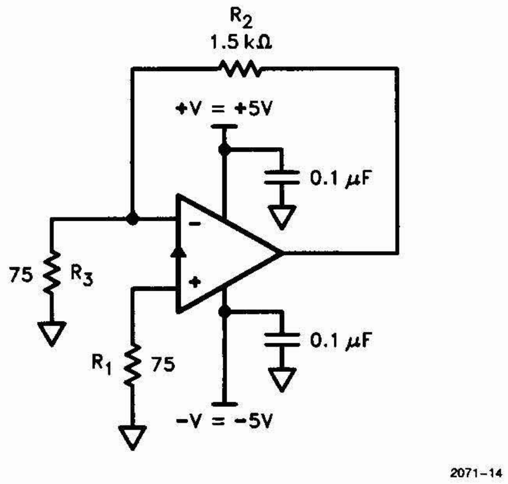
2071-11

Equivalent Circuit


7
V+
R1
R2
R3
R4
R5
R11
R13
Q1
Q2
Q3
Q4
Q5
Q7
Q9
Q6
Q8
DISABLE
8
Q19
Q20
IN+
3
Q10
Q12
6
OUT
Q11
Q13
IN-
2
R12
R14
Q14
Q15
Q16
Q17
Q18
R6
R7
R8
R9
R10
V-
4

2071-13

Burn-In Circuit



ALL PACKAGES USE THE SAME SCHEMATIC.

Applications Information

Theory of Operation

The EL2071/EL2171 have a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL2071/EL2171 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transimpedance (R_{OL}) of the EL2071/EL2171 [$V_{OUT} = (R_{OL}) * (-I_{IN})$]. Since R_{OL} is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:

1. The voltage across the inputs is approximately 0V.
2. The current into the inputs is approximately 0 mA.

Resistor Value Selection and Optimization

The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2071/EL2171. The nominal value for the feedback resistor is 1.5 kΩ, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Capacitive Feedback

The EL2071/EL2171 rely on their feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.

Applications Information — Contd.

Printed Circuit Layout

As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling to the ground plane as possible.

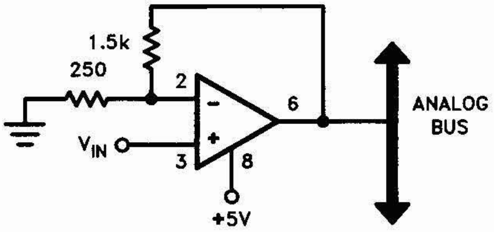
Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL2071/EL2171 allow a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

Disable/Enable Operation for EL2071C

The EL2071C has a disable/enable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or returned to ground. When the voltage at pin 8 is brought to within 0.4V of pin 7 (V_S+), the EL2071C is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is reduced to less than 2.2. mA. There are internal resistors which limit the current at pin 8 to a safe level (~ ±500 μA) if pin 8 is shorted to either supply.

Typically, analog and digital circuits should have separate power supplies. This usually leads to slight differences between the power supply voltages. The EL2071C's disable feature is dependent on the voltage at pins 8 and 7. Therefore, to operate the disable feature of the EL2071C dependably over temperature, it is recommended that the logic circuitry which drives pin 8 of the EL2071C operate from the same +5V supply as the EL2071C to avoid voltage differences between the digital and analog power supplies. Since V_{DIS} is temperature dependent, it is recommended that 5V CMOS logic (with a $V_{OH} > 4.6V$ sourcing $> 750\ \mu A$ over temperature) be used to drive the disable pin of the EL2071C.

When disabled, (as well as in enabled mode), care must be taken to prevent a differential voltage between the + and − inputs greater than 5.0V. For example, in the figure below, the EL2071C is connected in a gain of +7 configuration and is disabled while the analog bus is driven externally to +5V. Pin 2 is consequently at +0.71V, and if V_{IN} is driven to −5V, then 5.71V appears between pins 3 and 2. Internally, this voltage appears across a forward biased V_{BE} in series with a reverse biased V_{BE} and is past the threshold for zenering the reverse biased V_{BE}. In a typical application, a 50Ω or 75Ω terminating resistor from pin 3 to ground will prevent pin 3 from approaching −5V.



2071-15

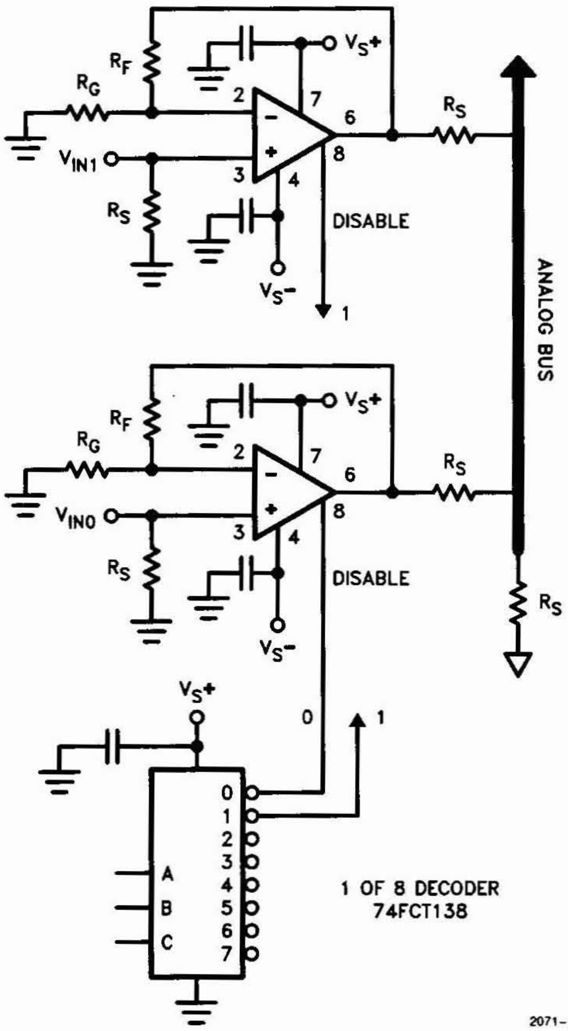
Applications Information — Contd.

Using the EL2071C as a Multiplexer

An interesting use of the enable feature is to combine several amplifiers in parallel with their outputs in common. This combination then acts similar to a MUX in front of an amplifier. A typical circuit is shown. The series resistance at each output helps to further increase isolation between amplifiers.

When the EL2071C is disabled, the DC output impedance is >100 kΩ in parallel with 2 pF capacitance.

To operate properly, the decoder that is used must have a $V_{OH} > (V_S+) - 0.4V$ with $I_{OH} = 750\ \mu A$, and should be connected to the same power supply as the EL2071C.


R_F
R_G
V_S+
2
7
6
R_S
V_IN1
3
4
8
R_S
DISABLE
V_S-
1
ANALOG BUS
R_F
R_G
V_S+
2
7
6
R_S
V_IN0
3
4
8
R_S
DISABLE
V_S-
R_S
V_S+
0
1
A
B
C
0
1
2
3
4
5
6
7
1 OF 8 DECODER
74FCT138

2071-16

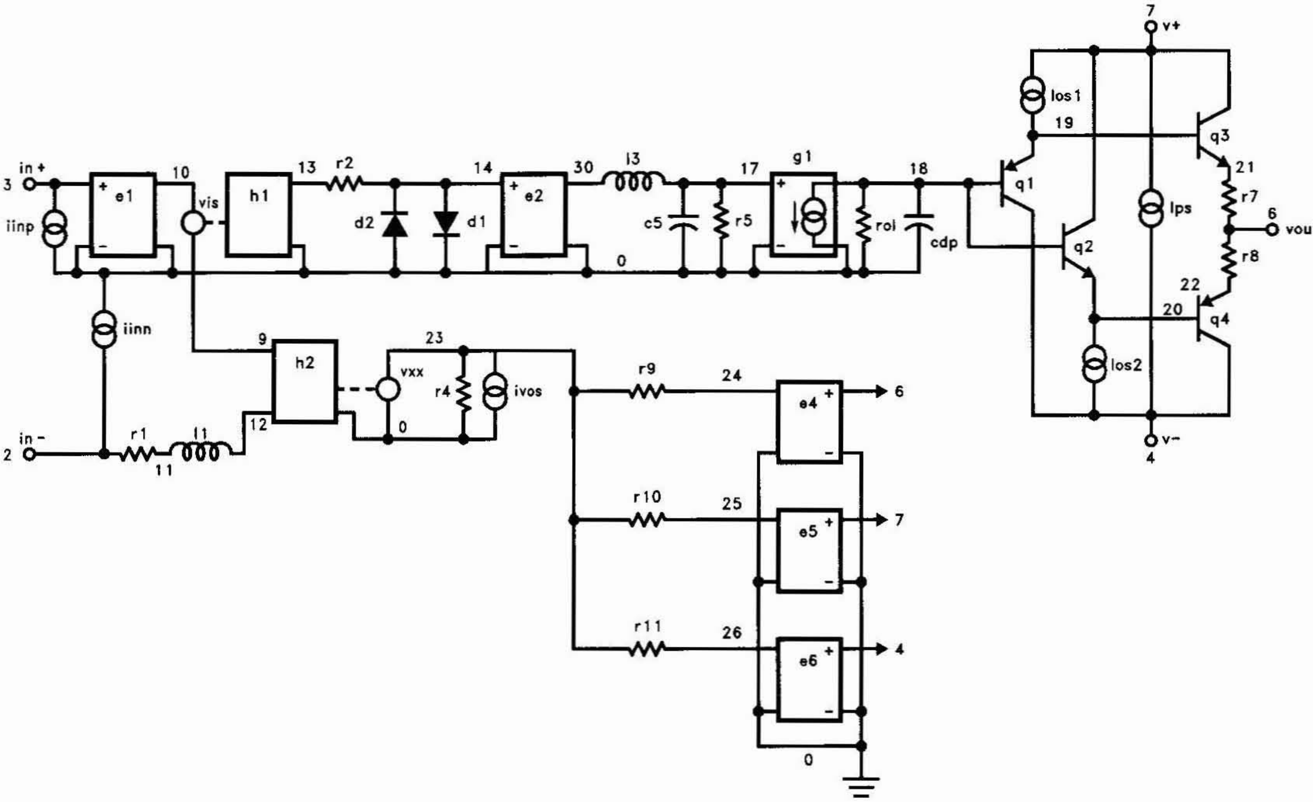
EL2071 Macromodel

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                    |     -input
*                    |       |     +Vsupply
*                    |       |       |     -Vsupply
*                    |       |       |       |     output
*                    |       |       |       |       |
.subckt M2071        3       2       7       4       6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 2
l1 11 12 1nH
iinp 3 0 10μA
iinm 2 0 10μA
*
* Slew Rate Limiting
*
*h1 13 0 vis 1K
h1 13 0 vis 600
r2 13 14 100
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
e2 30 0 14 0 0.001
13 30 17 1.0μH
c5 17 0 0.1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 1Meg
cdp 18 0 0.88pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 2
r8 22 6 2
```

EL2071 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 3mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 316
r10 25 23 562
r11 26 23 562
*
* Models
*
.model qn npn (is=5e-15 bf=500 tf=0.05nS)
.model qp pnp (is=5e-15 bf=500 tf=0.05nS)
.model dclamp d(is=1e-30 ibv=1pA bv=3.5 n=4)
.ends
```

EL2071 Macromodel


7
v+
ios1
19
q3
in+
3
e1
10
vis
h1
13
r2
14
e2
30
l3
17
g1
18
q1
21
r7
6
vout
iinp
d2
d1
c5
r5
rol
cdp
lps
q2
r8
0
22
20
q4
iinn
9
h2
23
vxx
r4
ivos
ios2
12
0
in−
2
r1
l1
11
v−
4
r9
24
e4
6
r10
25
e5
7
r11
26
e6
4
0

2071-17

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2072C

730 MHz Closed Loop Buffer

Features

- 730 MHz −3 dB bandwidth (0.5 V_{PP})
- 5 ns settling to 0.2%
- V_S = ±5V @ 15 mA
- Low distortion: HD2, HD3 of −65 dBc at 20 MHz
- Overload/short-circuit protected
- Closed-loop, unity gain
- Low cost
- Direct replacement for CLC110

Applications

- Video buffer
- Video distribution
- HDTV buffer
- High-speed A/D buffer
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2072CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2072CS	−40°C to +85°C	8-Pin SO	MDP0027

General Description

The EL2072 is a wide bandwidth, fast settling monolithic buffer built using an advanced complementary bipolar process. This buffer is closed loop to achieve lower output impedance and higher gain accuracy. Designed for closed-loop unity gain, the EL2072 has a 730 MHz −3 dB bandwidth and 5 ns settling to 0.2% while consuming only 15 mA of supply current.

The EL2072 is an obvious high-performance solution for video distribution and line-driving applications. With low 15 mA supply current and a 70 mA output drive, performance in these areas is assured.

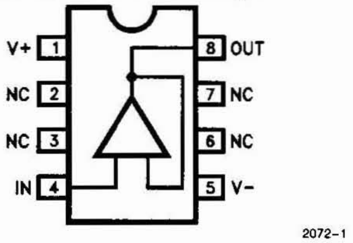
The EL2072's settling to 0.2% in 5 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 730 MHz bandwidth and extremely linear phase allow unmatched signal fidelity.

The EL2072 can be used inside an amplifier loop or PLL as its wide bandwidth and fast rise time have minimal effect on loop dynamics.

Elantec products and facilities comply with MIL-I-45028A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document *QRA-1: Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



Top View

Manufactured under U.S. Patent No. 4,893,091

EL2072C

730 MHz Closed Loop Buffer

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Input Voltage	±V_S
Operating Temperature	−40°C to +85°C
Junction Temperature	175°C
Storage Temperature	−60°C to +150°C
Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO

Note: See EL2071/EL2171 for Thermal Impedance curves.

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Output Offset Voltage		25°C		2.0	8.0	I	mV
			T_{MIN}			16.0	V	mV
			T_{MAX}			13.0	V	mV
TCV_{OS}	Average Offset Voltage Drift		25°C − T_{MAX}		20.0	50.0	IV	µV/°C
			25°C − T_{MIN}		20.0	100.0		
I_B	Input Bias Current		25°C, T_{MAX}		10.0	50.0	II	µA
			T_{MIN}			100.0	V	µA
TCI_B	Average Input Bias Current Drift		25°C − T_{MAX}		200.0	300.0	IV	nA/°C
			25°C − T_{MIN}		200.0	700.0		
A_V	Small Signal Gain	R_L = 100Ω	25°C	0.96	0.98		I	V/V
			T_{MIN}, T_{MAX}	0.95			V	V/V
ILIN	Integral End Point linearity	±2V F.S.	25°C		0.2	0.4	IV	%F.S.
			T_{MIN}			0.8	IV	%F.S.
			T_{MAX}			0.3	IV	%F.S.
PSRR	Power Supply Rejection Ratio		All	45.0	65.0		II	dB
I_S	Supply Current—Quiescent	No Load	All		15.0	20.0	II	mA

DC Electrical Characteristics

$V_S = \pm 5V$, $R_L = 100\Omega$, $R_S = 50\Omega$ unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
R_{IN}	Input Resistance		25°C	100.0	160.0		I	kΩ
			T_{MIN}	50.0			V	kΩ
			T_{MAX}	200.0			V	kΩ
C_{IN}	Input Capacitance		25°C		1.6	2.2	IV	pF
			T_{MIN}, T_{MAX}			2.5	IV	pF
R_{OUT}	Output Impedance (DC)		25°C		2.0	3.0	IV	Ω
			T_{MIN}, T_{MAX}			3.5	IV	Ω
I_{OUT}	Output Current		25°C, T_{MAX}	50.0	70.0		II	mA
			T_{MIN}	45.0			V	mA
V_{OUT}	Output Voltage Swing	$R_L = 100\Omega$	25°C, T_{MAX}	±3.2	±4.0		II	V
			T_{MIN}	±3.0			V	V

AC Electrical Characteristics

$V_S = \pm 5V$, $R_L = 100\Omega$, $R_S = 50\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
FREQUENCY RESPONSE								
SSBW	−3 dB Bandwidth ($V_{OUT} < 0.5\ V_{PP}$)		25°C	400.0	730.0		V	MHz
			T_{MIN}	400.0			IV	MHz
			T_{MAX}	300.0			IV	MHz
LSBW	−3 dB Bandwidth ($V_{OUT} = 5.0\ V_{PP}$)		25°C	55.0	90.0		IV	MHz
			T_{MIN}, T_{MAX}	50.0			IV	MHz
GAIN FLATNESS								
GFPL	Peaking $V_{OUT} < 0.5\ V_{PP}$	<200 MHz	25°C		0.0	0.5	V	dB
			T_{MAX}			0.6	IV	dB
			T_{MIN}			0.8	IV	dB
GFR	Rolloff $V_{OUT} < 0.5\ V_{PP}$	<200 MHz	25°C		0.0	0.8	V	dB
			T_{MIN}			1.0	IV	dB
			T_{MAX}			1.2	IV	dB
GDL	Group Delay	<200 MHz	25°C, T_{MIN}		0.75	1.0	IV	ns
			T_{MAX}			1.2	IV	ns
LPD	Linear Phase Deviation $V_{OUT} < 0.5\ V_{PP}$	<200 MHz	25°C, T_{MIN}		0.7	1.5	IV	°
			T_{MAX}			2.0	IV	°

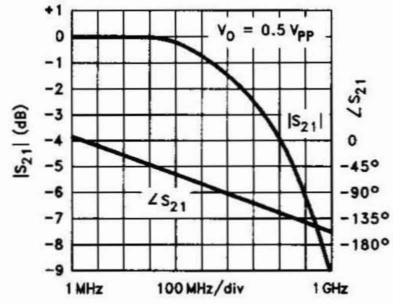
AC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_L = 100\Omega$, $R_S = 50\Omega$ unless otherwise specified

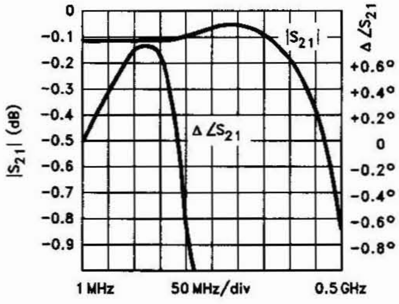
Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
TIME-DOMAIN RESPONSE								
TR1, TF1	Rise Time, Fall Time Input Signal Rise/Fall = 300 ps	0.5V Step	25°C, T_{MIN}		0.4	1.0	IV	ns
			T_{MAX}			1.4	IV	ns
TR2, TF2	Rise Time, Fall Time Input Signal Rise/Fall ≤ 1 ns	5.0V Step	25°C		4.5	7.5	IV	ns
			T_{MIN}, T_{MAX}			8.5	IV	ns
TS1	Settling Time to 0.2% Input Signal Rise/Fall ≤ 1 ns	2.0V Step	All		5.0	10.0	IV	ns
OS	Overshoot Input Signal Rise/Fall = 300 ps	0.5V Step	25°C		0.0	10.0	IV	%
			T_{MIN}, T_{MAX}			15.0	IV	%
SR	Slew Rate		25°C	500.0	800.0		IV	V/μs
			T_{MIN}, T_{MAX}	450.0			IV	V/μs
DISTORTION								
HD2	2nd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−55.0	−50.0	V	dBc
			T_{MIN}			−48.0	IV	dBc
			T_{MAX}			−55.0	IV	dBc
HD2A	2nd Harmonic Distortion at 50 MHz	2 V_{PP}	25°C, T_{MAX}		−50.0	−45.0	IV	dBc
			T_{MIN}			−40.0	IV	dBc
HD3	3rd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−65.0	−55.0	V	dBc
			T_{MIN}, T_{MAX}			−55.0	IV	dBc
HD3A	3rd Harmonic Distortion at 50 MHz	2 V_{PP}	25°C, T_{MIN}		−60.0	−50.0	IV	dBc
			T_{MAX}			−45.0	IV	dBc
EQUIVALENT INPUT NOISE								
NF	Noise Floor >100 kHz		25°C, T_{MIN}		−158.0	−155.0	IV	dBm (1 Hz)
			T_{MAX}			−154.0	IV	dBm (1 Hz)
INV	Integrated Noise 100 kHz to 200 MHz		25°C, T_{MIN}		40.0	57.0	IV	μV
			T_{MAX}			63.0	IV	μV

Typical Performance Curves ($V_S = \pm 5V$, $R_L = 100\Omega$, $R_S = 50\Omega$)

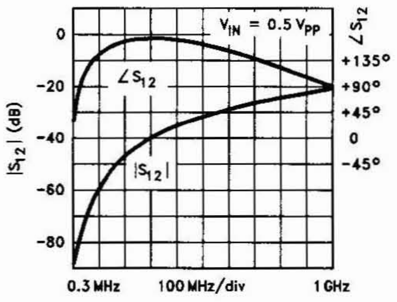
Forward Gain and Phase



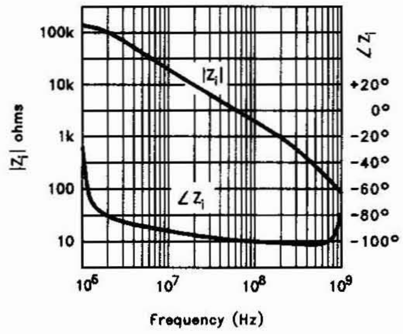
Gain Flatness & Deviation from Linear Phase



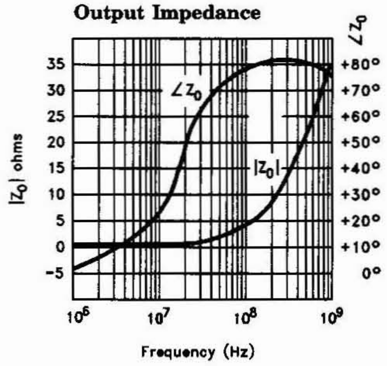
Reverse Gain and phase



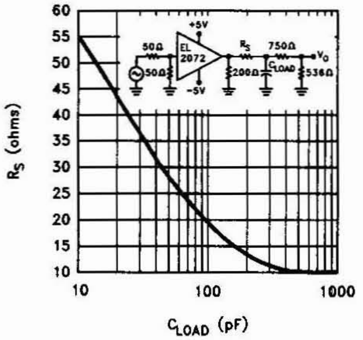
Input Impedance



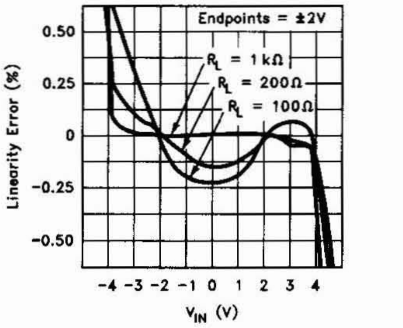
Output Impedance



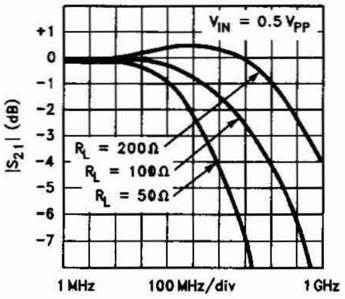
Recommended R_S vs Load Capacitance



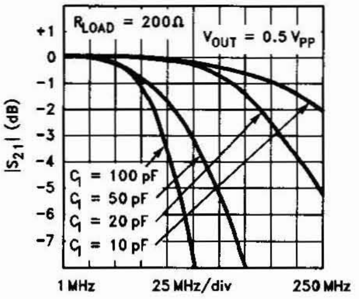
Integral Linearity Error



Frequency Response vs R_{load}



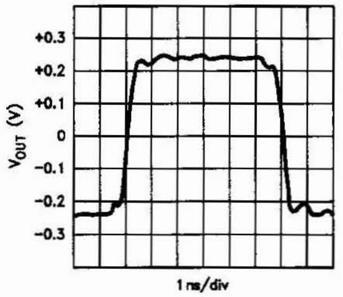
$|S_{21}|$ vs C_{load} with Recommended R_s



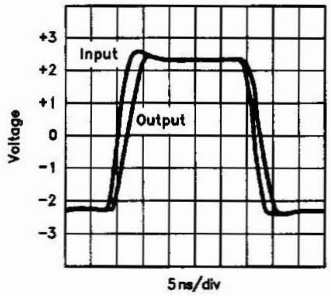
2072-2

Typical Performance Curves (V_S = ±5V, R_L = 100Ω, R_S = 50Ω) — Contd.

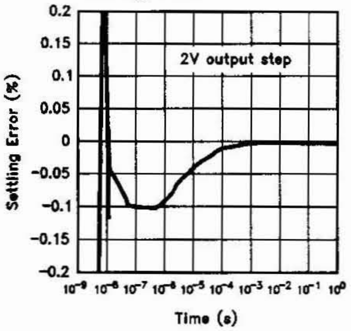
Small Signal Pulse Response



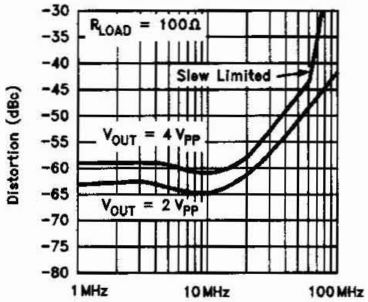
Large Signal Pulse Response



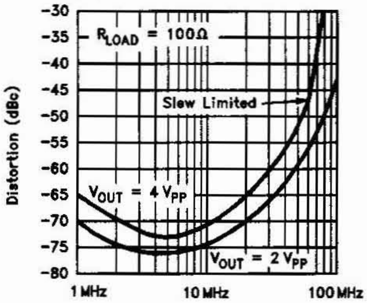
Long-Term Settling Time



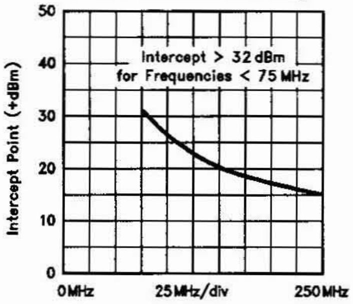
2nd Harmonic Distortion



3rd Harmonic Distortion

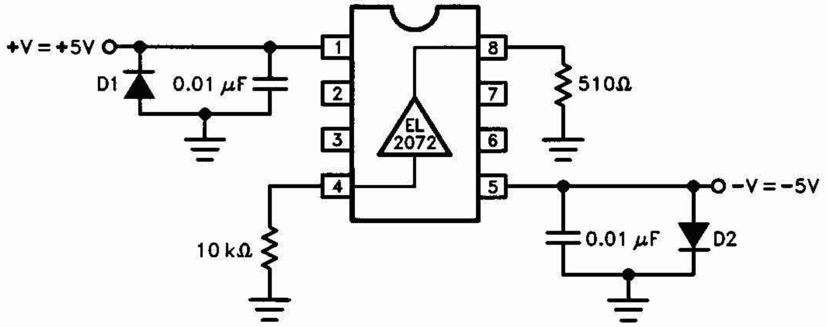


2-Tone, 3rd Order Intermodulation Intercept



2072-3

Burn-In Circuit



2072-4

Printed Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. This is especially important for the EL2072, which has a typical bandwidth of 730 MHz. Ground plane construction is a requirement, as is good power-supply bypassing close to the package. A closely-placed 0.01 μF ceramic capacitor between each supply pin and the ground plane is usually sufficient decoupling.

Pins 2, 3, 6, and 7 should be connected to the ground-plane to minimize capacitive feedthrough, and all input and output traces should be laid out as transmission lines and terminated as close to the EL2072 package as possible.

Increasing capacitance on the output of the EL2072 will add phase shift, decreasing phase margin and increasing frequency-response peaking. A small series resistor before the capacitance decouples this effect, and should be used for large capacitance values. Please refer to the graphs for the appropriate resistor value to be used.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2073C

200 MHz Unity-Gain Stable Operational Amplifier

Features

- 200 MHz gain-bandwidth product
- Unity-gain stable
- Ultra low video distortion = 0.01%/0.015° @ NTSC/PAL
- Conventional voltage-feedback topology
- Low offset voltage = 200 μV
- Low bias current = 2 μA
- Low offset current = 0.1 μA
- Output current = 50 mA over temperature
- Fast settling = 13 ns to 0.1%
- Low distortion = −60 dB HD2, −70 dB HD3 @ 20 MHz, 2 V_{PP}, $A_V = +1$

Applications

- High resolution video
- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2073CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2073CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

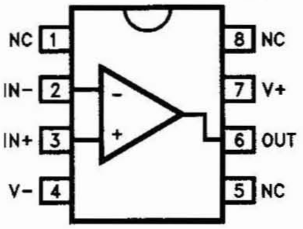
The EL2073 is a precision voltage-feedback amplifier featuring a 200 MHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50 mA output current drive over temperature.

The EL2073 is unity-gain stable with a −3 dB bandwidth of 400 MHz. It has a very low 200 μV of input offset voltage, only 2 μA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2073 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2073 the ideal choice for all op-amp applications requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2073 an ideal amplifier for signal-processing and digitizing systems.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



2073-1

January 1995 Rev D

EL2073C

200 MHz Unity-Gain Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Common-Mode Input	$\pm V_S$
Differential Input Voltage	5V

Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO-8
Operating Temperature	−40°C to +85°C
Junction Temperature	175°C
Storage Temperature	−60°C to +150°C

Note: See EL2071/EL2171 for Thermal Impedance curves.

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0V	25°C		0.2	1.5	I	mV
			T_{MIN}, T_{MAX}			3	IV	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)	All		8		V	μV/°C
I_B	Input Bias Current		25°C		2	6	I	μA
			T_{MIN}, T_{MAX}		2	6	IV	μA
I_{OS}	Input Offset Current	V_{CM} = 0V	25°C		0.1	1	I	μA
			T_{MIN}, T_{MAX}			2	IV	μA
PSRR	Power Supply Rejection Ratio	(Note 2)	25°C	60	80		I	dB
			T_{MIN}, T_{MAX}	60			IV	dB
CMRR	Common Mode Rejection Ratio	(Note 3)	25°C	65	90		I	dB
			T_{MIN}, T_{MAX}	65			IV	dB
I_S	Supply Current—Quiescent	No Load	25°C		21	25	I	mA
			T_{MIN}, T_{MAX}			25	IV	mA
R_{IN} (diff)	R_{IN} (Differential)	Open-Loop	25°C		15		V	kΩ
C_{IN} (diff)	C_{IN} (Differential)	Open-Loop	25°C		1		V	pF
R_{IN} (cm)	R_{IN} (Common-Mode)		25°C		1		V	MΩ
C_{IN} (cm)	C_{IN} (Common-Mode)		25°C		1		V	pF

Open Loop DC Electrical Characteristics

$V_S = \pm 5V$, $R_L = 100\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
R_{OUT}	Output Resistance		25°C		20		V	mΩ
CMIR	Common-Mode Input Range		25°C	±3	±3.5		IV	V
			T_{MIN}, T_{MAX}	±2.5			IV	V
I_{OUT}	Output Current		25°C	50	70		I	mA
			T_{MIN}, T_{MAX}	50			IV	mA
V_{OUT}	Output Voltage Swing	No Load	25°C	±3.5	±4		I	V
			T_{MIN}, T_{MAX}	±3.5			IV	V
V_{OUT} 100	Output Voltage Swing	100Ω	25°C	±3	±3.6		I	V
			T_{MIN}, T_{MAX}	±3			IV	V
V_{OUT} 50	Output Voltage Swing	50Ω	25°C	±3	±3.4		I	V
			T_{MIN}, T_{MAX}	±2.5			IV	V
A_{VOL} 100	Open-Loop Gain	100Ω	25°C	500	1000		I	V/V
			T_{MIN}, T_{MAX}	400			IV	V/V
A_{VOL} 50	Open-Loop Gain	50Ω	25°C	400	800		I	V/V
			T_{MIN}, T_{MAX}	300			IV	V/V
eN@ > 1 MHz	Noise Voltage 1–100 MHz		25°C		2.3		V	nV/$\sqrt{Hz}$
iN@ > 100 kHz	Noise Current 100k–100 MHz		25°C		3.2		V	pA/$\sqrt{Hz}$

Closed Loop AC Electrical Characteristics

$V_S = \pm 5V$, $A_V = +1$, Rf $= 0\Omega$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
SSBW	−3 dB Bandwidth ($V_{OUT} = 0.4V_{PP}$)	$A_V = +1$	25°C	150	300		V	MHz
		$A_V = -1$	25°C		200		V	MHz
		$A_V = +2$	25°C	150	200		IV	MHz
			T_{MIN}, T_{MAX}	125			IV	MHz
		$A_V = +5$	25°C		40		V	MHz
		$A_V = +10$	25°C		20		V	MHz
GBWP	Gain-Bandwidth Product	$A_V = +10$	25°C		200		V	MHz
LSBWa	−3 dB Bandwidth	$V_{OUT} = 2\ V_{PP}$ (Note 4)	All	50	85		IV	MHz
LSBWb	−3 dB Bandwidth	$V_{OUT} = 5\ V_{PP}$ (Note 4)	All	11	16		IV	MHz
GFPL	Peaking (<50 MHz)	$V_{OUT} = 0.4\ V_{PP}$	25°C		0	0.5	IV	dB
			T_{MIN}, T_{MAX}			0.5	IV	dB
GFPH	Peaking (>50 MHz)	$V_{OUT} = 0.4\ V_{PP}$	25°C		1	3	IV	dB
			T_{MIN}, T_{MAX}			3	IV	dB
GFR	Rolloff (<100 MHz)	$V_{OUT} = 0.4\ V_{PP}$	25°C		0.1	0.5	IV	dB
			T_{MIN}, T_{MAX}			0.5	IV	dB

Closed Loop AC Electrical Characteristics

$V_S = \pm 5V$, $A_V = +1$, $Rf = 0\Omega$, $R_L = 100\Omega$ unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
LPD	Linear Phase Deviation (<100 MHz)	$V_{OUT} = 0.4\ V_{PP}$	All		1	1.8	IV	°
PM	Phase Margin	$A_V = +1$	25°C		60		V	°
tr1, tf1	Rise Time, Fall Time	0.4V Step, $A_V = +2$	25°C		2		V	ns
tr2, tf2	Rise Time, Fall Time	5V Step, $A_V = +2$	25°C		15		V	ns
ts1	Settling to 0.1% ($A_V = -1$)	2V Step	25°C		13		V	ns
ts2	Settling to 0.01% ($A_V = -1$)	2V Step	25°C		25		V	ns
OS	Overshoot	2V Step	25°C		5		V	%
SR	Slew Rate	2V Step	All	175	250		IV	V/μs
DISTORTION (Note 5)								
HD2a	2nd Harmonic Distortion	@ 10 MHz, $A_V = +2$	25°C		−65	−55	IV	dBc
HD2b	2nd Harmonic Distortion	@ 20 MHz, $A_V = +1$	25°C		−60	−50	IV	dBc
HD2c	2nd Harmonic Distortion	@ 20 MHz, $A_V = +2$	25°C		−55	−50	IV	dBc
			T_{MIN}, T_{MAX}			−45	IV	dBc
HD3a	3rd Harmonic Distortion	@ 10 MHz, $A_V = +2$	25°C		−72	−60	IV	dBc
HD3b	3rd Harmonic Distortion	@ 20 MHz, $A_V = +1$	25°C		−70	−55	IV	dBc
HD3c	3rd Harmonic Distortion	@ 20 MHz, $A_V = +2$	25°C		−70	−60	IV	dBc
			T_{MIN}, T_{MAX}			−60	IV	dBc
VIDEO PERFORMANCE (Note 6)								
dG	Differential Gain	NTSC	25°C		0.01	0.05	IV	$\%_{pp}$
dP	Differential Phase	NTSC	25°C		0.015	0.05	IV	$^{\circ}_{pp}$
dG	Differential Gain	30 MHz	25°C		0.1		V	$\%_{pp}$
dP	Differential Phase	30 MHz	25°C		0.1		V	$^{\circ}_{pp}$
VBW	±0.1 dB Bandwidth Flatness		25°C	25	50		IV	MHz

Note 1: Measured from T_{MIN}, T_{MAX}.

Note 2: $\pm V_{CC} = \pm 4.5V$ to 5.5V.

Note 3: $\pm V_{IN} = \pm 2.5V$, $V_{OUT} = 0V$

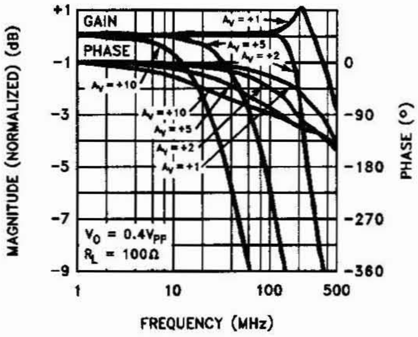
Note 4: Large-signal bandwidth calculated using $LSBW = \dfrac{\text{Slew Rate}}{2\pi\ V_{PEAK}}$.

Note 5: All distortion measurements are made with $V_{OUT} = 2\ V_{PP}$, $R_L = 100\Omega$.

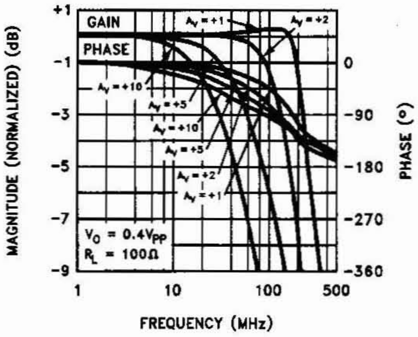
Note 6: Video performance measured at $A_V = +1$ with 2 times normal video level across $R_L = 100\Omega$. This corresponds to standard video levels across a back-terminated 50Ω load, i.e., 0–100 IRE, 40IREpp giving a 1 V_{PP} video signal across the 50Ω load. For other values of R_L, see curves.

Typical Performance Curves (T$_A$ = 25°C)

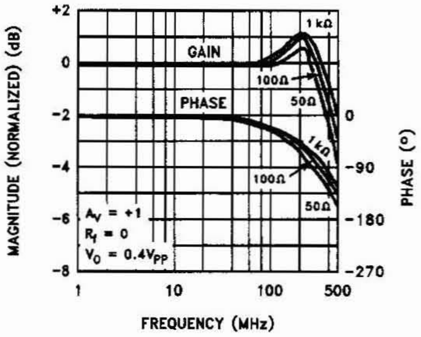
Non-Inverting Frequency Response



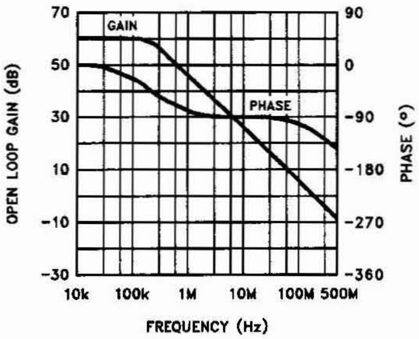
Inverting Frequency Response



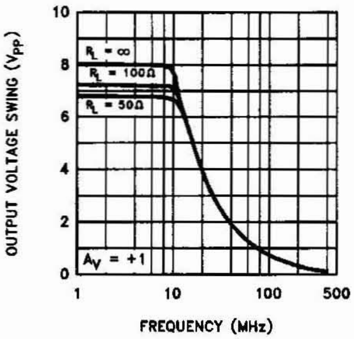
Frequency Response for Various R$_L$s



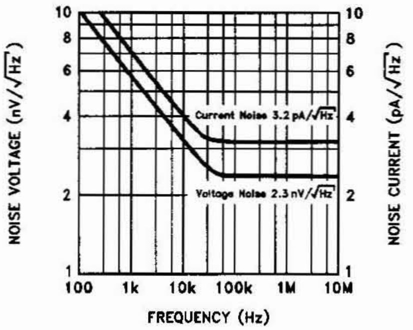
Open Loop Gain and Phase



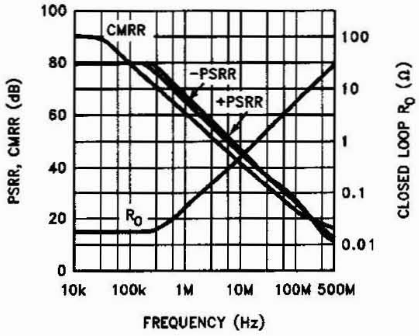
Output Voltage Swing vs Frequency



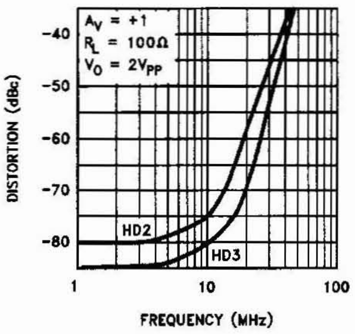
Equivalent Input Noise



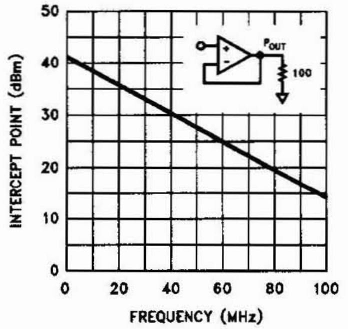
PSRR, CMRR, and Closed-Loop R$_O$ vs Frequency



2nd and 3rd Harmonic Distortion vs Frequency



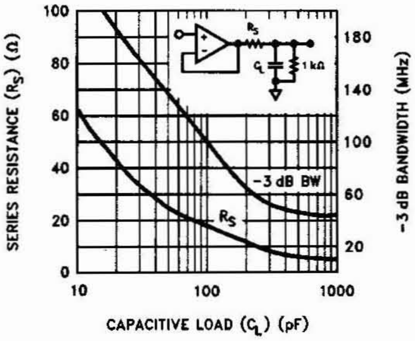
2-Tone, 3rd Order Intermodulation Intercept



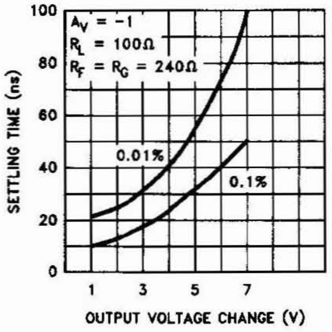
2073-2

Typical Performance Curves (T_A = 25°C unless otherwise specified) — Contd.

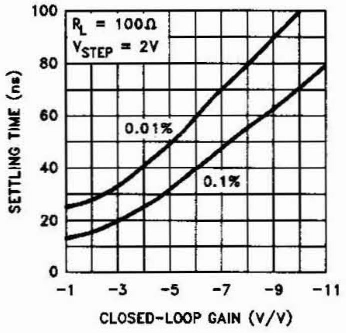
Series Resistor and Resulting Bandwidth vs Capacitive Load



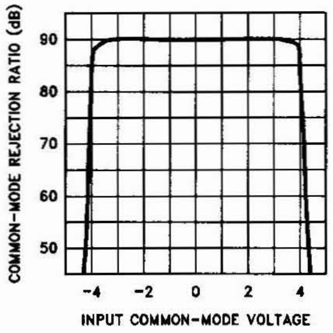
Settling Time vs Output Voltage Change



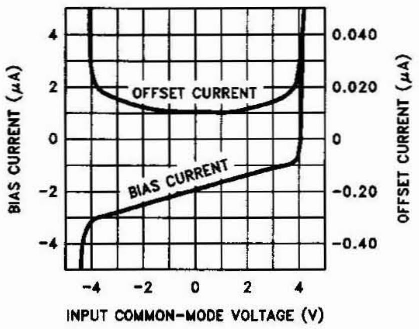
Settling Time vs Closed-Loop Gain



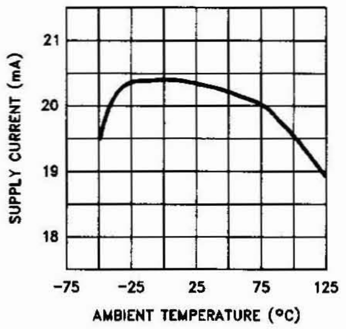
Common-Mode Rejection Ratio vs Input Common-Mode Voltage



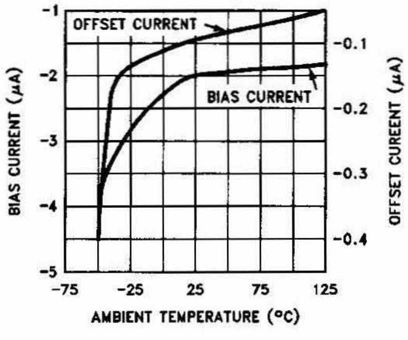
Bias and Offset Current vs Input Common-Mode Voltage



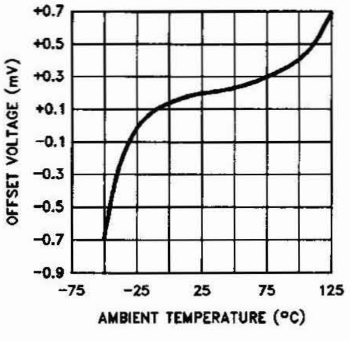
Supply Current vs Temperature



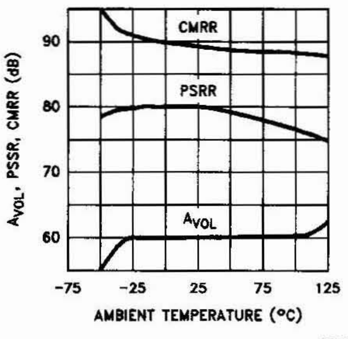
Bias and Offset Current vs Temperature



Offset Voltage vs Temperature



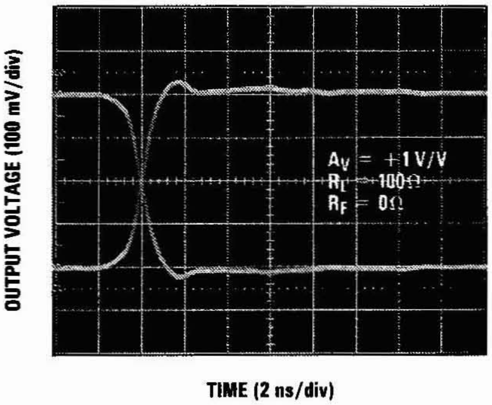
A_{VOL}, PSRR, and CMRR vs Temperature



2073-3

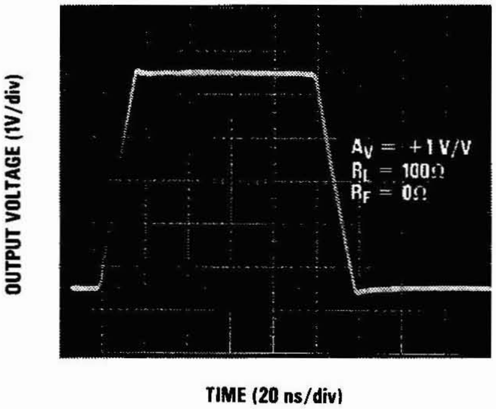
Typical Performance Curves (T_A = 25°C) — Contd.

Small Signal Transient Response



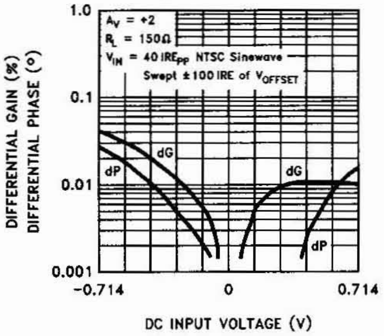
2072-4

Large Signal Transient Response

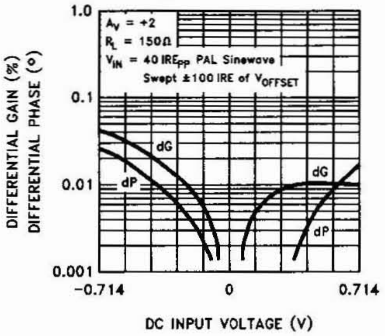


2072-5

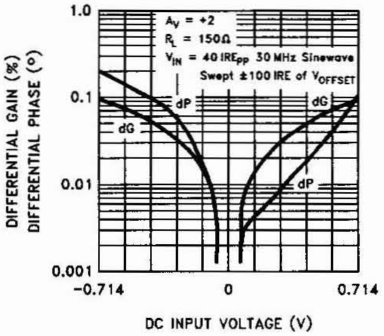
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



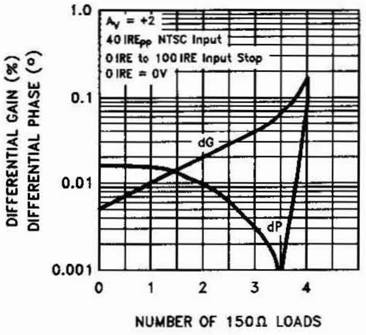
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



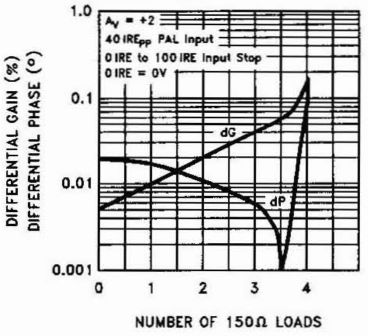
Differential Gain and Phase vs DC Input Offset at 30 MHz



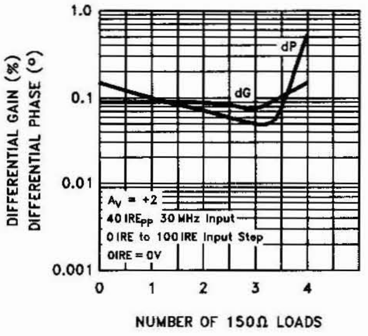
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz

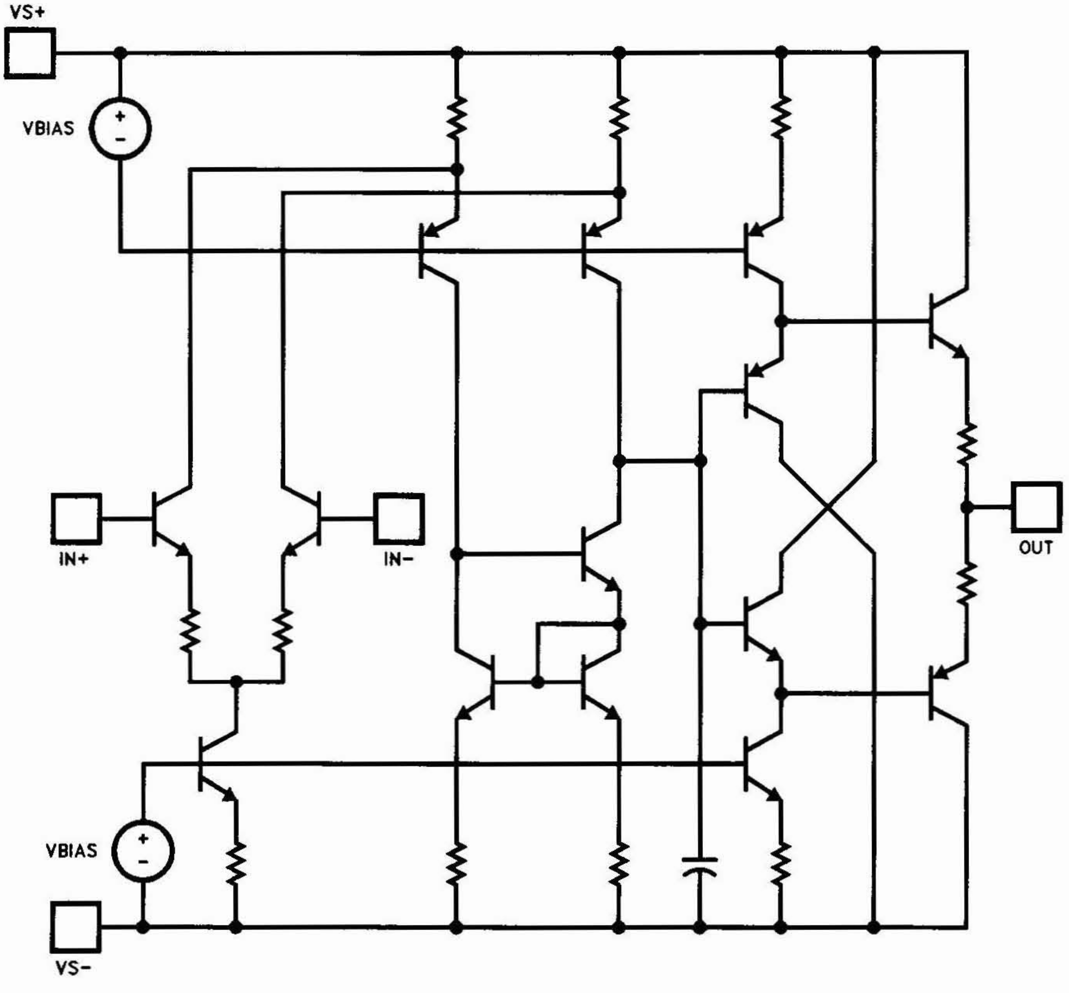


Differential Gain and Phase vs Number of 150Ω Loads at 30 MHz



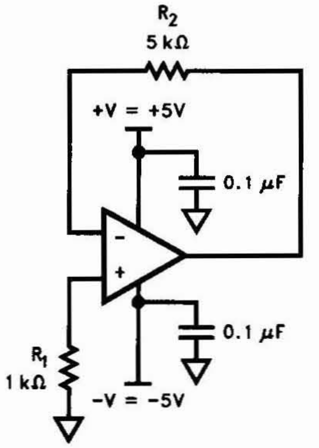
2073-6

Equivalent Circuit


VS+
VBIAS
IN+
IN−
OUT
VBIAS
VS−

2073-7

Burn-In Circuit


R2
5 kΩ
+V = +5V
0.1 μF
0.1 μF
R1
1 kΩ
−V = −5V

2073-8

All Packages Use The Same Schematic

Applications Information

Product Description

The EL2073 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2073 uses a classical voltage-feedback topology which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2073 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2073 is an excellent choice for applications such as log amplifiers.

The EL2073 also has excellent DC specifications: 200 μV, V_{OS}, 2 μA I_B, 0.1 μA I_{OS}, and 90 dB of CMRR. These specifications allow the EL2073 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2073 is only 3.2 pA/$\sqrt{\text{Hz}}$, making it an excellent choice for high-sensitivity transimpedance amplifier configurations.

Gain-Bandwidth Product

The EL2073 has a gain-bandwidth product of 200 MHz. For gains greater than 4, its closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2073 has a −3 dB bandwidth of 400 MHz at a gain of +1, dropping to 200 MHz at a gain of +2. It is important to note that the EL2073 has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2073 in a gain of +1 only exhibits 1 dB of peaking with a 100Ω load.

Video Performance

An industry-standard method of measuring the video distortion of a component such as the EL2073 is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC, 4.43 MHz for PAL, or 30 MHz for HDTV. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2073 has been designed to be among the best video amplifiers in the marketplace today. It has been thoroughly characterized for video performance in the topology described above, and the results have been included as minimum dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2073 exhibits dG and dP of only 0.01% and 0.015° at NTSC and PAL. Because dG and dP vary with different DC offsets, the superior video performance of the EL2073 has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The excellent output drive capability of the EL2073 allows it to drive up to 4 back-terminated loads with excellent video performance. With 4 150Ω loads, dG and dP are only 0.15% and 0.08° at NTSC and PAL. For more information, refer to the curves for Video Performance vs Number of 150Ω Loads.

Output Drive Capability

The EL2073 has been optimized to drive 50Ω and 75Ω loads. It can easily drive 6 V_{PP} into a 50Ω load. This high output drive capability makes the EL2073 an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2073 remains a minimum of 50 mA at low temperatures. The EL2073 is current-limited at

Applications Information

the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

Although the EL2073 has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10 pF should be buffered with a series resistor (Rs) to isolate the load capacitance from the amplifier output. A curve of recommended Rs vs Cload has been included for reference. Values of Rs were chosen to maximize resulting bandwidth without peaking.

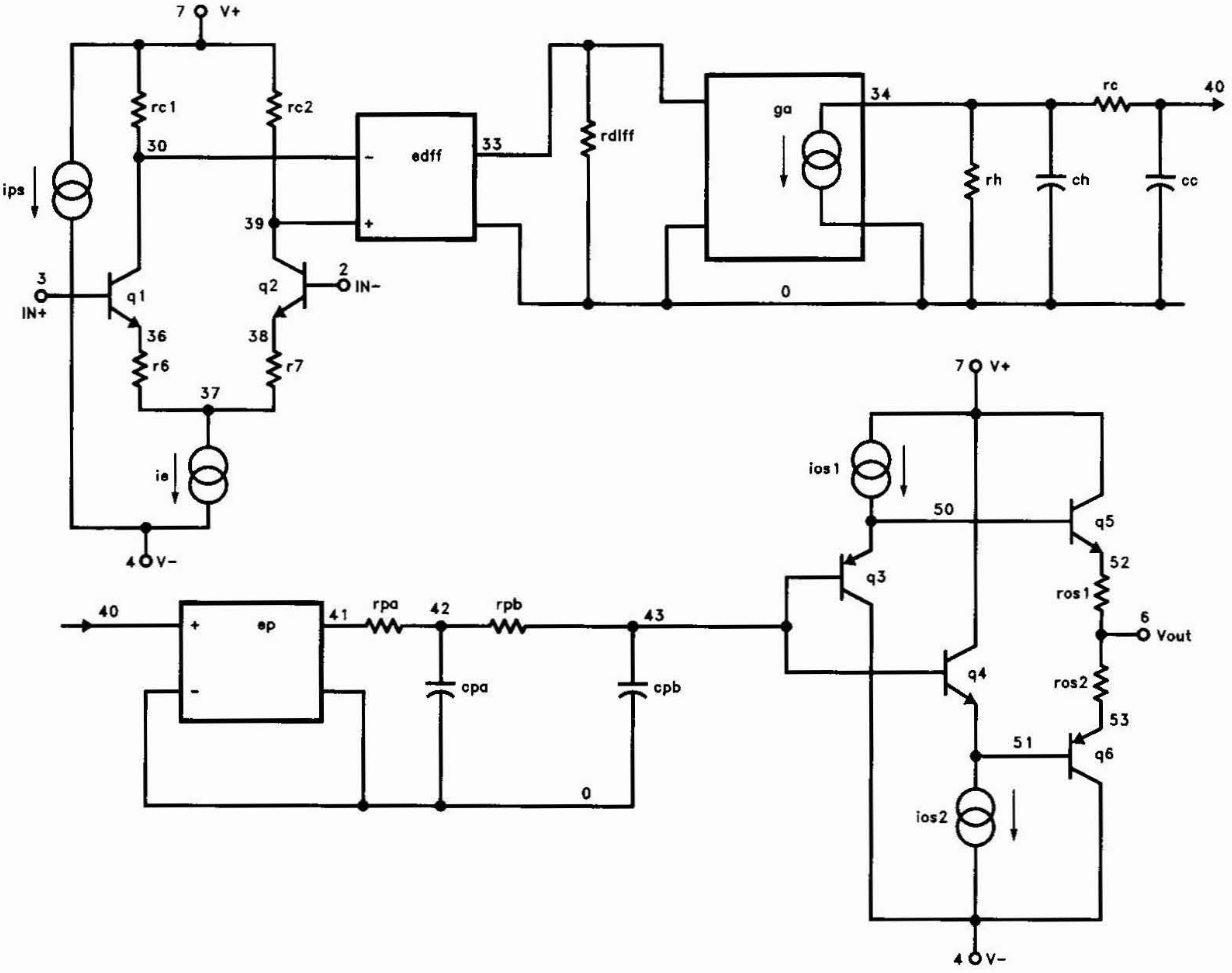
Printed-Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1 μF–10 μF tantalum capacitor is recommended in parallel with a 0.01 μF ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2073 directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.

EL2073 Macromodel

```
*
* Connections:                     +input
*                                  | -input
*                                  | | +Vsupply
*                                  | | | -Vsupply
*                                  | | | | output
*                                  | | | | |
.subckt M2073                      3 2 7 4 6
*
*Input Stage
*
ie 37 4 1mA
r6 36 37 125
r7 38 37 125
rc1 7 30 200
rc2 7 39 200
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 1
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 1.2pF
rc 34 40 400
cc 40 0 0.3pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 0.5pF
rpb 42 43 50
cpb 43 0 0.5pF
*
* Output Stage
*
ios1 7 50 3.0mA
ios2 51 4 3.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 2
ros2 6 53 2
*
Power Supply Current
*
ips 7 4 11.4mA
*
Models
*
.model qna npn(is=800e-18 bf=170 tf=0.2ns)
.model qn  npn(is=810e-18 bf=200 tf=0.2ns)
.model qp  pnp(is=800e-18 bf=200 tf=0.2ns)
.ends
```

EL2073 Macromodel — Contd.


7 V+
rc1
rc2
30
ips
39
edff
33
rdiff
ga
34
rc
40
rh
ch
cc
3
IN+
q1
q2
2
IN−
0
36
38
r6
r7
37
ie
4 V−
7 V+
ios1
50
q5
52
q3
ros1
6
Vout
40
ep
41
rpa
42
rpb
43
cpa
cpb
0
q4
ros2
53
51
q6
ios2
4 V−

2073-9

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2074C

400 MHz GBWP Gain-of-2 Stable Operational Amplifier

Features

- 400 MHz gain-bandwidth product
- Gain-of-2 stable
- Ultra low video distortion = 0.01%/0.015° @ NTSC/PAL
- Conventional voltage-feedback topology
- Low offset voltage = 200 μV
- Low bias current = 2 μA
- Low offset current = 0.1 μA
- Output current = 50 mA over temperature
- Fast settling = 13 ns to 0.1%
- Low distortion = −55 dB HD2, −70 dB HD3 @ 20 MHz, 2 V_{PP}, $A_V = +2$

Applications

- High resolution video
- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2074CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2074CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

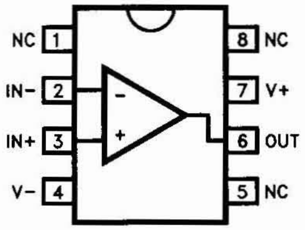
The EL2074 is a precision voltage-feedback amplifier featuring a 400 MHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50 mA output current drive over temperature.

The EL2074 is gain-of-2 stable with a −3 dB bandwidth of 400 MHz at $A_V = +2$. It has a very low 200 μV of input offset voltage, only 2 μA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2074 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2074 the ideal choice for all op-amp applications at a noise gain of 2 or greater requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2074 an ideal amplifier for signal-processing and digitizing systems.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



2074-1

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Common-Mode Input	±V_S
Differential Input Voltage	5V

Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO-8
Operating Temperature	0°C to +75°C
Junction Temperature	175°C
Storage Temperature	−60°C to +150°C

Note: See EL2071/EL2171 for Thermal Impedance curves.

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0V	25°C		0.2	1.5	I	mV
			T_{MIN}, T_{MAX}			3	III	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)	All		8		V	µV/°C
I_B	Input Bias Current	V_{CM} = 0V	All		2	6	II	µA
I_{OS}	Input Offset Current	V_{CM} = 0V	25°C		0.1	1	I	µA
			T_{MIN}, T_{MAX}			2	III	µA
PSRR	Power Supply Rejection Ratio	(Note 2)	All	60	80		II	dB
CMRR	Common Mode Rejection Ratio	(Note 3)	All	65	90		II	dB
I_S	Supply Current—Quiescent	No Load	25°C		21	25	I	mA
			T_{MIN}, T_{MAX}			25	III	mA
R_{IN} (diff)	R_{IN} (Differential)	Open-Loop	25°C		15		V	kΩ
C_{IN} (diff)	C_{IN} (Differential)	Open-Loop	25°C		1		V	pF
R_{IN} (cm)	R_{IN} (Common-Mode)		25°C		1		V	MΩ
C_{IN} (cm)	C_{IN} (Common-Mode)		25°C		1		V	pF

Open Loop DC Electrical Characteristics

$V_S = \pm 5V$, $R_L = 100\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
R_{OUT}	Output Resistance		25°C		20		V	mΩ
CMIR	Common-Mode Input Range		25°C	±3	±3.5		IV	V
			T_{MIN}, T_{MAX}	±2.5			IV	V
I_{OUT}	Output Current		All	50	70		II	mA
V_{OUT}	Output Voltage Swing	No Load	All	±3.5	±4		II	V
V_{OUT} 100	Output Voltage Swing	100Ω	All	±3	±3.6		II	V
V_{OUT} 50	Output Voltage Swing	50Ω	All	±2.5	±3.4		II	V
A_{VOL} 100	Open-Loop Gain	100Ω	25°C	500	1000		I	V/V
			T_{MIN}, T_{MAX}	400			III	V/V
A_{VOL} 50	Open-Loop Gain	50Ω	25°C	400	800		I	V/V
			T_{MIN}, T_{MAX}	300			III	V/V
eN@ > 1 MHz	Noise Voltage 1–100 MHz		25°C		2.3		V	$nV/\sqrt{Hz}$
iN@ > 100 kHz	Noise Current 100k–100 MHz		25°C		3.2		V	$pA/\sqrt{Hz}$

Closed Loop AC Electrical Characteristics

$V_S = \pm 5V$, $A_V = +2$, $Rf = Rg = 250\Omega$, $Cf = 3pF$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
SSBW	−3 dB Bandwidth ($V_{OUT} = 0.4V_{PP}$)	$A_V = -1$	25°C		400		V	MHz
		$A_V = +2$	25°C	250	400		V	MHz
			T_{MIN}, T_{MAX}	250			V	MHz
		$A_V = +5$	25°C		100		V	MHz
		$A_V = +10$	25°C		40		V	MHz
GBWP	Gain-Bandwidth Product	$A_V = +10$	25°C		400		V	MHz
LSBWa	−3 dB Bandwidth	$V_{OUT} = 2\ V_{PP}$ (Note 4)	All	43	63		IV	MHz
LSBWb	−3 dB Bandwidth	$V_{OUT} = 5\ V_{PP}$ (Note 4)	All	17	25		IV	MHz
GFPL	Peaking (<50 MHz)	$V_{OUT} = 0.4\ V_{PP}$	25°C		0	1	V	dB
			T_{MIN}, T_{MAX}			1	V	dB
GFPH	Peaking (>50 MHz)	$V_{OUT} = 0.4\ V_{PP}$	25°C		0	2	V	dB
			T_{MIN}, T_{MAX}			2	V	dB
GFR	Rolloff (<100 MHz)	$V_{OUT} = 0.4\ V_{PP}$	25°C		0.1	0.5	V	dB
			T_{MIN}, T_{MAX}			0.5	V	dB

Closed Loop AC Electrical Characteristics

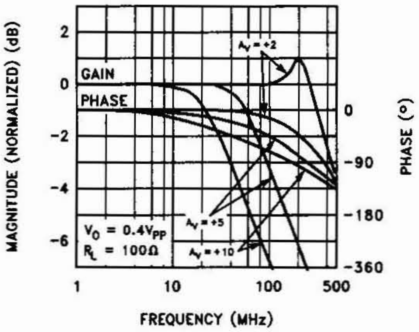
V_S = ±5V, A_V = +2, Rf = Rg = 250Ω, Cf = 3pF, R_L = 100Ω unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
LPD	Linear Phase Deviation (<100 MHz)	V_{OUT} = 0.4 V_{PP}	All		1	1.8	IV	°
PM	Phase Margin	A_V = +2	25°C		50		V	°
tr1, tf1	Rise Time, Fall Time	0.4V Step, A_V = +2	25°C		1.8		V	ns
tr2, tf2	Rise Time, Fall Time	5V Step, A_V = +2	25°C		8		V	ns
ts1	Settling to 0.1% (A_V = −1)	2V Step	25°C		13		V	ns
ts2	Settling to 0.01% (A_V = −1)	2V Step	25°C		25		V	ns
OS	Overshoot	2V Step	25°C		5		V	%
SR	Slew Rate	2V Step	All	275	400		IV	V/µs
DISTORTION (Note 5)								
HD2a	2nd Harmonic Distortion	@ 10 MHz, A_V = +2	25°C		−65	−55	V	dBc
HD2c	2nd Harmonic Distortion	@ 20 MHz, A_V = +2	25°C		−55	−45	V	dBc
			T_{MIN}, T_{MAX}			−45	V	dBc
HD3a	3rd Harmonic Distortion	@ 10 MHz, A_V = +2	25°C		−72	−60	V	dBc
HD3c	3rd Harmonic Distortion	@ 20 MHz, A_V = +2	25°C		−70	−60	V	dBc
			T_{MIN}, T_{MAX}			−60	V	dBc
VIDEO PERFORMANCE (Note 6)								
dG	Differential Gain	NTSC	25°C		0.01	0.05	V	$\%_{pp}$
dP	Differential Phase	NTSC	25°C		0.015	0.05	V	$^\circ_{pp}$
dG	Differential Gain	30 MHz	25°C		0.1		V	$\%_{pp}$
dP	Differential Phase	30 MHz	25°C		0.1		V	$^\circ_{pp}$
VBW	±0.1 dB Bandwidth Flatness		25°C	25	50		V	MHz

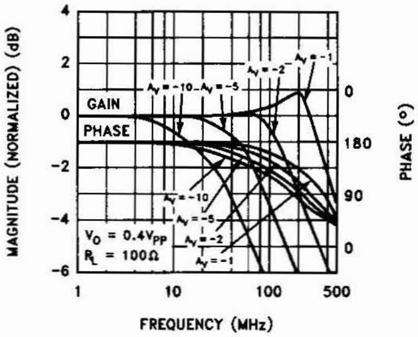
Note 1: Measured from T_{MIN}, T_{MAX}.
Note 2: $\pm V_{CC}$ = ±4.5V to 5.5V.
Note 3: $\pm V_{IN}$ = ±2.5V, V_{OUT} = 0V
Note 4: Large-signal bandwidth calculated using $LSBW = \frac{\text{Slew Rate}}{2\pi\, V_{PEAK}}$.
Note 5: All distortion measurements are made with V_{OUT} = 2 V_{PP}, R_L = 100Ω.
Note 6: Video performance measured at A_V = +2 with 2 times normal video level across R_L = 100Ω. This corresponds to standard video levels across a back-terminated 50Ω load, i.e., 0–100 IRE, 40IREpp giving a 1 V_{PP} video signal across the 50Ω load. For other values of R_L, see curves.

Typical Performance Curves (T_A = 25°C)

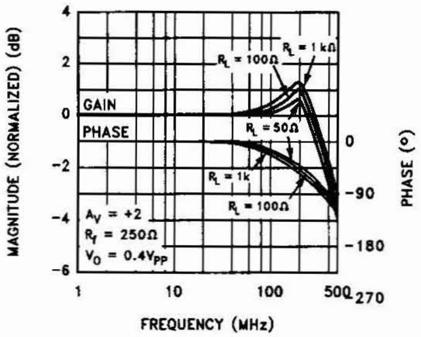
Non-Inverting Frequency Response



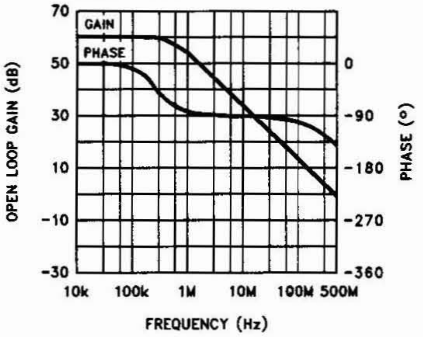
Inverting Frequency Response



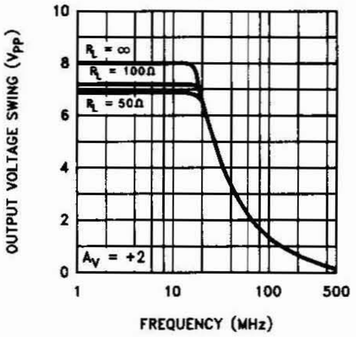
Frequency Response for Various R_Ls



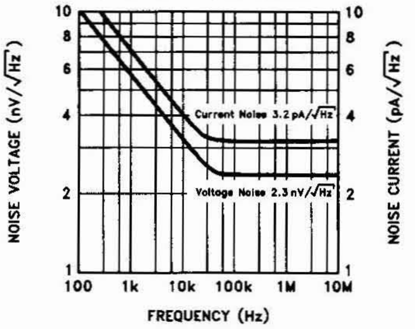
Open Loop Gain and Phase



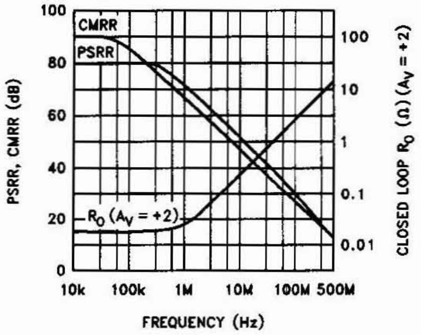
Output Voltage Swing vs Frequency



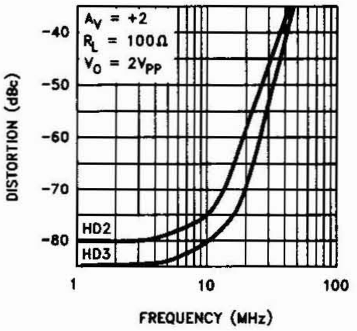
Equivalent Input Noise



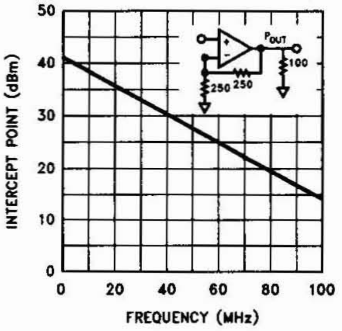
PSRR, CMRR, and Closed-Loop R_O vs Frequency



2nd and 3rd Harmonic Distortion vs Frequency



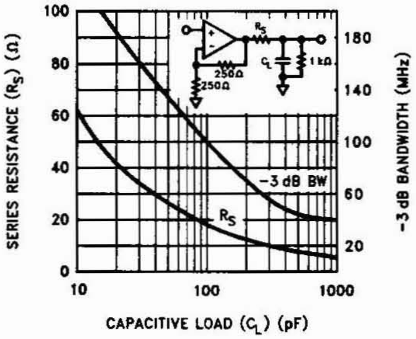
2-Tone, 3rd Order Intermodulation Intercept



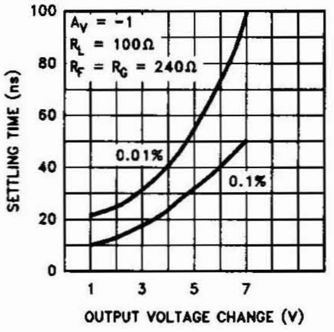
2074-2

Typical Performance Curves (T$_A$ = 25°C unless otherwise specified) — Contd.

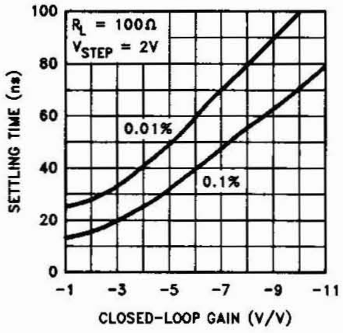
Series Resistor and Resulting Bandwidth vs Capacitive Load



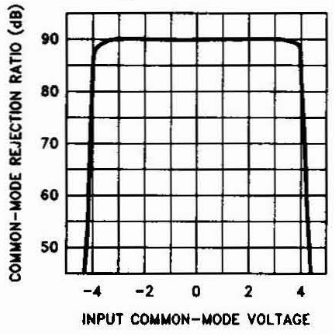
Settling Time vs Output Voltage Change



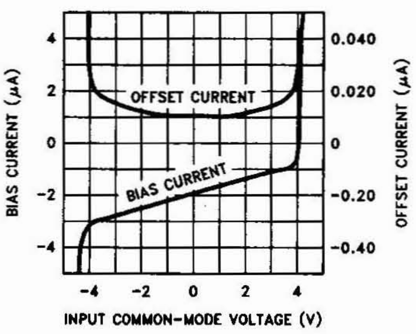
Settling Time vs Closed-Loop Gain



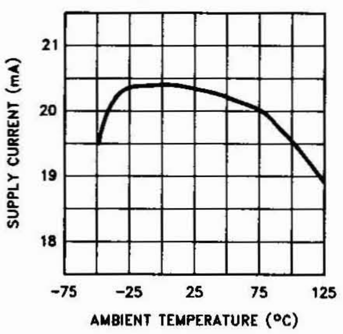
Common-Mode Rejection Ratio vs Input Common-Mode Voltage



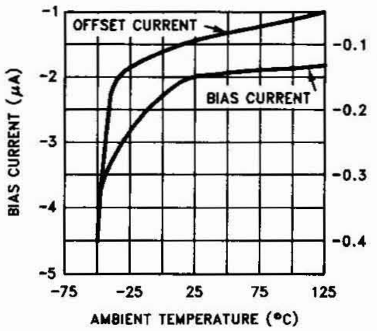
Bias and Offset Current vs Input Common-Mode Voltage



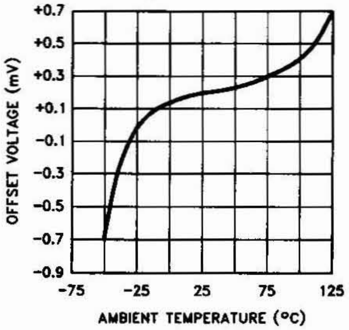
Supply Current vs Temperature



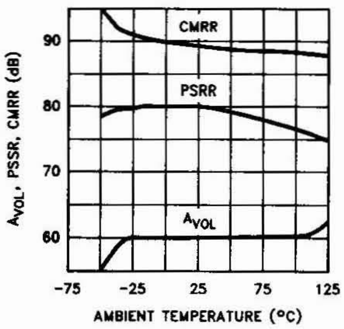
Bias and Offset Current vs Temperature



Offset Voltage vs Temperature



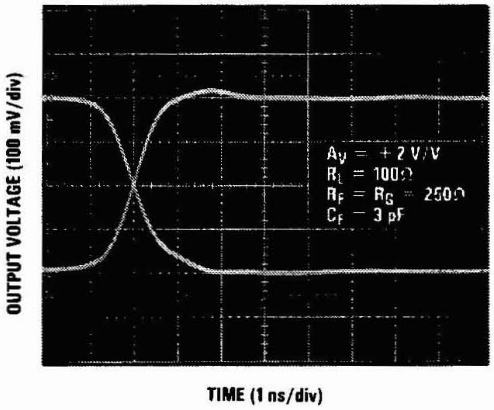
A$_{VOL}$, PSRR, and CMRR vs Temperature



2074-3

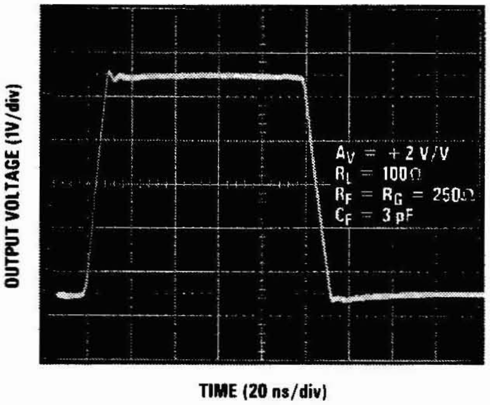
Typical Performance Curves (T_A = 25°C) — Contd.

Small Signal Transient Response



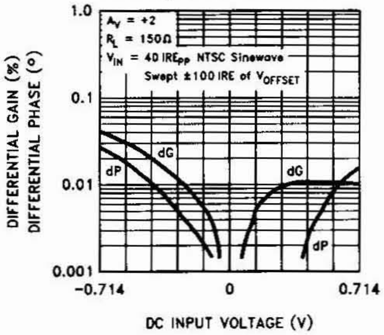
2074-4

Large Signal Transient Response

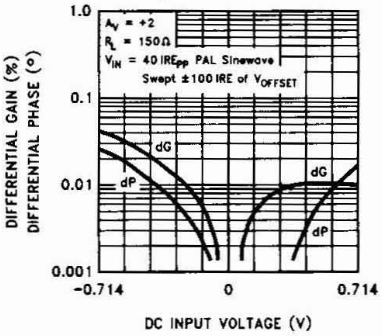


2074-5

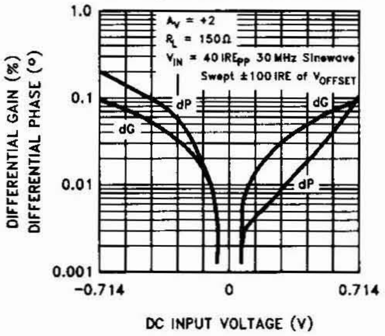
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



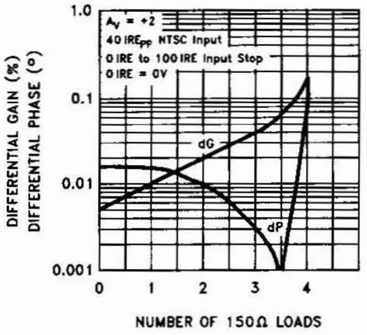
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



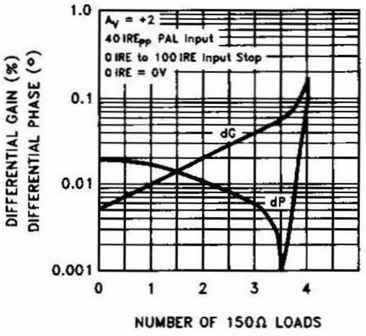
Differential Gain and Phase vs DC Input Offset at 30 MHz



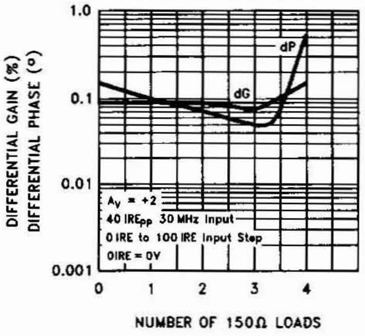
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz

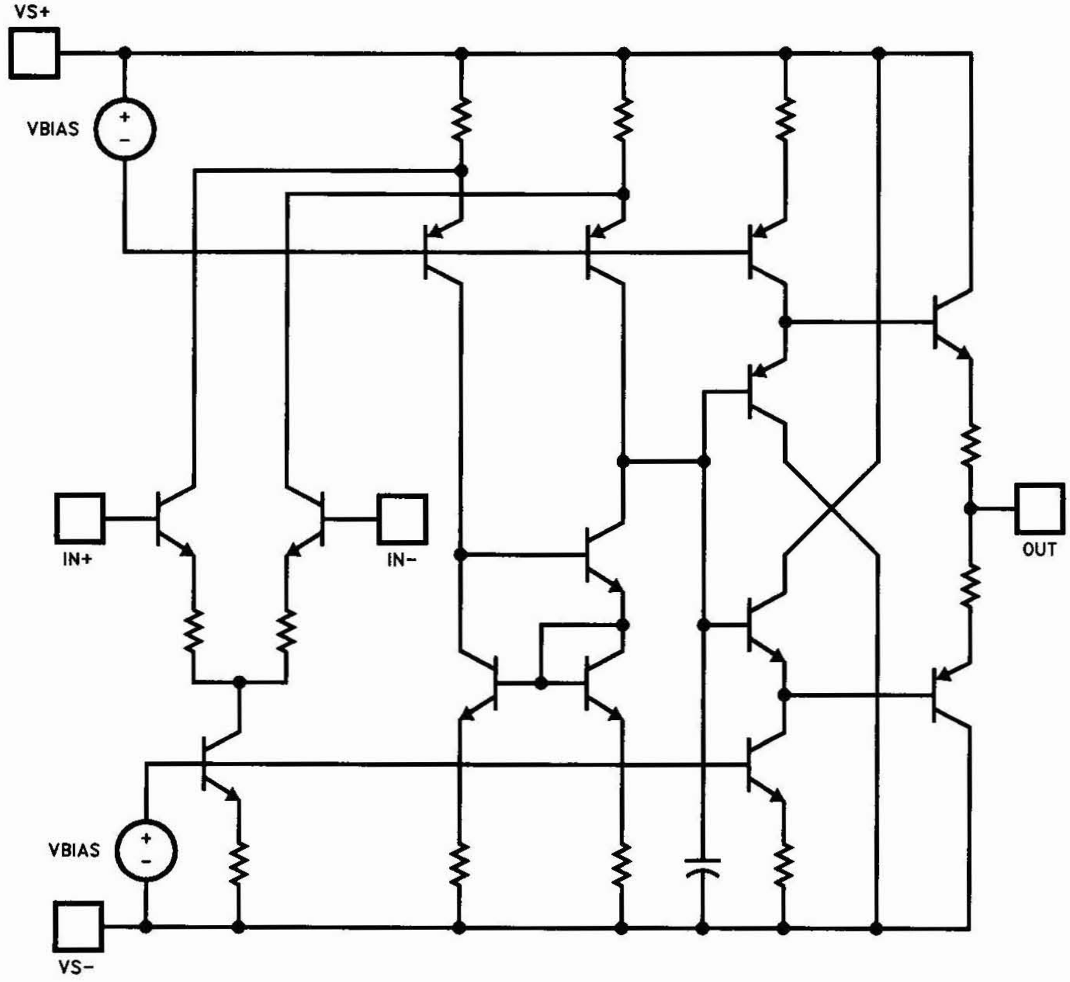


Differential Gain and Phase vs Number of 150Ω Loads at 30 MHz



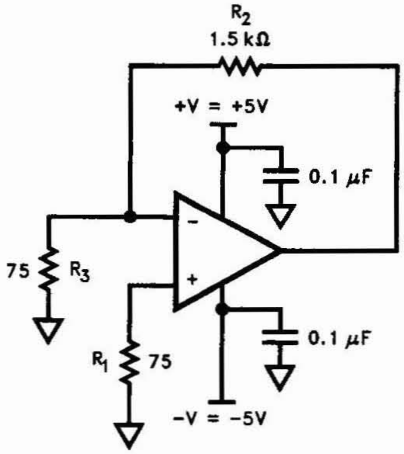
2074-6

Equivalent Circuit


VS+
VBIAS
IN+
IN−
OUT
VBIAS
VS−

2074-7

Burn-In Circuit


R2
1.5 kΩ
+V = +5V
0.1 μF
−
+
75
R3
R1
75
0.1 μF
−V = −5V

2074-8

All Packages Use The Same Schematic

Applications Information

Product Description

The EL2074 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2074 uses a classical voltage-feedback topology which allows it to be used in a variety of applications requiring a noise gain ≥2 where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2074 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2074 is an excellent choice for applications such as log amplifiers.

The EL2074 also has excellent DC specifications: 200 μV, V_{OS}, 2 μA I_B, 0.1 μA I_{OS}, and 90 dB of CMRR. These specifications allow the EL2074 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2074 is only 3.2 pA/$\sqrt{Hz}$, making it an excellent choice for high-sensitivity transimpedance amplifier configurations.

Gain-Bandwidth Product

The EL2074 has a gain-bandwidth product of 400 MHz. For gains greater than 8, its closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 8, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2074 has a −3 dB bandwidth of 400 MHz at a gain of +2, dropping to 200 MHz at a gain of +4. It is important to note that the EL2074 has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2074 in a gain of +2 only exhibits 1 dB of peaking with a 100Ω load.

Parasitic Capacitances and Stability

When used in positive-gain configurations, the EL2074 can be quite sensitive to parasitic capacitances at the inverting input, especially with values ≥250Ω for the gain resistor. The problem stems from the feedback and gain resistance in conjunction with the approximately 3pF of board-related parasitic capacitance from the inverting input to ground. Assuming a gain-of-2 configuration with Rf = Rg = 250Ω, a feedback pole occurs at 424 MHz, which is equivalent to a zero in the forward path at the same frequency. This zero reduces stability by reducing the effective phase-margin from about 50° to about 30°.

A common solution to this problem is to add an additional capacitor from the inverting input to the output. This capacitor, in conjunction with the parasitic capacitance, maintains a constant voltage-divider between the output and the inverting input. This technique is used for AC testing of the EL2074. A 3pF capacitor is placed in parallel with the feedback resistor for all AC tests. When this capacitor is used, it is also possible to increase the resistance values of the feedback and gain resistors without loss of stability, resulting in less loading of the EL2074 from the feedback network.

Video Performance

An industry-standard method of measuring the video distortion of a component such as the EL2074 is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC, 4.43 MHz for PAL, or 30 MHz for HDTV. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

Applications Information — Contd.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2074 has been designed to be among the best video amplifiers in the marketplace today. It has been thoroughly characterized for video performance in the topology described above, and the results have been included as minimum dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2074 exhibits dG and dP of only 0.01% and 0.015° at NTSC and PAL. Because dG and dP vary with different DC offsets, the superior video performance of the EL2074 has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The excellent output drive capability of the EL2074 allows it to drive up to 4 back-terminated loads with excellent video performance. With 4 150Ω loads, dG and dP are only 0.15% and 0.08° at NTSC and PAL. For more information, refer to the curves for Video Performance vs Number of 150Ω Loads.

Output Drive Capability

The EL2074 has been optimized to drive 50Ω and 75Ω loads. It can easily drive 6 V_{PP} into a 50Ω load. This high output drive capability makes the EL2074 an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2074 remains a minimum of 50 mA at low temperatures. The EL2074 is current-limited at the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

Although the EL2074 has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10 pF should be buffered with a series resistor (Rs) to isolate the load capacitance from the amplifier output. A curve of recommended Rs vs Cload has been included for reference. Values of Rs were chosen to maximize resulting bandwidth without peaking.

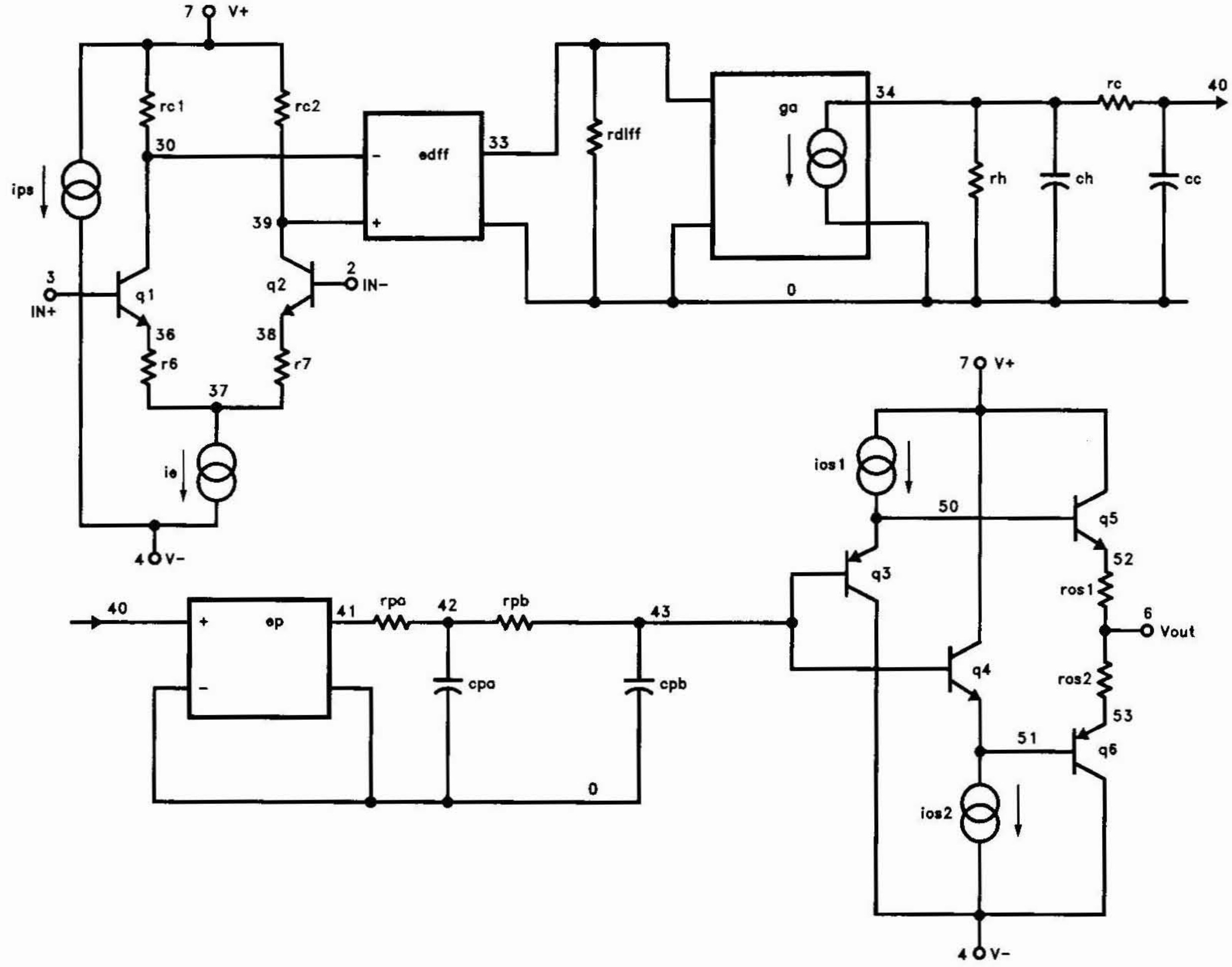
Printed-Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1 μF–10 μF tantalum capacitor is recommended in parallel with a 0.01 μF ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2074 directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.

EL2074 Macromodel

```
*
* Connections:                     +input
*                                  | -input
*                                  | | +Vsupply
*                                  | | | -Vsupply
*                                  | | | | output
*                                  | | | | |
.subckt M2074                      3 2 7 4 6
*
*Input Stage
*
ie 37 4 1 mA
r6 36 37 125
r7 38 37 125
rc1 7 30 200
rc2 7 39 200
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 1
rdiff 33 0 1 Meg
*
* Compensation Section
*
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 0.8 pF
rc 34 40 50
cc 40 0 0.05 pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 150
cpa 42 0 0.5 pF
rpb 42 43 50
cpb 43 0 0.5 pF
*
* Output Stage
*
ios1 7 50 3.0 mA
ios2 51 4 3.0 mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 2
ros2 6 53 2
*
Power Supply Current
*
ips 7 4 11.4 mA
*
Models
*
.model qna npn(is=800e-18 bf=170 tf=0.2 ns)
.model qn  npn(is=810e-18 bf=200 tf=0.2 ns)
.model qp  pnp(is=800e-18 bf=200 tf=0.2 ns)
.ends
```

EL2074 Macromodel — Contd.


7 V+
rc1
rc2
30
ips
39
3
IN+
q1
q2
2
IN−
36
38
r6
r7
37
ie
4 V−
−
+
ediff
33
rdiff
ga
34
rh
ch
rc
40
cc
0
7 V+
ios1
50
q5
52
q3
ros1
6
Vout
40
+
ep
−
41
rpa
42
rpb
43
cpa
cpb
0
q4
ros2
53
51
q6
ios2
4 V−

2074-9

elantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2075C

2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Features

- 2 GHz gain-bandwidth product
- Gain-of-10 stable
- Conventional voltage-feedback topology
- Low offset voltage = 200 μV
- Low bias current = 2 μA
- Low offset current = 0.1 μA
- Output current = 50 mA over temperature
- Fast settling = 13 ns to 0.1%

Applications

- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2075CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2075CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

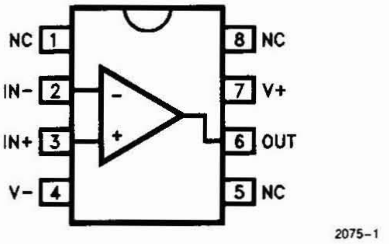
The EL2075 is a precision voltage-feedback amplifier featuring a 2 GHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50 mA output current drive over temperature.

The EL2075 is gain-of-10 stable with a −3 dB bandwidth of 400 MHz at $A_V = +10$. It has a very low 200 μV of input offset voltage, only 2 μA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2075 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2075 the ideal choice for all op-amp applications at a gain of 10 or greater requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2075 an ideal amplifier for signal-processing and digitizing systems.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



January 1995 Rev D

EL2075C

2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Absolute Maximum Ratings ($T_A = 25°C$)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Common-Mode Input	$\pm V_S$
Differential Input Voltage	5V

Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO-8
Operating Temperature	0°C to +75°C
Junction Temperature	175°C
Storage Temperature	−60°C to +150°C

Note: See EL2071/EL2171 for Thermal Impedance curves.

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

$V_S = \pm 5V$, $R_L = 100\Omega$, unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL2075C	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0V	25°C		0.2	1	I	mV
			T_{MIN}, T_{MAX}			2.5	III	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)	All		8		V	µV/°C
I_B	Input Bias Current	V_{CM} = 0V	All		2	6	II	µA
I_{OS}	Input Offset Current	V_{CM} = 0V	25°C		0.1	1	I	µA
			T_{MIN}, T_{MAX}			2	III	µA
PSRR	Power Supply Rejection Ratio	(Note 2)	All	70	90		II	dB
CMRR	Common Mode Rejection Ratio	(Note 3)	All	70	90		II	dB
I_S	Supply Current—Quiescent	No Load	25°C		21	25	I	mA
			T_{MIN}, T_{MAX}			25	III	mA
R_{IN} (diff)	R_{IN} (Differential)	Open-Loop	25°C		15		V	kΩ
C_{IN} (diff)	C_{IN} (Differential)	Open-Loop	25°C		1		V	pF
R_{IN} (cm)	R_{IN} (Common-Mode)		25°C		1		V	MΩ
C_{IN} (cm)	C_{IN} (Common-Mode)		25°C		1		V	pF

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
							EL2075C	
R_{OUT}	Output Resistance		25°C		50		V	mΩ
CMIR	Common-Mode Input Range		25°C	±3	±3.5		IV	V
			T_{MIN}, T_{MAX}	±2.5			IV	V
I_{OUT}	Output Current		All	50	70		II	mA
V_{OUT}	Output Voltage Swing	No Load	All	±3.5	±4		II	V
V_{OUT} 100	Output Voltage Swing	100Ω	All	±3	±3.6		II	V
V_{OUT} 50	Output Voltage Swing	50Ω	All	±2.5	±3.4		II	V
A_{VOL} 100	Open-Loop Gain	100Ω	25°C	1000	2800		I	V/V
			T_{MIN}, T_{MAX}	800			III	V/V
A_{VOL} 50	Open-Loop Gain	50Ω	25°C	800	2300		I	V/V
			T_{MIN}, T_{MAX}	600			III	V/V
eN@ > 1 MHz	Noise Voltage 1–100 MHz		25°C		2.3		V	nV/√Hz
iN@ > 100 kHz	Noise Current 100k–100 MHz		25°C		3.2		V	pA/√Hz

Closed Loop AC Electrical Characteristics

V_S = ±5V, A_V = +20, Rf = 1500Ω, R_L = 100Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
							EL2075C	
SSBW	−3 dB Bandwidth (V_{OUT} = 0.4V_{PP})	A_V = +10	25°C		400		V	MHz
		A_V = +20	25°C	150	200		V	MHz
			T_{MIN}, T_{MAX}	125			V	MHz
		A_V = +50	25°C		40		V	MHz
GBWP	Gain-Bandwidth Product	A_V = +100	25°C		2.0		V	GHz
LSBWa	−3 dB Bandwidth	V_{OUT} = 2 V_{PP} (Note 4)	All	80	128		IV	MHz
LSBWb	−3 dB Bandwidth	V_{OUT} = 5 V_{PP} (Note 4)	All	32	50		IV	MHz
GFPL	Peaking (<50 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0	0.5	V	dB
			T_{MIN}, T_{MAX}			0.5	V	dB
GFPH	Peaking (>50 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0	1	V	dB
			T_{MIN}, T_{MAX}			1	V	dB
GFR	Rolloff (<100 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0.1	0.5	V	dB
			T_{MIN}, T_{MAX}			0.5	V	dB

Closed Loop AC Electrical Characteristics

V_S = ±5V, A_V = +20, Rf = 1500Ω, R_L = 100Ω unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL2075C	Units
LPD	Linear Phase Deviation (<100 MHz)	V_{OUT} = 0.4 V_{PP}	All		1	1.8	IV	°
PM	Phase Margin	A_V = +10	25°C		60		V	°
tr1, tf1	Rise Time, Fall Time	0.4V Step, A_V = +10	25°C		1.2		V	ns
tr2, tf2	Rise Time, Fall Time	5V Step, A_V = +10	25°C		6		V	ns
ts1	Settling to 0.1% (A_V = −20)	2V Step	25°C		13		V	ns
ts2	Settling to 0.01% (A_V = −20)	2V Step	25°C		25		V	ns
OS	Overshoot	2V Step, A_V = +10	25°C		10		V	%
SR	Slew Rate	2V Step, A_V = +10	All	500	800		IV	V/µs
DISTORTION (Note 5)								
HD2	2nd Harmonic Distortion	@ 20 MHz, A_V = +20	25°C		−40	−30	V	dBc
			T_{MIN}, T_{MAX}			−30	V	dBc
HD3	3rd Harmonic Distortion	@ 20 MHz, A_V = +20	25°C		−65	−50	V	dBc
			T_{MIN}, T_{MAX}			−50	V	dBc

Note 1: Measured from T_{MIN}, T_{MAX}.

Note 2: $\pm V_{CC}$ = ±4.5V to 5.5V.

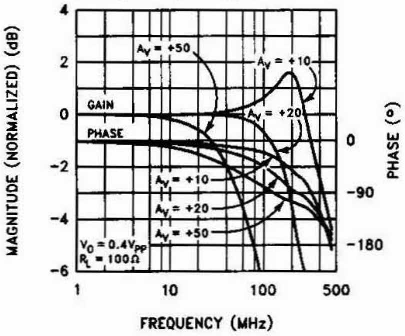
Note 3: $\pm V_{IN}$ = ±2.5V, V_{OUT} = 0V

Note 4: Large-signal bandwidth calculated using $LSBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.

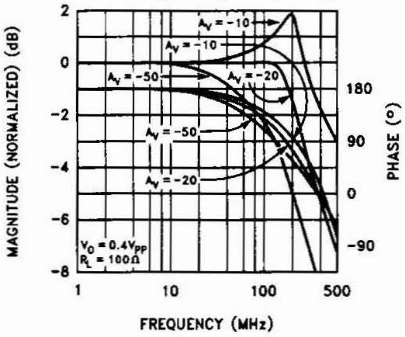
Note 5: All distortion measurements are made with V_{OUT} = 2 V_{PP}, R_L = 100Ω.

Typical Performance Curves (T_A = 25°C)

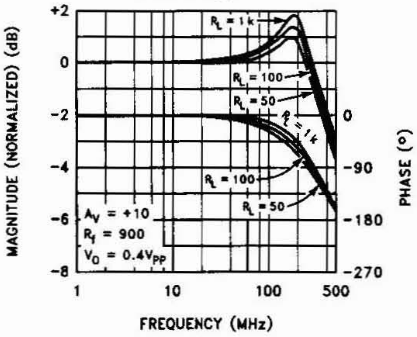
Non-Inverting Frequency Response



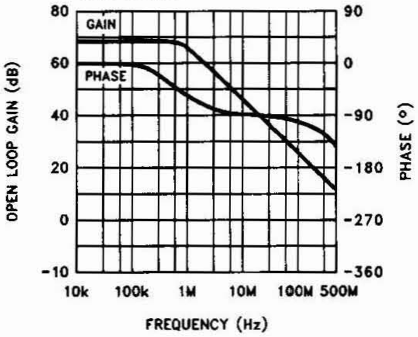
Inverting Frequency Response



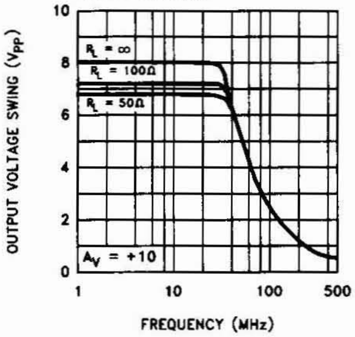
Frequency Response for Various R_Ls



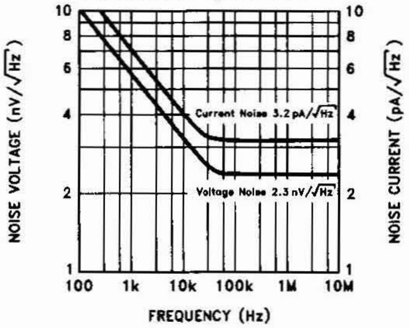
Open Loop Gain and Phase



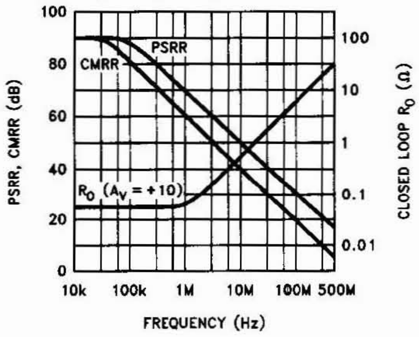
Output Voltage Swing vs Frequency



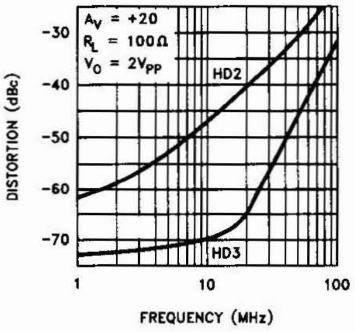
Equivalent Input Noise



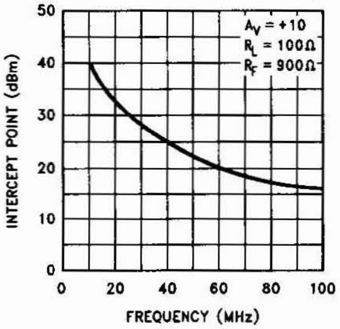
PSRR, CMRR, and Closed-Loop R_O Frequency



2nd and 3rd Harmonic Distortion vs Frequency



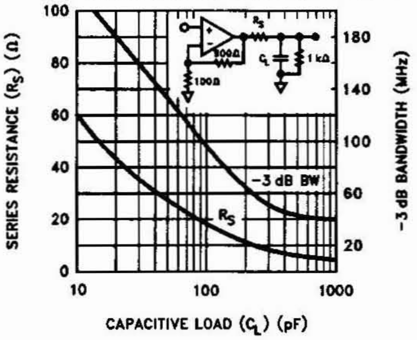
2-Tone, 3rd Order Intermodulation Intercept



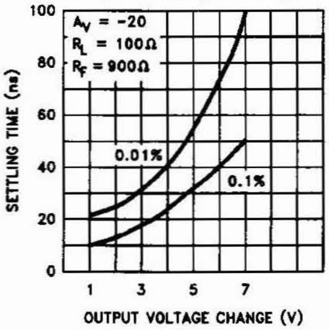
2075-2

Typical Performance Curves (T_A = 25°C unless otherwise specified) — Contd.

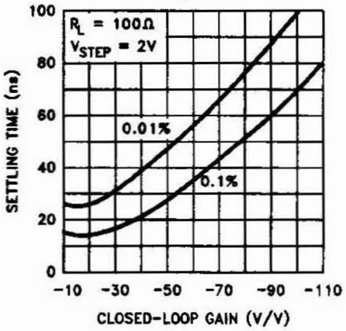
Series Resistor and Resulting Bandwidth vs Capacitive Load



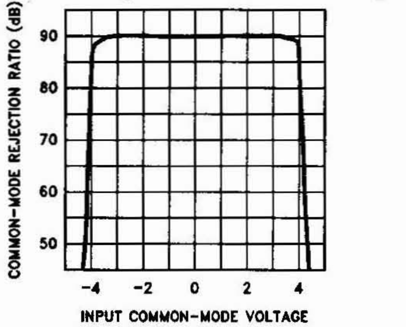
Settling Time vs Output Voltage Change



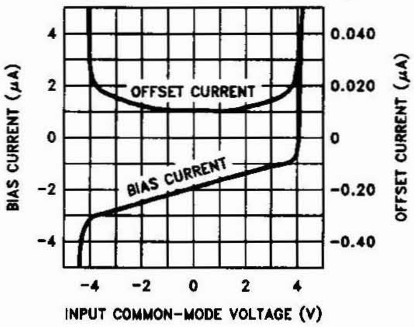
Settling Time vs Closed-Loop Gain



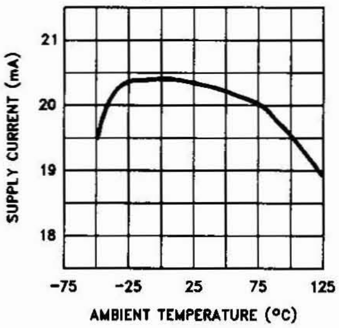
Common-Mode Rejection Ratio vs Input Common-Mode Voltage



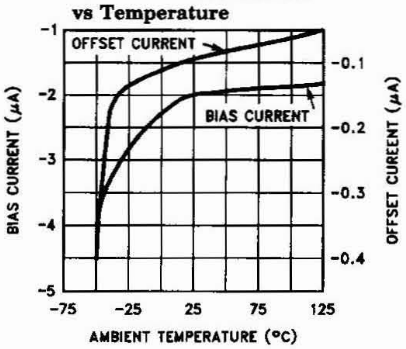
Bias and Offset Current vs Input Common-Mode Voltage



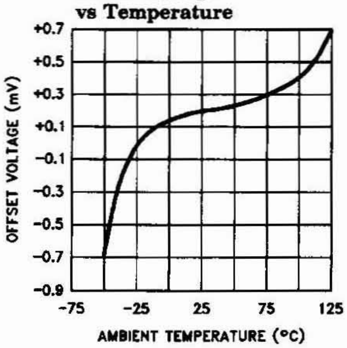
Supply Current vs Temperature



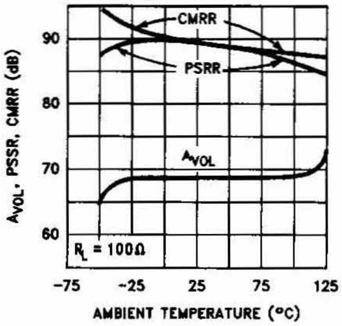
Bias and Offset Current vs Temperature



Offset Voltage vs Temperature



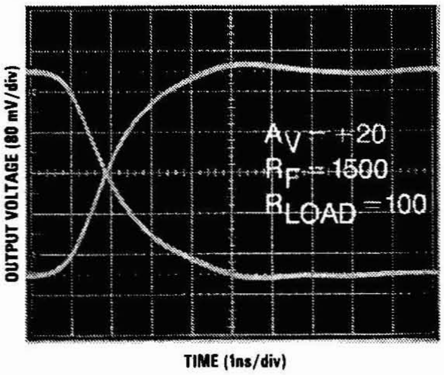
A_{VOL}, PSRR, and CMRR vs Temperature



2075-3

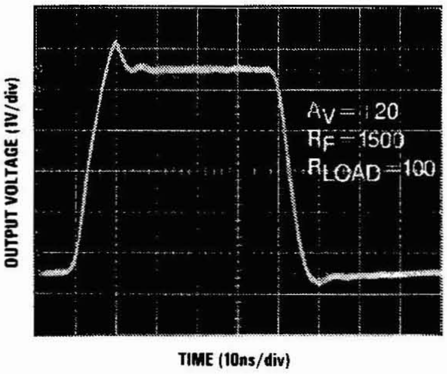
Typical Performance Curves (T$_A$ = 25°C) — Contd.

Small Signal Transient Response



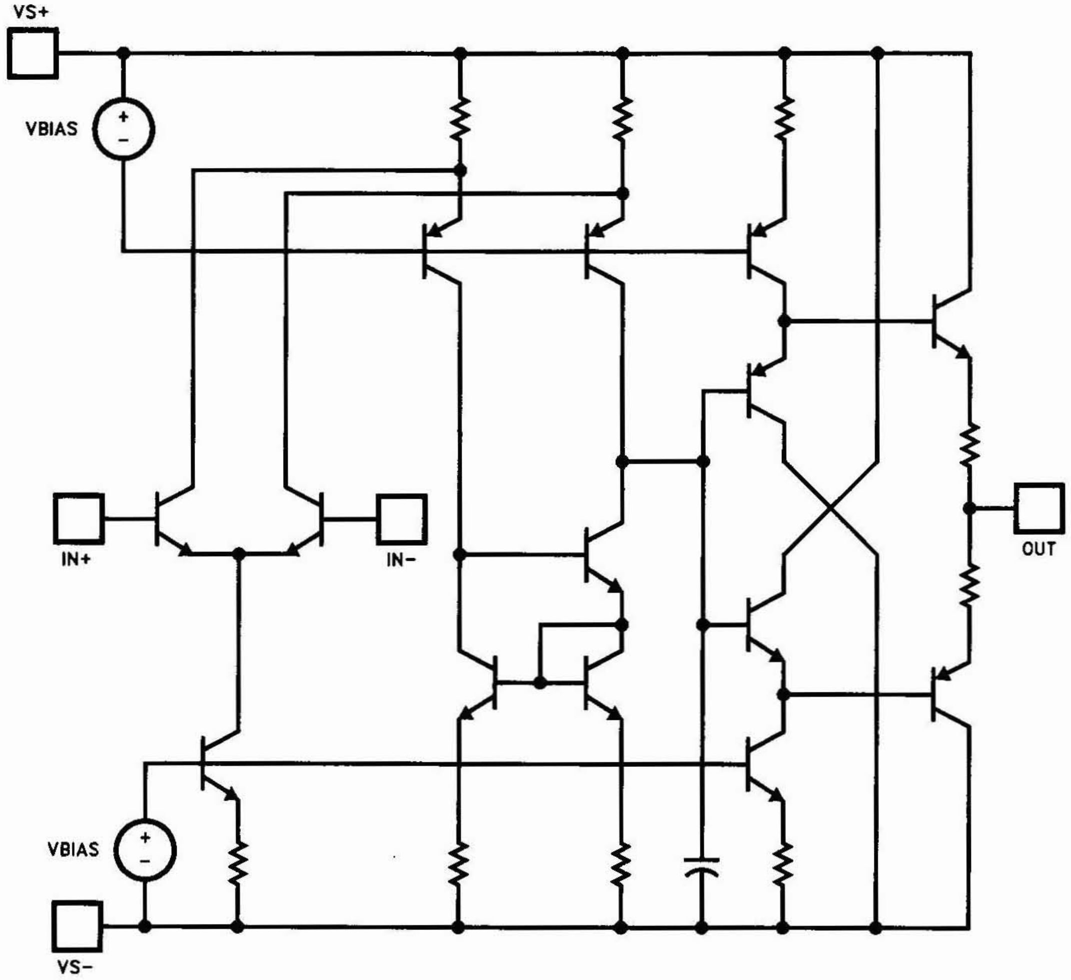
2075-4

Large Signal Transient Response



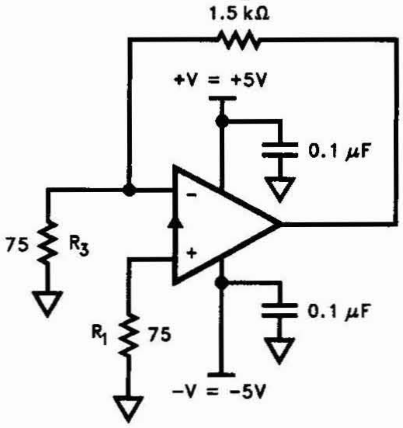
2075-5

Equivalent Circuit


VS+
VBIAS
IN+
IN-
OUT
VBIAS
VS-

2075-6

Burn-In Circuit


R2
1.5 kΩ
+V = +5V
0.1 μF
-
+
75
R3
R1
75
0.1 μF
-V = -5V

2075-7

All Packages Use The Same Schematic

EL2075C

2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Applications Information

Product Description

The EL2075 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2075 uses a classical voltage-feedback topology which allows it to be used in a variety of applications requiring a noise gain ≥ 10 where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2075 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2075 is an excellent choice for applications such as log amplifiers.

The EL2075 also has excellent DC specifications: 200 µV, V_{OS}, 2 µA I_B, 0.1 µA I_{OS}, and 90 dB of CMRR. These specifications allow the EL2075 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2075 is only 3.2 $pA/\sqrt{Hz}$, making it an excellent choice for high-sensitivity transimpedance amplifier configurations.

Gain-Bandwidth Product

The EL2075 has a gain-bandwidth product of 2 GHz. For gains greater than 40, its closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 40, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2075 has a −3 dB bandwidth of 400 MHz at a gain of +10, dropping to 200 MHz at a gain of +20. It is important to note that the EL2075 has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2075 in a gain of +10 only exhibits 1.5 dB of peaking with a 100Ω load.

Output Drive Capability

The EL2075 has been optimized to drive 50Ω and 75Ω loads. It can easily drive 6 V_{PP} into a 50Ω load. This high output drive capability makes the EL2075 an ideal choice for RF and IF applications. Furthermore, the current drive of the EL2075 remains a minimum of 50 mA at low temperatures. The EL2075 is current-limited at the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

Although the EL2075 has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10 pF should be buffered with a series resistor (Rs) to isolate the load capacitance from the amplifier output. A curve of recommended Rs vs Cload has been included for reference. Values of Rs were chosen to maximize resulting bandwidth without additionl peaking.

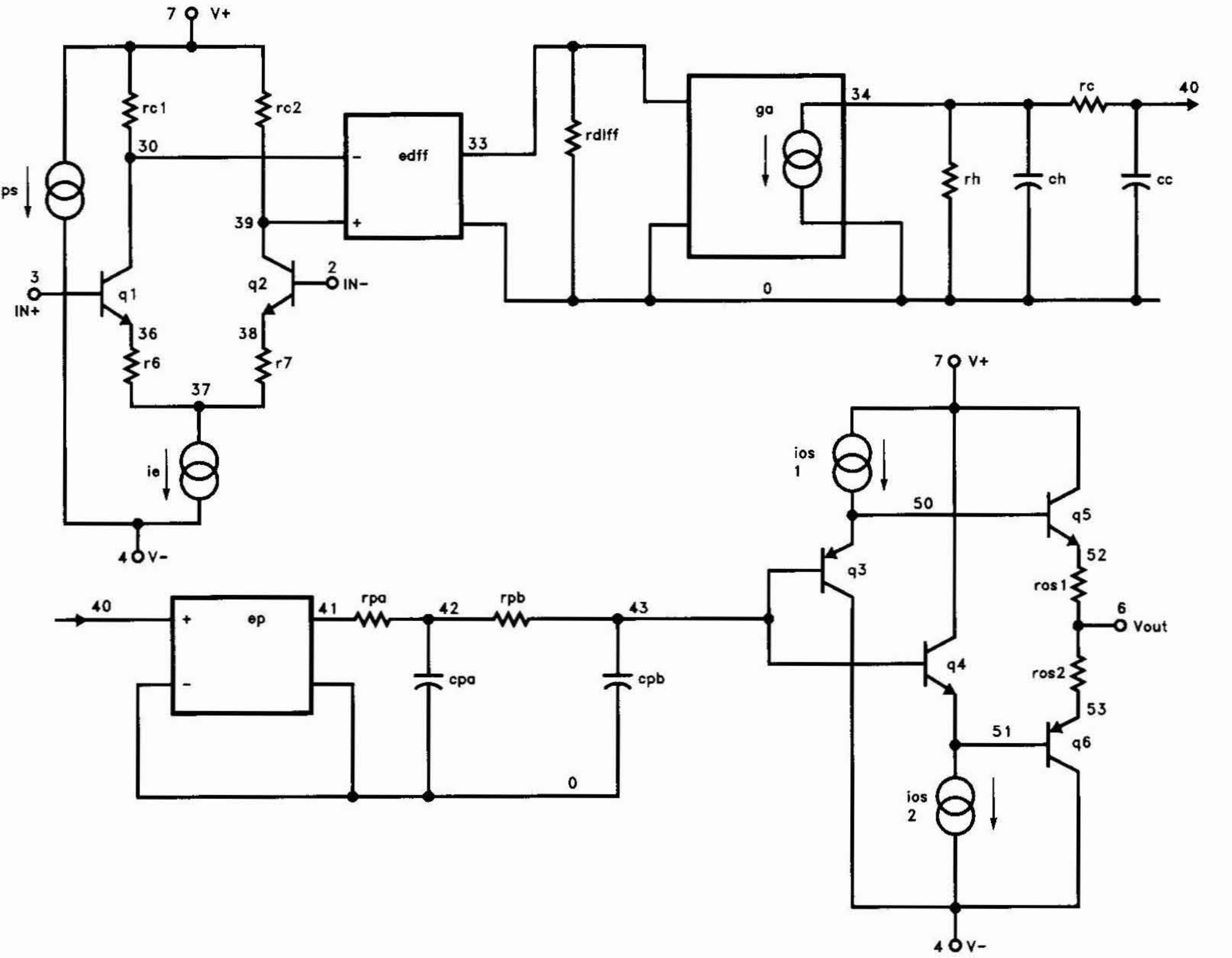
Printed-Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1 µF–10 µF tantalum capacitor is recommended in parallel with a 0.01 µF ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2075 directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.

EL2075 Macromodel

```
*
* Connections:                      +input
*                                   | -input
*                                   |  |  +Vsupply
*                                   |  |  |  -Vsupply
*                                   |  |  |  |  output
*                                   |  |  |  |  |
.subckt M2075                       3  2  7  4  6
*
*Input Stage
*
ie 37 4 1 mA
r6 36 37 15
r7 38 37 15
rc1 7 30 200
rc2 7 39 200
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 1
rdiff 33 0 1 Meg
*
* Compensation Section
*
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 0.4 pF
rc 34 40 50
cc 40 0 0.05 pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 250
cpa 42 0 0.8 pF
rpb 42 43 50
cpb 43 0 0.5 pF
*
* Output Stage
*
ios1 7 50 3.0 mA
ios2 51 4 3.0 mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 2
ros2 6 53 2
*
* Power Supply Current
*
ips 7 4 11.4 mA
*
* Models
*
.model qna npn(is=800e-18 bf=170 tf=0.2 ns)
.model qn  npn(is=810e-18 bf=200 tf=0.2 ns)
.model qp  pnp(is=800e-18 bf=200 tf=0.2 ns)
.ends
```

EL2075 Macromodel — Contd.


7 V+
rc1
rc2
30
edff
33
rdiff
ga
34
rc
40
ips
39
rh
ch
cc
3
IN+
q1
q2
2
IN−
0
36
38
r6
r7
37
ie
4 V−
7 V+
ios
1
50
q5
52
q3
ros1
40
ep
41
rpa
42
rpb
43
6
Vout
cpa
cpb
q4
ros2
53
51
q6
0
ios
2
4 V−

2075-8

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2099C
Video Distribution Amplifier

Features

- 50 MHz −3 dB bandwidth, $A_V = +2$
- Differential gain 0.03%
- Differential phase 0.05°
- Output short circuit current 800 mA
- Can drive six 75Ω double terminated cables ±11V
- Slew rate = 1000V/µs
- Wide supply voltage range ±5V to ±15V

Applications

- Video line driver
- ATE pin driver
- High speed data acquisition

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2099CT	0°C to +75°C	5-Pin TO-220	MDP0028

General Description

The EL2099C is a high speed, monolithic operational amplifier* featuring excellent video performance and high output current capability. Built using Elantec's Complementary Bipolar process, the EL2099C uses current mode feedback to achieve wide bandwidth, and is stable in unity gain configuration.

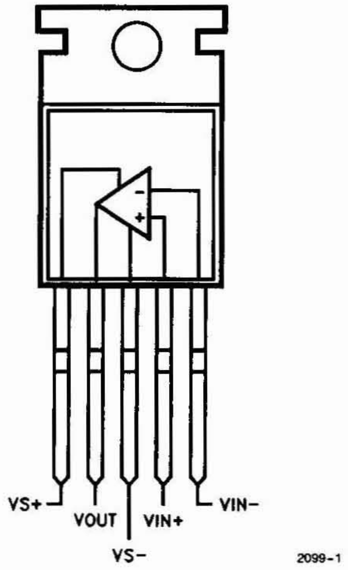
Operation from power supplies ranging from ±5V to ±15V makes the EL2099C extremely versatile. With supplies at ±15V, the EL2099C can deliver ±11V into 25Ω at slew rates of 1000V/µs. At ±5V supplies, output voltage range is ±3V into 25Ω. Its speed and output current capability make this device ideal for video line driver and automatic test equipment applications.

Differential Gain and Phase of the EL2099C are 0.03% and 0.05° respectively, and −3 dB bandwidth is 50 MHz. These features make the EL2099C especially well suited for video distribution applications.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

5-Pin TO-220



Manufactured under U.S. Patent Nos. 5,179,355, 4,893,091, U.K. Patent No. 2261786.

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+33V	Internal Power Dissipation	See Curves
Voltage at V_S+	+16.5V	Operating Ambient Temperature Range	0°C to +75°C
Voltage at V_S-	−16.5V	Operating Junction Temperature	150°C
Voltage between V_{IN+} and V_{IN-}	±6V	Storage Temperature Range	−65°C to +150°C
Current into V_{IN+} or V_{IN-}	±10 mA		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 25Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	25°C		5	20	I	mV
		T_{MIN}, T_{MAX}			25	IV	mV
TC V_{OS}	Average Offset Voltage Drift	Full		20		V	μV/°C
$+I_{IN}$	+ Input Current	25°C		5	20	I	μA
		T_{MIN}, T_{MAX}			30	IV	μA
$-I_{IN}$	− Input Current	25°C		8	35	I	μA
		T_{MIN}, T_{MAX}			50	IV	μA
CMRR	Common Mode Rejection Ratio (Note 1)	25°C	50	60		I	dB
PSRR	Power Supply Rejection Ratio (Note 2)	25°C	60	70		I	dB
R_{OL}	Transimpedance	25°C	85	140		I	kΩ
$+R_{IN}$	+ Input Resistance (Note 3)	25°C	700	1000		I	kΩ
		T_{MIN}, T_{MAX}	600			IV	kΩ
$+C_{IN}$	+ Input Capacitance	25°C		3		V	pF
CMIR	Common Mode Input Range	25°C		±12.5		V	V

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 15V$, $R_L = 25\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing $V_S = \pm 15V$	25°C	±9	±11		I	V
	Output Voltage Swing $V_S = \pm 5V$	25°C	±2.4	±3.0		I	V
I_{OUT}	Output Current	25°C	360	440		I	mA
I_{SC}	Output Short-Circuit Current	25°C	600	800		I	mA
		T_{MIN}, T_{MAX}		800		V	mA
I_S	Supply Current	25°C		32	45	I	mA

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +2$, $R_F = 510\Omega$, $R_L = 25\Omega$, $T_A = 25°C$ unless otherwise specified

Paremeter	Description	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Notes 4, 7)	500	1000		IV	V/μs
BW	−3 dB Bandwidth (Note 7)		50		V	MHz
Peaking	(Note 7)		0.3		V	dB
t_r, t_f	Rise Time, Fall Time (Notes 5, 7)		7		V	ns
dG	Differential Gain; DC Input Offset from 0V through +0.714V, AC Amplitude 286 mV_{p-p}, f = 3.58 MHz (Notes 6, 7)		0.03		V	%
dP	Differential Phase; DC Input Offset from 0V through +0.714V, AC Amplitude 286 mV_{p-p}, f = 3.58 MHz (Notes 6, 7)		0.05		V	deg. (°)

Note 1: The input is moved from −10V to +10V.

Note 2: The supplies are moved from ±5V to ±15V.

Note 3: $V_{IN} = \pm 5V$. See typical performance curve for larger values of V_{IN}.

Note 4: Slew Rate is with V_{OUT} from +5V to −5V and measured at 20% and 80%.

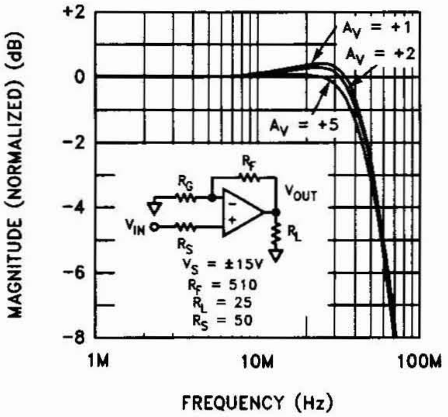
Note 5: Rise and Fall Times are with V_{OUT} between −0.5V and +0.5V and measured at 10% and 90%.

Note 6: See typical performance curves for other conditions.

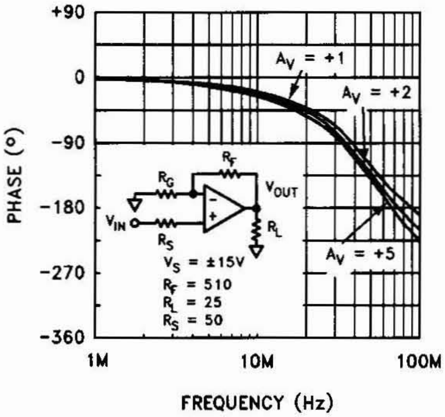
Note 7: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

Typical Performance Curves ($T_A = 25°C, R_L = 25\Omega, A_V = +2, R_F = 510$ unless otherwise specified)

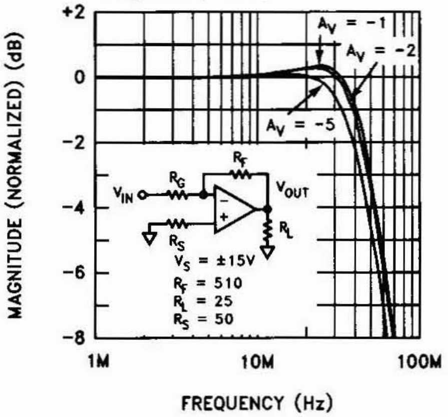
Non-Inverting Frequency Response (GAIN)



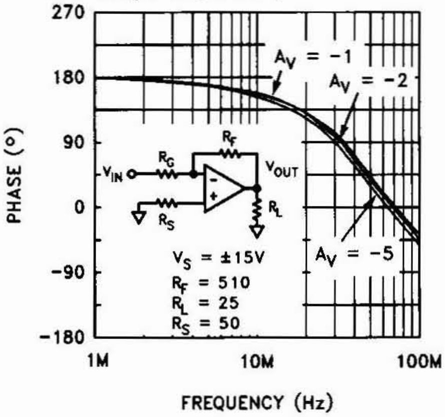
Non-Inverting Frequency Response (PHASE)



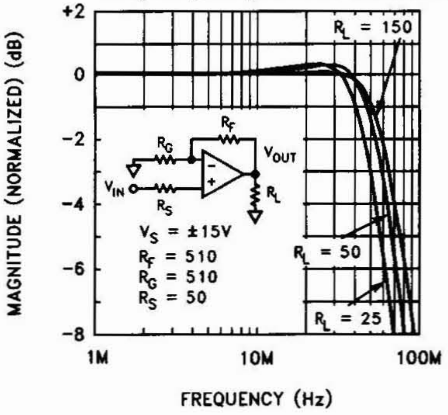
Inverting Frequency Response (GAIN)



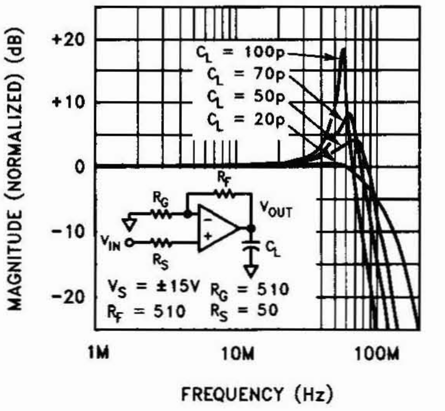
Inverting Frequency Response (PHASE)



Frequency Response for Various R_L



Frequency Response for Various C_L

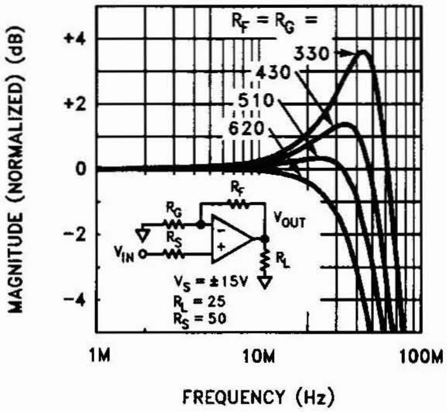


2099-2

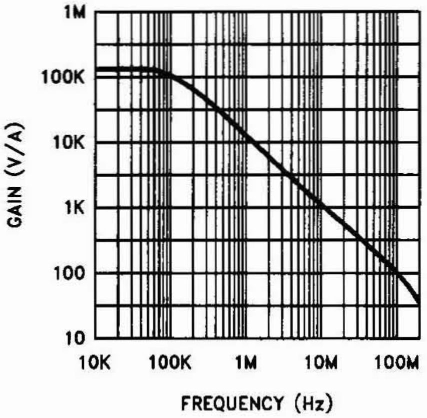
Typical Performance Curves

(T_A = 25°C, R_L = 25Ω, A_V = +2, R_F = 510 unless otherwise specified) — Contd.

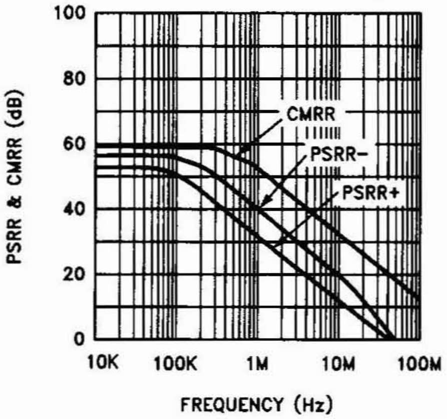
Frequency Response for Various R_F & R_G



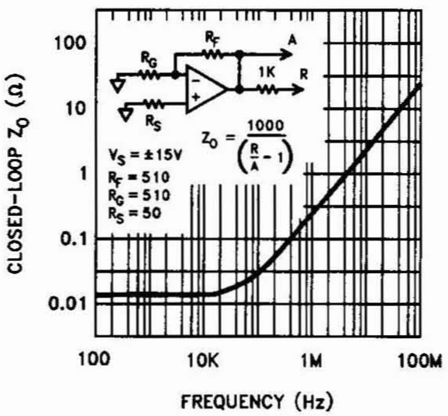
Transimpedance (R_{OL})



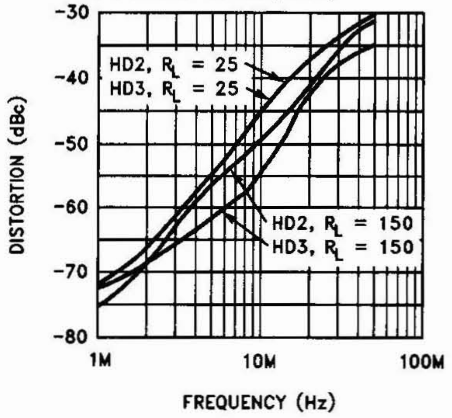
PSRR & CMRR vs Frequency



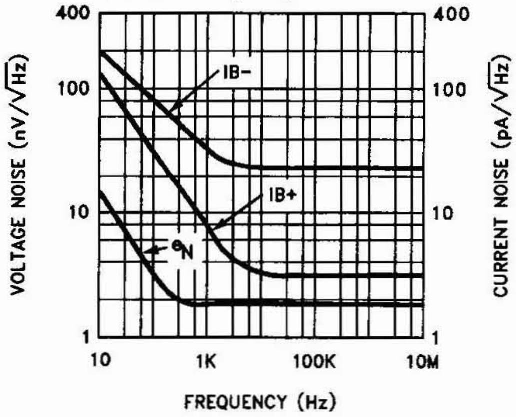
Closed-Loop Output Impedance vs Frequency



2nd and 3rd Harmonic Distortion vs Frequency



Voltage and Current Noise vs Frequency

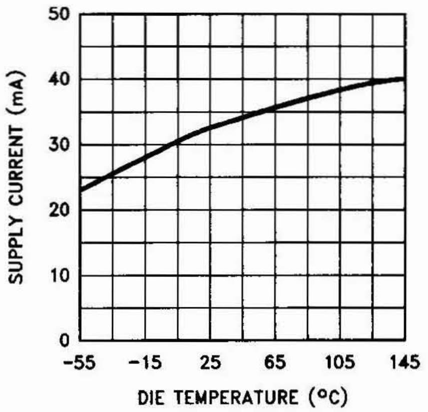


2099-3

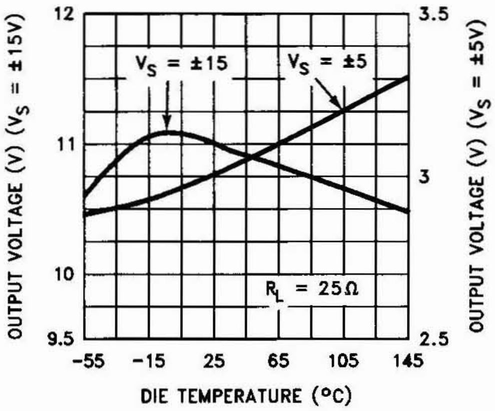
Typical Performance Curves

(T_A = 25°C, R_L = 25Ω, A_V = +2, R_F = 510 unless otherwise specified) — **Contd.**

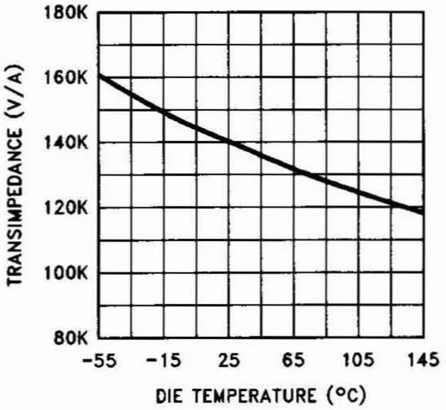
Supply Current vs Die Temperature



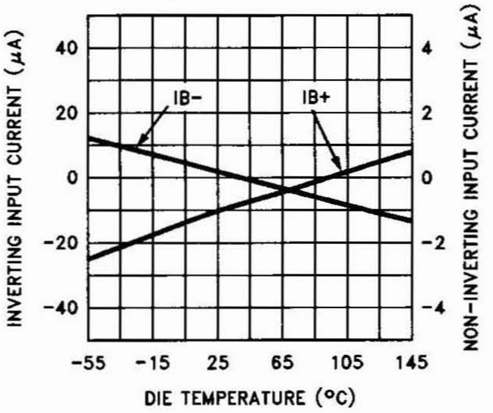
Output Voltage vs Die Temperature



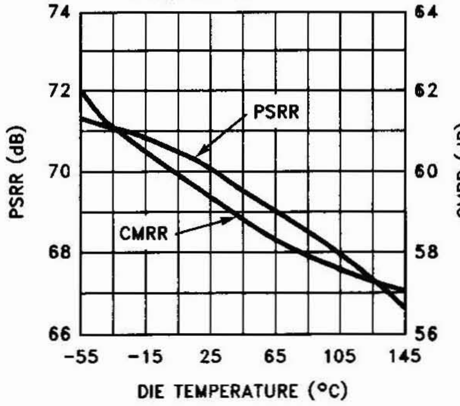
Transimpedance (R_{OL}) vs Die Temperature



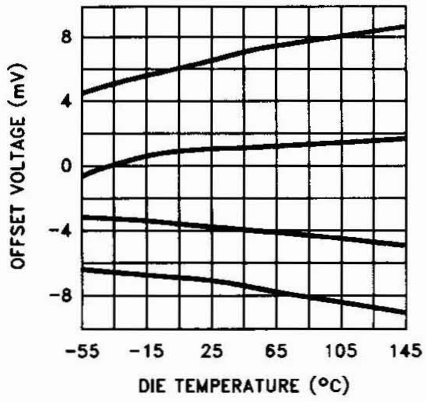
Input Current vs Die Temperature



PSRR & CMRR vs Die Temperature



Offset Voltage vs Die Temperature (4 Samples)

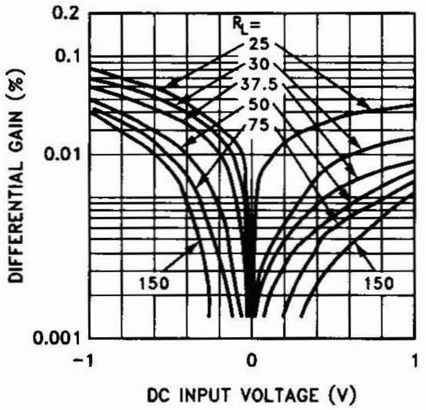


2099-4

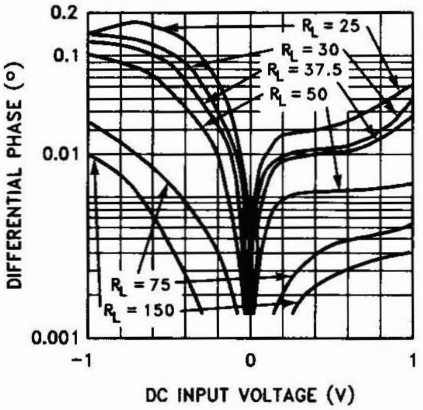
Typical Performance Curves

(T$_A$ = 25°C, R$_L$ = 25Ω, A$_V$ = +2, R$_F$ = 510 unless otherwise specified) — Contd.

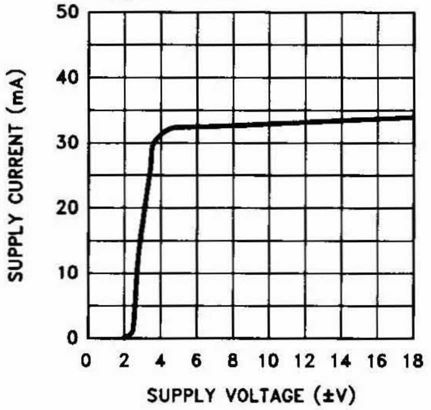
Differential Gain vs DC Input Voltage for Various R$_L$s



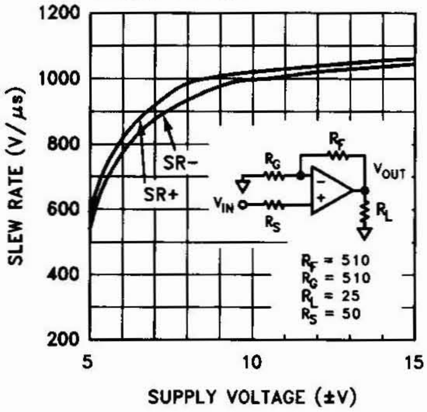
Differential Phase vs DC Input Voltage for Various R$_L$s



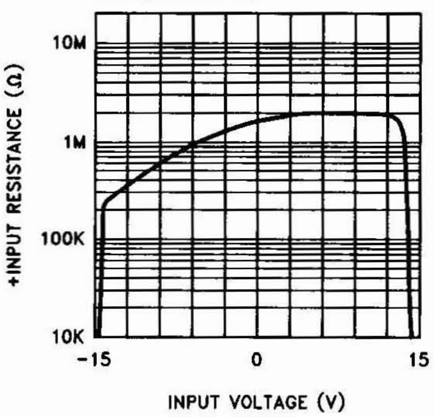
Supply Current vs Supply Voltage



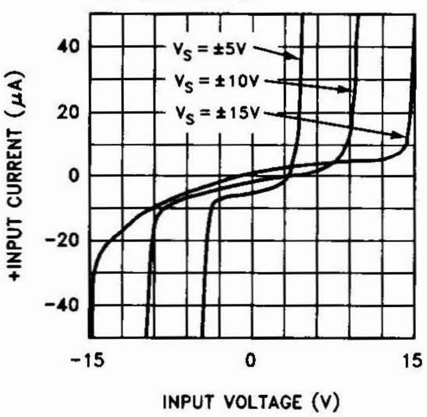
Slew Rate vs Supply Voltage



+Input Resistance vs Input Voltage



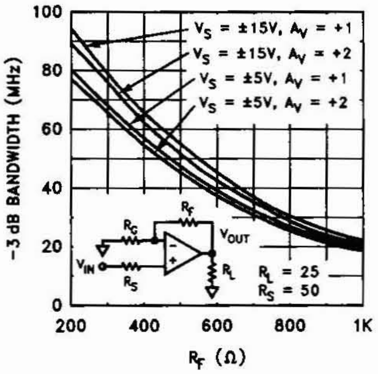
+Input Bias Current vs Input Voltage



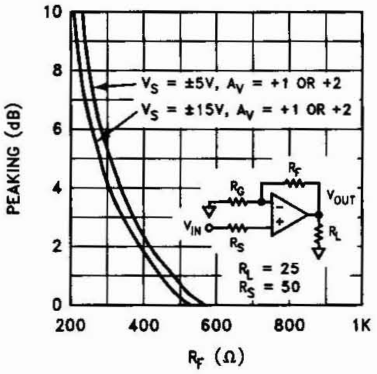
2099-5

Typical Performance Curves

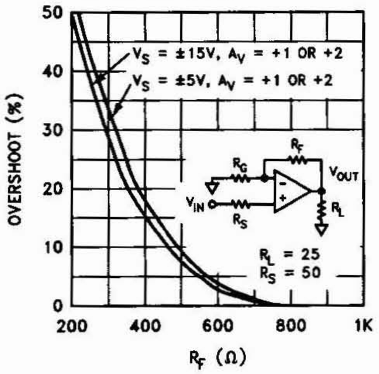
($T_A = 25°C$, $R_L = 25\Omega$, $A_V = +2$, $R_F = 510$ unless otherwise specified) — Contd.



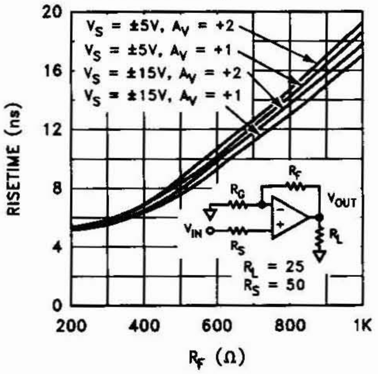
−3 dB Bandwidth vs R_F



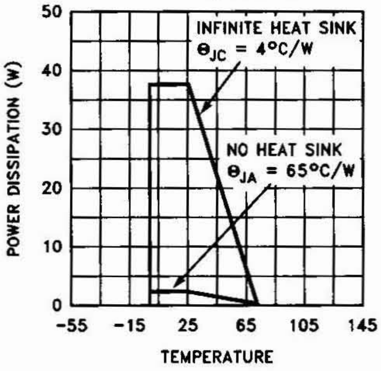
Peaking vs R_F



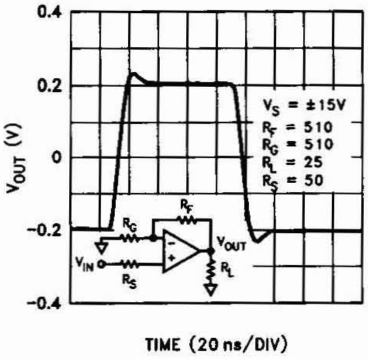
Overshoot vs R_F



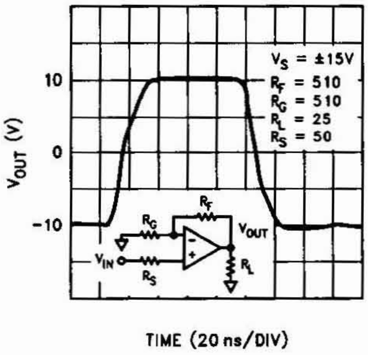
Rise Time vs R_F



5-Lead TO-220 Maximum Power Dissipation vs Ambient Temperature



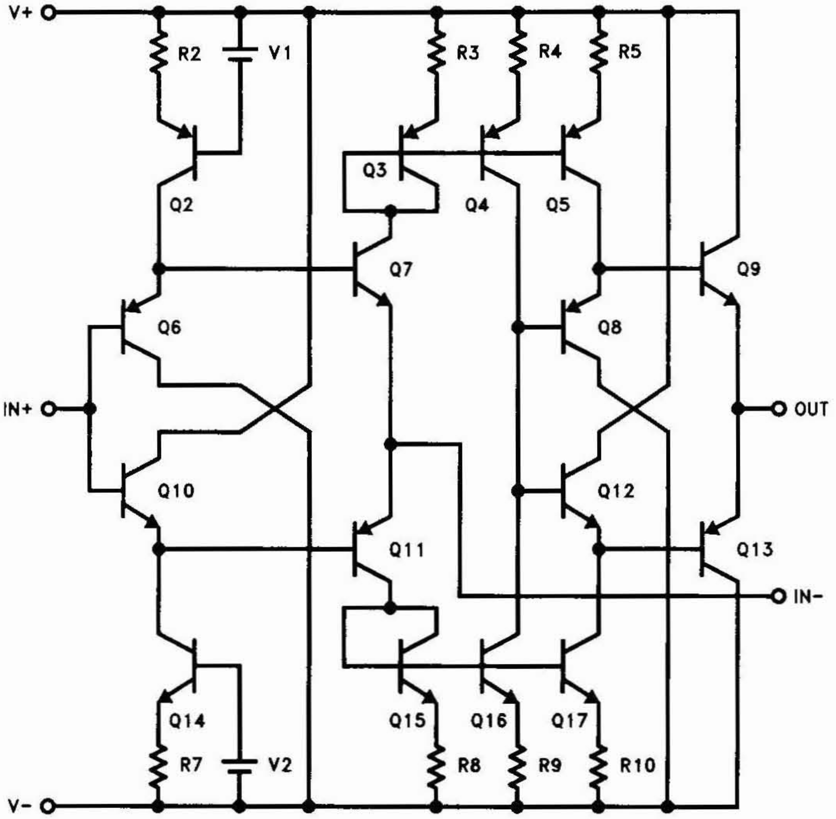
Small Signal Pulse Response



Large Signal Pulse Response

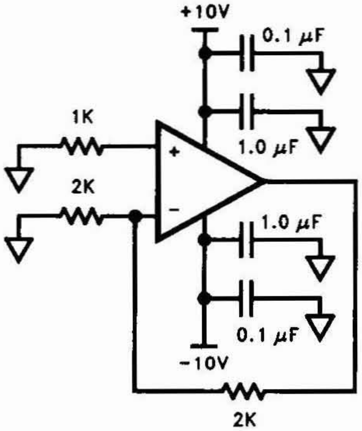
2099-6

Simplified Schematic


V+
R2
V1
R3
R4
R5
Q3
Q2
Q4
Q5
Q7
Q9
Q6
Q8
IN+
OUT
Q10
Q12
Q11
Q13
IN-
Q14
Q15
Q16
Q17
R7
V2
R8
R9
R10
V-

2099-7

Burn-In Circuit


+10V
0.1 μF
1K
1.0 μF
+
2K
–
1.0 μF
0.1 μF
–10V
2K

2099-8

EL2099C
Video Distribution Amplifier

Applications Information

Product Description

The EL2099C is a current mode feedback amplifier that has high output current drive capability. It is built using Elantec's proprietary dielectric isolation process that produces NPN and PNP complimentary transistors. The high output current can be useful to drive many standard video loads in parallel, as well as digital sync pulses that are 8V or greater.

+ Input Resistor Value

A small value resistor located in the + Input lead is necessary to keep the EL2099C from oscillating under certain conditions. A 50Ω resistor is recommended for all applications, although smaller values will work under some circumstances. All tests listed in this datasheet are performed with 50Ω in the + Input lead, as well as all typical performance curves. The 50Ω resistor along with the + Input bias current creates an additional typical Offset Voltage of only 250 μV at $T = 25°C$, and a maximum of 1.25 mV over temperature variations.

Feedback Resistor Values

The EL2099C has been designed and specified with $R_F = 510\Omega$ and $A_V = +2$. This value of feedback resistor yields extremely flat frequency response with little to no peaking. However, 3 dB bandwidth is reduced somewhat because of this. Wider bandwidth, at the expense of slight peaking, can be accomplished by reducing the value of the feedback resistor. For example, at a gain of +2, reducing the feedback resistor to 330Ω increases the −3 dB bandwidth to 70 MHz with 3 dB of peaking. Inversely, larger values of feedback resistor will cause roll off to occur at a lower frequency. There is essentially no peaking with $R_F > 510\Omega$.

Power Supplies

The EL2099C may be operated with single or split supplies as low as ±5V (10V total) to as high as ±18V (36V total). Bandwidth and slew rate are almost constant from $V_S = \pm 10V$ to ±18V, and decrease slightly as supplies are reduced to ±5V, as shown in the characteristic curves. It is not necessary to use equal value split supplies. For example, −5V and −12V would be fine for 0V to 1V video signals.

Good power supply bypassing should be used to reduce the risk of oscillation. A 1 μF to 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor is recommended for bypassing each supply pin. They should be kept as close as possible to the device pins.

Due to the internal construction of the TO-220 package, the tab of the EL2099C is connected to the V_{S-} pin. Therefore, care must be taken to avoid connecting the tab to the ground plane of the system.

Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input, which is sensitive to stray capacitance. This implies keeping the ground plane away from this pin. Metal film and carbon resistors are both acceptable, while use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance.

Driving Cables and Capacitive Loads

The EL2099C was designed with driving multiple coaxial cables in mind. With 440 mA of output drive and low output impedance, driving six 75Ω double terminated coaxial cables to ±11V with one EL2099C is practical.

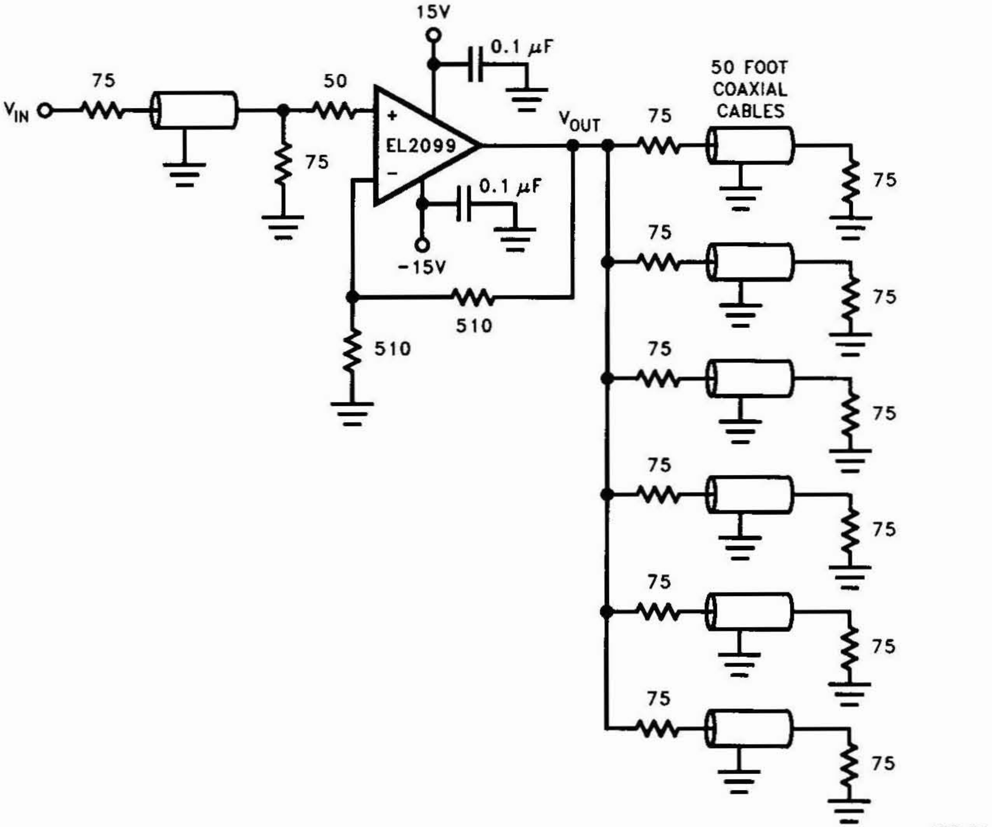
When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2099C from the capacitive cable and allow extensive capacitive drive. For a discussion on some of the other ways to drive cables, see the application section on driving cables in the EL2003 data sheet.

Applications Information — Contd.

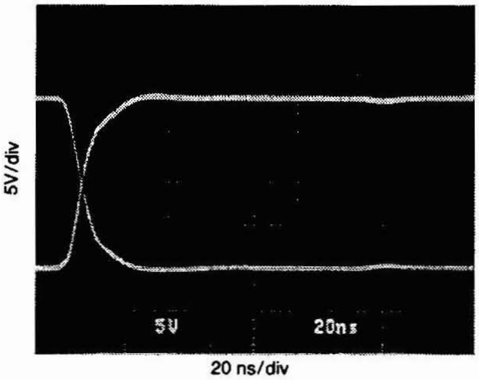
Other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking.

The schematic below shows the EL2099C driving 6 double terminated cables, each of average length of 50 feet.

This represents driving an effective load of 25Ω to over ±10V. The resulting performance is shown in the scope photo. Notice that double termination results in reflection free performance.


15V
0.1 μF
V_{IN}
75
50
75
+
EL2099
−
0.1 μF
−15V
510
510
V_{OUT}
75
50 FOOT COAXIAL CABLES
75
75
75
75
75
75
75
75
75
75
75

2099-10



2099-11

EL2099 Macromodel

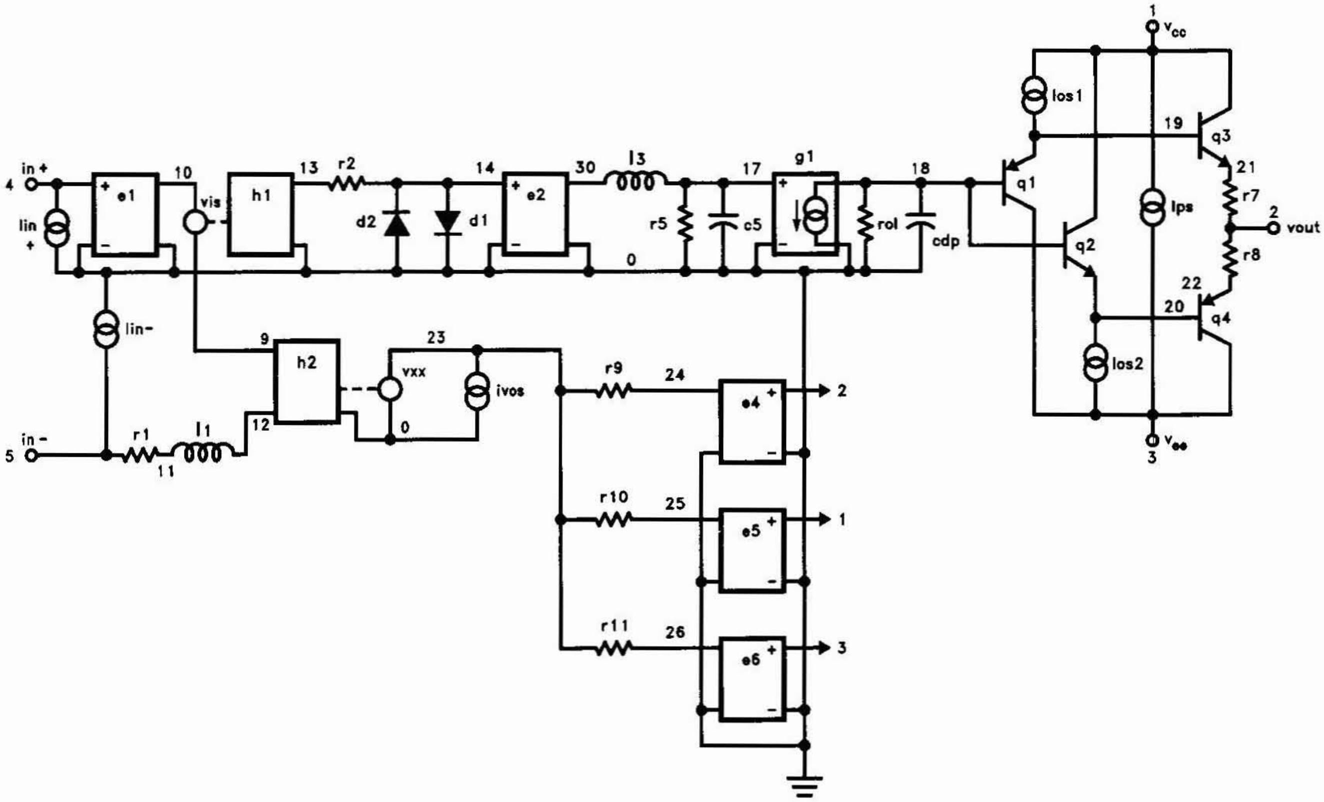
```
* Connections:    +input
*                  |      -input
*                  |       |      +Vsupply
*                  |       |       |      -Vsupply
*                  |       |       |       |      output
*                  |       |       |       |       |
.subckt M2099      4       5       1       3       2
*
* Input Stage
*
e1 10 0 4 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 5 11 50
l1 11 12 48nH
iinp 4 0 5µA
iinm 5 0 −8µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.001667
13 30 17 1.5µH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
ro1 18 0 150K
cdp 18 0 8pF
*
* Output Stage
*
q1 3 18 19 qp
q2 1 18 20 qn
q3 1 19 21 qn
q4 3 20 22 qp
r7 21 2 1
r8 22 2 1
```

EL2099 Macromodel — Contd.

```
ios1 1 19 5mA
ios2 20 3 5mA
*
* Supply Current
*
ips 1 3 19mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 2 0 1.0
e5 25 0 1 0 1.0
e6 26 0 3 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K

* Models
*
.model qn npn (is=5e-15  bf=200  tf=0.1nS)
.model qp pnp (is=5e-15  bf=200  tf=0.1nS)
.model dclamp d (is=1e-30  ibv=0.266  bv=5  n=4)
.ends
```

EL2099 Macromodel — Contd.


in +
4
Iin
+
e1
10
vis
h1
13
r2
14
d2
d1
e2
30
l3
17
g1
18
r5
c5
rol
cdp
0
Iin-
9
h2
23
vxx
ivos
12
0
in -
5
r1
l1
11
r9
24
e4
2
r10
25
e5
1
r11
26
e6
3
1
Vcc
Ios1
19
q3
q1
21
r7
2
vout
q2
Ips
r8
22
20
q4
Ios2
Vee
3

2099-9

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2120C

100 MHz Current Feedback Amplifier

Features

- Excellent differential gain and phase on ±5V to ±15V supplies
- 100 MHz −3 dB bandwidth from gains of ±1 to ±10
- 700 V/µs slew rate
- 0.1 dB flatness to 20 MHz
- Output disable in 50 ns - remains high impedance even when driven with large slew rates
- Single +5V supply operation
- AC characteristics are lot and temperature stable
- Available in small SO-8 package

Applications

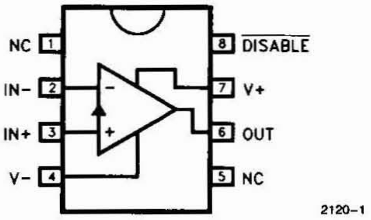
- Video gain block
- Residue amplifier
- Multiplexer
- Current to voltage converter
- Coax cable driver with gain of 2
- ADC driver

Ordering Information

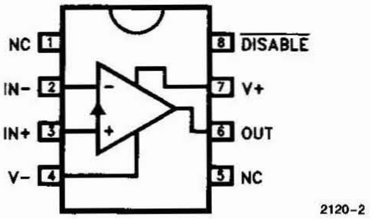
Part No.	Temp. Range	Package	Outline #
EL2120CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2120CS	0°C to +75°C	8-Lead SO	MDP0027

Connection Diagrams

P-DIP



SO



Top View

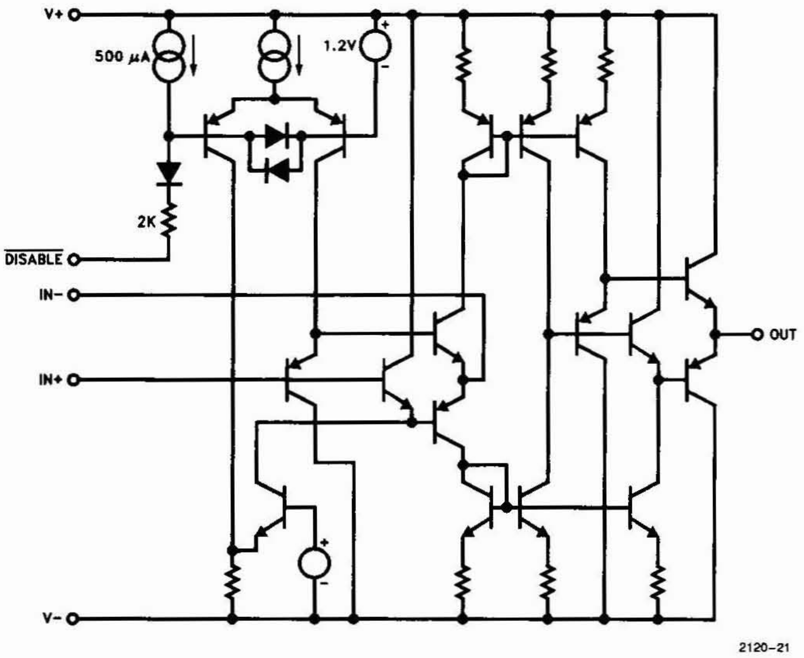
General Description

The EL2120C is a wideband current feedback amplifier optimized for video performance. Its 0.01% differential gain and 0.03 degree differential phase performance when at ±5V supplies exceeds the performance of other amplifiers running on ±15V supplies. Operating on ±8 to ±15V supplies reduces distortions to 0.01% and 0.01 degrees and below. The EL2120C can operate with supplies as low as ±2.5V or a single +5V supply.

Being a current feedback design, bandwidth is a relatively constant 100 MHz over the ±1 to ±10 gain range. The EL2120C has been optimized for flat gain over frequency and all characteristics are maintained at positive unity gain. Because the input slew rate is similar to the 700 V/µs output slew rate the part makes an excellent high-speed buffer.

The EL2120C has a superior output disable function. Time to enable or disable is 50 ns and does not change markedly with temperature. Furthermore, in disable mode the output does not draw excessive currents when driven with 1000 V/µs slew rates. The output appears as a 3 pF load when disabled.

Simplified Schematic



Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	33V
Voltage at +IN, −IN, V_{OUT}	(V−) − 0.5V to (V+) + 0.5V
Voltage between +IN and − IN	±5V
Voltage at /Disable	(V+) − 10V to (V+) + 0.5V
Current into +IN, −IN, and /Disable	±5 mA
Output Current	±50 mA
Internal Power Dissipation	See Curves
Operating Ambient Temperature Range	0° to 75°C
Operating Junction Temperature P-DIP or SO	150°C
Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V; R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	Full		4	20	II	mV
	V_S = ±15V	Full		2	25	II	mV
$\Delta V_{OS}/\Delta T$	Input Offset Drift	Full		20		V	µV/°C
I_{B+}	$+V_{IN}$ Input Bias Current	Full		5	15	II	µA
I_{B-}	$-V_{IN}$ Input Bias Current	Full		10	50	II	µA
CMRR	Common-Mode Rejection (Note 1)	Full	50	55		II	dB
−ICMR	−Input Current Common-Mode Rejection (Note 1)	Full		8	20	II	µA/V
PSRR	Power Supply Rejection (Note 2)	Full	65	80		II	dB
+IPSR	+Input Current Power Supply Rejection (Note 2)	25°C		0.03		V	µA/V
−IPSR	−Input Current Power Supply Rejection (Note 2)	Full		0.6	5	II	µA/V
R_{OL}	Transimpedance	Full	70	140		II	kΩ
A_{VOL}	Voltage Gain	Full	58	66		II	dB
$+R_{IN}$	$+V_{IN}$ Input Impedance	25°C		2		V	MΩ

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 5V$; $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{IN}	$+V_{IN}$ Range	Full	±3.0	±3.5		II	V
V_O	Output Voltage Swing	Full	±3.0	±3.5		II	V
I_{SC}	Output Short-Circuit Current	25°C		100		II	mA
$I_{O,DIS}$	Output Current, Disabled	Full		5	50	II	μA
$V_{DIS,ON}$	Disable Pin Voltage for Output Enabled	Full	(V+) − 1			II	V
$V_{DIS,OFF}$	Disable Pin Voltage for Output Disabled	Full			(V+) − 4	II	V
$I_{DIS,ON}$	Disable Pin Current for Output Enabled	Full			5	II	μA
$I_{DIS,OFF}$	Disable Pin Current for Output Disabled	Full	1.0			II	mA
I_S	Supply Current ($V_S = \pm 15V$)	Full		17	20	II	mA

Note 1: The input is moved from −3V to +3V.
Note 2: The supplies are moved from ±5V to ±15V.

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$; $A_V = +2$ ($R_F = R_G = 270\Omega$); $R_L = 150\Omega$; $C_L = 7$ pF; $C_{IN-} = 2$ pF; $T_A = 25°C$

Parameter	Description		Min	Typ	Max	Test Level	Units
SR	Slew Rate; V_{OUT} from −3V to +3V Measured at −2V and +2V	$V_S = \pm 15V$		750		V	V/μs
		$V_S = \pm 5V$		550		V	V/μs
t_S	Settling Time to 0.25% of a 0 to +10V Swing; $A_V = +1$ with $R_F = 270\Omega$, $R_G = \infty$, and $R_L = 400\Omega$			50		V	ns
BW	Bandwidth	−3 dB		95		V	MHz
		±1 dB		50		V	MHz
		±0.1 dB		16		V	MHz
BW@2.5V	Bandwidth at $V_S = \pm 2.5V$	−3 dB		75		V	MHz
		±1 dB		35		V	MHz
		±0.1 dB		11		V	MHz
Peaking				0.5		V	dB

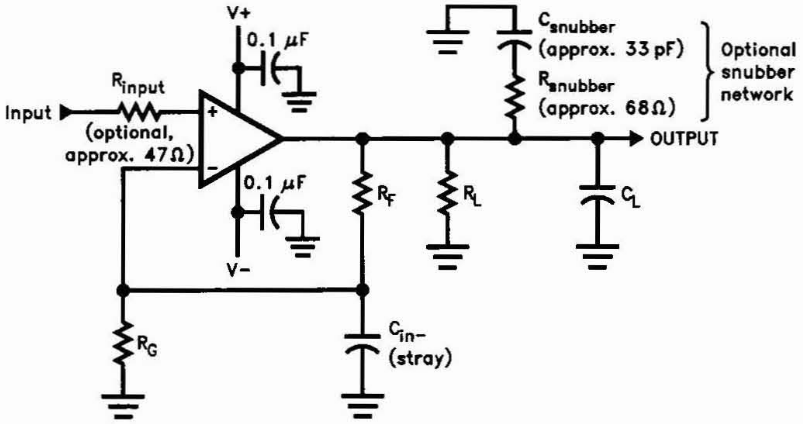
Closed Loop AC Electrical Characteristics — Contd.

$V_S = \pm 15V$; $A_V = +2$ ($R_F = R_G = 270\Omega$); $R_L = 150\Omega$; $C_L = 7$ pF; $C_{IN-} = 2$ pF; $T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level	Units
dG	Differential Gain; DC Offset from −0.7V through +0.7V, AC Amplitude 286 mVp-p					
	$V_S = \pm 15V$, f = 3.58 MHz		<0.01		V	%
	$V_S = \pm 15V$, f = 30 MHz		0.1		V	%
	$V_S = \pm 5V$, f = 3.58 MHz		0.01		V	%
dθ	Differential Phase; DC Offset from −0.7V through +0.7V, AC Amplitude 286 mVp-p					
	$V_S = \pm 15V$, f = 3.58 MHz		0.01		V	°
	$V_S = \pm 15V$, f = 30 MHz		0.1		V	°
	$V_S = \pm 5V$, f = 3.58 MHz		0.06		V	°

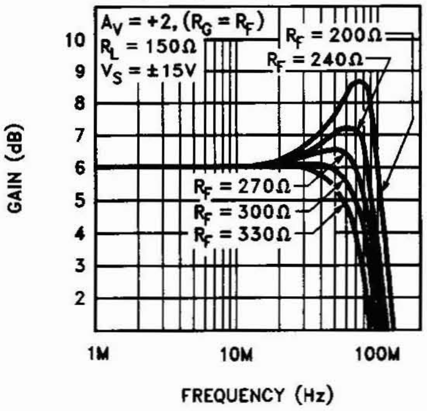
Typical Performance Curves

AC Test Circuit


V+
0.1 μF
R_input
Input
(optional, approx. 47Ω)
+
−
0.1 μF
V−
C_snubber (approx. 33 pF)
R_snubber (approx. 68Ω)
Optional snubber network
OUTPUT
R_F
R_L
C_L
R_G
C_in− (stray)

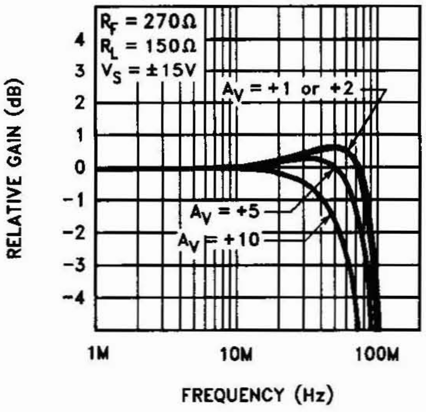
2120-3

Frequency Response vs R_F



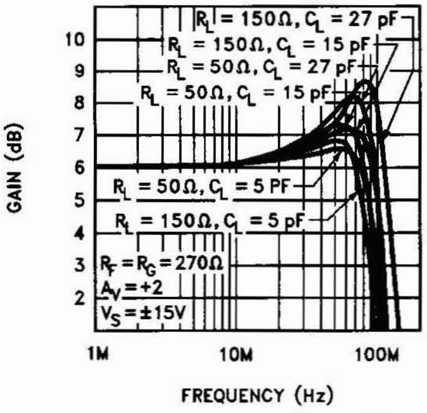
2120-4

Frequency Response vs Gain



2120-5

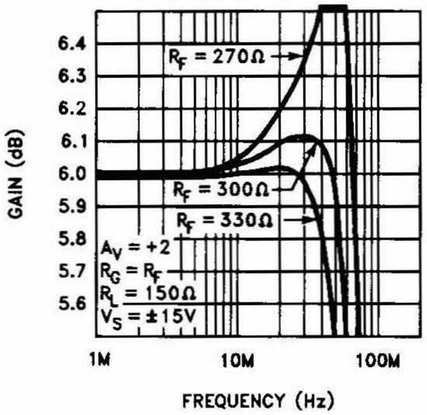
Frequency Response vs Load



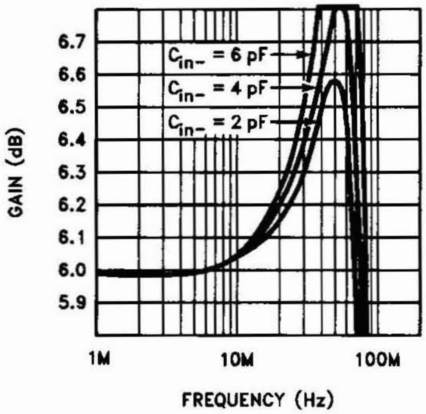
2120-6

Typical Performance Curves — Contd.

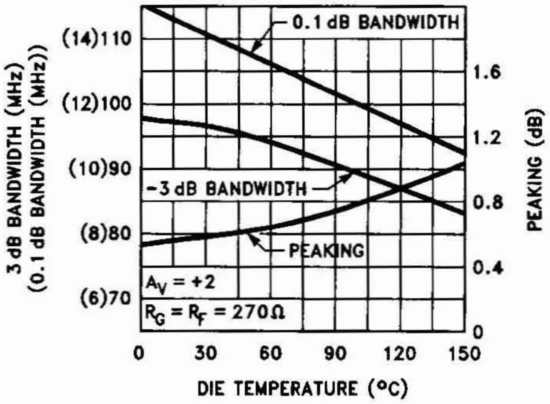
Gain Flatness vs R_F



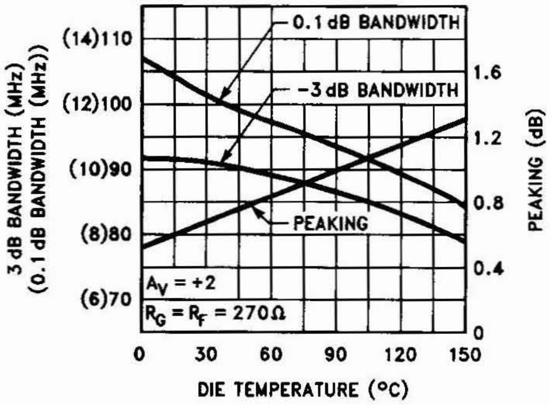
Gain Flatness vs C_{IN-}



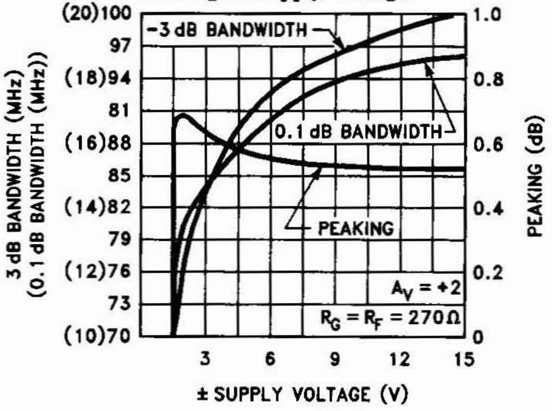
−3 dB Bandwidth, 0.1 dB Bandwidth, and Peaking vs Temperature at V_S ±15V



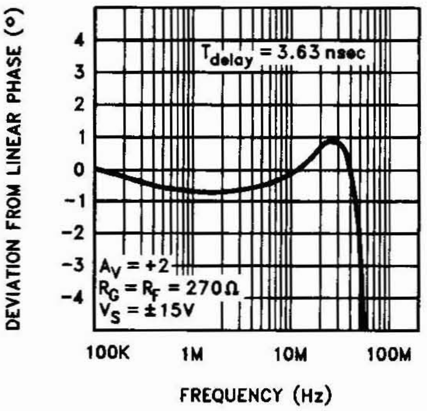
−3 dB Bandwidth, 0.1 dB Bandwidth, and Peaking vs Temperature at V_S ±5V



−3 dB Bandwidth,
0.1 dB Bandwidth, and
Peaking vs Supply Voltage



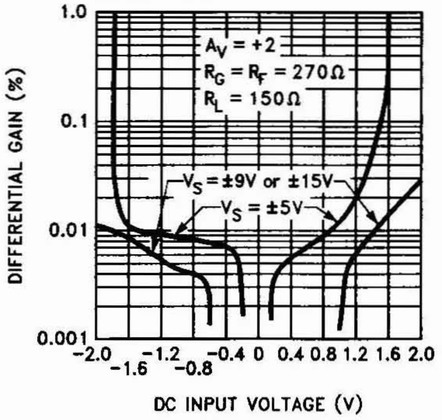
Deviation From Linear
Phase vs Frequency



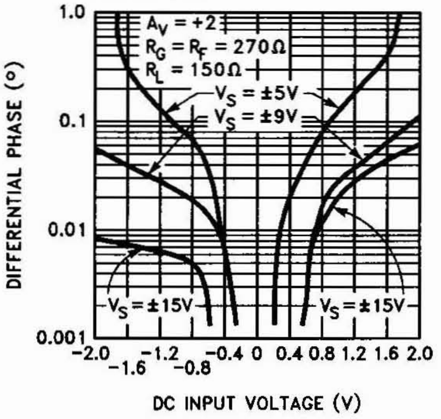
2120-7

Typical Performance Curves — Contd.

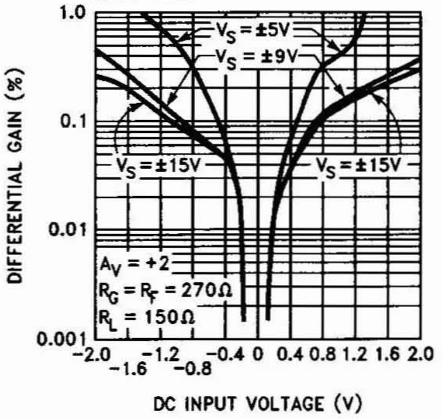
Differential Gain vs DC Input Offset at 3.58 MHz



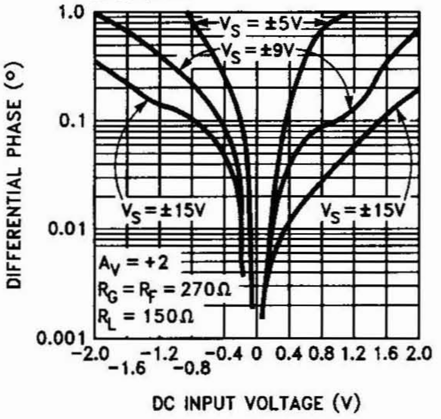
Differential Phase vs DC Input Offset at 3.58 MHz



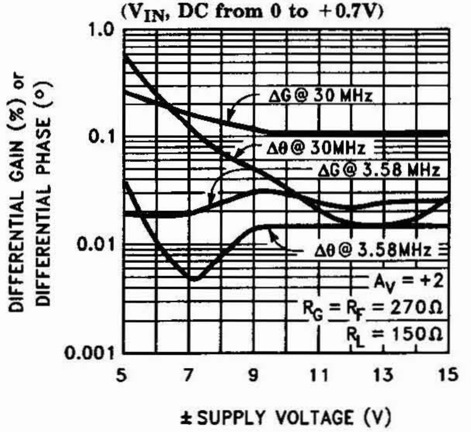
Differential Gain vs DC Input Offset at 30 MHz



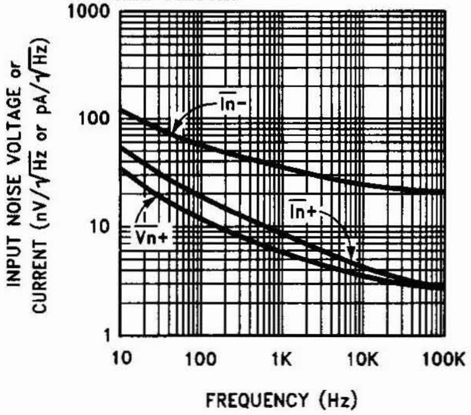
Differential Phase vs DC Input Offset at 30 MHz



Differential Gain and Phase vs Supply Voltage (V_{IN}, DC from 0 to +0.7V)



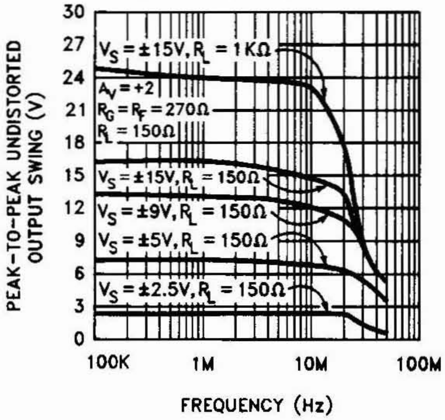
Input Noise Voltage and Current



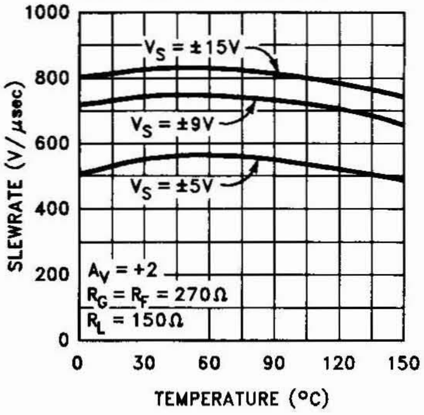
2120-8

Typical Performance Curves — Contd.

Undistorted Output Swing vs Frequency

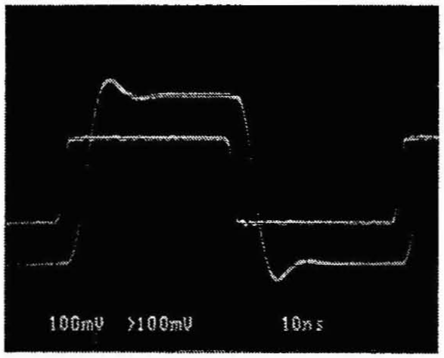


Slew Rate vs Temperature



2120-9

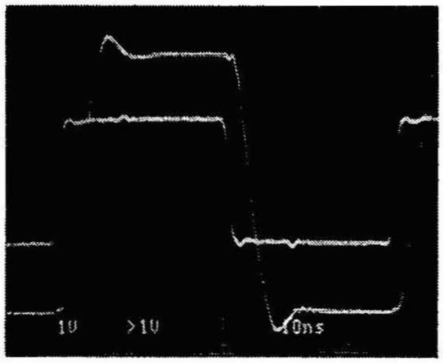
Small-Signal Transient Response



$A_V = +2, R_F = R_G = 270\Omega,$
$R_L = 150\Omega$

2120-10

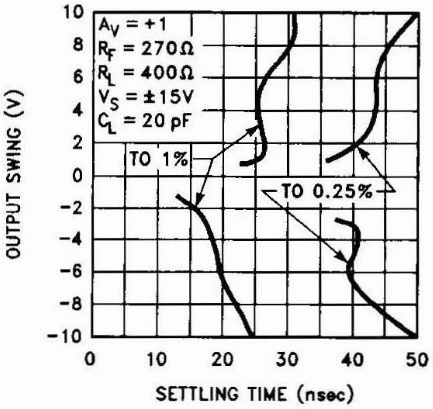
Large-Signal Transient Response



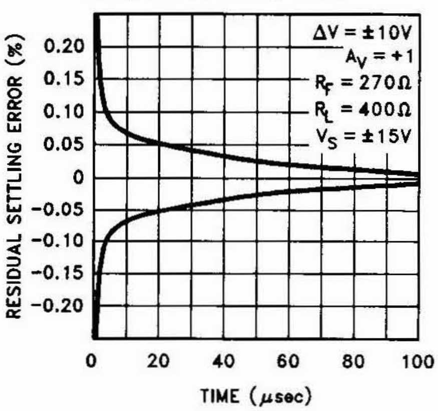
$A_V = +2, R_F = R_G = 270\Omega,$
$R_L = 150\Omega, V_S = \pm15V$

2120-11

Settling Time vs Swing



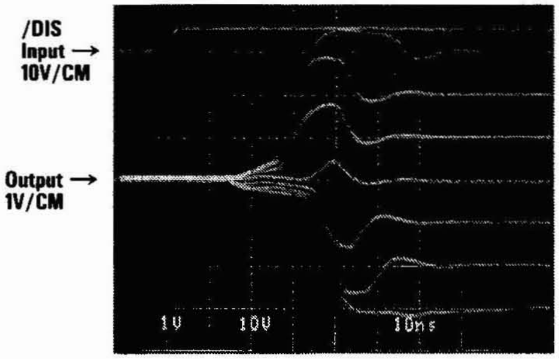
Long Term Settling Error



2120-12

Typical Performance Curves — Contd.

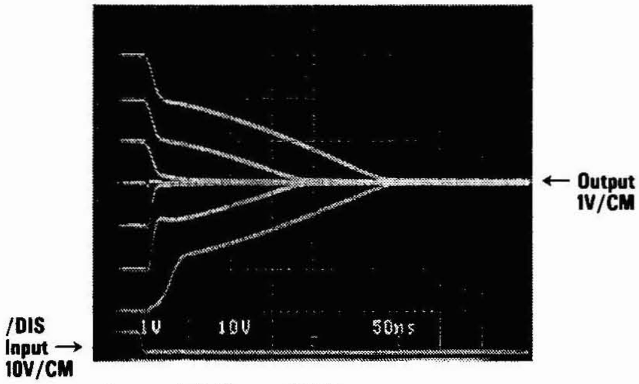
Enable Response for a Family of Inputs



$A_V = +2$, $R_L = 150\Omega$,
$V_S = \pm 5V$

2120-13

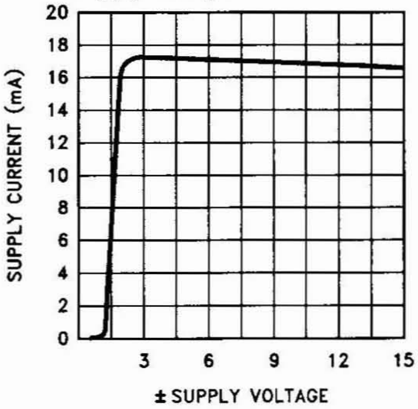
Disable Response for a Family of Inputs



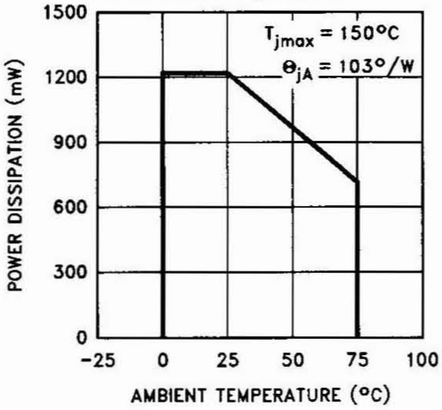
$A_V = +2$, $R_L = 150\Omega$,
$V_S = \pm 5V$

2120-14

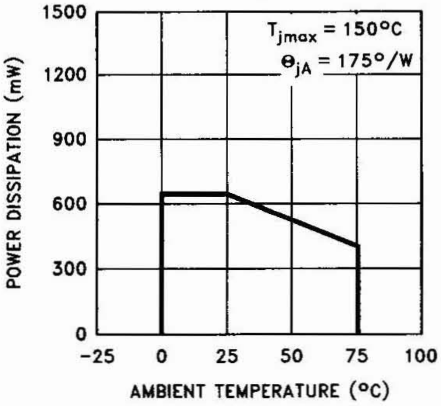
Supply Current vs Supply Voltage



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead SO Maximum Power Dissipation vs Ambient Temperature



2120-15

Applications Information

The EL2120C represents the third generation of current-feedback amplifier design. It is designed to provide good high-frequency performance over wide supply voltage, load impedance, gain, temperature, and manufacturing lot variations. It is a well-behaved amplifier in spite of its 100 MHz bandwidth, but a few precautions should be taken to obtain maximum performance.

The power supply pins must be well bypassed. 0.01 μF ceramic capacitors are adequate, but lead length should be kept below ¼″ and a ground plane is recommended. Bypassing with 4.7 μF tantalum capacitors can improve settling characteristics, and smaller capacitors in parallel will not be needed. The lead length of sockets generally deteriorates the amplifier's frequency response by exaggerating peaking and increasing ringing in response to transients. Short sockets cause little degradation.

Load capacitance also increases ringing and peaking. Capacitance greater than 35 pF should be isolated with a series resistor. Capacitance at the V_{IN-} terminal has a similar effect, and should be kept below 5 pF. Often, the inductance of the leads of a load capacitance will be self-resonant at frequencies from 40 MHz to 200 MHz and can cause oscillations. A resonant load can be de-Q'ed with a small series or parallel resistor. A "snubber" can sometimes be used to reduce resonances. This is a resistor and capacitor in series connected from output to ground. Values of 68Ω and 33 pF are typical. Increasing the feedback resistor can also improve frequency flatness.

The V_{IN+} pin can oscillate in the 200 MHz to 500 MHz realm if presented with a resonant or inductive source impedance. A series 27Ω to 68Ω resistor right on the V_{IN+} pin will suppress such oscillations without affecting frequency response.

−3 dB bandwidth is inversely proportional to the value of feedback resistor R_F. The EL2120C will tolerate values as low as 180Ω for a maximum bandwidth of about 140 MHz, but peaking will increase and tolerance to stray capacitance will reduce. At gains greater than 5, −3 dB bandwidth begins to reduce, and a smaller R_F can be used to maximize frequency response.

The greatest frequency response flatness (to 0.1 dB, for instance) occurs with R_F = 300Ω to 330Ω. Even the moderate peaking caused by lower values of R_F will cause the gain to peak out of the 0.1 dB window, and higher values of R_F will cause an overcompensated response where the gain falls below the 0.1 dB level. Parasitic capacitances will generally degrade the frequency flatness.

The EL2120C should not output a continuous current above 50 mA, as stated in the ABSOLUTE MAXIMUM RATINGS table. The output current limit is set to 120 mA at a die temperature of 25°C and reduces to 85 mA at a die temperature of 150°C. This large current is needed to slew load capacitance and drive low impedance loads with low distortion but cannot be supported continuously. Furthermore, package dissipation capabilities cannot be met under short-circuit conditions. Current limit should not occur longer than a few seconds.

The output disable function of the EL2120C is optimized for video performance. While in disable mode, the feedthrough of the circuit can be modeled as a 0.2 pF capacitor from V_{IN+} to the output. No more than ±5V can be placed between V_{IN+} and V_{IN-} in disable mode, but this is compatible with common video signal levels. In disabled state the output can withstand about 1000 V/μs slew rate signals impressed on it without the output transistors turning on.

The /Disable pin logic level is referred to V+. With ±5V supplies, a CMOS or TTL driver with pull-up resistor will suffice. ±15V supplies require a +14/+11V drive span, or +15/+10V nominally. Open-collector TTL with a tapped pull-up resistor can provide these spans. The impedance of the divider should be 1k or less for optimum enable/disable speed.

The EL2120C enables in 50 ns or less. When V_{IN} = 0, only a small switching glitch occurs at the output. When V_{IN} is some other value, the output overshoots by about 0.7V when settling toward its new enabled value.

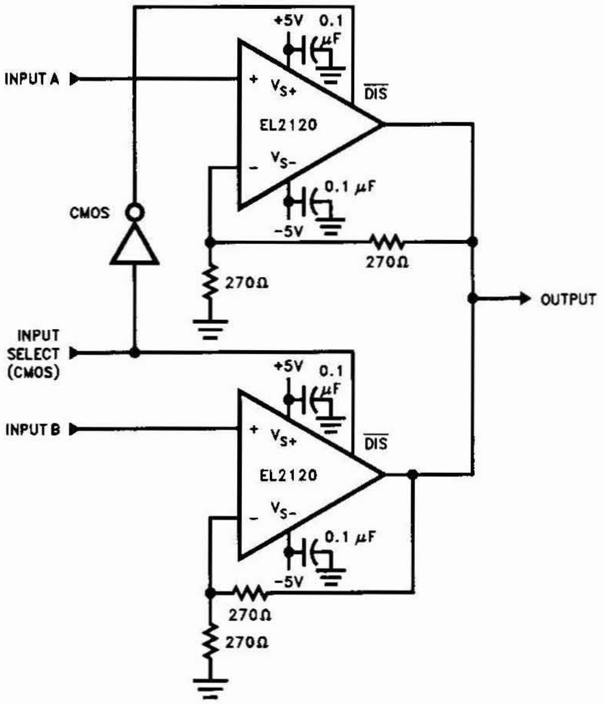
Applications Information — Contd.

When the EL2120C disables, it turns off very rapidly for inputs of ±1V or less, and the output sags more slowly for inputs larger than this. For inputs as large as ±2.5V the output current can be absorbed by another EL2120C simultaneously enabled. Under these conditions, switching will be properly completed in 50 ns or less.

The greater thermal resistance of the SO-8 package requires that the EL2120C be operated from ±10V supplies or less to maintain the 150°C maximum die temperature over the commercial temperature range. The P-DIP package allows the full ±16.5V supply operation.

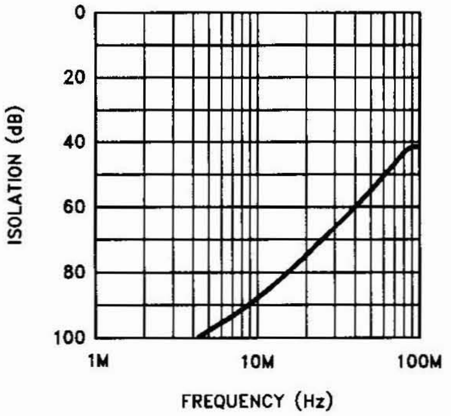
Typical Applications Circuit—A High Quality Two-Input Multiplexer

Dual EL2120C Multiplexer


+5V
0.1 µF
INPUT A
+
V_{S+}
$\overline{DIS}$
EL2120
-
V_{S-}
0.1 µF
-5V
CMOS
270Ω
270Ω
OUTPUT
INPUT SELECT (CMOS)
+5V
0.1 µF
INPUT B
+
V_{S+}
$\overline{DIS}$
EL2120
-
V_{S-}
0.1 µF
-5V
270Ω
270Ω

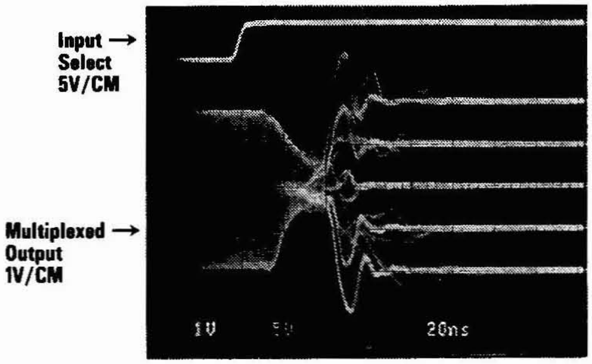
2120-16

Channel-to-Channel Isolation of Dual EL2120C Multiplexer



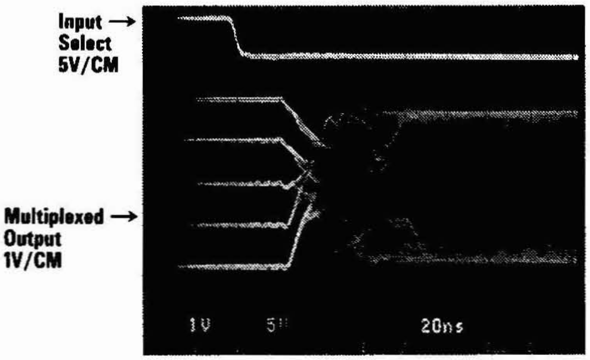
2120-17

Dual EL2120C Multiplexer Switching Channels: Uncorrelated Sinewave Switched to a Family of DC Levels



2120-18

Dual EL2120C Multiplexer Switching Channels: a Family of DC Levels Switched to an Uncorrelated Sinewave



2120-19

The EL2120C Macromodel

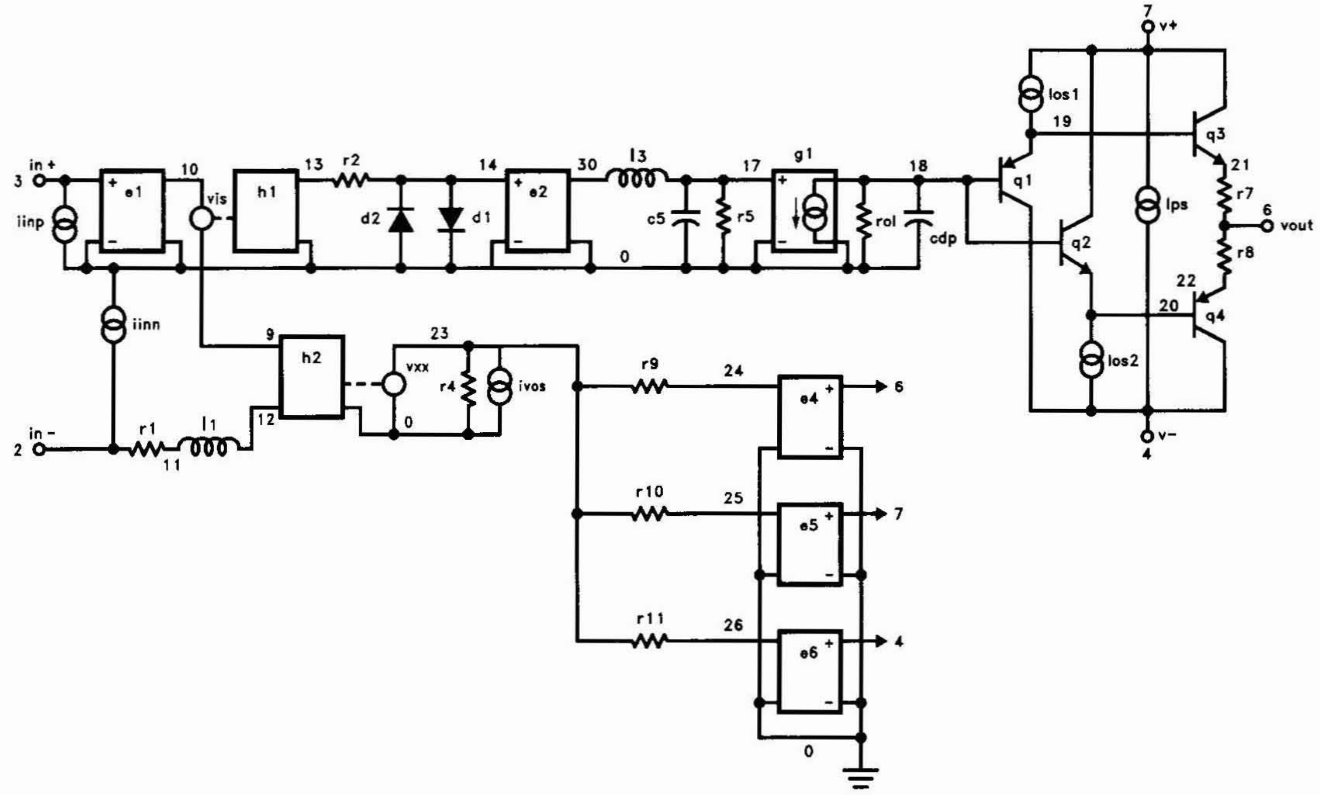
This macromodel has been developed to assist the user in simulating the EL2120C with surrounding circuitry. It was developed for the PSPICE simulator (copywritten by the Microsim corporation), and may need to be rearranged for other simulators, particularly the H operator. It approximates frequency response and small-signal transients as well, although the effects of load capacitance does not show. This model is slightly more complicated than the models used for low-frequency op-amps, but is much more accurate for AC.

The model does not simulate these characteristics accurately:

noise	non-linearities
slew rate limitations	temperature effects
settling time	manufacturing variations
input or output resonances	CMRR and PSRR

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:  +input
*                 |    -input
*                 |     |    +Vsupply
*                 |     |     |    -Vsupply
*                 |     |     |     |    output
*                 |     |     |     |     |
.subckt M2120     3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 25
l1 11 12 20nH
iinp 3 0 10μA
iinm 2 0 5μA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
s2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
15 30 17 1μH
c5 17 0 0.5pF
r5 17 0 600
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 140K
cdp 18 0 7.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply
*
ips 7 4 10mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 6 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 10K
r11 26 23 10K
*
* Models
*
.model qn npn (is=5e-15 bf=500 tf=0.1nS)
.model qp pnp (is=5e-15 bf=500 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.02 bv=4 n =4)
.ends
```

The EL2120C Macromodel — Contd.


7
v+
los1
19
q3
21
r7
6
vout
r8
22
20
q4
q1
q2
lps
los2
v-
4
in +
3
iinp
e1
10
vis
h1
13
r2
d2
d1
14
e2
30
l3
c5
r5
17
g1
rol
18
cdp
0
iinn
9
h2
23
vxx
r4
ivos
12
0
in -
2
r1
11
l1
r9
24
e4
6
r10
25
e5
7
r11
26
e6
4
0

2120-20

EL2120 Macromodel

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2130C

85 MHz Current Feedback Amplifier

Features

- −3 dB bandwidth = 85 MHz, $A_V = 1$
- −3 dB bandwidth = 75 MHz, $A_V = 2$
- NTSC/PAL dG ≤ 0.03%, dP ≤ 0.1°
- 50 mA output current
- Drives ±2.5V into 100Ω load
- Low voltage noise = 4 nV/$\sqrt{\text{Hz}}$
- Current mode feedback
- Low cost

Applications

- Video amplifier
- Video distribution amplifier
- Residue amplifiers in ADC
- Current to voltage converter
- Coaxial cable driver

Ordering Information

Part No.	Temp. Range	Pkg.	Outline*
EL2130CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2130CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

The EL2130 is a wideband current mode feedback amplifier optimized for gains between −10 and +10 while operating on ±5V power supplies. Built using Elantec's Complementary Bipolar process, this device exhibits −3 dB bandwidths in excess of 85 MHz at unity gain and 75 MHz at a gain of two. The EL2130 is capable of output currents in excess of 50 mA giving it the ability to drive either double or single terminated 50Ω coaxial cables.

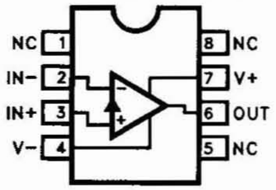
Exhibiting a Differential Gain of 0.03% and a Differential Phase of 0.1° at NTSC and PAL frequencies. The EL2130 is an excellent low cost solution to most video applications.

In addition, the EL2130 exhibits very low gain peaking, typically below 0.1 dB to frequencies in excess of 40 MHz as well as 50 ns settling time to 0.2% making it an excellent choice for driving flash A/D converters.

The device is available in the plastic 8-lead narrow-body small outline (SO) and the 8-pin mini DIP packages, and operates over the temperature range of 0°C to +75°C.

Connection Diagram

Mini DIP and SO



2130-1

Manufactured under U.S. Patent No. 4,893,091.

2

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±6V	I_{OP}	Output Short Circuit Duration	≤5 sec
V_{IN}	Input Voltage	$\pm V_S$	T_A	Operating Temperature Range:	0°C to +75°C
ΔV_{IN}	Differential Input Voltage	±6V	T_J	Operating Junction Temperature	150°C
P_D	Maximum Power Dissipation	See Curves	T_{ST}	Storage Temperature	−65°C to +150°C
I_{IN}	Input Current	±10 mA			

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±5V; R_L = ∞, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		25°C		2.0	10	I	mV
			T_{MIN}, T_{MAX}			15	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift				7		V	µV/°C
$+I_{IN}$	+Input Current		25°C		5.5	15	I	µA
			T_{MIN}, T_{MAX}			25	III	µA
$-I_{IN}$	+Input Current		25°C		10	40	I	µA
			T_{MIN}, T_{MAX}			50	III	µA
$+R_{IN}$	+Input Resistance		25°C	1.0	2.0		I	MΩ
C_{IN}	+Input Capacitance		25°C		1.0		V	pF
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V	25°C	50	60		I	dB
−ICMR	Input Current Common Mode Rejection	V_{CM} = ±2.5V	25°C		5	10	I	µA/V
			T_{MIN}, T_{MIN}			20	III	µA/V
PSRR	Power Supply Rejection Ratio	$\pm 4.5V \le V_S \le \pm 6V$	25°C	60	70		I	dB
+IPSR	+Input Current Power Supply Rejection	$\pm 4.5V \le V_S \le \pm 6V$	25°C		0.1	0.5	I	µA/V
			T_{MIN}, T_{MIN}			1.0	III	µA/V
−IPSR	−Input Current Power Supply Rejection	$\pm 4.5V \le V_S \le \pm 6V$	25°C		0.5	5.0	I	µA/V
			T_{MIN}, T_{MIN}			8.0	III	µA/V

Open Loop DC Electrical Characteristics

V_S = ±5V; R_L = ∞, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
R_{OL}	Transimpedance	V_{OUT} = ±2.5V, R_L = 100Ω	25°C	80	145		I	V/mA
			T_{MIN}, T_{MAX}	70			III	V/mA
A_{VOL}	Open Loop DC Voltage Gain	V_{OUT} = ±2.5V, R_L = 100Ω	25°C	60	66		I	dB
			T_{MIN}, T_{MAX}	56			III	dB
V_O	Output Voltage Swing	R_L = 100Ω	25°C	3	3.5		I	V
I_{OUT}	Output Current		25°C	30	50		I	mA
R_{OUT}	Output Resistance		25°C		5		V	Ω
I_S	Quiescent Supply Current		Full		17	21	I	mA
I_{SC}	Short Circuit Current		25°C		85		V	mA

Closed Loop AC Electrical Characteristics

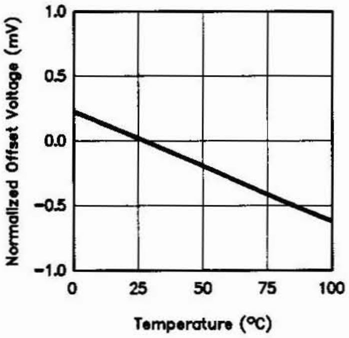
V_S = ±5V, A_V = +2, R_F = R_G = 820Ω, R_L = 100Ω, T_A = 25°C

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Note 1)	V_O = 5 V_{p-p}		625		V	V/μs
t_r	Rise Time	V_O = 200 mV		4.6		V	ns
t_f	Fall Time	V_O = 200 mV		4.6		V	ns
t_{pd}	Prop Delay	V_O = 200 mV		4.0		V	ns
SSBW	3 dB Bandwidth	V_O = 100 mV		75		V	MHz
dG	NTSC/PAL Diff Gain			0.03		V	%
dP	NTSC/PAL Diff Phase			0.10		V	deg (°)
GFPL	Gain Flatness	f < 40 MHz		0.08		V	dB

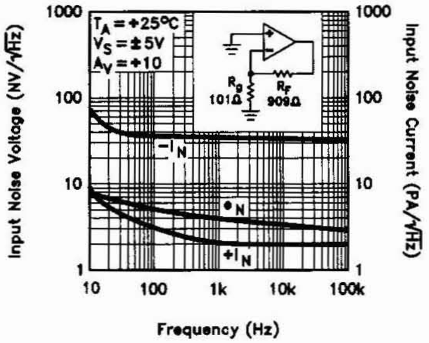
Note 1: Slew rate is measured with V_O = 5V_{p-p} between −1.25V and +1.25V and +1.25V and −1.25V.

Typical Performance Curves

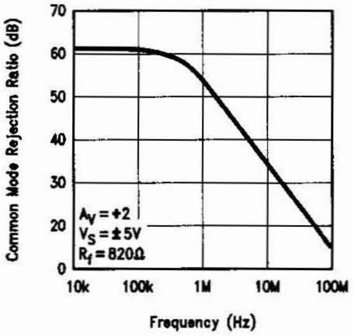
Normalized Offset Voltage vs Temperature



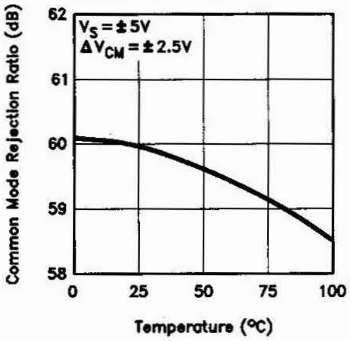
Equivalent Input Noise



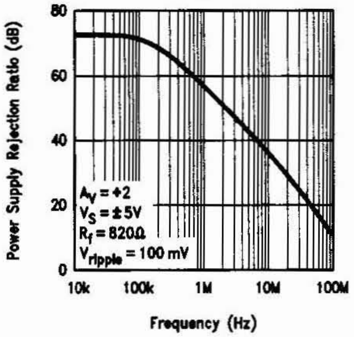
Common Mode Rejection Ratio vs Frequency



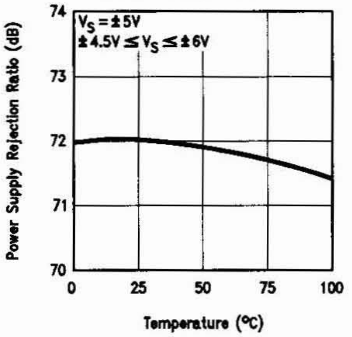
Common Mode Rejection Ratio vs Temperature



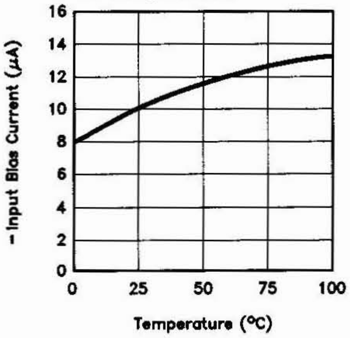
Power Supply Rejection Ratio vs Frequency



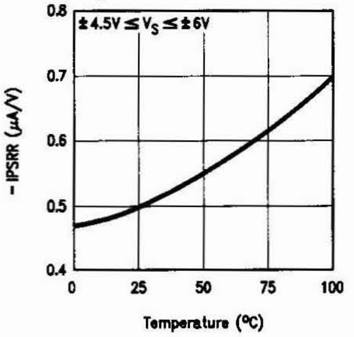
Power Supply Rejection Ratio vs Temperature



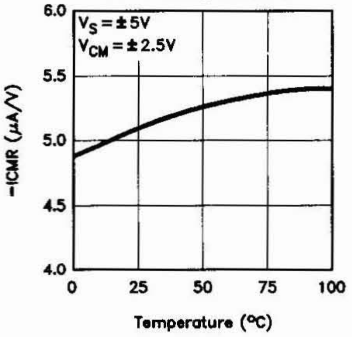
−Input Bias Current vs Temperature



−Input Bias Current Power Supply Rejection Ratio



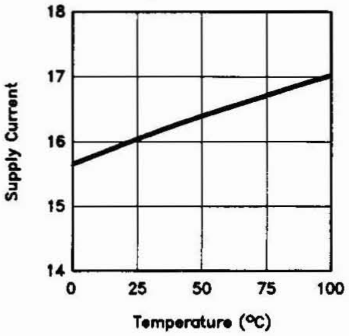
−Input Bias Current Common Mode Rejection Ratio vs Temperature



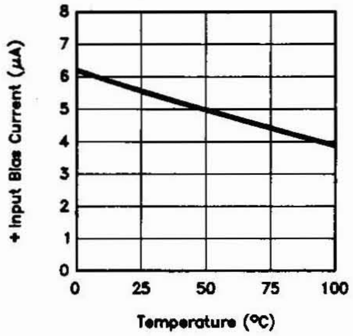
2130-2

Typical Performance Curves — Contd.

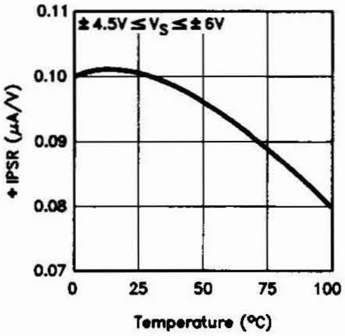
Supply Current vs Temperature



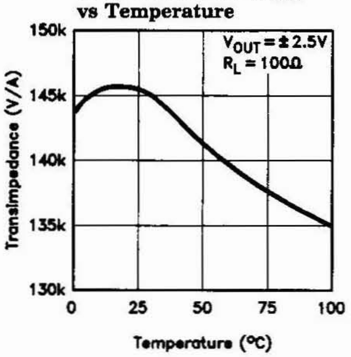
+Input Bias Current vs Temperature



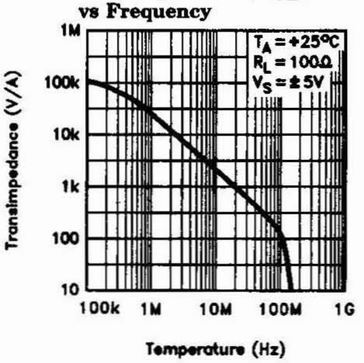
+Input Bias Current Power Supply Rejection Ratio vs Temperature



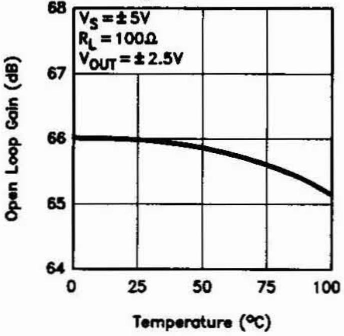
Transimpedance (R_{OL}) vs Temperature



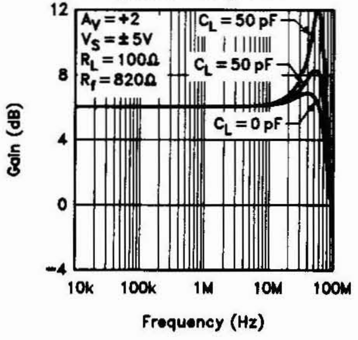
Transimpedance (R_{OL}) vs Frequency



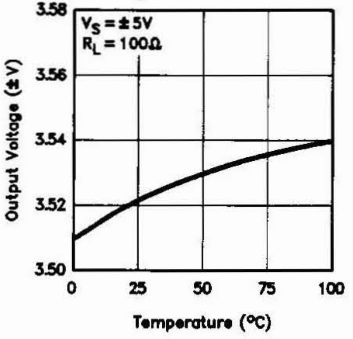
Open Loop Gain vs Temperature



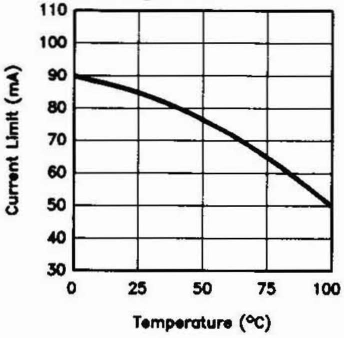
Frequency Response



Output Voltage vs Temperature



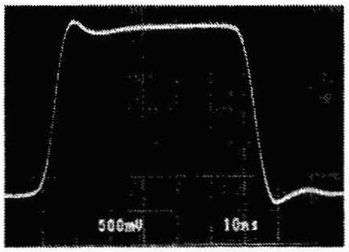
Short Circuit Current vs Temperature



2130-3

Typical Performance Curves — Contd.

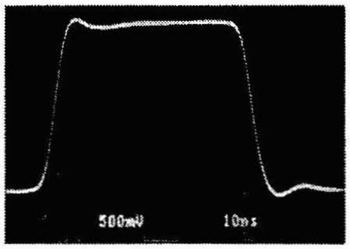
Large Signal Response



2130-4

$A_V = +1$, $R_F = 820\Omega$
$R_L = 100\Omega$, $C_L = 12$ pF

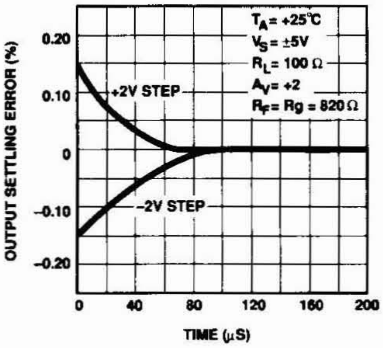
Large Signal Response



2130-5

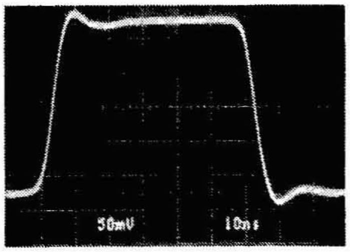
$A_V = +2$, $R_F = 820\Omega$
$R_L = 100\Omega$, $C_L = 12$ pF

Long-Term Output Settling Error vs Time, $V_S = \pm 5V$



2130-6

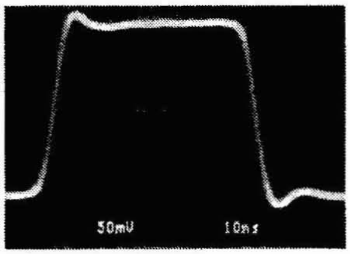
Small Signal Response



2130-7

$A_V = +1$, $R_F = 820\Omega$
$R_L = 100\Omega$, $C_L = 12$ pF

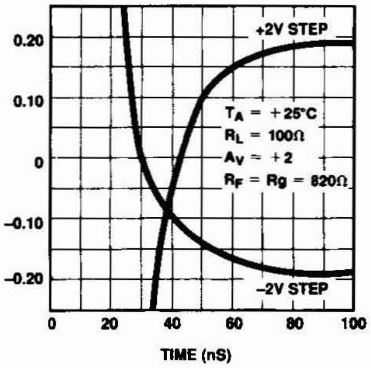
Small Signal Response



2130-8

$A_V = +2$, $R_F = 820\Omega$
$R_L = 100\Omega$, $C_L = 12$ pF

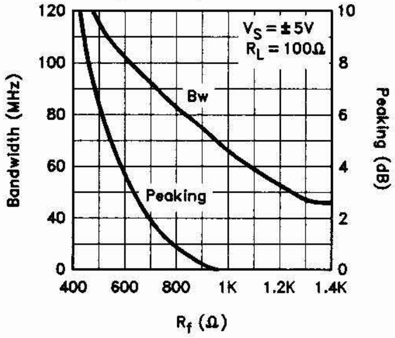
Short Term Output Settling Error vs Time, $V_S = \pm 5V$



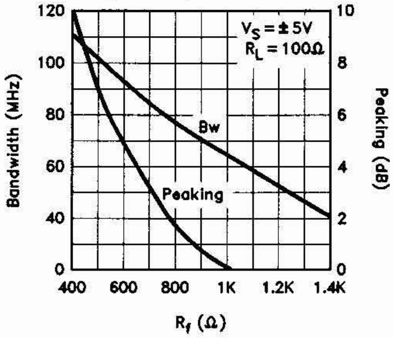
2130-9

Typical Performance Curves — Contd.

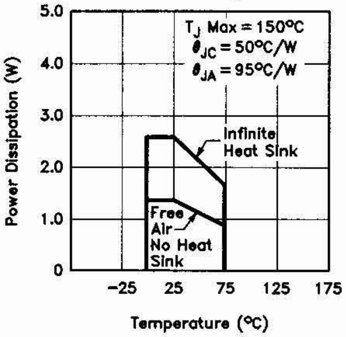
Bandwidth and Peaking vs R_F for $A_V = +1$



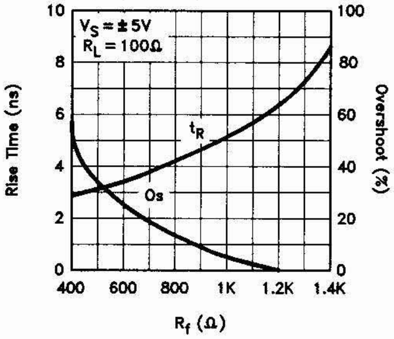
Bandwidth and Peaking vs R_F for $A_V = +2$



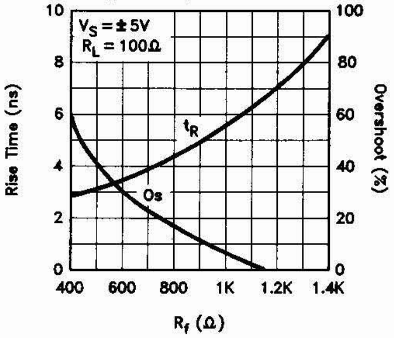
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



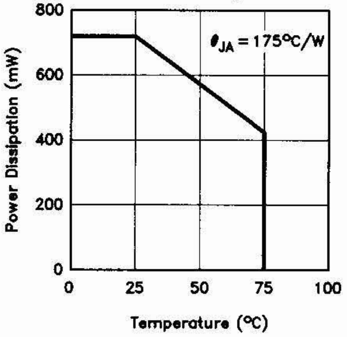
Rise Time and Overshoot vs R_F for $A_V = 1$



Rise Time and Overshoot vs R_F for $A_V = 2$



8-Lead SO Maximum Power Dissipation vs Ambient Temperature



2130-10

Applications Information

Power Supply Bypassing

The EL2130 will exhibit ringing or oscillation if the power supply leads are not adequately bypassed. 0.1 μF ceramic disc capacitors are suggested for both supply pins at a distance no greater than ½ inch from the device. Surface mounting chip capacitors are strongly recommended.

Lead Dress

A ground plane to which decoupling capacitors and gain setting resistors are terminated will eliminate overshoot and ringing. However, the ground plane should not extend to the vicinity of both the non-inverting and inverting inputs (pins 3 and 2) which would add capacitance to these nodes, and lead lengths from these pins should be made as short as possible.

Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Video Characteristics and Applications

Frequency domain testing is performed at Elantec using a computer controlled HP model 8656B Signal Generator and an HP Model 4195A Network/Spectrum Analyzer. The DUT test board is built using microwave/strip line techniques, and solid coaxial cables route the stimulus to the DUT socket. Signals are routed to and from the DUT test fixture using subminiature coaxial cable.

Differential Gain and Phase are tested at a noise gain of 2 with 100Ω load. Gain and Phase measurements are made with a DC input reference

Applications Information — Contd.

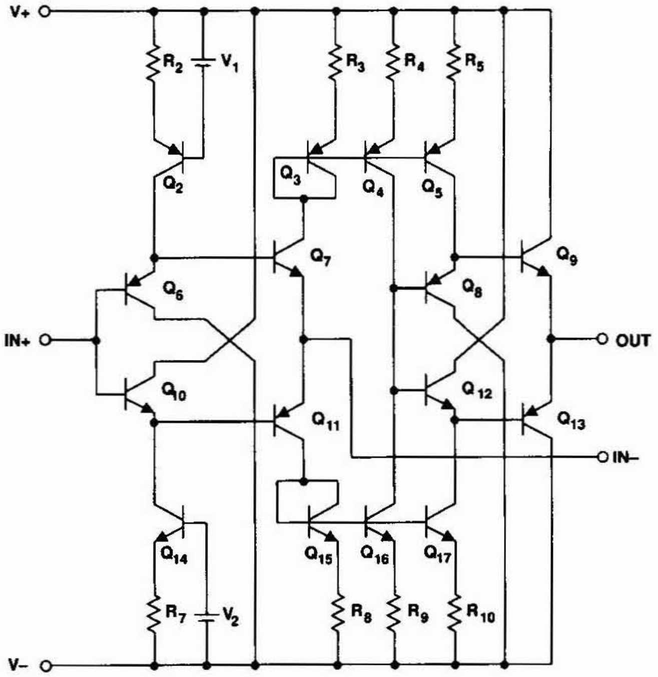
voltage at 0V and compared to those made at V_{ref} equal to 0.7V at frequencies extending to 30 MHz.

The EL2130 is capable of driving 100Ω to a minimum of 2.5V peak which means that it can naturally drive double terminated (50Ω) coaxial cables.

Capacitive Loads

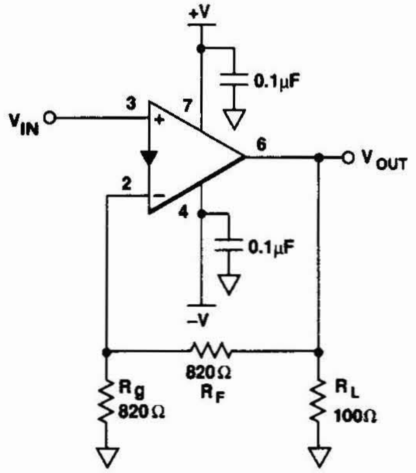
As can be seen from the Bode plot, the EL2130 will peak into capacitive loads greater than 20 pf. In many applications such as flash A/D's, capacitive loading is unavoidable. In these cases, the use of a snubber network consisting of a 100Ω resistor in series with 47 pF capacitor from the output to ground is recommended.

Equivalent Circuit


V+
R2
V1
R3
R4
R5
Q2
Q3
Q4
Q5
Q7
Q9
Q6
Q8
IN+
OUT
Q10
Q12
Q11
Q13
IN−
Q14
Q15
Q16
Q17
R7
V2
R8
R9
R10
V−

2130-11

AC Test Circuit


+V
0.1μF
VIN
3
7
+
6
V OUT
2
−
4
0.1μF
−V
820Ω
RF
Rg
820Ω
RL
100Ω

2130-12

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2150C/EL2157C

125 MHz Single Supply, Clamping Op Amps

Features

- Specified for + 3V, + 5V, or ± 5V Applications
- Power Down to 0 μA (EL2157C)
- Output Voltage Clamp (EL2157C)
- Large Input Comon Mode Range 0V < V_{CM} < Vs - 1.2V
- Output Swings to Ground Without Saturating
- −3 dB Bandwidth = 125 MHz
- ± 0.1 dB Bandwidth = 30 MHz
- Low Supply Current = 5 mA
- Slew Rate = 275V/μs
- Low Offset Voltage = 2 mV max (PDIP and SO Packages)
- Output Current = ±100 mA
- High Open Loop Gain = 80 dB
- Differential Gain = 0.05%
- Differential Phase = 0.05°

Applications

- Video Amplifier
- PCMCIA Applications
- A/D Driver
- Line Driver
- Portable Computers
- High Speed Communications
- RGB Applications
- Broadcast Equipment
- Active Filtering

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2150CN	−40°C to +85°C	8 Pin PDIP	MDP0031
EL2150CS	−40°C to +85°C	8 Pin SOIC	MDP0027
EL2150CW	−40°C to +85°C	5 Pin SOT23*	MDP0038
EL2157CN	−40°C to +85°C	8 Pin PDIP	MDP0031
EL2157CS	−40°C to +85°C	8 Pin SOIC	MDP0027

*See Ordering Information section of databook.

General Description

The EL2150C/EL2157C are the electronics industry's fastest single supply op amps available. Prior single supply op amps have generally been limited to bandwidths and slew rates ¼ that of the EL2150C/EL2157C. The 125 MHz bandwidth, 275 V/μs slew rate, and 0.05%/0.05° differential gain/differential phase makes this part ideal for single or dual supply video speed applications. With its voltage feedback architecture, this amplifier can accept reactive feedback networks, allowing them to be used in analog filtering applications. The inputs can sense signals below the bottom supply rail and as high as 1.2V below the top rail. Connecting the load resistor to ground and operating from a single supply, the outputs swing completely to ground without saturating. The outputs can also drive to within 1.2V of the top rail. The EL2150C/EL2157C will output ±100 mA and will operate with single supply voltages as low as 2.7V, making it ideal for portable, low power applications.

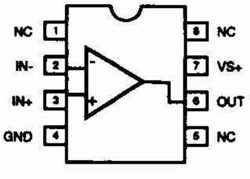
The EL2157C has a high speed disable feature. Applying a low logic level to this pin reduces the supply current to 0 μA within 50 ns. This is useful for both multiplexing and reducing power consumption.

The EL2157C also has an output voltage clamp feature. This clamp is a fast recovery (<7 ns) output clamp that prevents the output voltage from going above the preset clamp voltage. This feature is desirable for A/D applications, as A/D converters can require long times to recover if overdriven.

For applications where board space is critical the EL2150C is available in the tiny 5 lead SOT23 package, which has a footprint 28% the size of an 8 lead SOIC. The EL2150C/EL2157C are also both available in 8 pin plastic DIP and SOIC packages. All parts operate over the industrial temperature range of −40°C to +85°C. For dual, triple, or quad applications, contact the factory.

Connection Diagrams

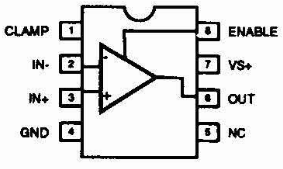
EL2150C
SO, P-DIP



2150-1

Top View

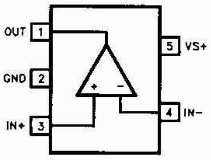
EL2157C
SO, P-DIP



2150-2

Top View

EL2150C
SOT23-5



2150-3

Top View

EL2150C/EL2157C

125 MHz Single Supply, Clamping Op Amps

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_{S+} and GND	+12.6V	Power Dissipation	See Curves
Input Voltage (IN+, IN−, ENABLE, CLAMP)	GND−0.3V, V_S+0.3V	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	±6V	Ambient Operating Temperature Range	−40°C to +85°C
Maximum Output Current	90 mA	Operating Junction Temperature	150°C
Output Short Circuit Duration	(note 1)		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	**Test Procedure**
I	**100% production tested and QA sample tested per QA test plan QCX0002.**
II	**100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.**
III	**QA sample tested per QA test plan QCX0002.**
IV	**Parameter is guaranteed (but not tested) by Design and Characterization Data.**
V	**Parameter is typical value at T_A = 25°C for information purposes only.**

DC Electrical Characteristics

(Note 2) V_S = +5V, GND = 0V, T_A = 25°C, V_{CM} = 1.5V, V_{OUT} = 1.5V, V_{CLAMP} = +5V, V_{ENABLE} = +5V, unless otherwise specified.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage	PDIP and SOIC Packages	−2		2	I	mV
		SOT23-5 Package	−3		3	I	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from Tmin to Tmax		10		V	µV/°C
IB	Input Bias Current	V_{IN} = 0V		−5.5	−10	I	µA
I_{OS}	Input Offset Current	V_{IN} = 0V	−750	150	750	I	nA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from Tmin to Tmax		50		V	nA/°C
PSRR	Power Supply Rejection Ratio	$V_S = V_{ENABLE}$ = +2.7V to +12V, V_{CLAMP} = OPEN	55	70		I	dB
CMRR	Common Mode Rejection Ratio	VCM = 0V to +3.8V	55	65		I	dB
		VCM = 0V to +3.0V	55	70		I	dB
CMIR	Common Mode Input Range		0		V_S − 1.2	I	V
R_{IN}	Input Resistance	Common Mode	1	2		I	MΩ
C_{IN}	Input Capacitance	SOIC Package		1		V	pF
		PDIP Package		1.5		V	pF
R_{OUT}	Output Resistance	Av = +1		40		V	mΩ
$I_{S,ON}$	Supply Current—Enabled	$V_S = V_{CLAMP}$ = +12V, V_{ENABLE} = +12V		5	6.5	I	mA
$I_{S,OFF}$	Supply Current—Shut Down	$V_S = V_{CLAMP}$ = +10V, V_{ENABLE} = +0.5V		0	50	I	µA
		$V_S = V_{CLAMP}$ = +12V, V_{ENABLE} = +0.5V		5		V	µA
PSOR	Power Supply Operating Range		2.7		12.0	I	v

DC Electrical Characteristics — Contd.

(Note 2) $V_S = +5V$, $GND = 0V$, $T_A = 25°C$, $V_{CM} = +1.5V$, $V_{OUT} = +1.5V$, $V_{CLAMP} = +5V$, $V_{ENABLE} = +5V$, unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
PSOR	Power Supply Operating Range		2.7		12.0	I	V
AVOL	Open Loop Gain	$V_S = V_{CLAMP} = +12V$, $V_{OUT} = +2V$ to $+9V$, $R_L = 1\ k\Omega$ to GND	65	80		I	dB
		$V_{OUT} = +1.5V$ to $+3.5V$, $R_L = 1\ k\Omega$ to GND		70		V	dB
		$V_{OUT} = +1.5V$ to $+3.5V$, $R_L = 150\Omega$ to GND		60		V	dB
V_{OP}	Positive Output Voltage Swing	$V_S = +12V$, $A_V = +1$, $R_L = 1\ k\Omega$ to 0V		10.8		V	V
		$V_S = +12V$, $A_V = +1$, $R_L = 150\Omega$ to 0V	9.6	10.0		I	V
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 1\ k\Omega$ to 0V		4.0		V	V
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 150\Omega$ to 0V	3.4	3.8		I	V
		$V_S = +3V$, $A_V = +1$, $R_L = 150\Omega$ to 0V	1.8	1.95		I	V
V_{ON}	Negative Output Voltage Swing	$V_S = +12V$, $A_V = +1$, $R_L = 150\Omega$ to 0V		5.5	8	I	mV
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 1\ k\Omega$ to 0V		−4.0		V	V
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 150\Omega$ to 0V		−3.7	−3.4	I	V
I_{OUT}	Output Current (Note 1)	$V_S = \pm 5V$, $A_V = +1$, $R_L = 10\Omega$ to 0V	±75	±100		I	mA
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 50\Omega$ to 0V		±60		V	mA
$I_{OUT,OFF}$	Output Current, Disabled	$V_{ENABLE} = +0.5V$		0	20	I	μA
$V_{IH\text{-}EN}$	ENABLE pin Voltage for Power Up	Relative to GND pin	2.0			I	V
$V_{IL\text{-}EN}$	ENABLE pin Voltage for Shut Down	Relative to GND pin			0.5	I	V
$I_{IH\text{-}EN}$	ENABLE pin Input Current-High (Note 3)	$V_S = V_{CLAMP} = +12V$, $V_{ENABLE} = +12V$		340	410	I	μA
$I_{IL\text{-}EN}$	ENABLE pin Input Current-Low (Note 3)	$V_S = V_{CLAMP} = +12V$, $V_{ENABLE} = +0.5V$		0	1	I	μA
$V_{OR\text{-}CL}$	Voltage Clamp Operating Range (Note 4)	Relative to GND pin	1.2		V_{OP}	I	V
$V_{ACC\text{-}CL}$	CLAMP Accuracy (Note 5)	$V_{IN} = +4V$, $R_L = 1\ k\Omega$ to GND $V_{CLAMP} = +1.5V$ and $+3.5V$	−250	100	250	I	mV
$I_{IH\text{-}CL}$	CLAMP pin Input Current—High	$V_S = V_{CLAMP} = +12V$		12	25	I	μA
$I_{IL\text{-}CL}$	CLAMP pin Input Current—Low	$V_S = +12V$, $V_{CLAMP} = +1.2V$	−20	−15		I	μA

Closed Loop AC Electrical Characteristics

(Notes 2 & 6) $V_S = +5V$, $GND = 0V$, $T_A = 25°C$, $V_{CM} = +1.5V$, $V_{OUT} = +1.5V$, $V_{CLAMP} = +5V$, $V_{ENABLE} = +5V$, $A_V = +1$, $R_F = 0\Omega$, $R_L = 150\Omega$ to GND pin, unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth ($V_{OUT} = 400$ mVp-p)	$V_S = +5V$, $A_V = +1$, $R_F = 0\Omega$		125		V	MHz
		$V_S = +5V$, $A_V = -1$, $R_F = 500\Omega$		60		V	MHz
		$V_S = +5V$, $A_V = +2$, $R_F = 500\Omega$		60		V	MHz
		$V_S = +5V$, $A_V = +10$, $R_F = 500\Omega$		6		V	MHz
		$V_S = +12V$, $A_V = +1$, $R_F = 0\Omega$		150		V	MHz
		$V_S = +3V$, $A_V = +1$, $R_F = 0\Omega$		100		V	MHz
BW	±0.1 dB Bandwidth ($V_{OUT} = 400$ mVp-p)	$V_S = +12V$, $A_V = +1$, $R_F = 0\Omega$		25		V	MHz
		$V_S = +5V$, $A_V = +1$, $R_F = 0\Omega$		30		V	MHz
		$V_S = +3V$, $A_V = +1$, $R_F = 0\Omega$		20		V	MHz
GBWP	Gain Bandwidth Product	$V_S = +12V$, @ $A_V = +10$		60		V	MHz
PM	Phase Margin	$R_L = 1\ k\Omega$, $CL = 6$ pF		55		V	°
SR	Slew Rate	$V_S = +10V$, $R_L = 150\Omega$, $V_{out} =$ 0V to +6V	200	275		I	V/µs
		$V_S = +5V$, $R_L = 150\Omega$, $V_{OUT} =$ 0V to +3V		300		V	V/µs
t_R, t_F	Rise Time, Fall Time	±0.1V step		2.8		V	ns
OS	Overshoot	±0.1V step		10		V	%
t_{PD}	Propagation Delay	±0.1V step		3.2		V	ns
t_S	0.1% Settling Time	$V_S = \pm 5V$, $R_L = 500\Omega$, $A_V = +1$, $V_{OUT} = \pm 3V$		40		V	ns
	0.01% Settling Time	$V_S = \pm 5V$, $R_L = 500\Omega$, $A_V = +1$, $V_{OUT} = \pm 3V$		75		V	ns
dG	Differential Gain (Note 7)	$A_V = +2$, $R_F = 1\ k\Omega$		0.05		V	%
dP	Differential Phase (Note 7)	$A_V = +2$, $R_F = 1\ k\Omega$		0.05		V	°
e_N	Input Noise Voltage	f = 10 kHz		48		V	$nV\sqrt{Hz}$
i_N	Input Noise Current	f = 10 kHz		1.25		V	$pA\sqrt{Hz}$
t_{DIS}	Disable Time (Note 8)			50		V	ns
t_{EN}	Enable Time (Note 8)			25		V	ns
t_{CL}	Clamp Overload Recovery			7		V	ns

Note 1: Internal short circuit protection circuitry has been built into the EL2150C/EL2157C. See the Applications section.

Note 2: CLAMP pin and ENABLE pin specifications apply only to the EL2157C.

Note 3: If the disable feature is not desired, tie the ENABLE pin to the V_S pin, or apply a logic high level to the ENABLE pin.

Note 4: The maximum output voltage that can be clamped is limited to the maximum positive output Voltage, or V_{OP}. Applying a Voltage higher than V_{OP} inactivates the clamp. If the clamp feature is not desired, either tie the CLAMP pin to the V_S pin, or simply let the CLAMP pin float.

Note 5: The clamp accuracy is affected by V_{IN} and R_L. See the Typical Curves Section and the Clamp Accuracy vs. V_{IN} & R_L curve.

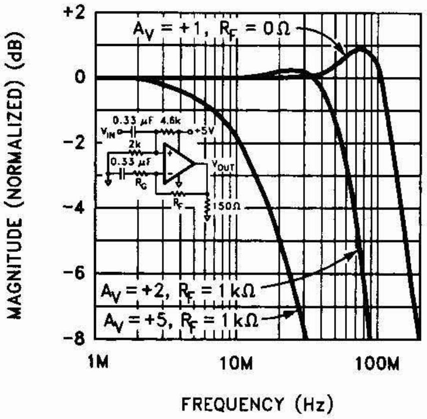
Note 6: All AC tests are performed on a "warmed up" part, except slew rate, which is pulse tested.

Note 7: Standard NTSC signal = 286 mVp-p, f = 3.58MHz, as VIN is swept from 0.6V to 1.314V. R_L is DC coupled.

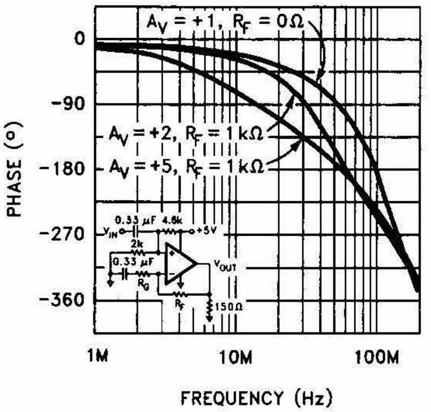
Note 8: Disable/Enable time is defined as the time from when the logic signal is applied to the ENABLE pin to when the supply current has reached half its final value.

Typical Performance Curves

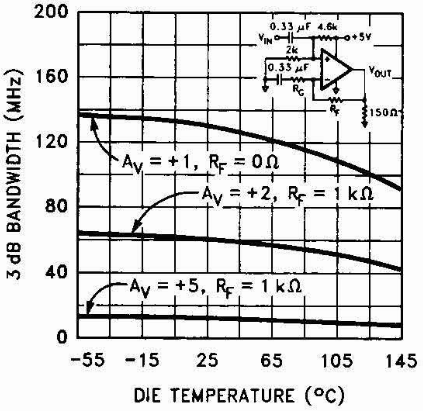
Non-Inverting Frequency Response (Gain)



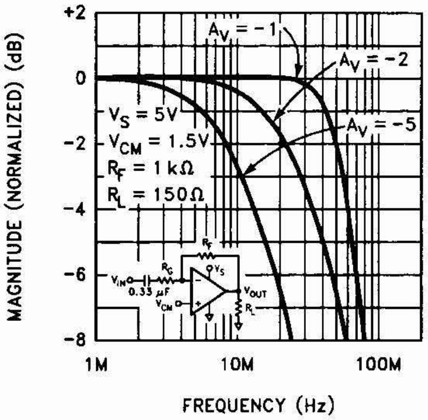
Non-Inverting Frequency Response (Phase)



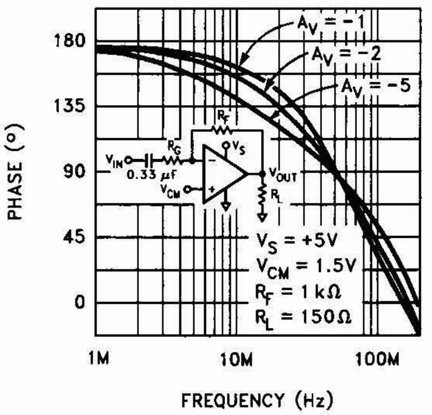
3 dB Bandwidth vs Temperature for Non-Inverting Gains



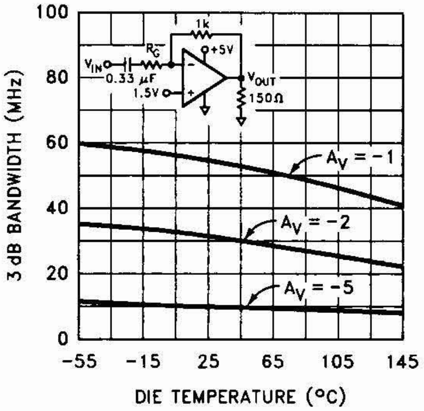
Inverting Frequency Response (Gain)



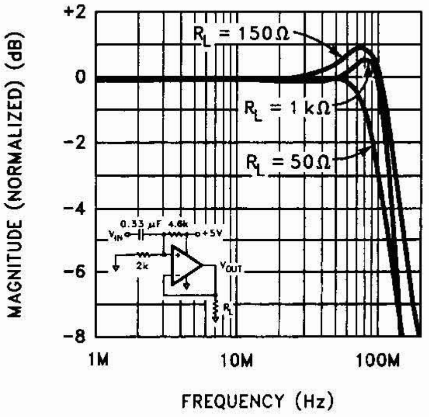
Inverting Frequency Response (Phase)



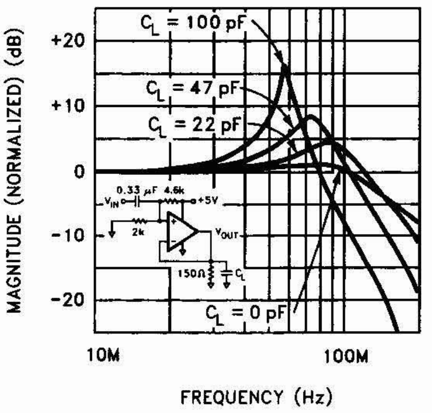
3 dB Bandwidth vs Temperature for Inverting Gains



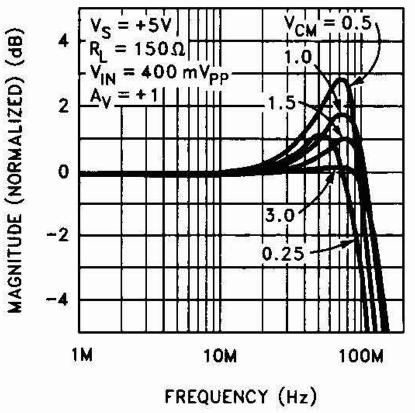
Frequency Response for Various R_L



Frequency Response for Various C_L

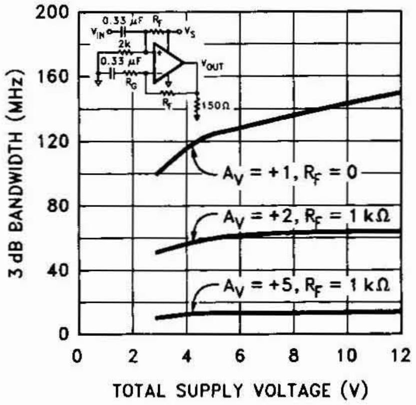


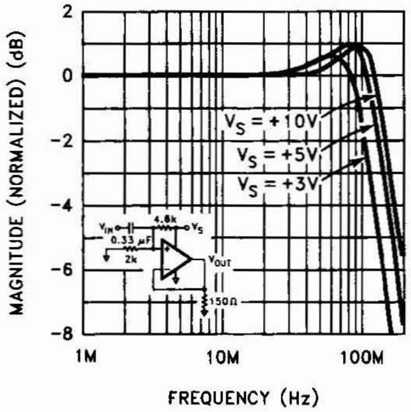
Non-Inverting Frequency Response vs Common Mode Voltage

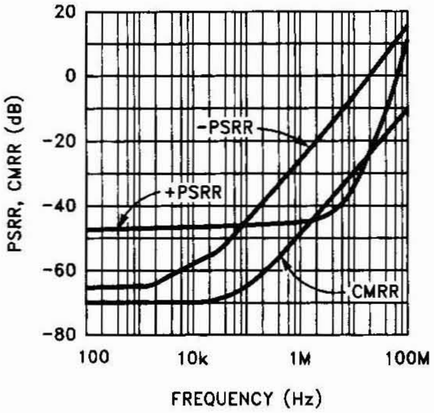


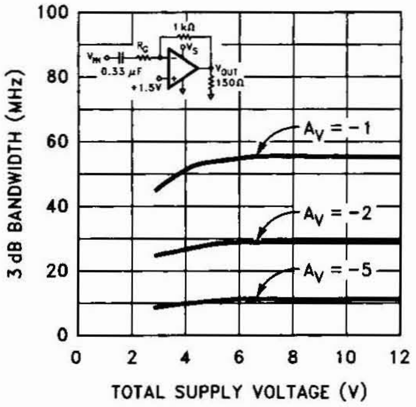
2150-74

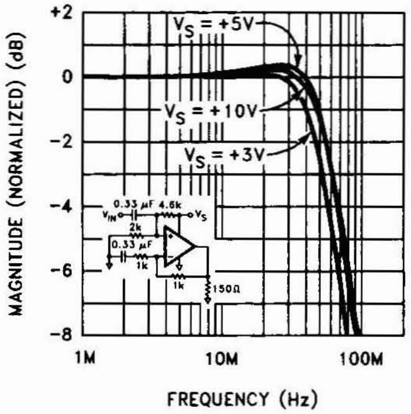
Typical Performance Curves — Contd.

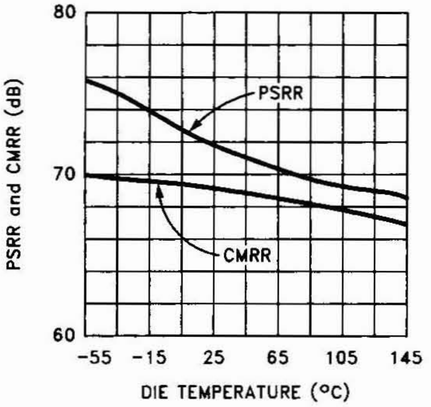

3 dB Bandwidth vs Supply Voltage for Non-Inverting Gains

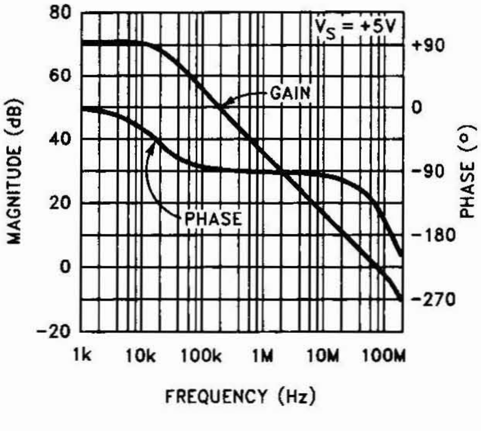

Frequency Response for Various Supply Voltages, A_V = + 1

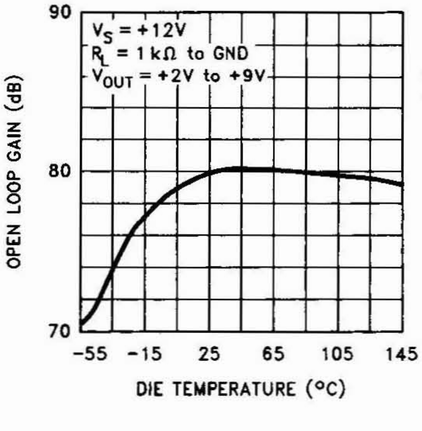

PSSR and CMRR vs Frequency

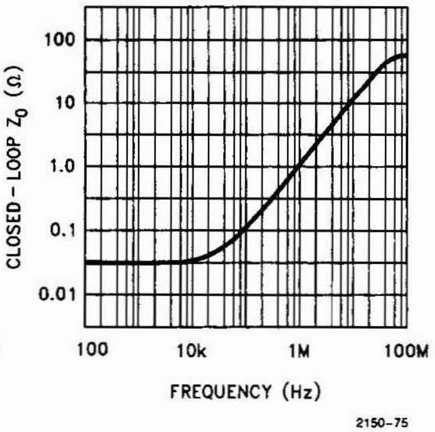

3 dB Bandwith vs Supply Voltage for Inverting Gains


Frequency Response for Various Supply Voltages, A_V = + 2


PSRR and CMRR vs Die Temperature


Open Loop Gain and Phase vs Frequency

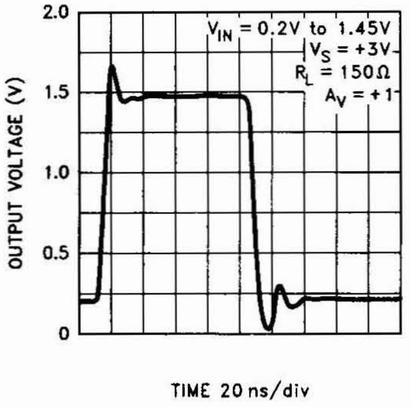

Open Loop Voltage Gain vs Die Temperature


Closed Loop Output Impedance vs Frequency

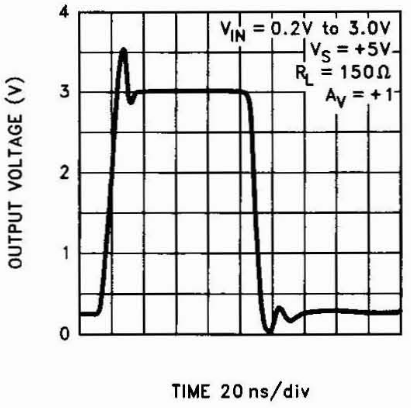
2150-75

Typical Performance Curves — Contd.

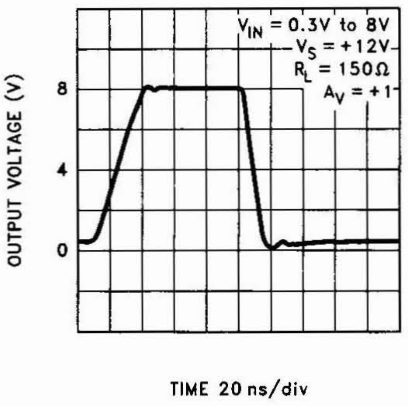
Large Signal Step Response, V_S = +3V



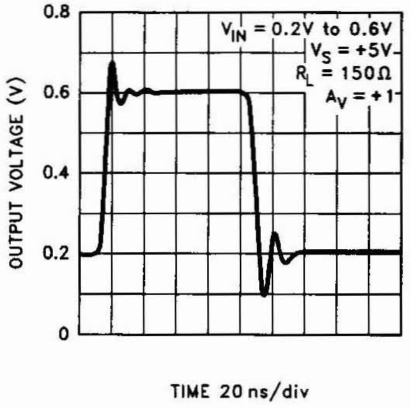
Large Signal Step Response, V_S = +5V



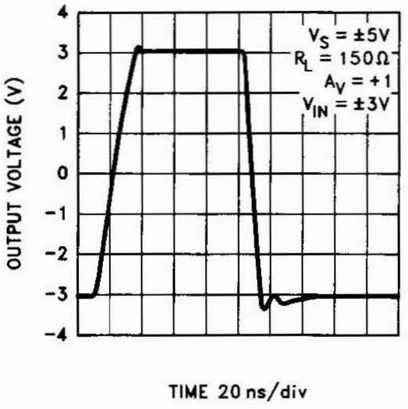
Large Signal Step Response, V_S = +12V



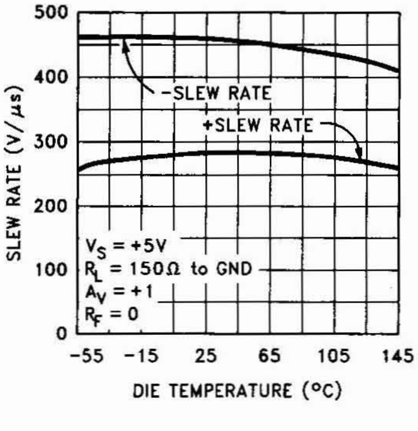
Small Signal Step Response



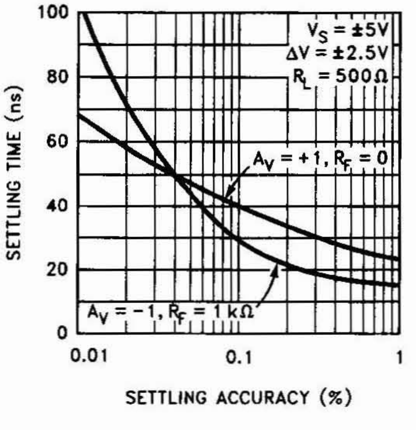
Large Signal Step Response, V_S = ±5V



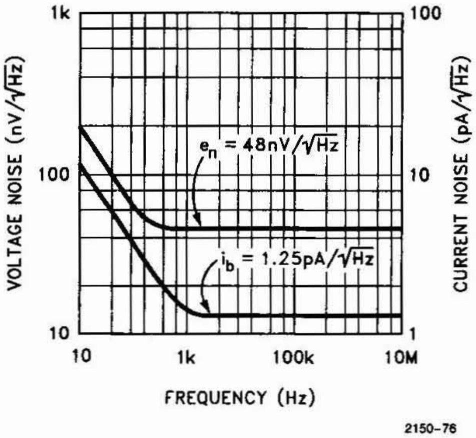
Slew Rate vs Temperature



Settling Time vs Settling Accuracy



Voltage and Current Noise vs Frequency



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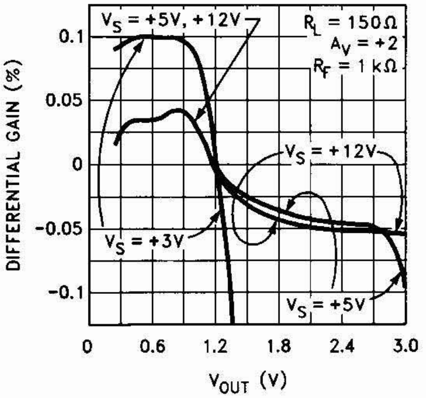
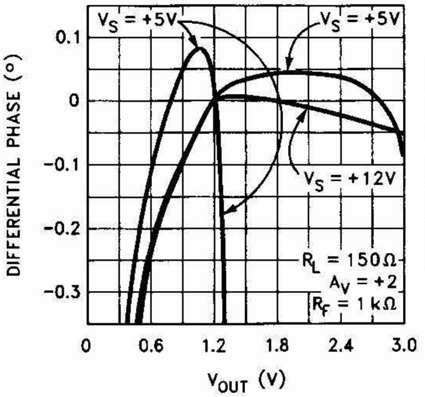
Typical Performance Curves — Contd.

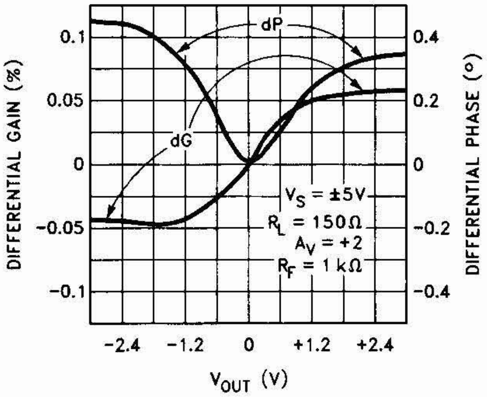
Differential Gain for Single Supply Operation



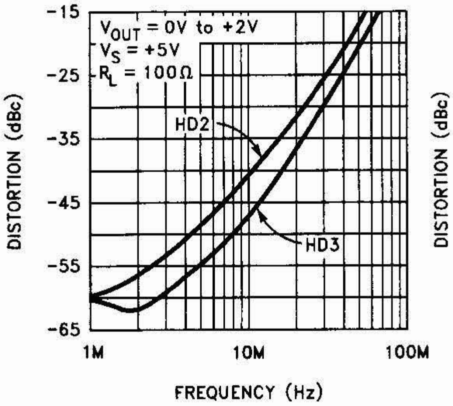
Differential Phase for Single Supply Operation



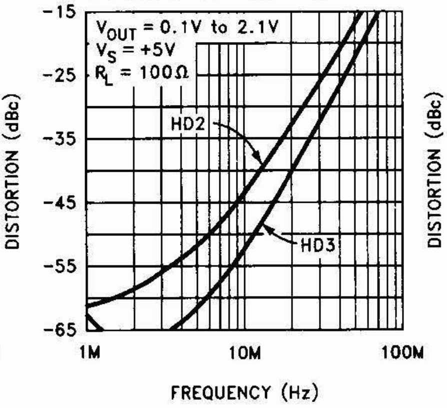
Differential Gain and Phase for Dual Supply Operation



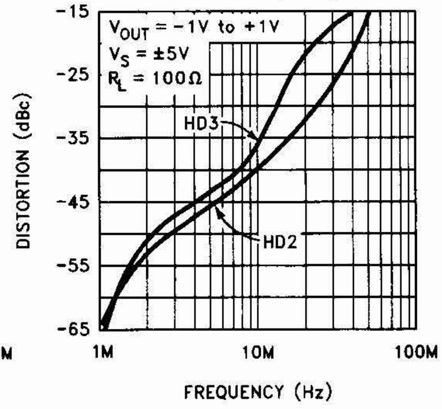
2nd and 3rd Harmonic Distortion vs Frequency



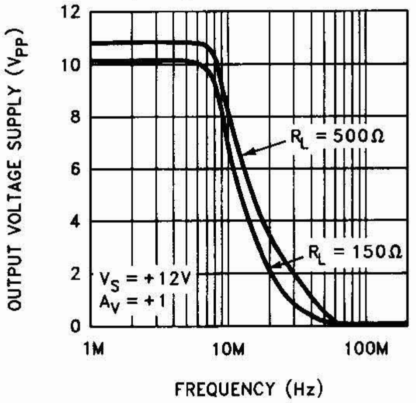
2nd and 3rd Harmonic Distortion vs Frequency



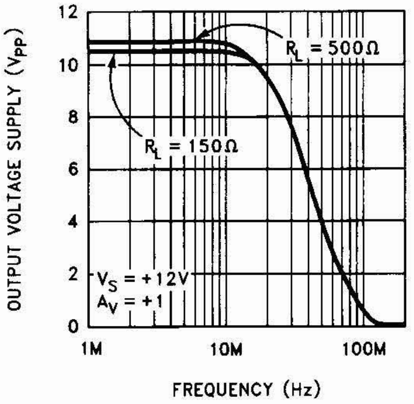
2nd and 3rd Harmonic Distortion vs Frequency



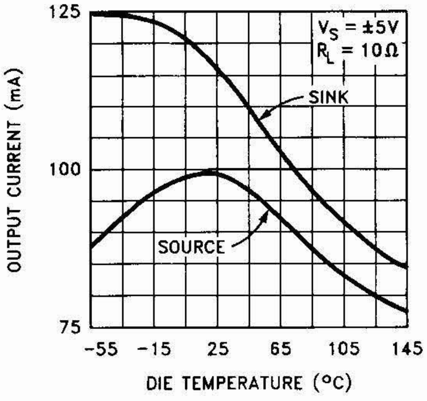
Output Voltage Swing vs Frequency for THD < 0.1%



Output Voltage Swing vs Frequency for Unlimited Distortion



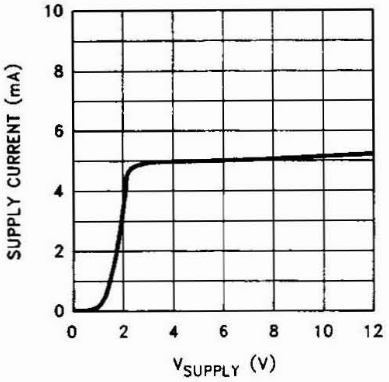
Output Current vs Die Temperature



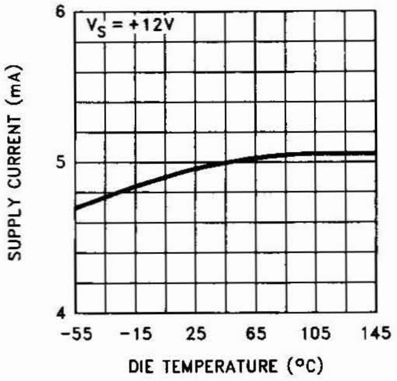
2150-77

Typical Performance Curves — Contd.

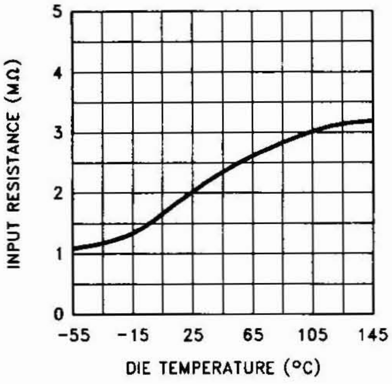
Supply Current vs Supply Voltage



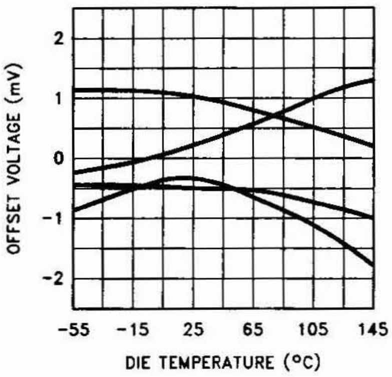
Supply Current vs Die Temperature



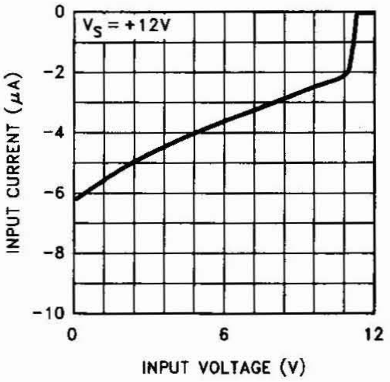
Input Resistance vs Die Temperature



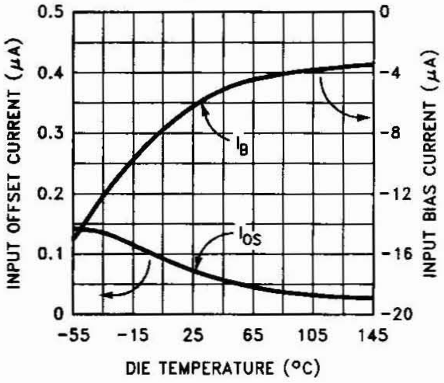
Offset Voltage vs Die Temperature (4 Samples)



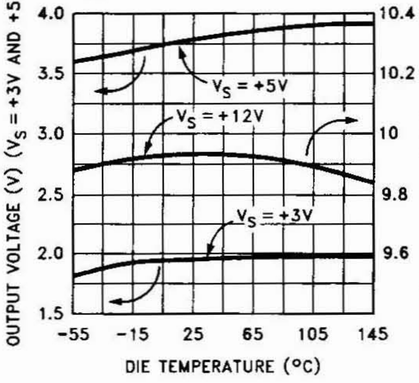
Input Bias Current vs Input Voltage



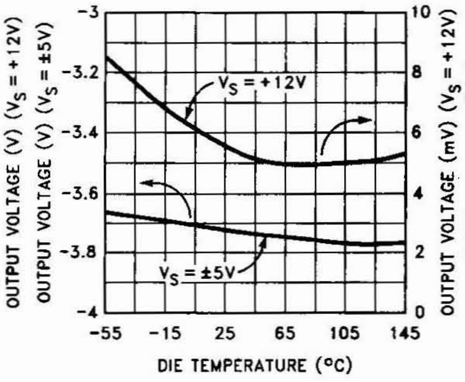
Input Offset Current and Input Bias Current vs Die Temperature



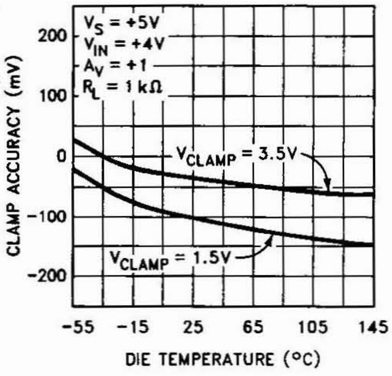
Positive Output Voltage Swing vs Die Temperature, R_L = 150Ω to GND



Negative Output Voltage Swing vs Die Temperature, R_L = 150Ω to GND



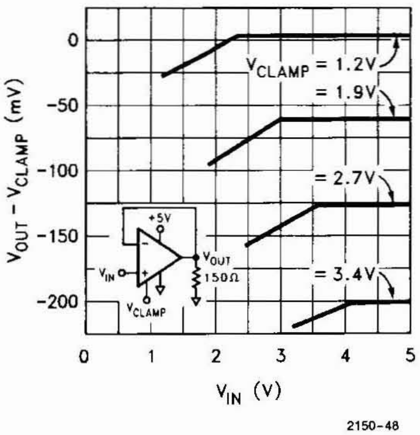
Clamp Accuracy vs Die Temperature



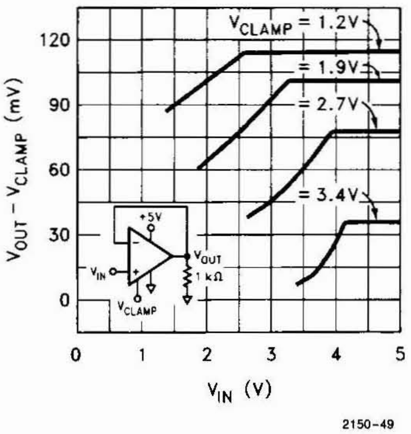
2150-78

Typical Performance Curves — Contd.

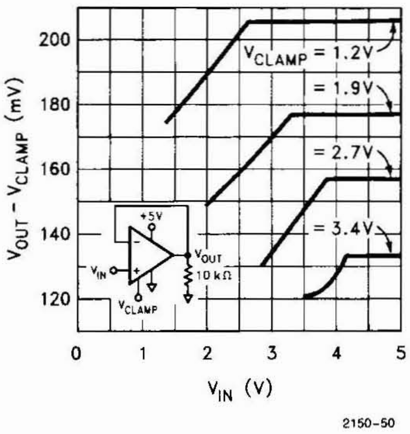
Clamp Accuracy
R_L = 150Ω



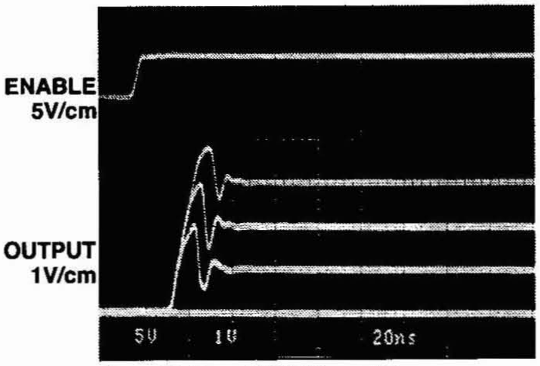
Clamp Accuracy
R_L = 1 kΩ



Clamp Accuracy
R_L = 10 kΩ

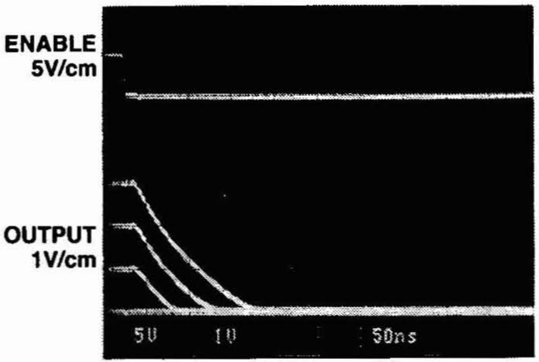


Enable Response for a Family of DC Inputs



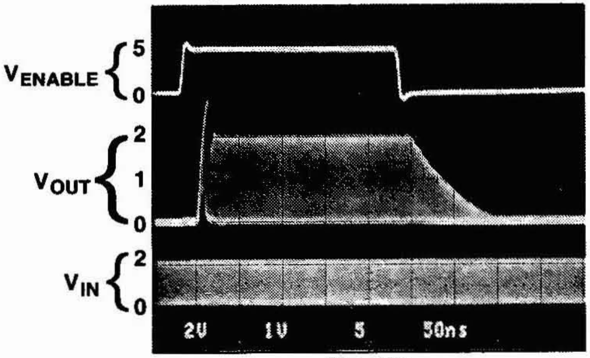
A_V = +1, R_L = 150Ω, V_S = +5V

Disable Response for a Family of DC Inputs



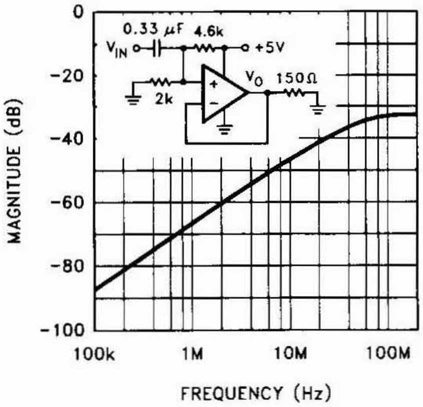
A_V = +1, R_L = 150Ω, V_S = +5V

Disable/Enable Response for a Family of Sine Waves



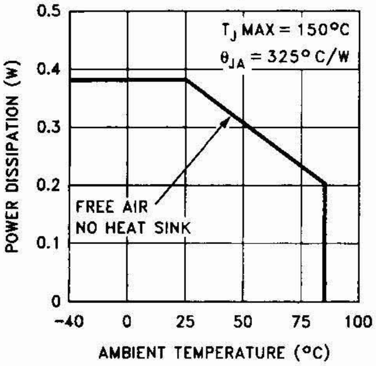
50 ns/div

OFF Isolation



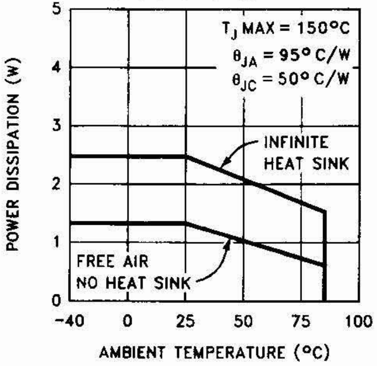
Typical Performance Curves — Contd.

5-Lead Plastic SOT23
Maximum Power Dissipation
vs Ambient Temperature



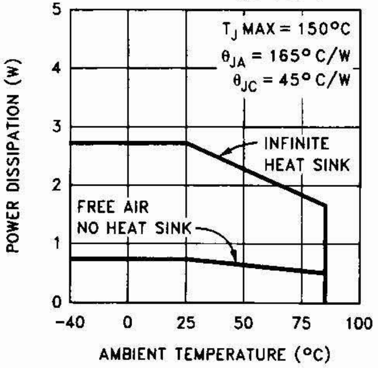
2150-54

8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



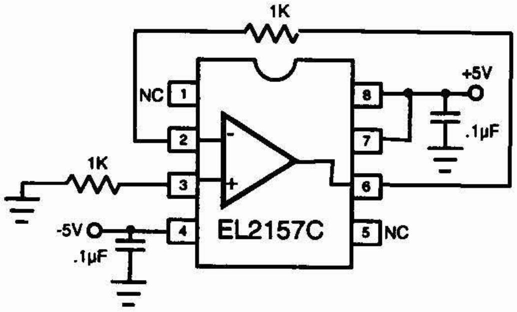
2150-55

8-Lead Plastic SO
Maximum Power Dissipation
vs Ambient Temperature



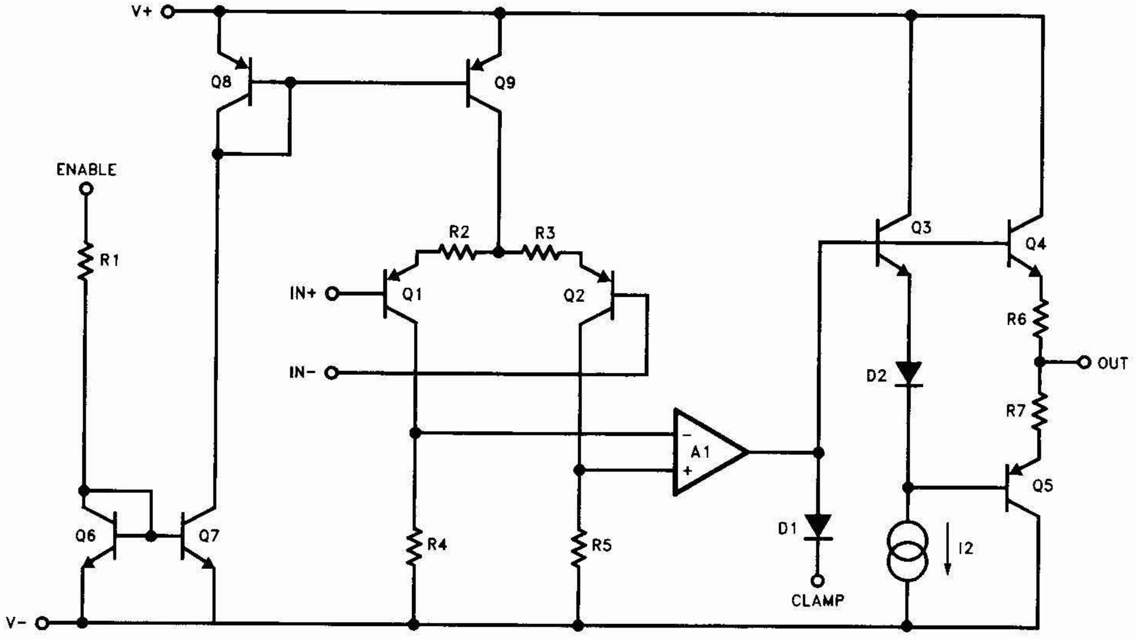
2150-56

Burn-In Circuit


1K
NC
1
2
3
4
8
7
6
5
NC
+5V
.1μF
1K
-5V
.1μF
EL2157C

2150-57

Simplified Schematic


V+
Q8
Q9
ENABLE
R1
R2
R3
IN+
Q1
Q2
IN-
Q3
Q4
R6
OUT
D2
R7
A1
Q5
Q6
Q7
R4
R5
D1
CLAMP
I2
V-

2150-58

Applications Information

Product Description

The EL2150C/EL2157C are the industry's fastest single supply operational amplifiers. Connected in voltage follower mode, their −3dB bandwidth is 125 MHz while maintaining a 275 V/μs slew rate. With an input and output common mode range that includes ground, these amplifiers were optimized for single supply operation, but will also accept dual supplies. They operate on a total supply voltage range as low as +2.7V or up to +12V. This makes them ideal for +3V applications, especially portable computers.

While many amplifiers claim to operate on a single supply, and some can sense ground at their inputs, most fail to truly drive their outputs to ground. If they do succeed in driving to ground, the amplifier often saturates, causing distortion and recovery delays. However, special circuitry built into the EL2150C/EL2157C allows the output to follow the input signal to ground without recovery delays.

Power Supply Bypassing And Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor has been shown to work well when placed at each supply pin. For single supply operation, where pin 4 (V_{S-}) is connected to the ground plane, a single 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor across pins 7 and 4 will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction should be used. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Supply Voltage Range and Single-Supply Operation

The EL2150C/EL2157C have been designed to operate with supply voltages having a span of greater than 2.7V, and less than 12V. In practical terms, this means that the EL2150C/EL2157C will operate on dual supplies ranging from ±1.35V to ±6V. With a single-supply, the EL2150C/EL2157C will operate from +2.7V to +12V. Performance has been optimized for a single +5V supply.

Pins 7 and 4 are the power supply pins. The positive power supply is connected to pin 7. When used in single supply mode, pin 4 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2150C/EL2157C have an input voltage range that includes the negative supply and extends to within 1.2V of the positive supply. So, for example, on a single +5V supply, the EL2150C/EL2157C have an input range which spans from 0V to 3.8V.

The output range of the EL2150C/EL2157C is also quite large. It includes the negative rail, and extends to within 1V of the top supply rail. On a +5V supply, the output is therefore capable of swinging from 0V to +4V. On split supplies, the output will swing ±4V. If the load resistor is tied to the negative rail and split supplies are used, the output range is extended to the negative rail.

Choice Of Feedback Resistor, R_F

The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value which should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few picofarad range in parallel with R_F can help to reduce this ringing and peaking at the expense of reducing the bandwidth.

Applications Information — Contd.

As far as the output stage of the amplifier is concerned, $R_F + R_G$ appear in parallel with R_L for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F has a minimum value that should not be exceeded for optimum performance.

For $A_V = +1$, $R_F = 0\Omega$ is optimum. For $Av = -1$ or $+2$ (noise gain of 2), optimum response is obtained with R_F between 500Ω and 1 kΩ. For $Av = -4$ or $+5$ (noise gain of 5), keep R_F between 2 kΩ and 10 kΩ.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This can be difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Differential Gain and Differential Phase for the EL2150C/EL2157C are specified with the black level of the output video signal set to +1.2V. This allows ample room for the sync pulse even in a gain of +2 configuration. This results in dG and dP specifications of 0.05% and 0.05° while driving 150Ω at a gain of +2. Setting the black level to other values, although acceptable, will compromise peak performance. For example, looking at the single supply dG and dP curves for $R_L = 150\ \Omega$, if the output black level clamp is reduced from 1.2V to 0.6V dG/dP will increase from 0.05%/0.05° to 0.08%/0.25° Note that in a gain of +2 configuration, this is the lowest black level allowed such that the sync tip doesn't go below 0V.

If your application requires that the output goes to ground, then the output stage of the EL2150C/EL2157C, like all other single supply op amps, requires an external pull down resistor tied to ground. As mentioned above, the current flowing through this resistor becomes the DC bias current for the output stage NPN transistor. As this current approaches zero, the NPN turns off, and dG and dP will increase. This becomes more critical as the load resistor is increased in value. While driving a light load, such as 1 kΩ, if the input black level is kept above 1.25V, dG and dP are a respectable 0.03% and 0.03°.

For other biasing conditions see the Differential Gain and Differential Phase vs. Input Voltage curves.

Output Drive Capability

In spite of their moderately low 5 mA of supply current, the EL2150C/EL2157C are capable of providing ±100 mA of output current into a 10Ω load, or ±60 mA into 50Ω. With this large output current capability, a 50Ω load can be driven to ±3V with $V_S = \pm 5V$, making it an excellent choice for driving isolation transformers in telecommunications applications.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will de-couple the EL2150C/EL2157C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output.

Disable/Power-Down

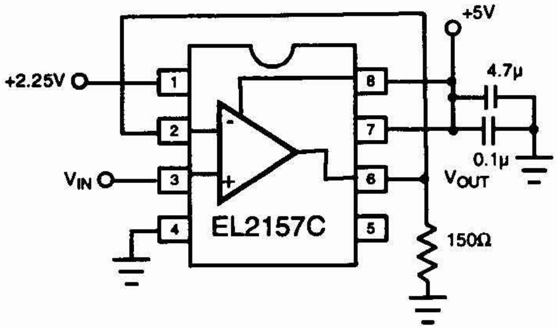
The EL2157C amplifier can be disabled, placing its output in a high-impedance state. The disable or enable action takes only about 40 nsec. When disabled, the amplifier's supply current is reduced to 0 mA, thereby eliminating all power consumption by the EL2157C. The EL2157C amplifier's power down can be controlled by standard CMOS signal levels at the ENABLE pin. The applied CMOS signal is relative to the GND pin. For example, if a single +5V supply is used, the logic voltage levels will be +0.5V and +2.0V. If using dual ±5V supplies, the logic levels will be −4.5V and −3.0V. Letting the ENABLE pin float will disable the EL2157C. If the power-down feature is not desired, connect the ENABLE pin to the V_S+ pin. The guaranteed logic levels of +0.5V and +2.0V are not standard TTL levels of +0.8V and +2.0V, so care must be taken if standard TTL will be used to drive the ENABLE pin.

Applications Information — Contd.

Output Voltage Clamp

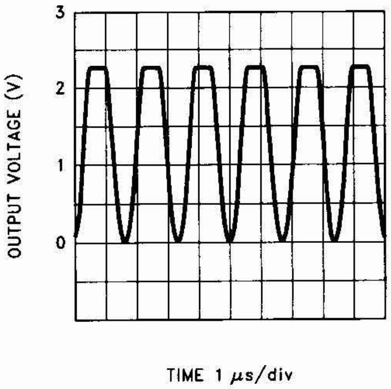
The EL2157C amplifier has an output voltage clamp. This clamping action is fast, being activated almost instantaneously, and being deactivated in < 7 ns, and prevents the output voltage from going above the preset clamp voltage. This can be very helpful when the EL2157C is used to drive an A/D converter, as some converters can require long times to recover if overdriven. The output voltage remains at the clamp voltage level as long as the product of the input voltage and the gain setting exceeds the clamp voltage. If the EL2157C is connected in a gain of 2, for example, and +3V DC is applied to the CLAMP pin, any voltage higher than +1.5V at the inputs will be clamped and +3V will be seen at the output.

Figure 1 below is a unity gain connected EL2157C being driven by a 3Vp-p sinewave, with 2.25V applied to the CLAMP pin. The resulting output waveform, with its output being clamped to 2.25V, is shown in Figure 2.



2150-59

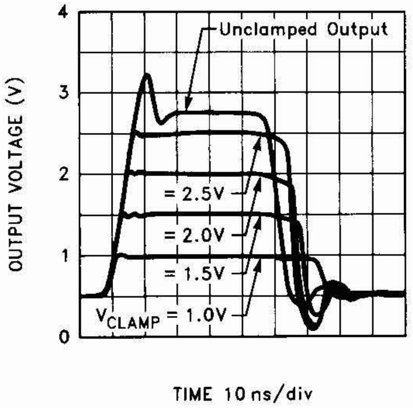
Figure 1



2150-60

Figure 2

Figure 3 shows the output of the same circuit being driven by a 0.5V to 2.75V square wave, as the clamp voltage is varied from 1.0V to 2.5V, as well as the unclamped output signal. The rising edge of the signal is clamped to the voltage applied to the CLAMP pin almost instantaneously. The output recovers from the clamped mode within 5 - 7 ns, depending on the clamp voltage. Even when the CLAMP pin is taken 0.2V below the minimum 1.2V specified, the output is still clamped and recovers in about 11 ns.



2150-61

Figure 3

The clamp accuracy is affected by 1) the CLAMP pin voltage, 2) the input voltage, and 3) the load resistor. Depending upon the application, the accuracy may be as little as a few tens of millivolts to a few hundred millivolts. Be sure to allow for these inaccuracies when choosing the clamp voltage. Curves of Clamp Accuracy vs. V_{CLAMP}, and V_{IN} for 3 values of R_L are included in the Typical Performance Curves Section

Unlike amplifiers that clamp at the input and are therefore limited to non-inverting applications only, the EL2157C output clamp architecture works for both inverting and non-inverting gain applications. There is also no maximum voltage difference limitation between V_{IN} and V_{CLAMP} which is common on input clamped architectures.

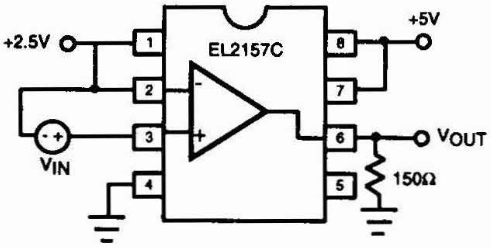
The voltage clamp operates for any voltage between +1.2V above the GND pin, and the minimum output voltage swing, V_{OP}. Forcing the CLAMP pin much below +1.2V can saturate transistors and should therefore be avoided.

Applications Information — Contd.

Forcing the CLAMP pin above V_{OP} simply deactivates the CLAMP feature. In other words, one cannot expect to clamp any voltage higher than what the EL2157C can drive to in the first place. If the clamp feature is not desired, either let the CLAMP pin float or connect it to the V_S+ pin.

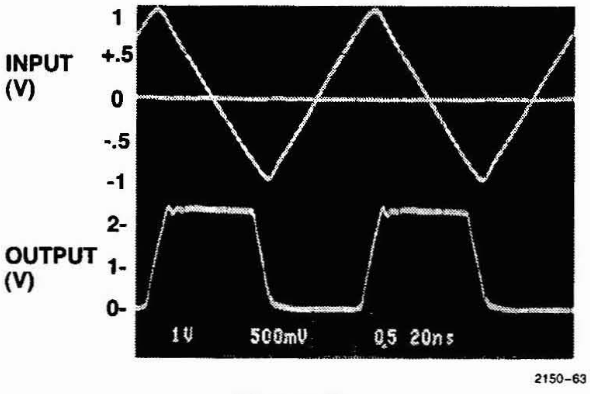
EL2157C Comparator Application

The EL2157C can be used as a very fast, single supply comparator by utilizing the clamp feature. Most op amps used as comparators allow only slow speed operation because of output saturation issues. However, by applying a DC voltage to the CLAMP pin of the EL2157C, the maximum output voltage can be clamped, thus preventing saturation. Figure 4 below is the EL2157C implemented as a comparator. 2.5V DC is applied to the CLAMP pin, as well as the IN− pin. A differential signal is then applied between the inputs. Figure 5 shows the output square wave that results when a ±1V, 10 MHz triangular wave is applied, while Figure 6 is a graph of propagation delay vs. overdrive as a square wave is presented at the input.



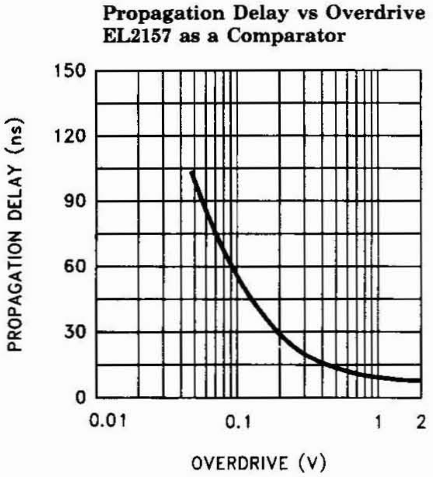
2150-62

Figure 4



2150-63

Figure 5

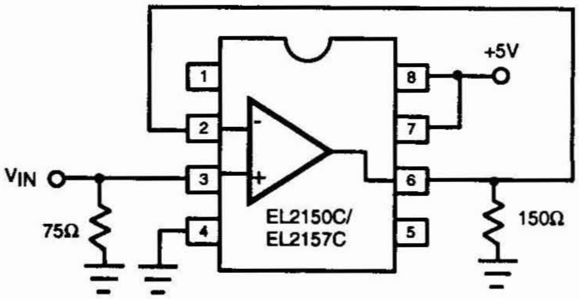


2150-64

Figure 6

Video Sync Pulse Remover Application

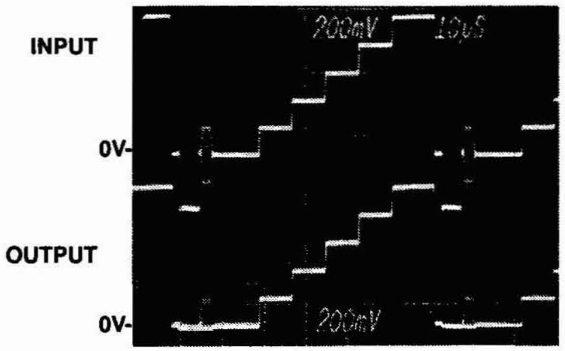
All CMOS Analog to Digital Converters (A/Ds) have a parasitic latch-up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off. Figure 7 shows a unity gain connected EL2150C/ EL2157C. Figure 8 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.



2150-65

Figure 7

Applications Information — Contd.

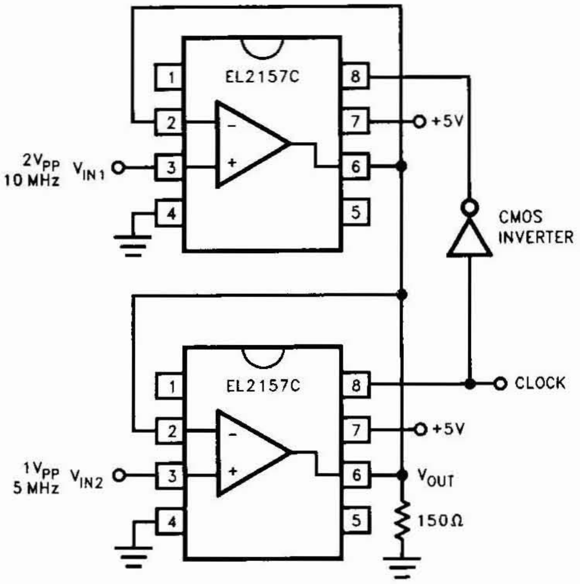


2150-66

Figure 8

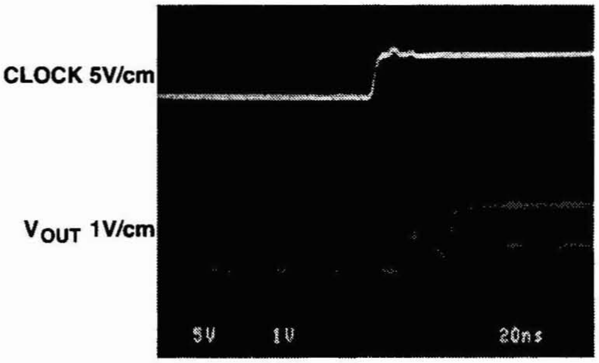
Multiplexing with the EL2157C

The ENABLE pin on the EL2157C allows for multiplexing applications. Figure 9 shows two EL2157Cs with their outputs tied together, driving a back terminated 75Ω video load. A 2 Vp-p 10 MHz sinewave is applied at one input, and a 1 Vp-p 5 MHz sinewave to the other. Figure 10 shows the CLOCK signal which is applied, and the resulting output waveform at V_{OUT}. Switching is complete in about 50 ns. Notice the outputs are tied directly together. Decoupling resistors at each output are not necessary. In fact, adding them approximately doubles the switching time to 100 nsec.



2150-67

Figure 9



2150-68

Figure 10

Short Circuit Current Limit

The EL2150C/EL2157C have internal short circuit protection circuitry that protect it in the event of its output being shorted to either supply rail. This limit is set to around 100 mA nominally and reduces with increasing junction temperature. It is intended to handle temporary shorts. If an output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ± 90 mA. A heat sink may be required to keep the junction temperature below absolute maximum when an output is shorted indefinitely.

Power Dissipation

With the high output drive capability of the EL2150C/EL2157C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2150C/EL2157C to remain in the safe operating area.

Applications Information — Contd.

The maximum power dissipation allowed in a package is determined according to [1]:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad [1]$$

where:

T_{JMAX} = Maximum Junction Temperature
T_{AMAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
PD_{MAX} = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or [2]

$$PD_{MAX} = V_S{}^*I_{SMAX} + (V_S - V_{OUT}){}^*\frac{V_{OUT}}{R_L} \quad [2]$$

where:

V_S = Total Supply Voltage
I_{SMAX} = Maximum Supply Current
V_{OUT} = Maximum Output Voltage of the Application
R_L = Load Resistance tied to Ground

If we set the two PD_{MAX} equations, [1] & [2], equal to each other, and solve for V_S, we can get a family of curves for various loads and output voltages according to [3]:

$$V_S = \frac{\dfrac{R_L * (T_{JMAX} - T_{AMAX})}{\theta_{JA}} + (V_{OUT})^2}{(I_S * R_L) + V_{OUT}} \quad [3]$$

Figures 11 through 13 show total single supply voltage V_S vs. R_L for various output voltage swings for the PDIP and SOIC packages. The curves assume WORST CASE conditions of T_A = +85°C and I_S = 6.5 mA.

Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (PDIP Package)

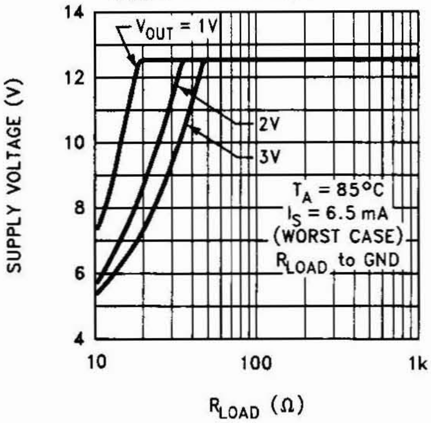


Figure 11

Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)

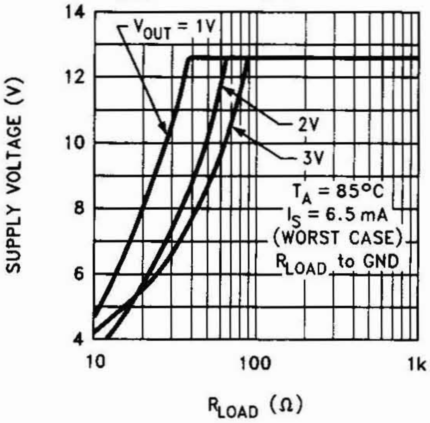


Figure 12

Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (SOT23-5 Package)

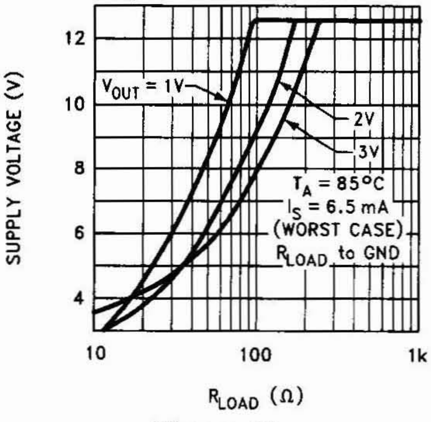


Figure 13

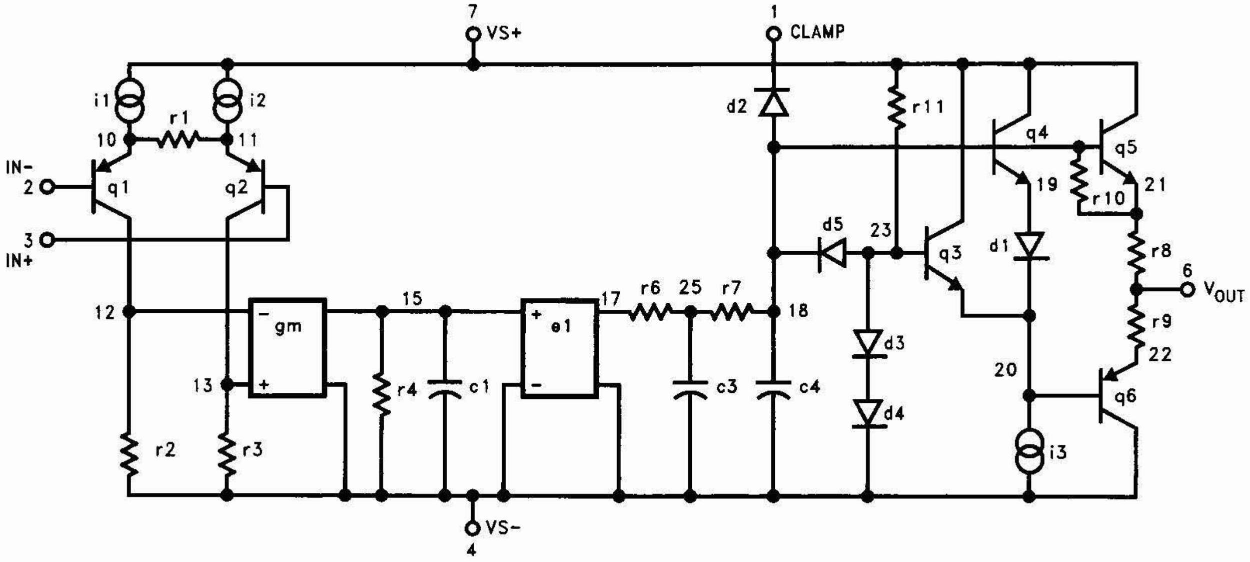
Applications Information — Contd.

EL2157C Macromodel

```
* Revision A, July 1995
* When not being used, the clamp pin, pin 1,
* should be connected to +Vsupply, pin 7
* Connections:     +input
*                    |   -input
*                    |     |   +Vsupply
*                    |     |     |   -Vsupply
*                    |     |     |     |   output
*                    |     |     |     |     |   clamp
*                    |     |     |     |     |     |
.subckt EL2157/el    3     2     7     4     6     1
*
* Input Stage
*
i1 7 10 250uA
i2 7 11 250uA
r1 10 11 4k
q1 12 2 10 qp
q2 13 3 11 qpa
r2 12 4 100
r3 13 4 100
*
* Second Stage & Compensation
*
gm 15 4 13 12 4.6m
r4 15 4 15Meg
c1 15 4 0.36pF
*
* Poles
*
e1 17 4 15 4 1.0
r6 17 25 400
c3 25 4 1pF
r7 25 18 500
c4 18 4 1pF
*
```

```
* Output Stage & Clamp
*
i3 20 4 1.0mA
q3 7 23 20 qn
q4 7 18 19 qn
q5 7 18 21 qn
q6 4 20 22 qp
q7 7 23 18 qn
d1 19 20 da
d2 18 1 da
r8 21 6 2
r9 22 6 2
r10 18 21 10k
r11   7 23 100k
d3 23 24 da
d4 24   4 da
d5 23 18 da
*
* Power Supply Current
*
ips 7 4 3.2mA
*
* Models
*
.model qn npn(is=800e-18 bf=150 tf=0.02nS)
.model qpa pnp(is=810e-18 bf=50 tf=0.02nS)
.model qp pnp(is=800e-18 bf=54 tf=0.02nS)
.model da d(tt=0nS)
.ends
```

EL2157C Macromodel — Contd.


7
VS+
1
CLAMP
i1
i2
r1
10
11
IN-
2
q1
q2
3
IN+
d2
r11
q4
q5
19
r10
21
d5
23
q3
d1
r8
6
VOUT
12
gm
15
e1
17
r6
25
r7
18
13
r4
c1
c3
c4
d3
d4
r9
22
20
q6
i3
r2
r3
VS-
4

2150-71

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2250C/EL2450C

125 MHz Single Supply Dual/Quad Op Amps

Features

- Specified for +3V, +5V, or ±5V Applications
- Large Input Common Mode Range
  $0V < V_{CM} < V_S - 1.2V$
- Output Swings to Ground Without Saturating
- −3 dB Bandwidth = 125 MHz
- ± 0.1 dB Bandwidth = 30 MHz
- Low Supply Current = 5 mA (per amplifier)
- Slew Rate = 275 V/µsec
- Low Offset Voltage = 2 mV max
- Output Current = ±100 mA
- High Open Loop Gain = 80 dB
- Differential Gain = 0.05%
- Differential Phase = 0.05°

Applications

- Video Amplifier
- PCMCIA Applications
- A/D Driver
- Line Driver
- Portable Computers
- High Speed Communications
- RGB Printer, FAX, Scanner
- Broadcast Equipment
- Active Filtering

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2250CN	−40°C to +85°C	8 Pin PDIP	MDP0031
EL2250CS	−40°C to +85°C	8 Pin SOIC	MDP0027
EL2450CN	−40°C to +85°C	14 Pin PDIP	MDP0031
EL2450CS	−40°C to +85°C	14 Pin SOIC	MDP0027

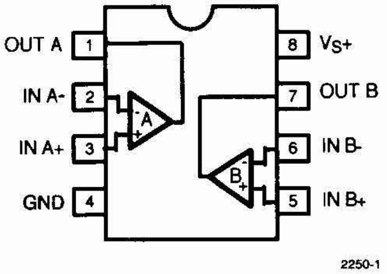
General Description

The EL2250C/EL2450C are part of a family of the electronics industries fastest single supply op amps available. Prior single supply op amps have generally been limited to bandwidths and slew rates ¼ that of the EL2250C/EL2450C. The 125 MHz bandwidth, 275 V/µsec slew rate, and 0.05%/0.05° differential gain/differential phase makes this part ideal for single or dual supply video speed applications. With its voltage feedback architecture, this amplifier can accept reactive feedback networks, allowing them to be used in analog filtering applications. The inputs can sense signals below the bottom supply rail and as high as 1.2V below the top rail. Connecting the load resistor to ground and operating from a single supply, the outputs swing completely to ground without saturating. The outputs can also drive to within 1.2V of the top rail. The EL2250C/EL2450C will output ±100 mA and will operate with single supply voltages as low as 2.7V, making them ideal for portable, low power applications.

The EL2250C/EL2450C are available in plastic DIP and SOIC packages in industry standard pin outs. Both parts operate over the industrial temperature range of −40°C to +85°C, and are part of a family of single supply op amps. For single amplifier applications, see the EL2150C/EL2157C. For dual and triple amplifiers with power down and output voltage clamps, see the EL2257C/EL2357C.

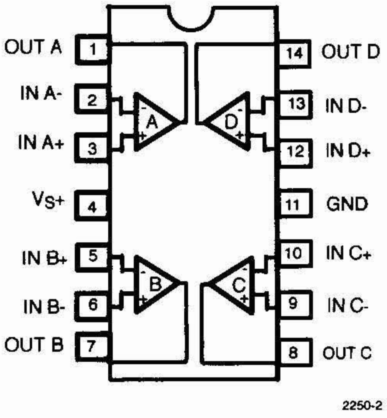
Connection Diagrams

EL2250C SO, P-DIP



Top View

EL2450C SO, P-DIP



Top View

April 1996 Rev A

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S and GND	+12.6V	Power Dissipation	See Curves
Input Voltage (IN+, IN−)	GND−0.3V, V_S+0.3V	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	±6V	Ambient Operating Temperature Range	−40°C to +85°C
Maximum Output Current	90 mA	Operating Junction Temperature	150°C
Output Short Circuit Duration	(Note 1)		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = +5V, GND = 0V, T_A = 25°C, V_{CM} = 1.5V, V_{OUT} = 1.5V, unless otherwise specified.

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage		−4		4	I	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{min} to T_{max}		10		V	µV/°C
IB	Input Bias Current	V_{IN} = 0V		−5.5	−10	I	µA
I_{OS}	Input Offset Current	V_{IN} = 0V	−750	150	750	I	nA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{min} to T_{max}		50		V	nA/°C
PSRR	Power Supply Rejection Ratio	V_S = +2.7V to +12V	55	70		I	dB
CMRR	Common Mode	VCM = 0V to +3.8V	55	65		I	dB
	Rejection Ratio	VCM = 0V to +3.0V	55	70		I	dB
CMIR	Common Mode Input Range		0		V_S − 1.2	I	V
R_{IN}	Input Resistance	Common Mode	1	2		I	MΩ
C_{IN}	Input Capacitance	SOIC Package		1		V	pF
		PDIP Package		1.5		V	pF
R_{OUT}	Output Resistance	A_V = +1		40		V	mΩ
I_S	Supply Current (per amplifier)	V_S = +12V		5	6.5	I	mA
PSOR	Power Supply Operating Range		2.7		12.0	I	V

DC Electrical Characteristics

$V_S = +5V$, GND = 0V, $T_A = 25°C$, $V_{CM} = +1.5V$, $V_{OUT} = +1.5V$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
AVOL	Open Loop Gain	$V_S = +12V$, $V_{OUT} = +2V$ to $+9V$, $R_L = 1\ k\Omega$ to GND	65	80		I	dB
		$V_{OUT} = +1.5V$ to $+3.5V$, $R_L = 1\ k\Omega$ to GND		70		V	dB
		$V_{OUT} = +1.5V$ to $+3.5V$, $R_L = 150\Omega$ to GND		60		V	dB
V_{OP}	Positive Output Voltage Swing	$V_S = +12V$, $A_V = +1$, $R_L = 1\ k\Omega$ to 0V		10.8		V	V
		$V_S = +12V$, $A_V = +1$, $R_L = 150\Omega$ to 0V	9.6	10.0		I	V
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 1\ k\Omega$ to 0V		4.0		V	V
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 150\Omega$ to 0V	3.4	3.8		I	V
		$V_S = +3V$, $A_V = +1$, $R_L = 150\Omega$ to 0V	1.8	1.95		I	V
V_{ON}	Negative Output Voltage Swing	$V_S = +12V$, $A_V = +1$, $R_L = 150\Omega$ to 0V		5.5	8	I	mV
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 1\ k\Omega$ to 0V		−4.0		V	V
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 150\Omega$ to 0V		−3.7	−3.4	I	V
I_{OUT}	Output Current (Note 1)	$V_S = \pm 5V$, $A_V = +1$, $R_L = 10\Omega$ to 0V	±75	±100		I	mA
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 50\Omega$ to 0V		±60		V	mA

Closed Loop AC Electrical Characteristics

(Note 2) $V_S = +5V$, GND = 0V, $T_A = 25°C$, $V_{CM} = +1.5V$, $V_{OUT} = +1.5V$, $A_V = +1$, $R_F = 0\Omega$, $R_L = 150\Omega$ to GND pin, unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
BW	−3dB Bandwidth ($V_{OUT} = 400$ mVp-p)	$V_S = +5V$, $A_V = +1$, $R_F = 0\Omega$		125		V	MHz
		$V_S = +5V$, $A_V = -1$, $R_F = 500\Omega$		60		V	MHz
		$V_S = +5V$, $A_V = +2$, $R_F = 500\Omega$		60		V	MHz
		$V_S = +5V$, $A_V = +10$, $R_F = 500\Omega$		6		V	MHz
		$V_S = +12V$, $A_V = +1$, $R_F = 0\Omega$		150		V	MHz
		$V_S = +3V$, $A_V = +1$, $R_F = 0\Omega$		100		V	MHz
BW	±0.1 dB Bandwidth ($V_{OUT} = 400$ mVp-p)	$V_S = +12V$, $A_V = +1$, $R_F = 0\Omega$		25		V	MHz
		$V_S = +5V$, $A_V = +1$, $R_F = 0\Omega$		30		V	MHz
		$V_S = +3V$, $A_V = +1$, $R_F = 0\Omega$		20		V	MHz
GBWP	Gain Bandwidth Product	$V_S = +12V$, @ $A_V = +10$		60		V	MHz
PM	Phase Margin	$R_L = 1\ k\Omega$, $C_L = 6$ pF		55		V	°
SR	Slew Rate	$V_S = +10V$, $R_L = 150\Omega$, $V_{OUT} = 0V$ to $+6V$	200	275		I	V/μs
		$V_S = +5V$, $R_L = 150\Omega$, $V_{OUT} = 0V$ to $+3V$		300		V	V/μs
t_R, t_F	Rise Time, Fall Time	±0.1V Step		2.8		V	ns
OS	Overshoot	±0.1V Step		10		V	%
t_{PD}	Propagation Delay	±0.1V Step		3.2		V	ns
t_S	0.1% Settling Time	$V_S = \pm 5V$, $R_L = 500\Omega$, $A_V = +1$, $V_{OUT} = \pm 3V$		40		V	ns
	0.01% Settling Time	$V_S = \pm 5V$, $R_L = 500\Omega$, $A_V = +1$, $V_{OUT} = \pm 3V$		75		V	ns
dG	Differential Gain (Note 3)	$A_V = +2$, $R_F = 1\ k\Omega$		0.05		V	%
dP	Differential Phase (Note 3)	$A_V = +2$, $R_F = 1\ k\Omega$		0.05		V	°
e_N	Input Noise Voltage	f = 10 kHz		48		V	nV/√Hz
i_N	Input Noise Current	f = 10 kHz		1.25		V	pA/√Hz

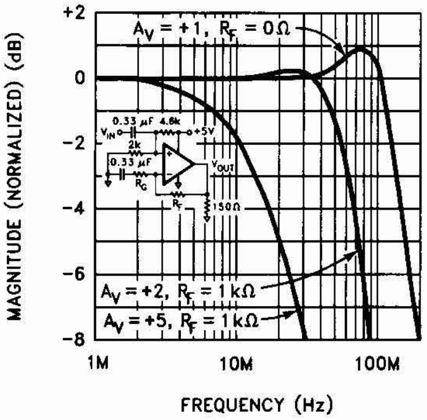
Note 1: Internal short circuit protection circuitry has been built into the EL2250C/EL2450C. See the Applications section.

Note 2: All AC tests are performed on a "warmed up" part, except slew rate, which is pulse tested.

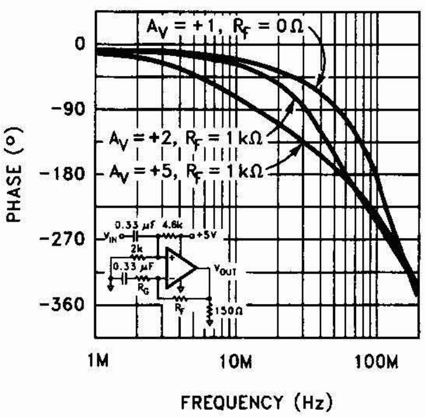
Note 3: Standard NTSC signal = 286 mVp-p, f = 3.58 MHz, as V_{IN} is swept from 0.6V to 1.314V. R_L is DC coupled.

Typical Performance Curves

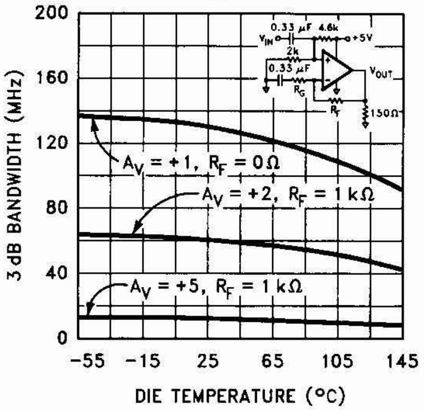
Non-Inverting Frequency Response (Gain)



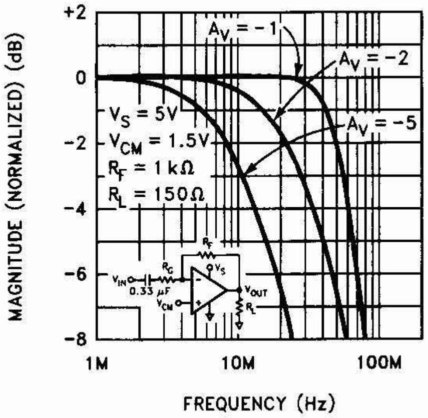
Non-Inverting Frequency Response (Phase)



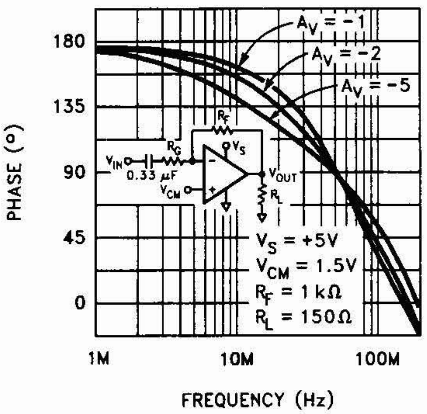
3 dB Bandwidth vs Temperature for Non-Inverting Gains



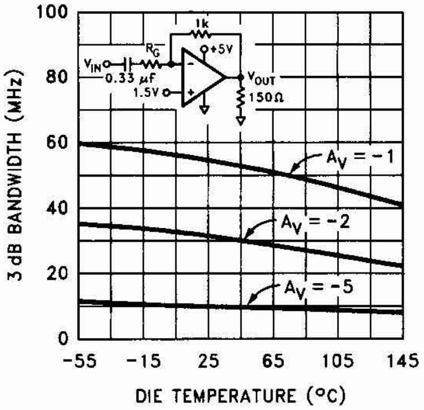
Inverting Frequency Response (Gain)



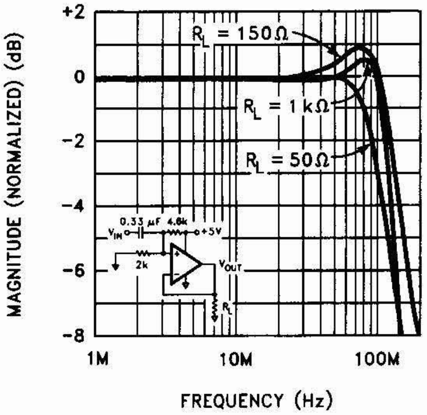
Inverting Frequency Response (Phase)



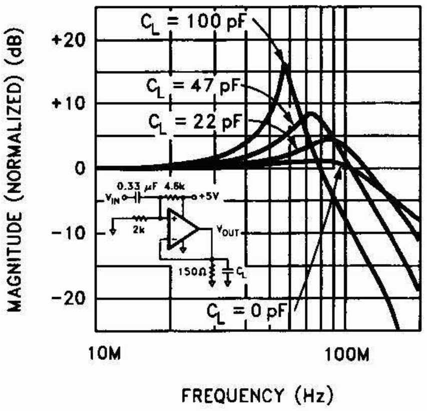
3 dB Bandwidth vs Temperature for Inverting Gains



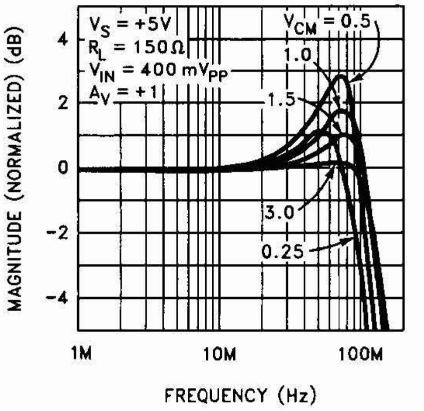
Frequency Response for Various R_L



Frequency Response for Various C_L



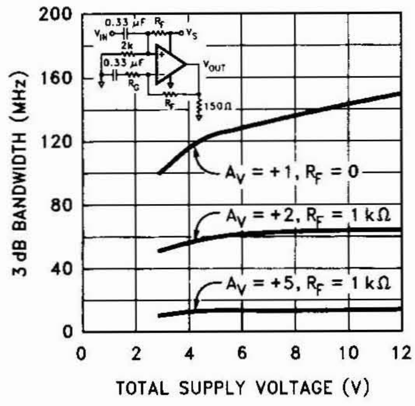
Non-Inverting Frequency Response vs Common Mode Voltage



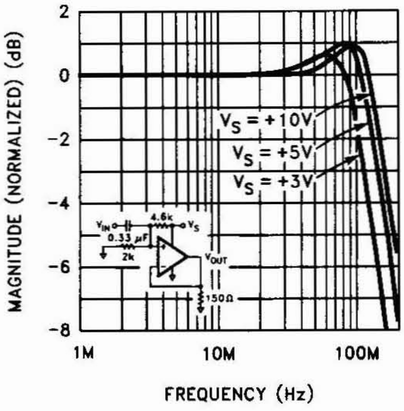
2250-3

Typical Performance Curves — Contd.

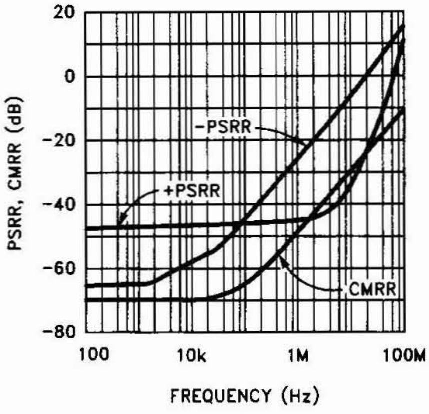
3 dB Bandwidth vs Supply Voltage for Non-Inverting Gains



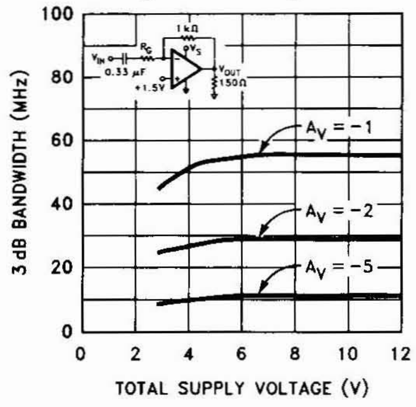
Frequency Response for Various Supply Voltages, A$_V$ = + 1



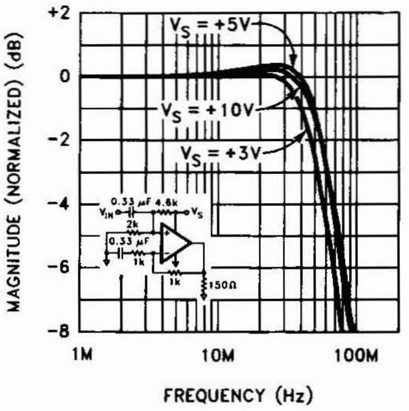
PSSR and CMRR vs Frequency



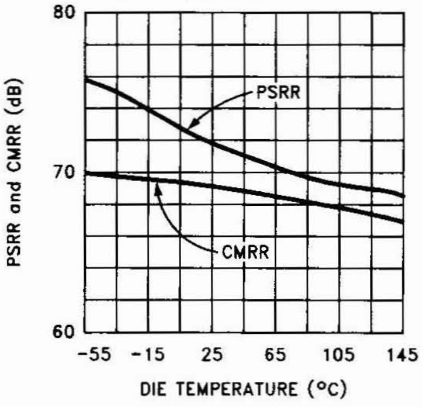
3 dB Bandwith vs Supply Voltage for Inverting Gains



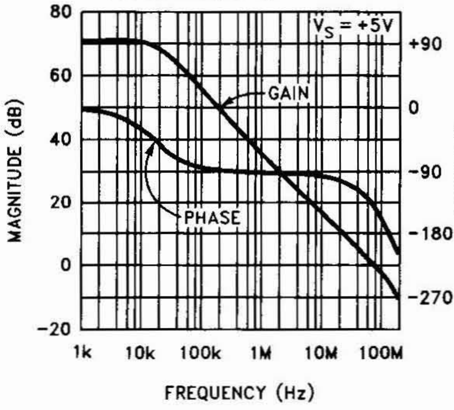
Frequency Response for Various Supply Voltages, A$_V$ = + 2



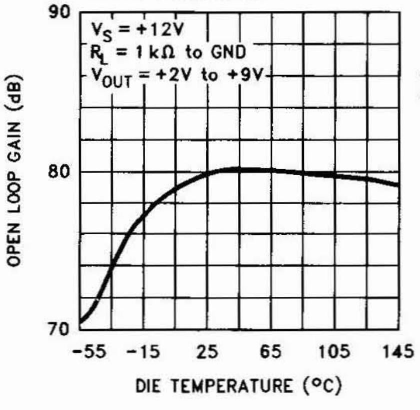
PSRR and CMRR vs Die Temperature



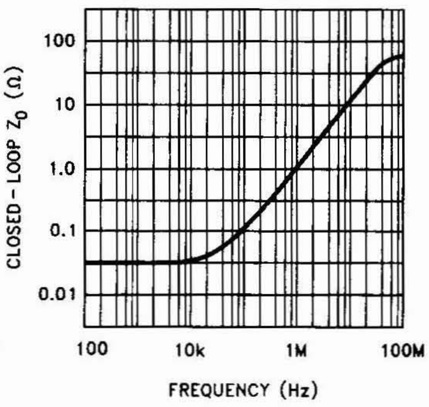
Open Loop Gain and Phase vs Frequency



Open Loop Voltage Gain vs Die Temperature



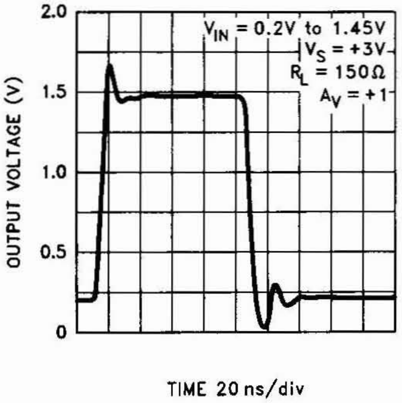
Closed Loop Output Impedance vs Frequency



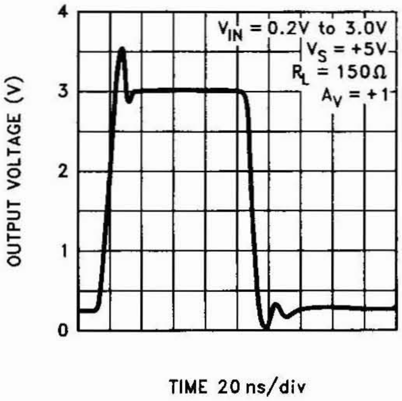
2250-4

Typical Performance Curves — Contd.

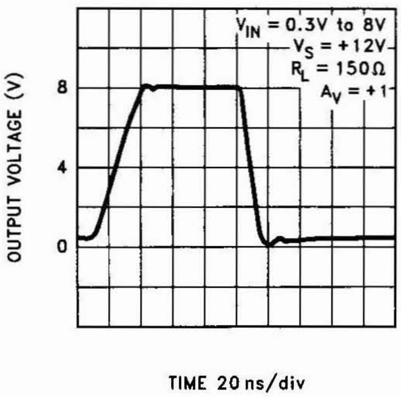
Large Signal Step Response, V_S = +3V



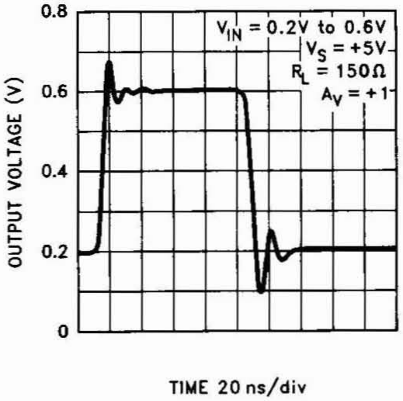
Large Signal Step Response, V_S = +5V



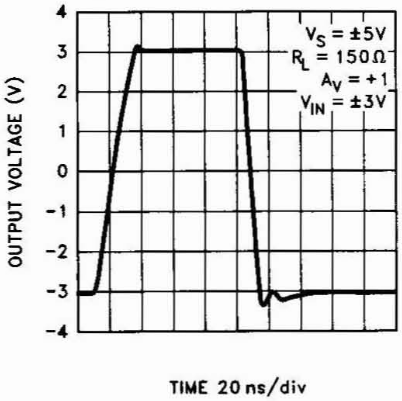
Large Signal Step Response, V_S = +12V



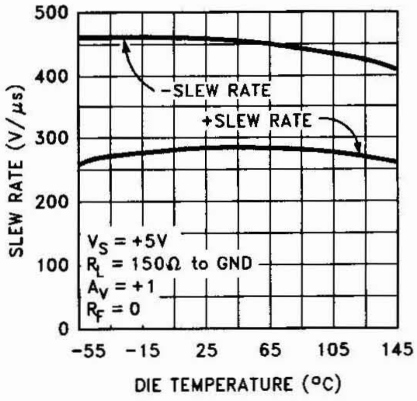
Small Signal Step Response



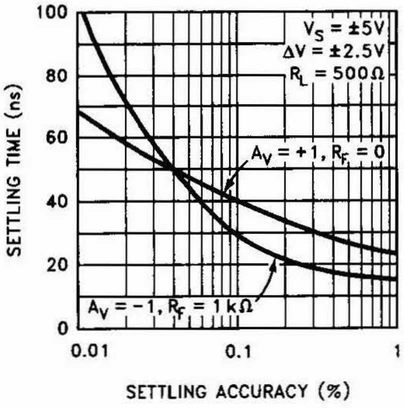
Large Signal Step Response, V_S = ±5V



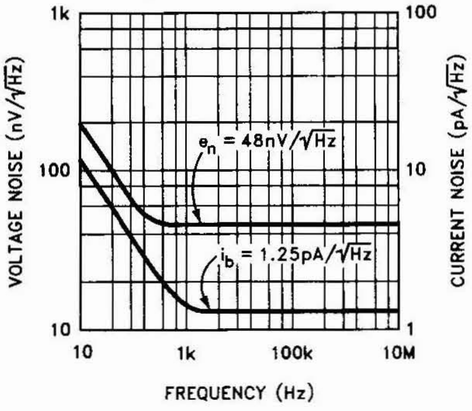
Slew Rate vs Temperature



Settling Time vs Settling Accuracy



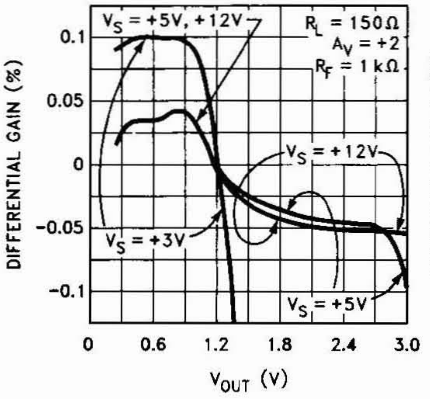
Voltage and Current Noise vs Frequency



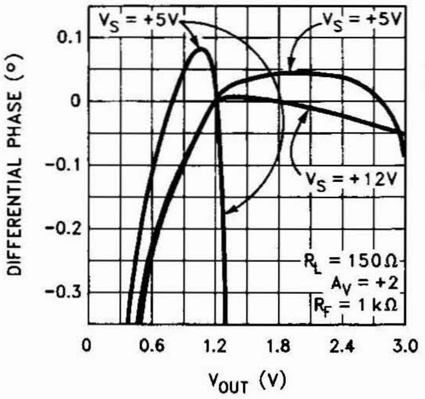
2250-5

Typical Performance Curves — Contd.

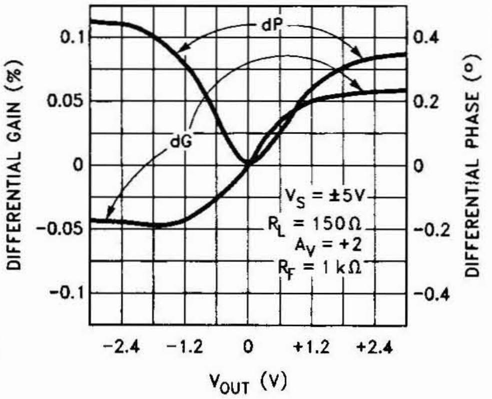
Differential Gain for Single Supply Operation



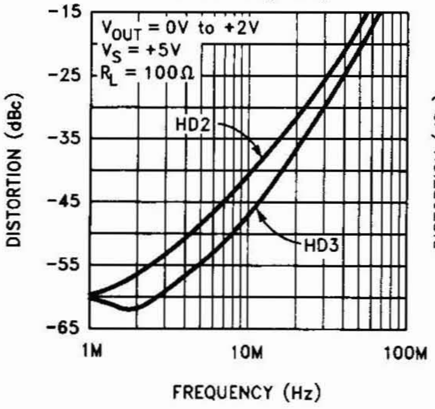
Differential Phase for Single Supply Operation



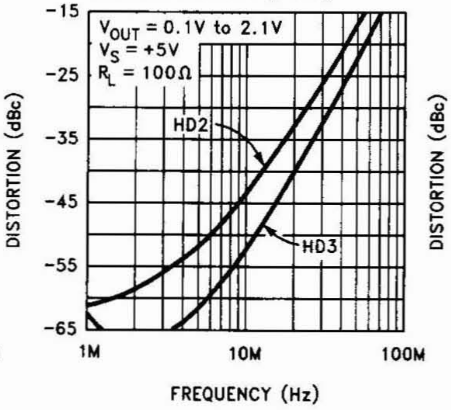
Differential Gain and Phase for Dual Supply Operation



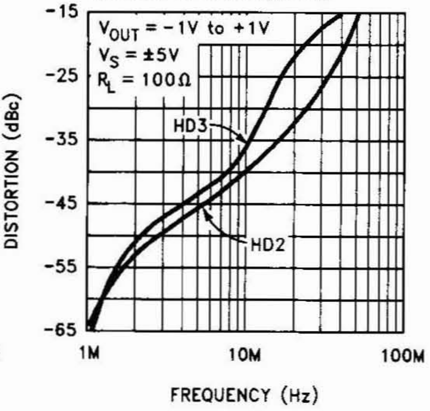
2nd and 3rd Harmonic Distortion vs Frequency



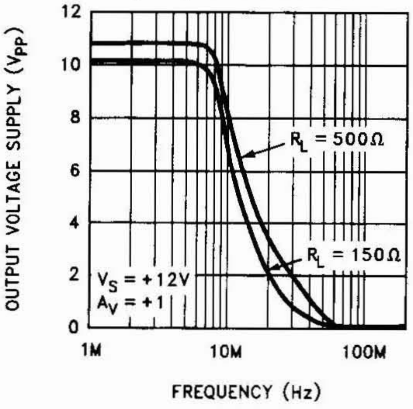
2nd and 3rd Harmonic Distortion vs Frequency



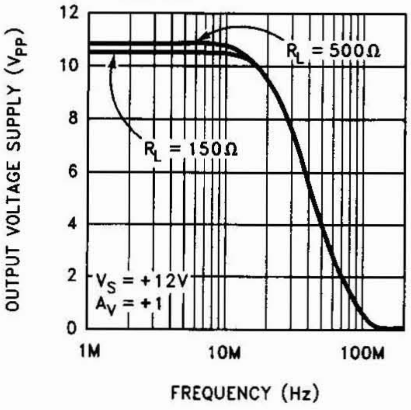
2nd and 3rd Harmonic Distortion vs Frequency



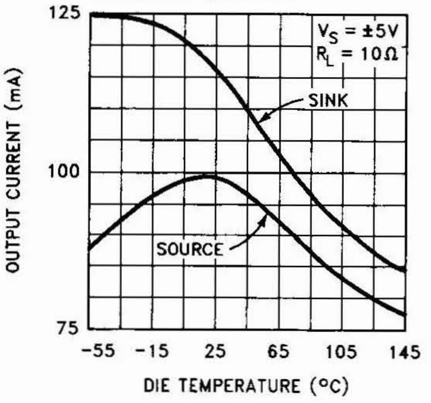
Output Voltage Swing vs Frequency for THD < 0.1%



Output Voltage Swing vs Frequency for Unlimited Distortion



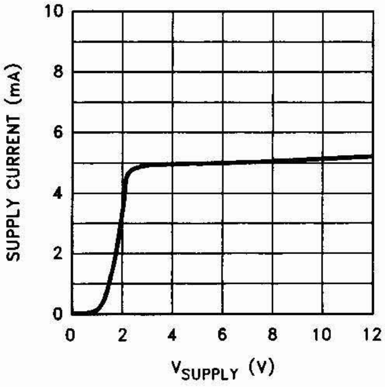
Output Current vs Die Temperature



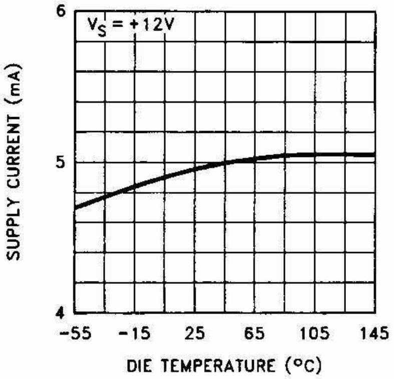
2250-6

Typical Performance Curves — Contd.

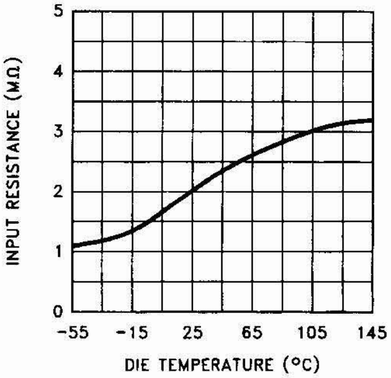
Supply Current vs Supply Voltage (per amplifier)



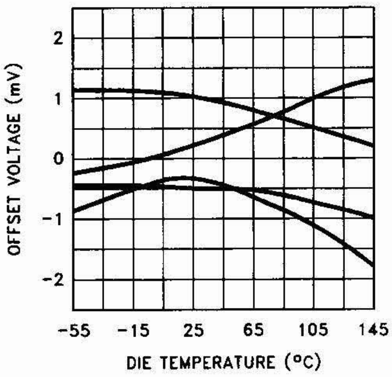
Supply Current vs Die Temperature (per amplifier)



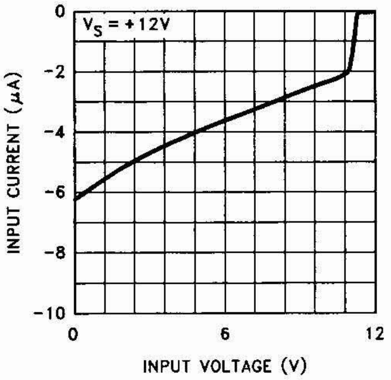
Input Resistance vs Die Temperature



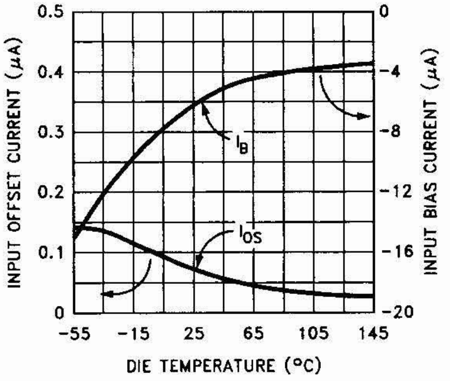
Offset Voltage vs Die Temperature (4 Samples)



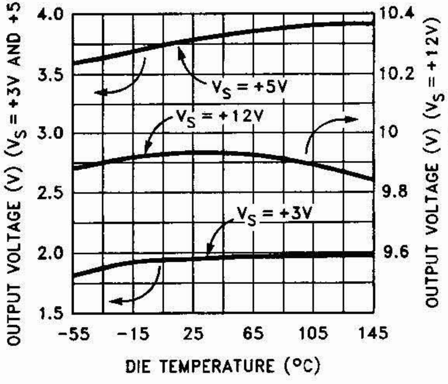
Input Bias Current vs Input Voltage



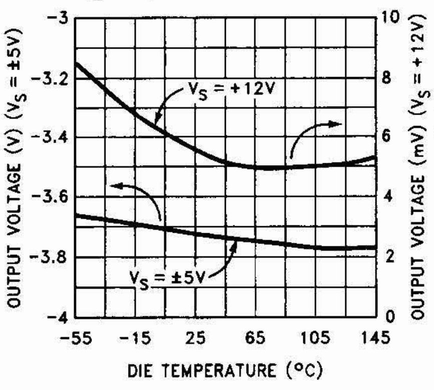
Input Offset Current and Input Bias Current vs Die Temperature



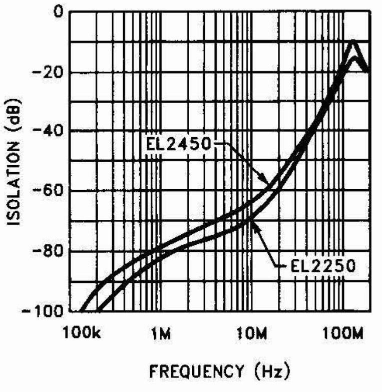
Positive Output Voltage Swing vs Die Temperature, R_L = 150Ω to GND



Negative Output Voltage Swing vs Die Temperature, R_L = 150Ω to GND



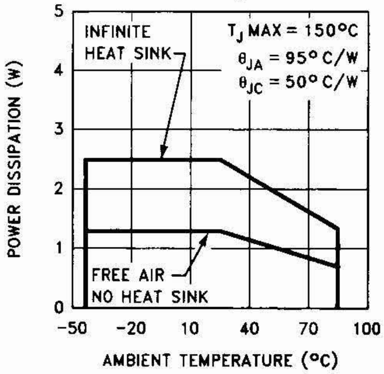
Channel to Channel Isolation vs Frequency



2250-7

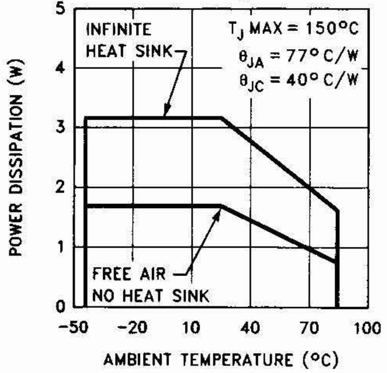
Typical Performance Curves — Contd.

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



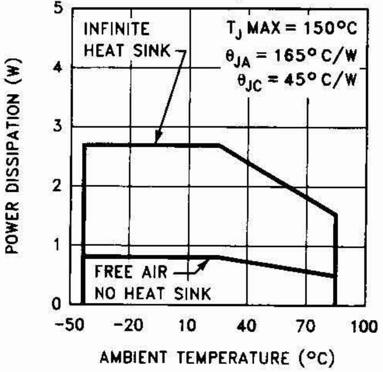
2250-8

14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



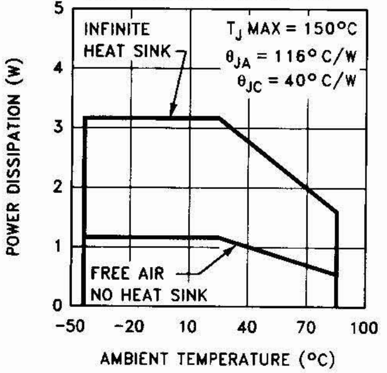
2250-9

8-Lead Plastic SOIC Maximum Power Dissipation vs Ambient Temperature



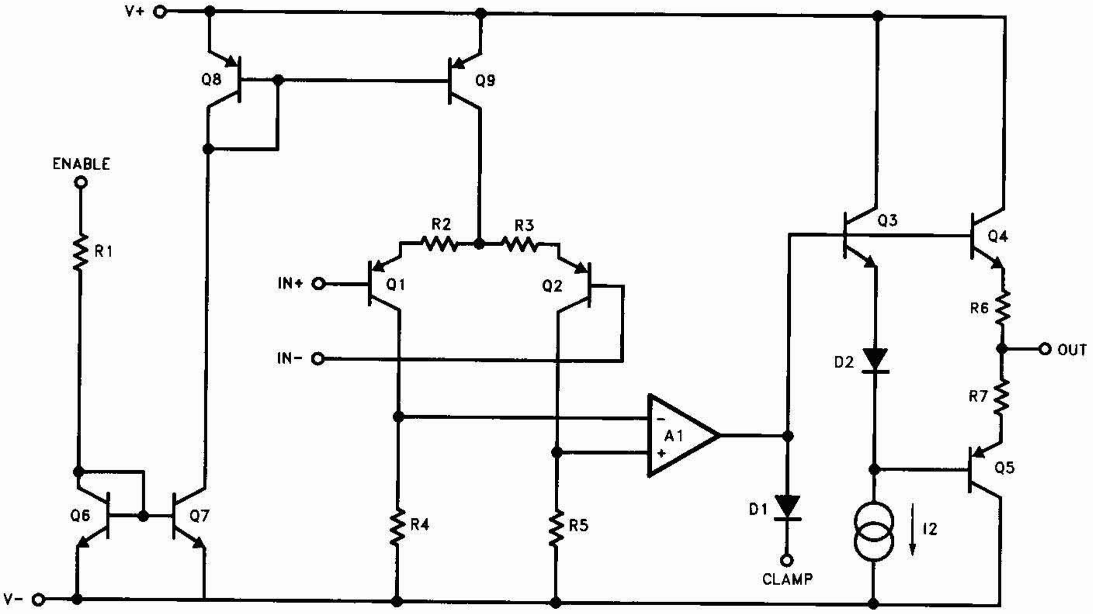
2250-10

14-Lead Plastic SOIC Maximum Power Dissipation vs Ambient Temperature



2250-11

Simplified Schematic


V+
Q8
Q9
ENABLE
R1
R2
R3
IN+
Q1
Q2
IN-
Q3
Q4
R6
OUT
D2
R7
A1
Q5
Q6
Q7
R4
R5
D1
CLAMP
I2
V-

2250-12

EL2250C/EL2450C

125 MHz Single Supply Dual/Quad Op Amps

Applications Information

Product Description

The EL2250C/EL2450C are part of a family of the industries fastest single supply operational amplifiers. Connected in voltage follower mode, their -3dB bandwidth is 125 MHz while maintaining a 275 V/μs slew rate. With an input and output common mode range that includes ground, these amplifiers were optimized for single supply operation, but will also accept dual supplies. They operate on a total supply voltage range as low as +2.7V or up to +12V. This makes them ideal for +3V applications, especially portable computers.

While many amplifiers claim to operate on a single supply, and some can sense ground at their inputs, most fail to truly drive their outputs to ground. If they do succeed in driving to ground, the amplifier often saturates, causing distortion and recovery delays. However, special circuitry built into the EL2250C/EL2450C allows the output to follow the input signal to ground without recovery delays.

Power Supply Bypassing And Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor has been shown to work well when placed at each supply pin. For single supply operation, where the GND pin is connected to the ground plane, a single 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor across the V_{S+} and GND pins will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction should be used. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Supply Voltage Range and Single-Supply Operation

The EL2250C/EL2450C have been designed to operate with supply voltages having a span of greater than 2.7V, and less than 12V. In practical terms, this means that the EL2250C/EL2450C will operate on dual supplies ranging from ±1.35V to ±6V. With a single-supply, the EL2250C/EL2450C will operate from +2.7V to +12V. Performance has been optimized for a single +5V supply.

Pins 8 and 4 are the power supply pins on the EL2250C. The positive power supply is connected to pin 8. When used in single supply mode, pin 4 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4.

Pins 4 and 11 are the power supply pins on the EL2450C. The positive power supply is connected to pin 4. When used in single supply mode, pin 11 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 11.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2250C/EL2450C have an input voltage range that includes the negative supply and extends to within 1.2V of the positive supply. So, for example, on a single +5V supply, the EL2250C/EL2450C have an input range which spans from 0V to 3.8V.

The output range of the EL2250C/EL2450C is also quite large. It includes the negative rail, and extends to within 1V of the top supply rail with a 1 kΩ load. On a +5V supply, the output is therefore capable of swinging from 0V to +4V. On split supplies, the output will swing ±4V. If the load resistor is tied to the negative rail and split supplies are used, the output range is extended to the negative rail.

Applications Information — Contd.

Choice Of Feedback Resistor, R_F

The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value which should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few picofarad range in parallel with R_F can help to reduce this ringing and peaking at the expense of reducing the bandwidth.

As far as the output stage of the amplifier is concerned, $R_F + R_G$ appear in parallel with R_L for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F has a minimum value that should not be exceeded for optimum performance.

For $A_V = +1$, $R_F = 0\ \Omega$ is optimum. For Av = -1 or +2 (noise gain of 2), optimum response is obtained with R_F between 500 Ω and 1 kΩ. For Av = -4 or +5 (noise gain of 5), keep R_F between 2 kΩ and 10 kΩ.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This can be difficult when driving a standard video load of 150 Ω, because of the change in output current with DC level. Differential Gain and Differential Phase for the EL2250C/EL2450C are specified with the black level of the output video signal set to +1.2V. This allows ample room for the sync pulse even in a gain of +2 configuration. This results in dG and dP specifications of 0.05% and 0.05° while driving 150 Ω at a gain of +2. Setting the black level to other values, although acceptable, will compromise peak performance. For example, looking at the single supply dG and dP curves for $R_L = 150\ \Omega$, if the output black level clamp is reduced from 1.2V to 0.6V dG/dP will increase from 0.05%/0.05° to 0.08%/0.25° Note that in a gain of +2 configuration, this is the lowest black level allowed such that the sync tip doesn't go below 0V.

If your application requires that the output goes to ground, then the output stage of the EL2250C/EL2450C, like all other single supply op amps, requires an external pull down resistor tied to ground. As mentioned above, the current flowing through this resistor becomes the DC bias current for the output stage NPN transistor. As this current approaches zero, the NPN turns off, and dG and dP will increase. This becomes more critical as the load resistor is increased in value. While driving a light load, such as 1 kΩ, if the input black level is kept above 1.25V, dG and dP are a respectable 0.03% and 0.03°.

For other biasing conditions see the Differential Gain and Differential Phase vs. Input Voltage curves.

Output Drive Capability

In spite of their moderately low 5 mA of supply current, the EL2250C/EL2450C are capable of providing ±100 mA of output current into a 10 Ω load, or ±60 mA into 50 Ω. With this large output current capability, a 50 Ω load can be driven to ±3V with $V_S = \pm 5V$, making it an excellent choice for driving isolation transformers in telecommunications applications.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will de-couple the EL2250C/EL2450C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5 Ω and 50 Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output.

Video Sync Pulse Remover Application

All CMOS Analog to Digital Converters (A/Ds) have a parasitic latch-up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off.

Application Information — Contd.

Figure 1 shows a unity gain connected amplifier A of an EL2250C. Figure 2 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.

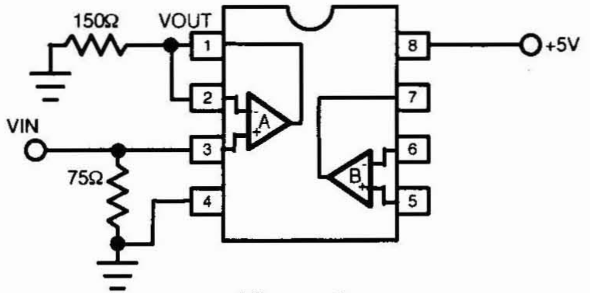


Figure 1

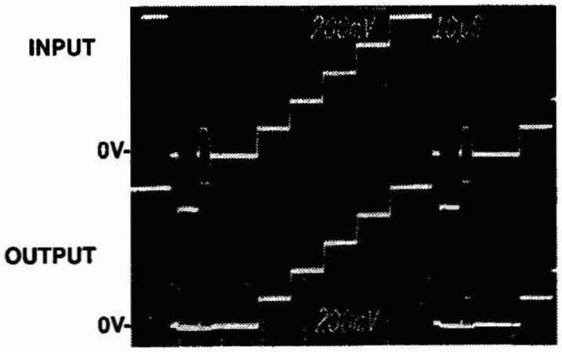


Figure 2

Short Circuit Current Limit

The EL2250C/EL2450C have internal short circuit protection circuitry that protect it in the event of its output being shorted to either supply rail. This limit is set to around 100 mA nominally and reduces with increasing junction temperature. It is intended to handle temporary shorts. If an output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±90 mA. A heat sink may be required to keep the junction temperature below absolute maximum when an output is shorted indefinitely.

Power Dissipation

With the high output drive capability of the EL2250C/EL2450C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2250C/EL2450C to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to [1]:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \qquad [1]$$

where:

T_{JMAX} = Maximum Junction Temperature
T_{AMAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
PD_{MAX} = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or [2]

$$PD_{MAX} = N^{*}(V_S{}^{*}I_{SMAX} + (V_S - V_{OUT}){}^{*}\frac{V_{OUT}}{R_L}) \qquad [2]$$

where:

N = Number of amplifiers
V_S = Total Supply Voltage
I_{SMAX} = Maximum Supply Current per amplifier
V_{OUT} = Maximum Output Voltage of the Application
R_L = Load Resistance tied to Ground

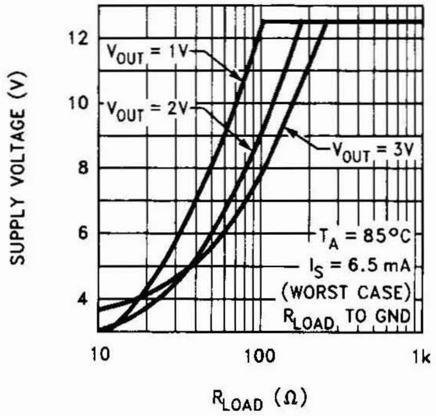
If we set the two PD_{MAX} equations, [1] & [2], equal to each other, and solve for V_S, we can get a family of curves for various loads and output voltages according to [3]:

$$V_S = \frac{\frac{R_L{}^{*}(T_{JMAX} - T_{AMAX})}{N^{*}\theta_{JA}} + (V_{OUT})^2}{(IS^{*}R_L) + V_{OUT}} \qquad [3]$$

Figures 3 through 6 below show total single supply voltage V_S vs. R_L for various output voltage swings for the PDIP and SOIC packages. The curves assume WORST CASE conditions of $T_A = +85°C$ and $I_S = 6.5$ mA per amplifier.

Application Information — Contd.

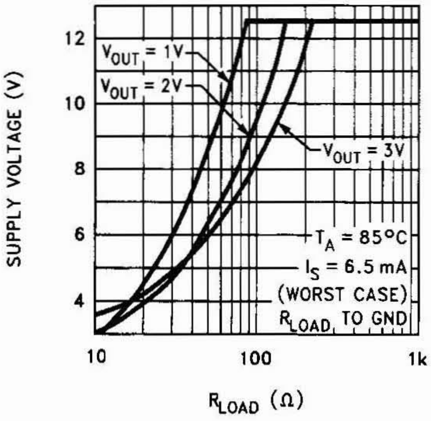
EL2250C Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (PDIP Package)



2250-15

Figure 3

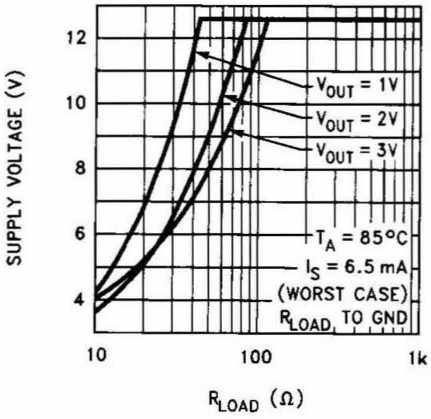
EL2450C Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (PDIP Package)



2250-17

Figure 5

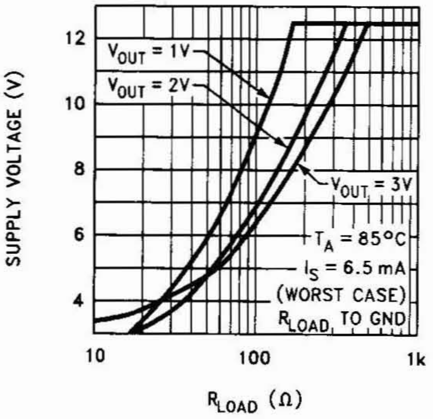
EL2250C Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)



2250-16

Figure 4

EL2450C Single Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)



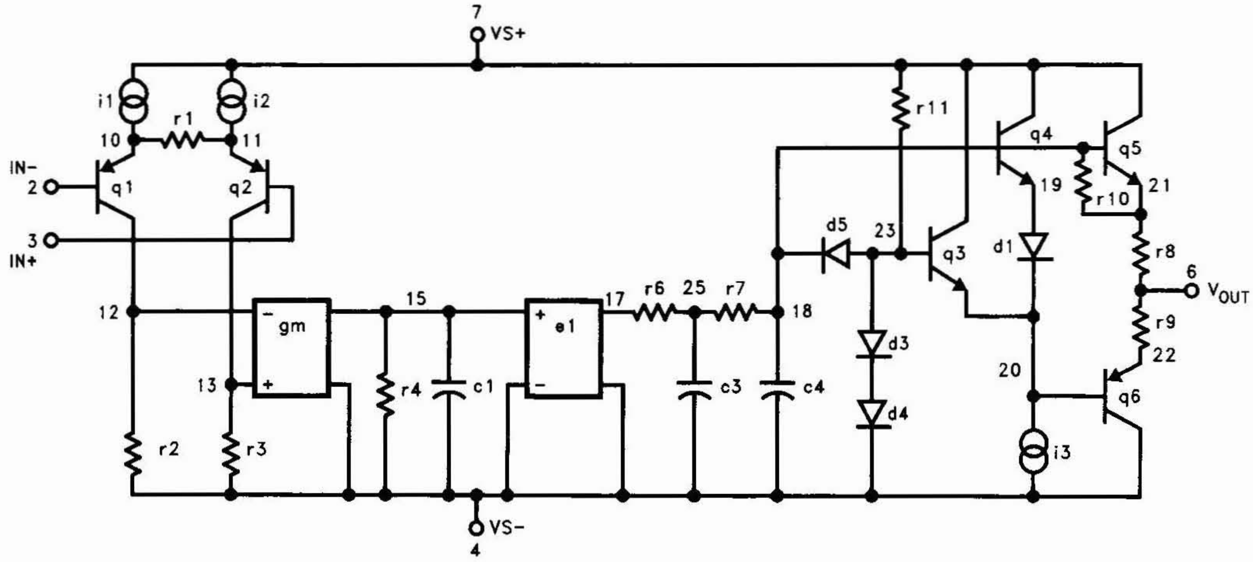
2250-18

Figure 6

EL2250C/EL2450C Macromodel (one amplifier)

```
* Revision A, April 1996
* Pin numbers reflect a standard single op amp.
* Connections:      +input
*                    |    -input
*                    |     |    +Vsupply
*                    |     |     |    -Vsupply
*                    |     |     |     |    output
.subckt EL2250/el    3     2     7     4     6
*
* Input Stage
*
i1 7 10 250µA
i2 7 11 250µA
r1 10 11 4k
q1 12 2 10 qp
q2 13 3 11 qpa
r2 12 4 100
r3 13 4 100
*
* Second Stage & Compensation
*
gm 15 4 13 12 4.6m
r4 15 4 15Meg
c1 15 4 0.36pF
*
* Poles
*
e1 17 4 15 4 1.0
r6 17 25 400
c3 25 4 1pF
r7 25 18 500
c4 18 4 1pF
*
* Output Stage
*
i3 20 4 1.0mA
q3 7 23 20 qn
q4 7 18 19 qn
q5 7 18 21 qn
q6 4 20 22 qp
q7 7 23 18 qn
d1 19 20 da
r8 21 6 2
r9 22 6 2
r10 18 21 10k
r11  7 23 100k
d2 23 24 da
d3 24 4 da
d4 23 18 da
*
* Power Supply Current
*
ips 7 4 3.2mA
*
* Models
*
.model qn npn(is=800e-18 bf=150 tf=0.02nS)
.model qpa pnp(is=810e-18 bf=50 tf=0.02nS)
.model qp pnp(is=800e-18 bf=54 tf=0.02nS)
.model da d(tt=0nS)
.ends
```

EL2250C/EL2450C Macromodel (one amplifier) — Contd.


7
VS+
i1
i2
r1
10
11
IN-
2
q1
q2
3
IN+
12
13
gm
-
+
15
r4
c1
e1
+
-
17
r6
25
r7
18
r2
r3
c3
c4
VS-
4
r11
q4
q5
19
21
r10
d5
23
q3
d1
r8
6
VOUT
r9
d3
22
20
d4
q6
i3

2250-19

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2257C/EL2357C

125 MHz Single Supply, Clamping Op Amps

Features

- Specified for +3V, +5V, or ± 5V Applications
- Power Down to 0 μA
- Output Voltage Clamp
- Large Input Common Mode Range
  $0V < V_{CM} < V_S - 1.2V$
- Output Swings to Ground Without Saturating
- −3 dB Bandwidth = 125 MHz
- ± 0.1 dB Bandwidth = 30 MHz
- Low Supply Current = 5 mA
- Slew Rate = 275 V/μs
- Low Offset Voltage = 3 mV max
- Output Current = ±100 mA
- High Open Loop Gain = 80 dB
- Differential Gain = 0.05%
- Differential Phase = 0.05°

Applications

- Video Amplifier
- PCMCIA Applications
- A/D Driver
- Line Driver
- Portable Computers
- High Speed Communications
- RGB Printer, FAX, Scanner Applications
- Broadcast Equipment
- Active Filtering
- Multiplexing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2257CN	−40°C to +85°C	14 Pin PDIP	MDP0031
EL2257CS	−40°C to +85°C	14 Pin SOIC	MDP0027
EL2357CN	−40°C to +85°C	16 Pin PDIP	MDP0031
EL2357CS	−40°C to +85°C	16 Pin SOIC	MDP0027

General Description

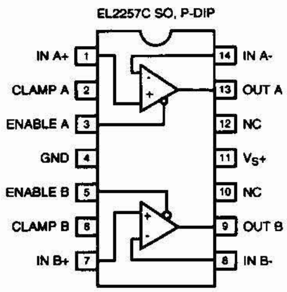
The EL2257C/EL2357C are the electronics industry's fastest single supply op amps available. Prior single supply op amps have generally been limited to bandwidths and slew rates ¼ that of the EL2257C/EL2357C. The 125 MHz bandwidth, 275 V/μs slew rate, and 0.05%/0.05° differential gain/differential phase makes this part ideal for single or dual supply video speed applications. With its voltage feedback architecture, this amplifier can accept reactive feedback networks, allowing them to be used in analog filtering applications. The inputs can sense signals below the bottom supply rail and as high as 1.2V below the top rail. Connecting the load resistor to ground and operating from a single supply, the outputs swing completely to ground without saturating. The outputs can also drive to within 1.2V of the top rail. The EL2257C/EL2357C will output ±100 mA and will operate with single supply voltages as low as 2.7V, making them ideal for portable, low power applications.

The EL2257C/EL2357C have a high speed disable feature. Applying a low logic level to all ENABLE pins reduces the supply current to 0 μA within 50 ns. Each amplifier has its own ENABLE pin. This is useful for both multiplexing and reducing power consumption.

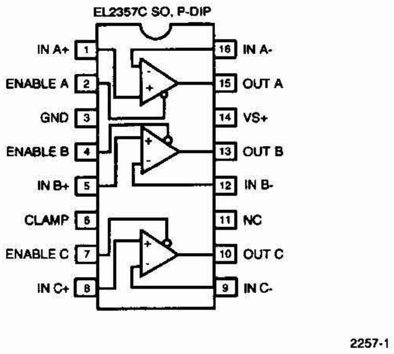
The EL2257C/EL2357C also have an output voltage clamp feature. This clamp is a fast recovery (<7 ns) output clamp that prevents the output voltage from going above the preset clamp voltage. This feature is desirable for A/D applications, as A/D converters can require long times to recover if overdriven.

The EL2257C/EL2357C are available in plastic DIP and SOIC packages. Both parts operate over the industrial temperature range of −40°C to +85°C. For single amplifier applications, see the EL2150C/EL2157C. For space saving, industry standard pin out dual and quad applications, see the EL2250C/EL2450C.

Connection Diagrams



Top View



Top View

January, 1996 Rev A

EL2257C/EL2357C

125 MHz Single Supply, Clamping Op Amps

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S and GND	12.6V	Power Dissipation	See Curves
Input Voltage (IN+, IN−, ENABLE, CLAMP)	GND−0.3V, V_S+0.3V	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	±6V	Ambient Operating Temperature Range	−40°C to +85°C
Maximum Output Current	90 mA	Operating Junction Temperature	150°C
Output Short Circuit Duration	(Note 1)		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = +5V, GND = 0V, T_A = 25°C, V_{CM} = 1.5V, V_{OUT} = 1.5V, V_{CLAMP} = +5V, V_{ENABLE} = +5V, unless otherwise specified.

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage	EL2257C	−2		2	I	mV
		EL2357C	−6		6	I	mV
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from Tmin to Tmax		10		V	µV/°C
IB	Input Bias Current	V_{IN} = 0V		−5.5	−10	I	µA
I_{OS}	Input Offset Current	V_{IN} = 0V	−750	150	750	I	nA
TCI_{OS}	Input Bias Current Temperature Coefficient	Measured from Tmin to Tmax		50		V	nA/°C
PSRR	Power Supply Rejection Ratio	V_S = V_{ENABLE} = +2.7V to +12V, V_{CLAMP} = OPEN	55	70		I	dB
CMRR	Common Mode Rejection Ratio	VCM = 0V to +3.8V	55	65		I	dB
		VCM = 0V to +3.0V	55	70		I	dB
CMIR	Common Mode Input Range		0		V_S − 1.2	I	V
R_{IN}	Input Resistance	Common Mode	1	2		I	MΩ
C_{IN}	Input Capacitance	SOIC Package		1		V	pF
		PDIP Package		1.5		V	pF
R_{OUT}	Output Resistance	Av = +1		40		V	mΩ
$I_{S,ON}$	Supply Current - Enabled (per amplifier)	V_S = V_{CLAMP} = +12V, V_{ENABLE} = +12V		5	6.5	I	mA
$I_{S,OFF}$	Supply Current - Shut Down (per amplifier)	V_S = V_{CLAMP} = +10V, V_{ENABLE} = +0.5V		0	50	I	µA
		V_S = V_{CLAMP} = +12V, V_{ENABLE} = +0.5V		5		V	µA
PSOR	Power Supply Operating Range		2.7		12.0	I	V

DC Electrical Characteristics — Contd.

$V_S = +5V$, GND = 0V, $T_A = 25°C$, $V_{CM} = +1.5V$, $V_{OUT} = +1.5V$, $V_{CLAMP} = +5V$, $V_{ENABLE} = +5V$, unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
AVOL	Open Loop Gain	$V_S = V_{CLAMP} = +12V$, $V_{OUT} = +2V$ to $+9V$, $R_L = 1\ k\Omega$ to GND	65	80		I	dB
		$V_{OUT} = +1.5V$ to $+3.5V$, $R_L = 1\ k\Omega$ to GND		70		V	dB
		$V_{OUT} = +1.5V$ to $+3.5V$, $R_L = 150\Omega$ to GND		60		V	dB
V_{OP}	Positive Output Voltage Swing	$V_S = +12V$, $A_V = +1$, $R_L = 1\ k\Omega$ to 0V		10.8		V	V
		$V_S = +12V$, $A_V = +1$, $R_L = 150\Omega$ to 0V	9.6	10.0		I	V
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 1\ k\Omega$ to 0V		4.0		V	V
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 150\Omega$ to 0V	3.4	3.8		I	V
		$V_S = +3V$, $A_V = +1$, $R_L = 150\Omega$ to 0V	1.8	1.95		I	V
V_{ON}	Negative Output Voltage Swing	$V_S = +12V$, $A_V = +1$, $R_L = 150\Omega$ to 0V		5.5	8	I	mV
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 1\ k\Omega$ to 0V		-4.0		V	V
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 150\Omega$ to 0V		-3.7	-3.4	I	V
I_{OUT}	Output Current (Note 1)	$V_S = \pm 5V$, $A_V = +1$, $R_L = 10\Omega$ to 0V	± 75	± 100		I	mA
		$V_S = \pm 5V$, $A_V = +1$, $R_L = 50\Omega$ to 0V		± 60		V	mA
$I_{OUT,OFF}$	Output Current, Disabled	$V_{ENABLE} = +0.5V$		0	20	I	µA
$V_{IH\text{-}EN}$	ENABLE pin Voltage for Power Up	Relative to GND Pin	2.0			I	V
$V_{IL\text{-}EN}$	ENABLE pin Voltage for Shut Down	Relative to GND Pin			0.5	I	V
$I_{IH\text{-}EN}$	ENABLE pin Input Current-High (Note 2)	$V_S = V_{CLAMP} = +12V$, $V_{ENABLE} = +12V$		340	410	I	µA
$I_{IL\text{-}EN}$	ENABLE pin Input Current-Low (Note 2)	$V_S = V_{CLAMP} = +12V$, $V_{ENABLE} = +0.5V$		0	1	I	µA
$V_{OR\text{-}CL}$	Voltage Clamp Operating Range (Note 3)	Relative to GND Pin	1.2		V_{OP}	I	V
$V_{ACC\text{-}CL}$	CLAMP Accuracy (Note 4)	$V_{IN} = +4V$, $R_L = 1\ k\Omega$ to GND $V_{CLAMP} = +1.5V$ and $+3.5V$	-250	100	250	I	mV
$I_{IH\text{-}CL}$	CLAMP pin Input Current - High	$V_S = V_{CLAMP} = +12V$		12	25	I	µA
$I_{IL\text{-}CL}$	CLAMP pin Input Current - Low	$V_S = +12V$, $V_{CLAMP} = +1.2V$	-20	-15		I	µA

Note 1: Internal short circuit protection circuitry has been built into the EL2257C/EL2357C. See the Applications section.

Note 2: If the disable feature is not desired, tie the ENABLE pins to the V_S pin, or apply a logic high level to the ENABLE pins.

Note 3: The maximum output voltage that can be clamped is limited to the maximum positive output Voltage, or V_{OP}. Applying a Voltage higher than V_{OP} inactivates the clamp. If the clamp feature is not desired, either tie the CLAMP pin to the V_S pin, or simply let the CLAMP pin float.

Note 4: The clamp accuracy is affected by V_{IN} and R_L. See the Typical Curves Section and the Clamp Accuracy vs. V_{IN} and R_L curve.

Closed Loop AC Electrical Characteristics

(Note 5) $V_S = +5V$, $GND = 0V$, $T_A = 25°C$, $V_{CM} = +1.5V$, $V_{OUT} = +1.5V$, $V_{CLAMP} = +5V$, $V_{ENABLE} = +5V$, $A_V = +1$, $RF = 0\Omega$, $RL = 150\Omega$ to GND pin, unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth (Vout = 400 mVp-p)	$V_S = +5V, A_V = +1, R_F = 0\Omega$		125		V	MHz
		$V_S = +5V, A_V = -1, R_F = 500\Omega$		60		V	MHz
		$V_S = +5V, A_V = +2, R_F = 500\Omega$		60		V	MHz
		$V_S = +5V, A_V = +10, R_F = 500\Omega$		6		V	MHz
		$V_S = +12V, A_V = +1, R_F = 0\Omega$		150		V	MHz
		$V_S = +3V, A_V = +1, R_F = 0\Omega$		100		V	MHz
BW	±0.1 dB Bandwidth (Vout = 400 mVp-p)	$V_S = +12V, A_V = +1, R_F = 0\Omega$		25		V	MHz
		$V_S = +5V, A_V = +1, R_F = 0\Omega$		30		V	MHz
		$V_S = +3V, A_V = +1, R_F = 0\Omega$		20		V	MHz
GBWP	Gain Bandwidth Product	$V_S = +12V$, @ $A_V = +10$		60		V	MHz
PM	Phase Margin	$R_L = 1\ k\Omega$, $CL = 6\ pF$		55		V	°
SR	Slew Rate	$V_S = +10V, R_L = 150\Omega$, Vout = 0V to +6V	200	275		I	V/µs
		$V_S = +5V, R_L = 150\Omega$, Vout = 0V to +3V		300		V	V/µs
t_R, t_F	Rise Time, Fall Time	±0.1V Step		2.8		V	ns
OS	Overshoot	±0.1V Step		10		V	%
t_{PD}	Propagation Delay	±0.1V step		3.2		V	ns
t_S	0.1% Settling Time	$V_S = \pm 5V, R_L = 500\Omega, A_V = +1, V_{OUT} = \pm 3V$		40		V	ns
	0.01% Settling Time	$V_S = \pm 5V, R_L = 500\Omega, A_V = +1, V_{OUT} = \pm 3V$		75		V	ns
dG	Differential Gain (Note 6)	$A_V = +2, R_F = 1\ k\Omega$		0.05		V	%
dP	Differential Phase (Note 6)	$A_V = +2, R_F = 1\ k\Omega$		0.05		V	°
e_N	Input Noise Voltage	f = 10 kHz		48		V	$nV/\sqrt{Hz}$
i_N	Input Noise Current	f = 10 kHz		1.25		V	$pA/\sqrt{Hz}$
t_{DIS}	Disable Time (Note 7)			50		V	ns
t_{EN}	Enable Time (Note 7)			25		V	ns
t_{CL}	Clamp Overload Recovery			7		V	ns

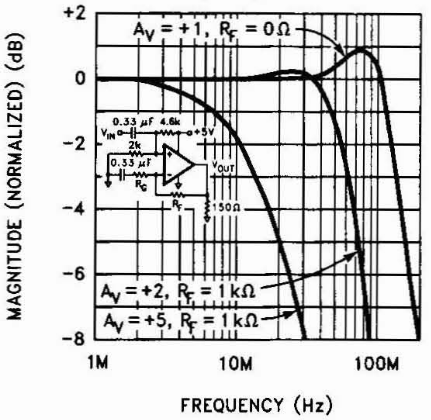
Note 5: All AC tests are performed on a "warmed up" part, except slew rate, which is pulse tested.

Note 6: Standard NTSC signal = 286 mVp-p, f = 3.58 MHz, as V_{IN} is swept from 0.6V to 1.314V. R_L is DC coupled.

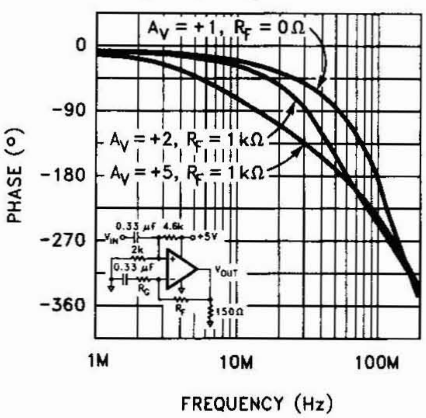
Note 7: Disable/Enable time is defined as the time from when the logic signal is applied to the ENABLE pin to when the supply current has reached half its final value.

Typical Performance Curves

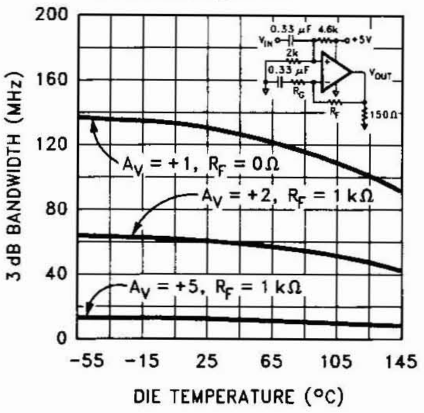
Non-Inverting Frequency Response (Gain)



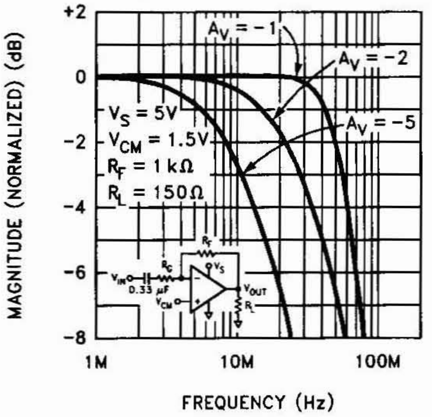
Non-Inverting Frequency Response (Phase)



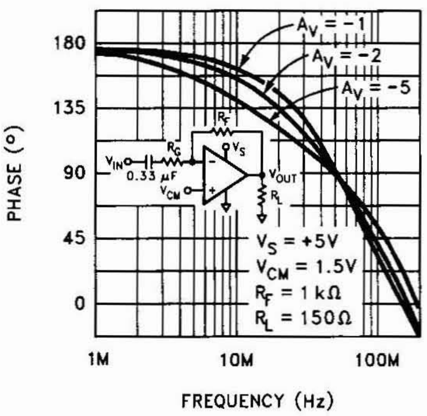
3 dB Bandwidth vs Temperature for Non-Inverting Gains



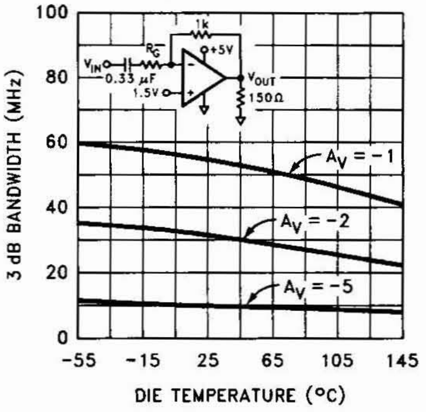
Inverting Frequency Response (Gain)



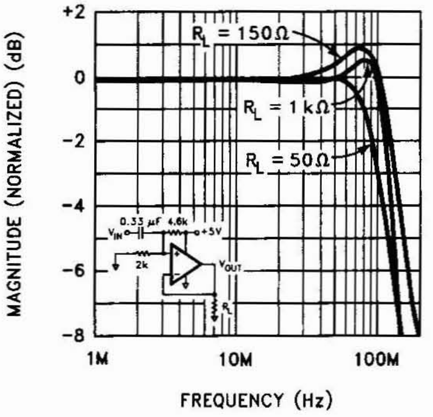
Inverting Frequency Response (Phase)



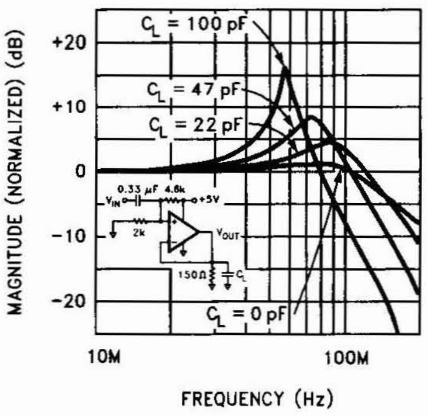
3 dB Bandwidth vs Temperature for Inverting Gains



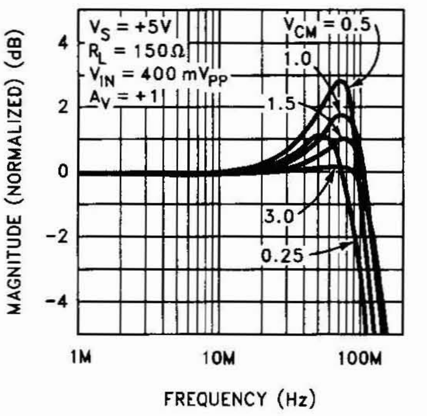
Frequency Response for Various R_L



Frequency Response for Various C_L



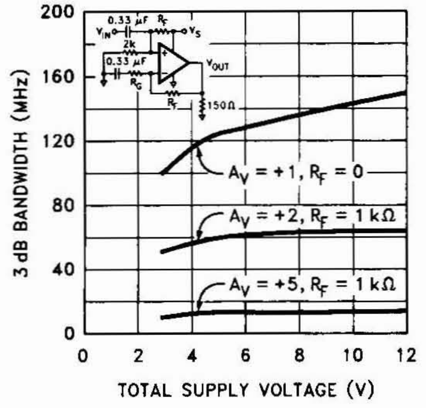
Non-Inverting Frequency Response vs Common Mode Voltage



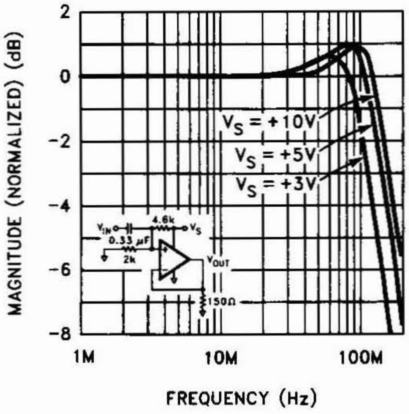
2257-2

Typical Performance Curves — Contd.

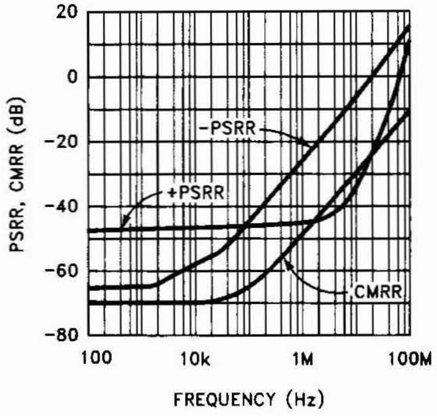
3 dB Bandwidth vs Supply Voltage for Non-Inverting Gains



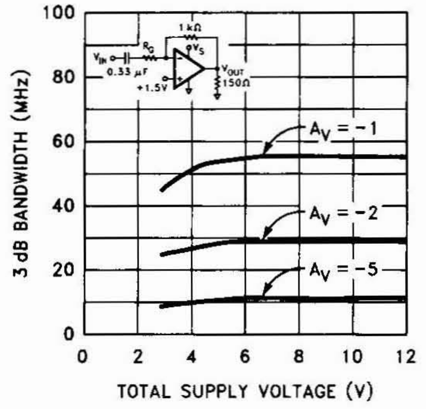
Frequency Response for Various Supply Voltages, A_V = + 1



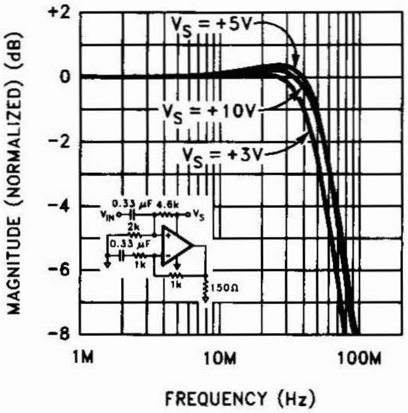
PSSR and CMRR vs Frequency



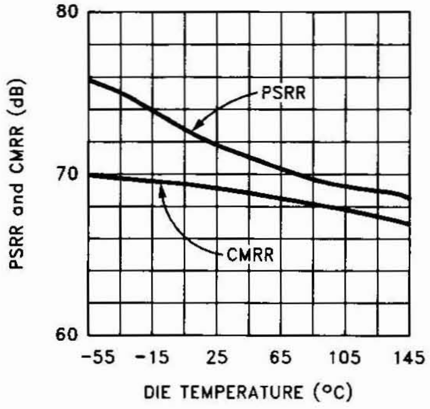
3 dB Bandwith vs Supply Voltage for Inverting Gains



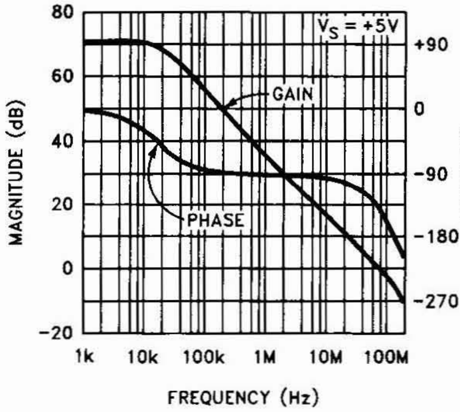
Frequency Response for Various Supply Voltages, A_V = + 2



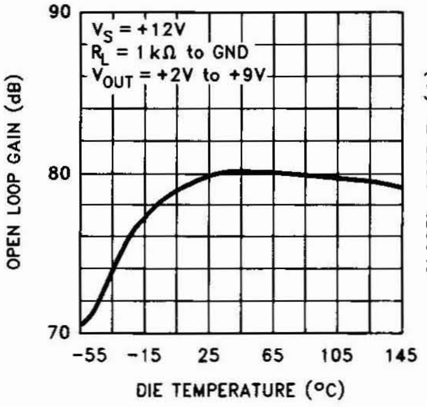
PSRR and CMRR vs Die Temperature



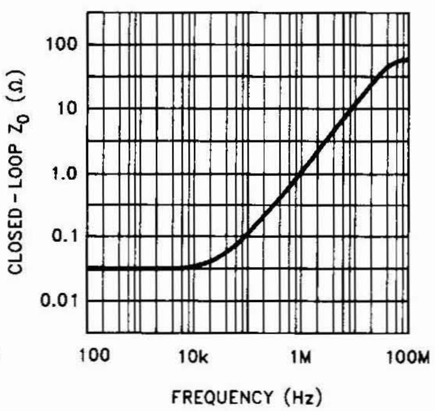
Open Loop Gain and Phase vs Frequency



Open Loop Voltage Gain vs Die Temperature



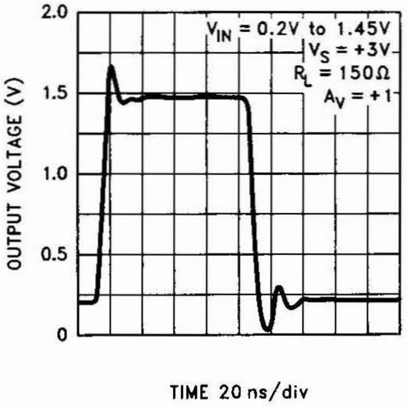
Closed Loop Output Impedance vs Frequency



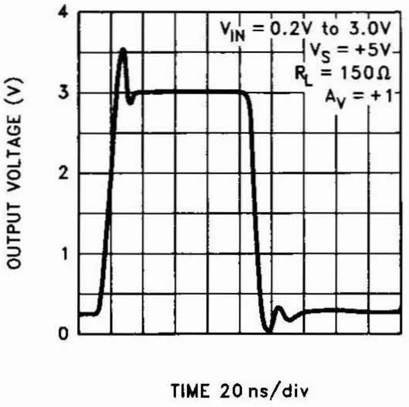
2257-3

Typical Performance Curves — Contd.

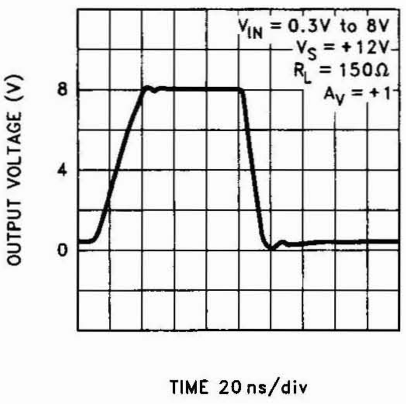
Large Signal Step Response, V_S = +3V



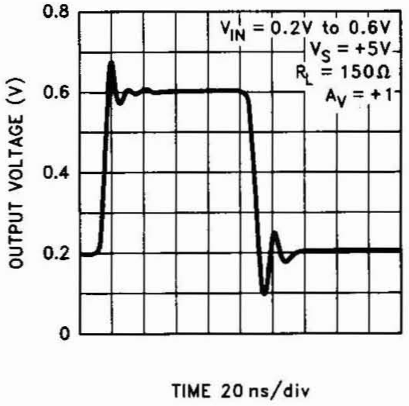
Large Signal Step Response, V_S = +5V



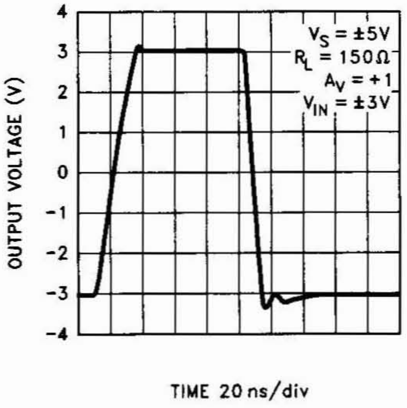
Large Signal Step Response, V_S = +12V



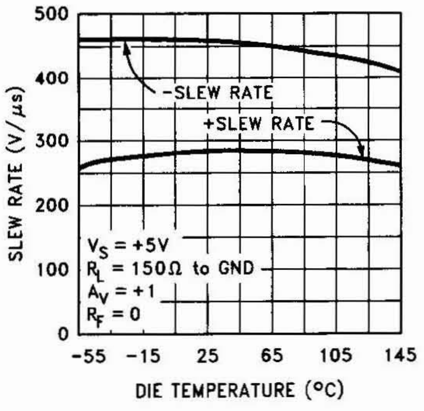
Small Signal Step Response



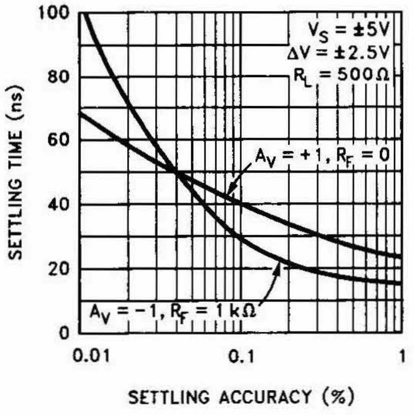
Large Signal Step Response, V_S = ±5V



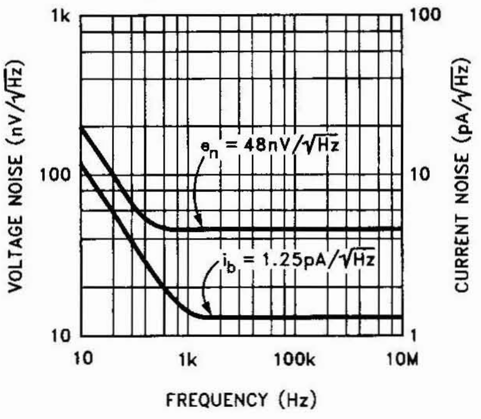
Slew Rate vs Temperature



Settling Time vs Settling Accuracy



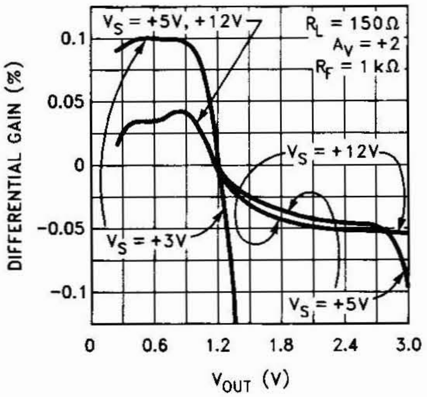
Voltage and Current Noise vs Frequency



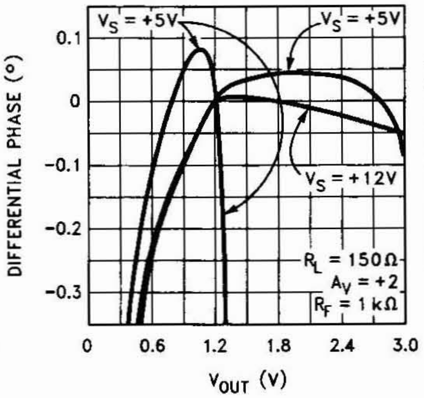
2257-4

Typical Performance Curves — Contd.

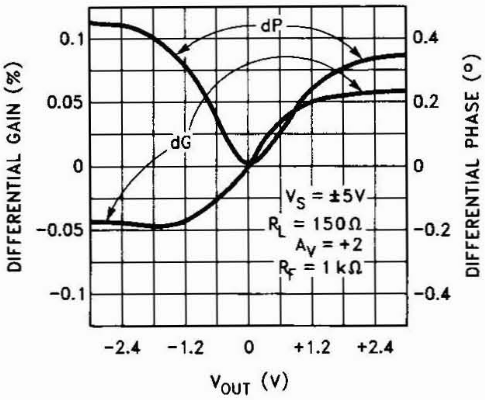
Differential Gain for Single Supply Operation



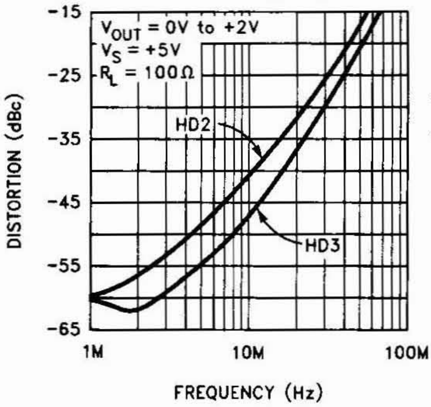
Differential Phase for Single Supply Operation



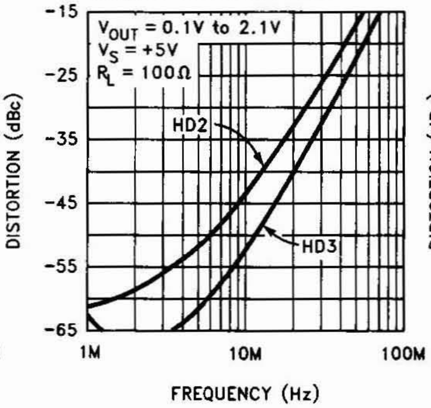
Differential Gain and Phase for Dual Supply Operation



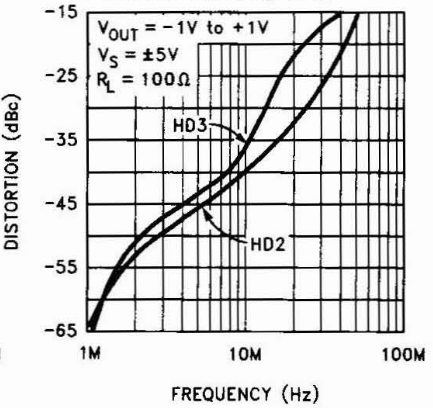
2nd and 3rd Harmonic Distortion vs Frequency



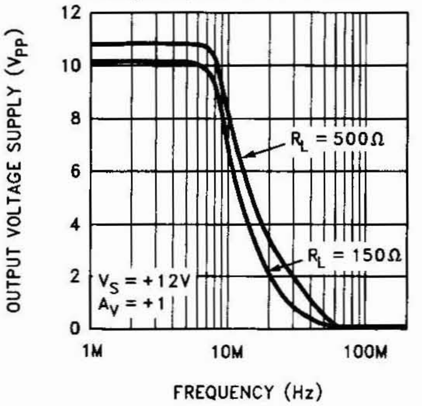
2nd and 3rd Harmonic Distortion vs Frequency



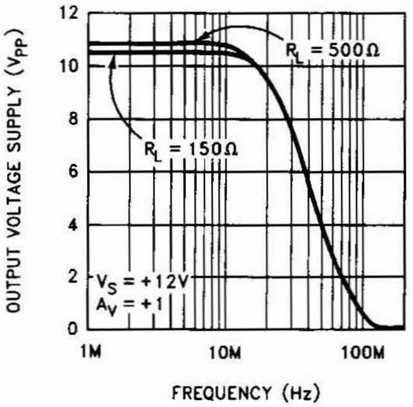
2nd and 3rd Harmonic Distortion vs Frequency



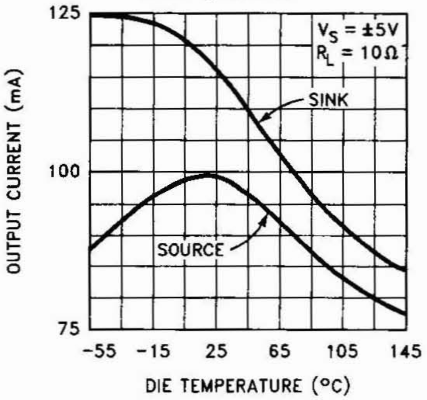
Output Voltage Swing vs Frequency for THD < 0.1%



Output Voltage Swing vs Frequency for Unlimited Distortion



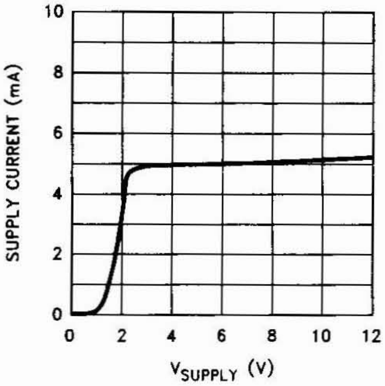
Output Current vs Die Temperature



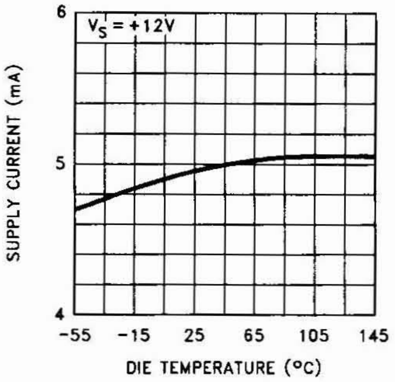
2257–5

Typical Performance Curves — Contd.

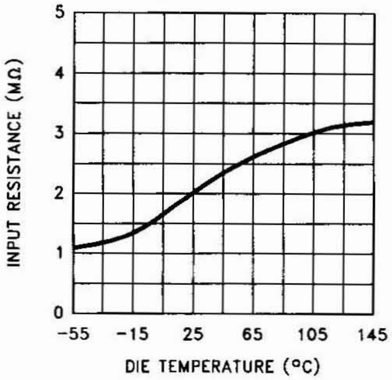
Supply Current vs Supply Voltage (per amplifier)



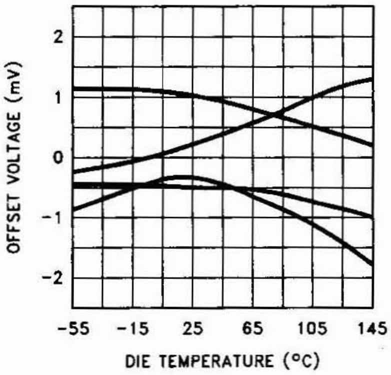
Supply Current vs Die Temperature (per amplifier)



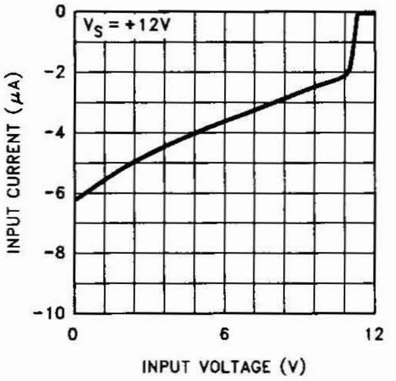
Input Resistance vs Die Temperature



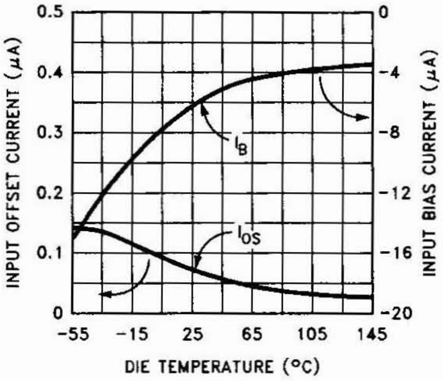
Offset Voltage vs Die Temperature (4 Samples)



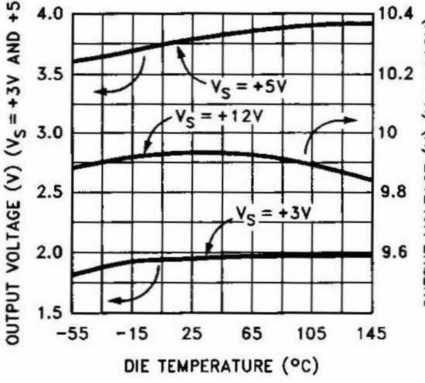
Input Bias Current vs Input Voltage



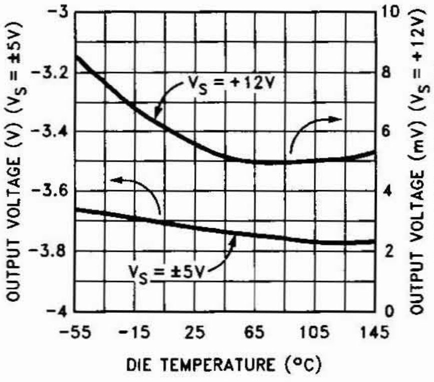
Input Offset Current and Input Bias Current vs Die Temperature



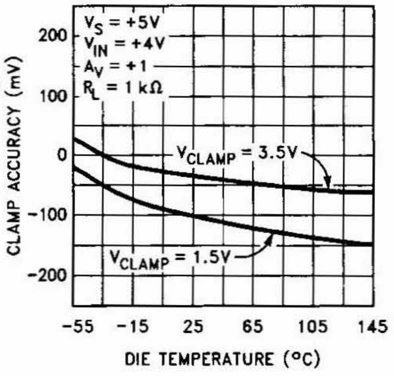
Positive Output Voltage Swing vs Die Temperature, R_L = 150Ω to GND



Negative Output Voltage Swing vs Die Temperature, R_L = 150Ω to GND



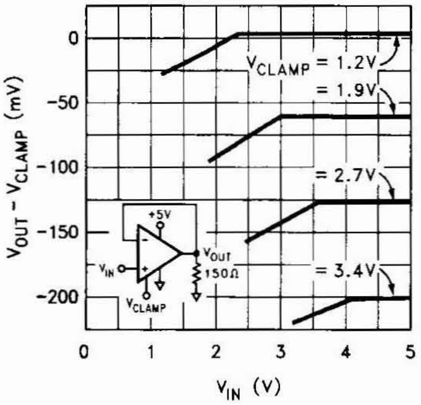
Clamp Accuracy vs Die Temperature



2257-6

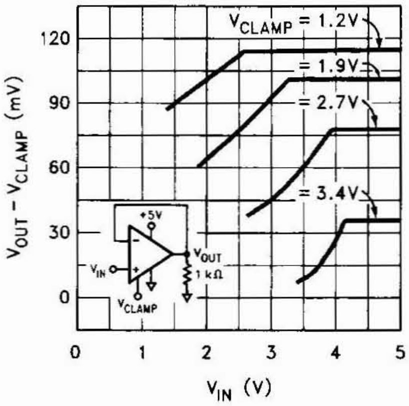
Typical Performance Curves — Contd.

Clamp Accuracy
R_L = 150Ω



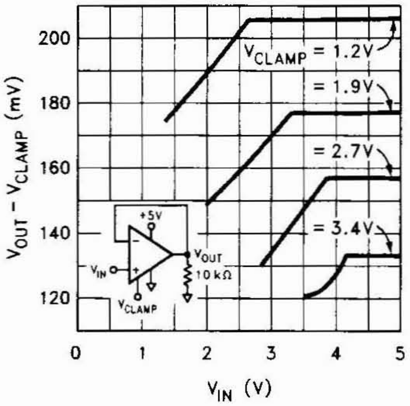
2257-7

Clamp Accuracy
R_L = 1 kΩ



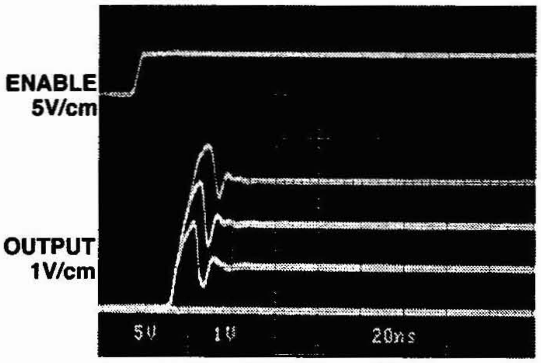
2257-8

Clamp Accuracy
R_L = 10 kΩ



2257-9

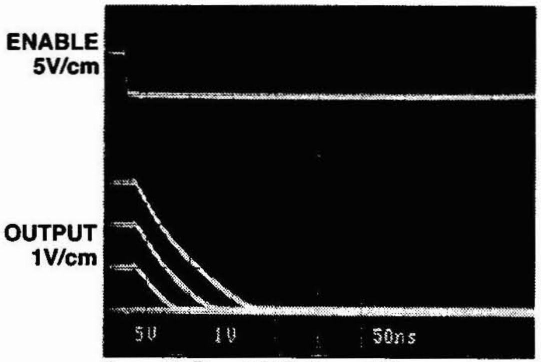
Enable Response for a Family of DC Inputs



$A_V = +1$, $R_L = 150\Omega$, $V_S = +5V$

2257-10

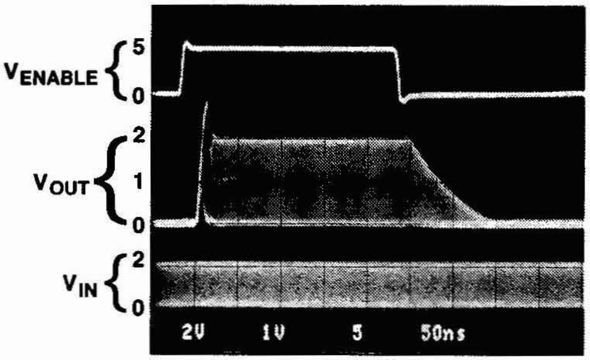
Disable Response for a Family of DC Inputs



$A_V = +1$, $R_L = 150\Omega$, $V_S = +5V$

2257-11

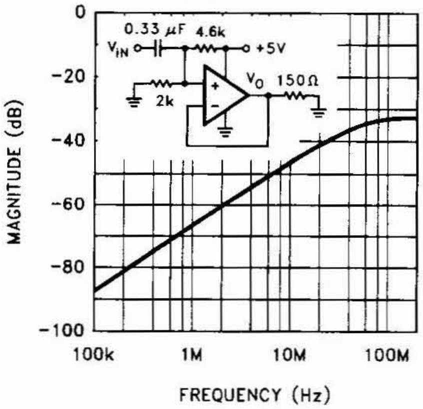
Disable/Enable Response for a Family of Sine Waves



50 ns/div

2257-12

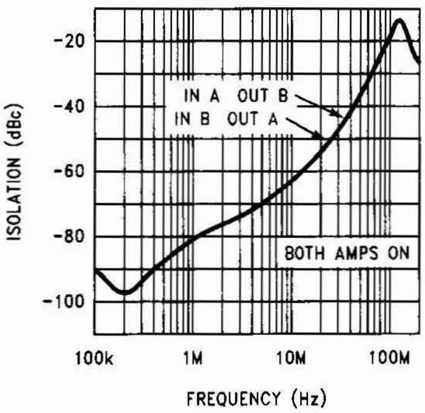
OFF Isolation



2257-13

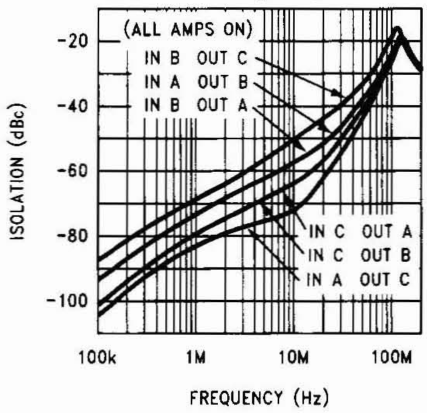
Typical Performance Curves — Contd.

EL2257
Channel to Channel Isolation vs Frequency



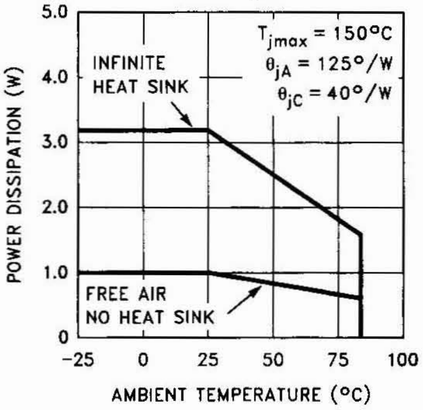
2257-14

EL2357
Channel to Channel Isolation vs Frequency



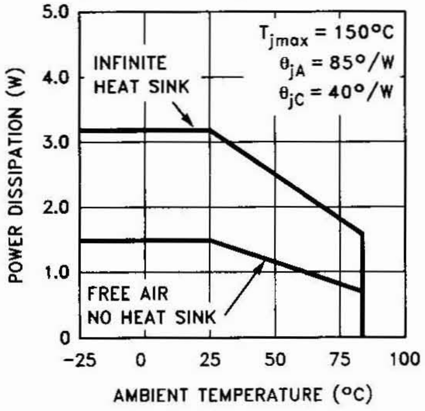
2257-17

14-Lead Plastic SO
Maximum Power Dissipation vs Ambient Temperature



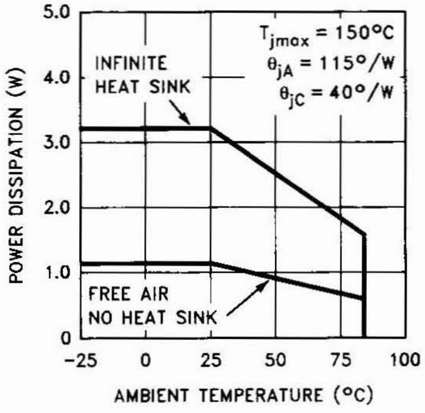
2257-15

14-Lead Plastic DIP
Maximum Power Dissipation vs Ambient Temperature



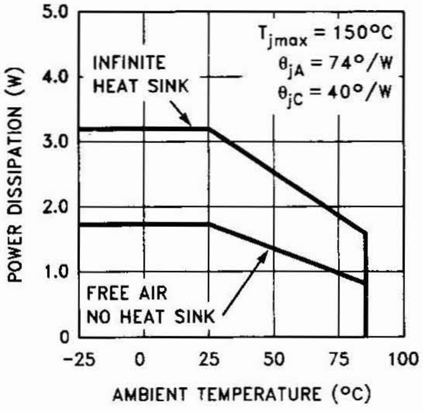
2257-16

16-Lead Plastic SO
Maximum Power Dissipation vs Ambient Temperature



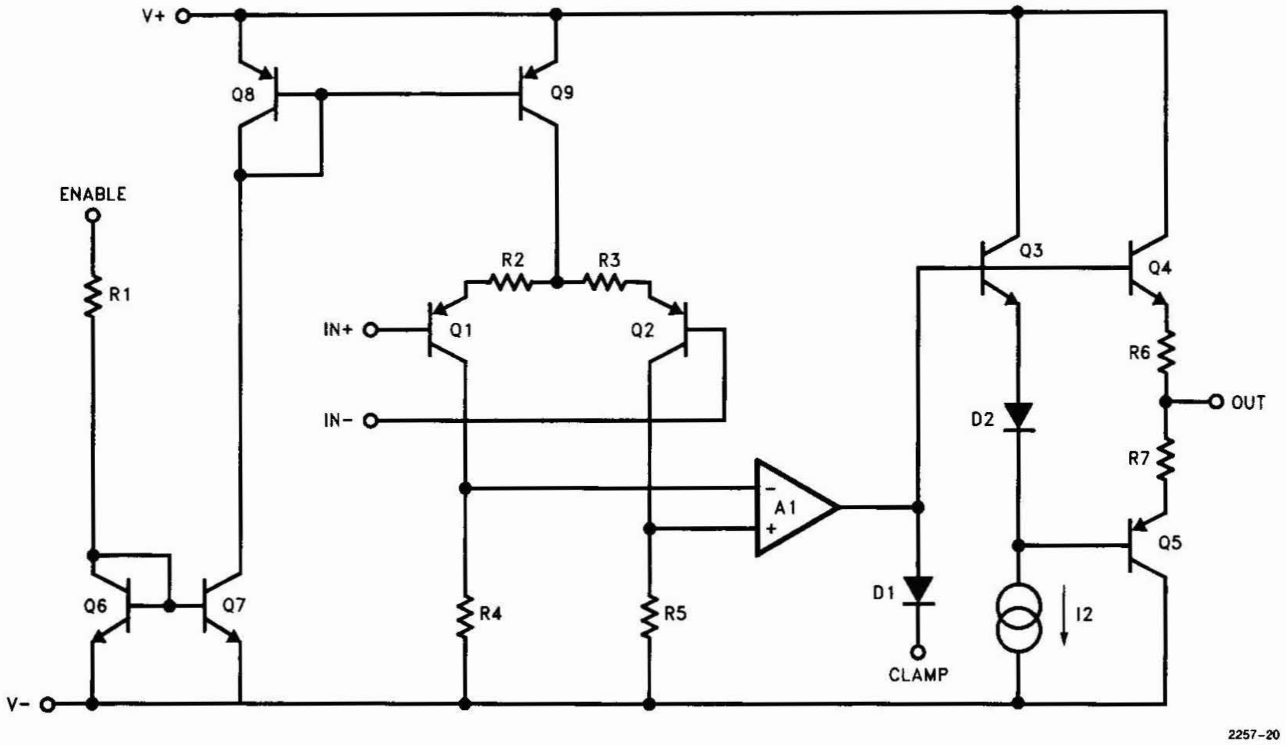
2257-18

16-Lead Plastic DIP
Maximum Power Dissipation vs Ambient Temperature



2257-19

Simplified Schematic (one channel)


V+
Q8
Q9
ENABLE
R1
R2
R3
IN+
Q1
Q2
IN−
Q3
Q4
R6
OUT
D2
R7
A1
−
+
Q5
Q6
Q7
R4
R5
D1
I2
CLAMP
V−
2257-20

Applications Information

Product Description

The EL2257C/EL2357C are the industries fastest single supply operational amplifiers. Connected in voltage follower mode, their −3 dB bandwidth is 125 MHz while maintaining a 275 V/µs slew rate. With an input and output common mode range that includes ground, these amplifiers were optimized for single supply operation, but will also accept dual supplies. They operate on a total supply voltage range as low as +2.7V or up to +12V. This makes them ideal for +3V applications, especially portable computers.

While many amplifiers claim to operate on a single supply, and some can sense ground at their inputs, most fail to truly drive their outputs to ground. If they do succeed in driving to ground, the amplifier often saturates, causing distortion and recovery delays. However, special circuitry built into the EL2257C/EL2357C allows the output to follow the input signal to ground without recovery delays.

Power Supply Bypassing And Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor has been shown to work well when placed at each supply pin. For single supply operation, where the GND pin is connected to the ground plane, a single 4.7 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor from the V_S+ pin to the GND pin will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction should be used. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Supply Voltage Range and Single-Supply Operation

The EL2257C/EL2357C have been designed to operate with supply voltages having a span of greater than 2.7V, and less than 12V. In practical terms, this means that the EL2257C/EL2357C will operate on dual supplies ranging from ±1.35V to ±6V. With a single-supply, the EL2257C/EL2357C will operate from +2.7V to +12V. Performance has been optimized for a single +5V supply.

Pins 11 and 4 (14 and 3) are the power supply pins on the EL2257C (EL2357C). The positive power supply is connected to pin 11 (14). When used in single supply mode, pin 4 (3) is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4 (3).

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2257C/EL2357C have an input voltage range that includes the negative supply and extends to within 1.2V of the positive supply. So, for example, on a single +5V supply, the EL2257C/EL2357C have an input range which spans from 0V to 3.8V.

The output range of the EL2257C/EL2357C is also quite large. It includes the negative rail, and extends to within 1V of the top supply rail with a 1 kΩ load. On a +5V supply, the output is therefore capable of swinging from 0V to +4V. On split supplies, the output will swing ±4V. If the load resistor is tied to the negative rail and split supplies are used, the output range is extended to the negative rail.

Choice Of Feedback Resistor, R_F

The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the

Applications Information — Contd.

time domain and peaking in the frequency domain. Therefore, R_F has some maximum value which should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few picofarad range in parallel with R_F can help to reduce this ringing and peaking at the expense of reducing the bandwidth.

As far as the output stage of the amplifier is concerned, $R_F + R_G$ appear in parallel with R_L for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F has a minimum value that should not be exceeded for optimum performance.

For $A_V = +1$, $R_F = 0\Omega$ is optimum. For $A_V = -1$ or $+2$ (noise gain of 2), optimum response is obtained with R_F between 500Ω and 1 kΩ. For $A_V = -4$ or $+5$ (noise gain of 5), keep R_F between 2 kΩ and 10 kΩ.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This can be difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Differential Gain and Differential Phase for the EL2257C/EL2357C are specified with the black level of the output video signal set to +1.2V. This allows ample room for the sync pulse even in a gain of +2 configuration. This results in dG and dP specifications of 0.05% and 0.05° while driving 150Ω at a gain of +2. Setting the black level to other values, although acceptable, will compromise peak performance. For example, looking at the single supply dG and dP curves for $R_L = 150\Omega$, if the output black level clamp is reduced from 1.2V to 0.6V dG/dP will increase from 0.05%/0.05° to 0.08%/0.25°. Note that in a gain of +2 configuration, this is the lowest black level allowed such that the sync tip doesn't go below 0V.

If your application requires that the output goes to ground, then the output stage of the EL2257C/EL2357C, like all other single supply op amps, requires an external pull down resistor tied to ground. As mentioned above, the current flowing through this resistor becomes the DC bias current for the output stage NPN transistor. As this current approaches zero, the NPN turns off, and dG and dP will increase. This becomes more critical as the load resistor is increased in value. While driving a light load, such as 1 kΩ, if the input black level is kept above 1.25V, dG and dP are a respectable 0.03% and 0.03°.

For other biasing conditions see the Differential Gain and Differential Phase vs. Input Voltage curves.

Output Drive Capability

In spite of their moderately low 5 mA of supply current, the EL2257C/EL2357C are capable of providing ±100 mA of output current into a 10Ω load, or ±60 mA into 50Ω. With this large output current capability, a 50Ω load can be driven to ±3V with $V_S = \pm 5V$, making it an excellent choice for driving isolation transformers in telecommunications applications.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will de-couple the EL2257C/EL2357C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output.

Applications Information — Contd.

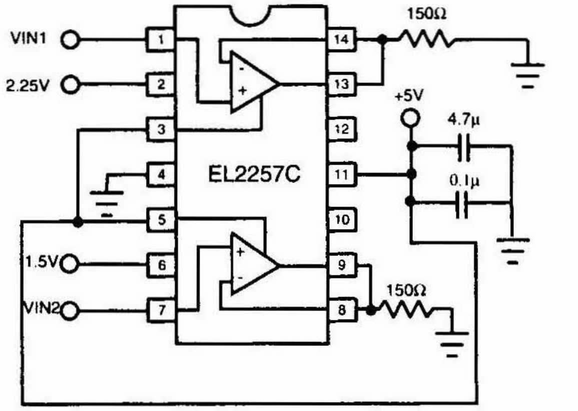
Disable/Power-Down

Each amplifier in the EL2257C/EL2357C can be individually disabled, placing each output in a high-impedance state. The disable or enable action takes only about 40 ns. When all amplifiers are disabled, the total supply current is reduced to 0 mA, thereby eliminating all power consumption by the EL2257C/EL2357C. The EL2257C/EL2357C amplifier's power down can be controlled by standard CMOS signal levels at each ENABLE pin. The applied CMOS signal is relative to the GND pin. For example, if a single +5V supply is used, the logic voltage levels will be +0.5V and +2.0V. If using dual ±5V supplies, the logic levels will be −4.5V and −3.0V. Letting all ENABLE pins float will disable the EL2257C/EL2357C. If the power-down feature is not desired, connect all ENABLE pins to the V_{S+} pin. The guaranteed logic levels of +0.5V and +2.0V are not standard TTL levels of +0.8V and +2.0V, so care must be taken if standard TTL will be used to drive the ENABLE pins.

Output Voltage Clamp

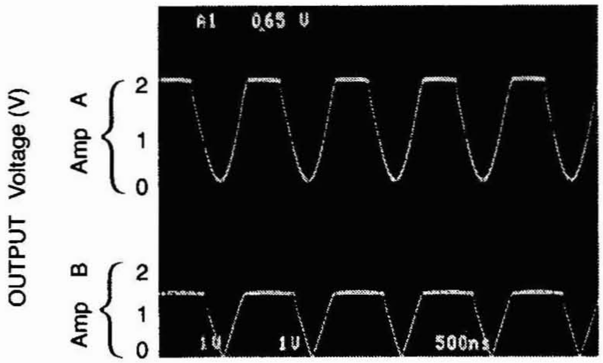
The EL2257C/EL2357C amplifiers have an output voltage clamp. This clamping action is fast, being activated almost instantaneously, and being deactivated in < 7 ns, and prevents the output voltage from going above the preset clamp voltage. This can be very helpful when the EL2257C/EL2357C are used to drive an A/D converter, as some converters can require long times to recover if overdriven. The output voltage remains at the clamp voltage level as long as the product of the input voltage and the gain setting exceeds the clamp voltage. For example, if the EL2257C/EL2357C is connected in a gain of 2, and +3V DC is applied to the CLAMP pin, any voltage higher than +1.5V at the inputs will be clamped and +3V will be seen at the output. Each amplifier of the EL2257C have their own CLAMP pin, so individual clamp levels may be set, whereas a single CLAMP pin controls the clamp level of the EL2357C.

Figure 1 below is the EL2257C with each amplifier unity gain connected. Amplifier A is being driven by a 3 Vp-p sinewave and has 2.25V applied to CLAMPA, while amplifier B is driven by a 3 Vp-p triangle wave and 1.5V is applied to CLAMPB. The resulting output waveforms, with their outputs being clamped is shown in Figure 2.



2257-21

Figure 1



2257-34

Figure 2

Applications Information — Contd.

Figure 3 shows the output of amplifier A of the same circuit being driven by a 0.5V to 2.75V square wave as the clamp voltage is varied from 1.0V to 2.5V, as well as the unclamped output signal. The rising edge of the signal is clamped to the voltage applied to the CLAMP pin almost instantaneously. The output recovers from the clamped mode within 5–7 ns, depending on the clamp voltage. Even when the CLAMP pin is taken 0.2V below the minimum 1.2V specified, the output is still clamped and recovers in about 11 ns.

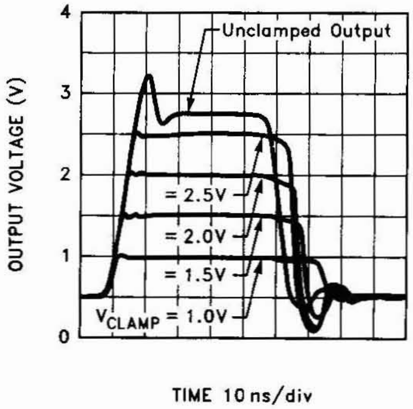


Figure 3

The clamp accuracy is affected by 1) the CLAMP pin voltage, 2) the input voltage, and 3) the load resistor. Depending upon the application, the accuracy may be as little as a few tens of millivolts up to a few hundred millivolts. Be sure to allow for these inaccuracies when choosing the clamp voltage. Curves of Clamp Accuracy vs. V_{CLAMP} and V_{IN} for 3 values of R_L are included in the Typical Performance Curves Section

Unlike amplifiers that clamp at the input and are therefore limited to non-inverting applications only, the EL2257C/EL2357C output clamp architecture works for both inverting and non-inverting gain applications. There is also no maximum voltage difference limitation between V_{IN} and V_{CLAMP} which is common on input clamped architectures.

The voltage clamp operates for any voltage between +1.2V above the GND pin, and the minimum output voltage swing, V_{OP}. Forcing the CLAMP pin much below +1.2V can saturate transistors and should therefore be avoided. Forcing the CLAMP pin above V_{OP} simply deactivates the CLAMP feature. In other words, one cannot expect to clamp any voltage higher than what the EL2257C/EL2357C can drive to in the first place. If the clamp feature is not desired, either let the CLAMP pin float or connect it to the V_{S+} pin.

EL2257C/EL2357C Comparator Application

The EL2257C/EL2357C can be used as a very fast, single supply comparator by utilizing the clamp feature. Most op amps used as comparators allow only slow speed operation because of output saturation issues. However, by applying a DC voltage to the CLAMP pin of the EL2257C/EL2357C, the maximum output voltage can be clamped, thus preventing saturation. Figure 4 below is amplifier A of an EL2257C implemented as a comparator. 2.25V DC is applied to the CLAMP pin, as well as the IN- pin. A differential signal is then applied between the inputs. Figure 5 shows the output square wave that results when a ±1V, 10 MHz triangular wave is applied, while Figure 6 is a graph of propagation delay vs. overdrive as a square wave is presented at the input.

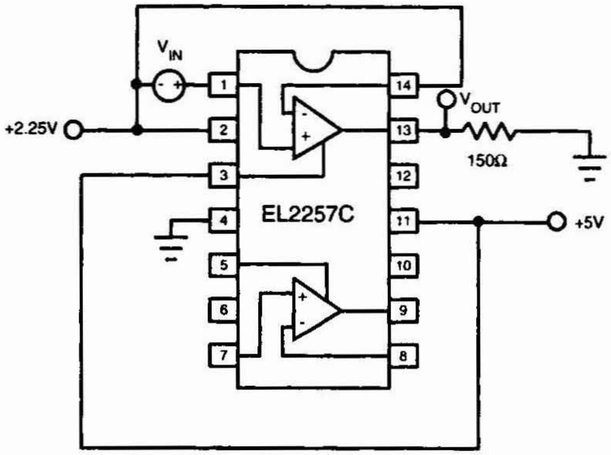
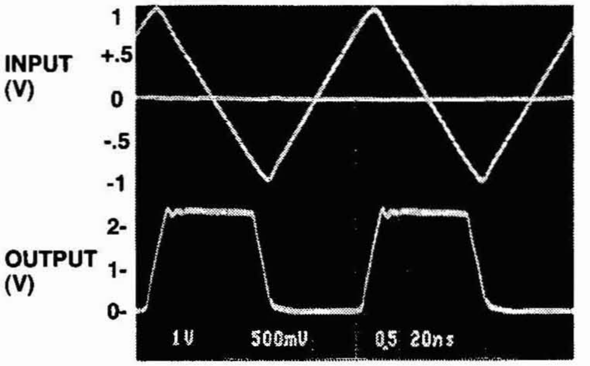


Figure 4

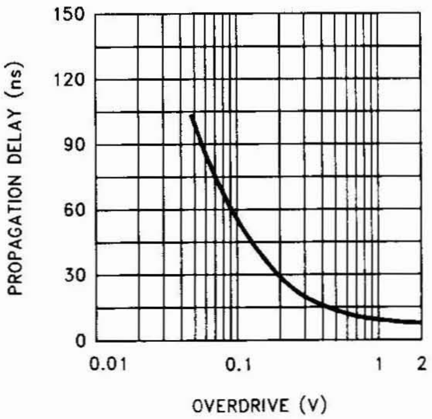
Applications Information — Contd.



2257-25

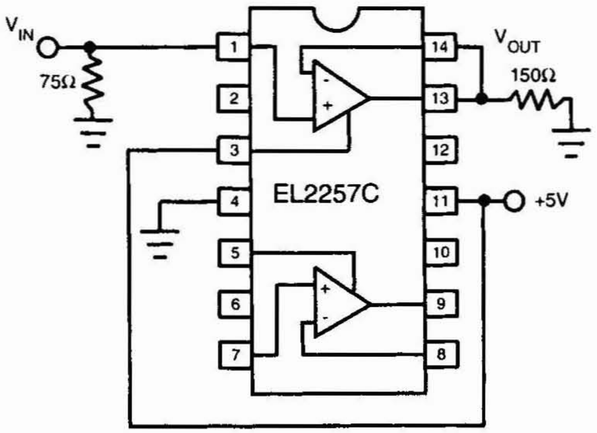
Figure 5

Propagation Delay vs Overdrive
EL2257/EL2357 as a Comparator



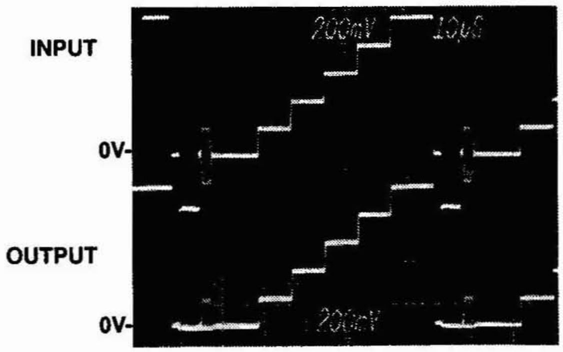
2257-26

Figure 6



2257-27

Figure 7



2257-28

Figure 8

Video Sync Pulse Remover Application

All CMOS Analog to Digital Converters (A/Ds) have a parasitic latch-up problem when subjected to negative input voltage levels. Since the sync tip contains no useful video information and it is a negative going pulse, we can chop it off. Figure 7 shows a unity gain connected amplifier A of an EL2257C. Figure 8 shows the complete input video signal applied at the input, as well as the output signal with the negative going sync pulse removed.

Multiplexing with the EL2257C/EL2357C

The ENABLE pins on the EL2257C/EL2357C allow for multiplexing applications. Figure 9 shows an EL2357C with all 3 outputs tied together, driving a back terminated 75Ω video load. Three sinewaves of varying amplitudes and frequencies are applied to the three inputs. Logic signals are applied to each of the ENABLE pins to cycle through turning each of the amplifiers on, one at a time. Figure 10 shows the resulting output waveform at V_{OUT}. Switching is complete

Applications Information — Contd.

in about 50 ns. Notice the outputs are tied directly together. Decoupling resistors at each output are not necessary. In fact, adding them approximately doubles the switching time to 100 ns.

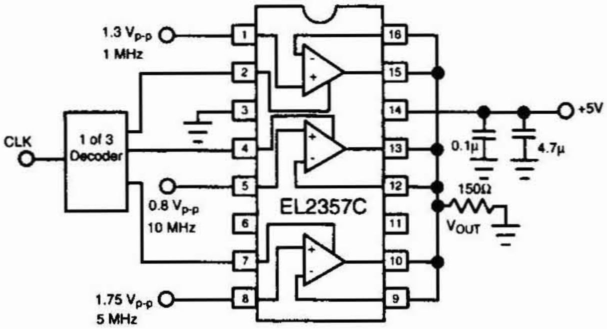


Figure 9

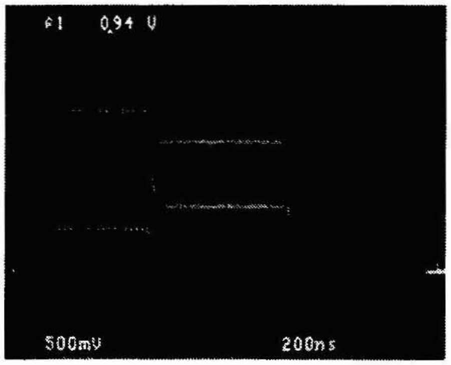


Figure 10

Short Circuit Current Limit

The EL2257C/EL2357C have internal short circuit protection circuitry that protect it in the event of its output being shorted to either supply rail. This limit is set to around 100 mA nominally and reduces with increasing junction temperature. It is intended to handle temporary shorts. If an output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±90 mA. A heat sink may be required to keep the junction temperature below absolute maximum when an output is shorted indefinitely.

Power Dissipation

With the high output drive capability of the EL2257C/EL2357C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2257C/EL2357C to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to [1]:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad [1]$$

where:

T_{JMAX} = Maximum Junction Temperature
T_{AMAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
PD_{MAX} = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or [2]

$$PD_{MAX} = N^{*}(V_S * I_{SMAX} + (V_S - V_{OUT}) * \frac{V_{OUT}}{R_L}) \quad [2]$$

where:

N = Number of amplifiers
V_S = Total Supply Voltage
I_{SMAX} = Maximum Supply Current per amplifier
V_{OUT} = Maximum Output Voltage of the Application
R_L = Load Resistance tied to Ground

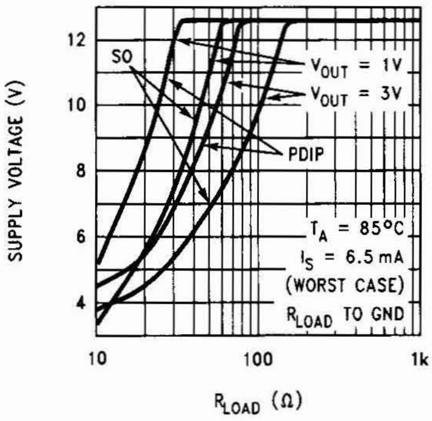
If we set the two PD_{MAX} equations, [1] and [2], equal to each other, and solve for V_S, we can get a family of curves for various loads and output voltages according to [3]:

$$V_S = \frac{\frac{R_L * (T_{JMAX} - T_{AMAX})}{N * \theta_{JA}} + (V_{OUT})^2}{(I_S * R_L) + V_{OUT}} \quad [3]$$

Applications Information — Contd.

Figures 11 and 12 below show total single supply voltage V_S vs. R_L for various output voltage swings for the PDIP and SOIC packages. The curves assume WORST CASE conditions of $T_A = +85°C$ and $I_S = 6.5$ mA per amplifier.

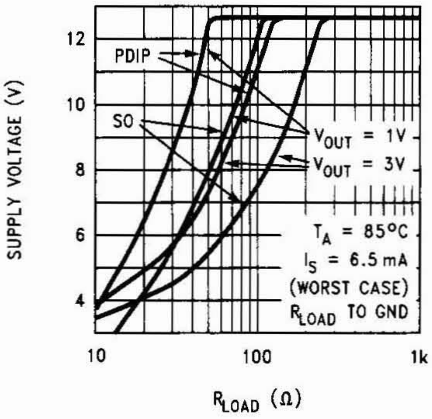
EL2257 Single Supply Voltage vs. R_{Load} for Various V_{OUT} and Packages



2257-31

Figure 11

EL2357 Single Supply Voltage vs. R_{Load} for Various V_{OUT} and Packages



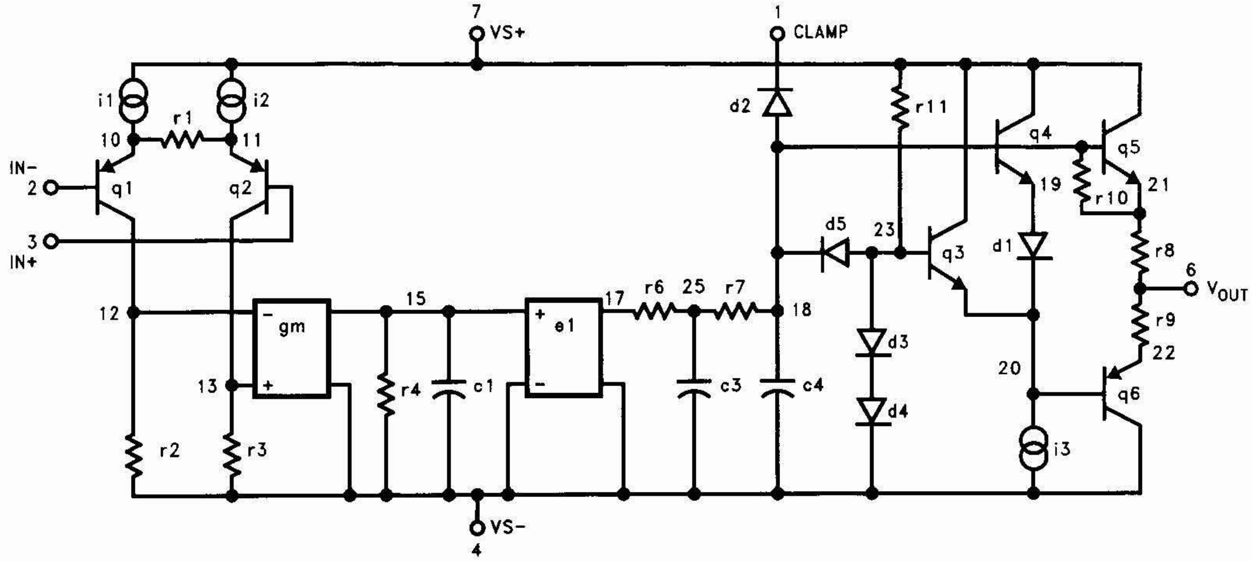
2257-32

Figure 12

EL2257C/EL2357C Macromodel -
(one channel)

```
* Revision A, October 1995
* Pin numbers reflect a standard single opamp.
* When not being used, the clamp pin, pin 1,
* should be connected to +Vsupply, pin 7
* Connections:    +input
*                 |   -input
*                 |   |   +Vsupply
*                 |   |   |   -Vsupply
*                 |   |   |   |   output
*                 |   |   |   |   |   clamp
*                 |   |   |   |   |   |
.subckt EL2257/el 3   2   7   4   6   1
*
* Input Stage
*
i1 7 10 250μA
i2 7 11 250μA
r1 10 11 4K
q1 12 2 10 qp
q2 13 3 11 qpa
r2 12 4 100
r3 13 4 100
*
* Second Stage & Compensation
*
gm 15 4 13 12 4.6m
r4 15 4 15Meg
c1 15 4 0.36pF
*
* Poles
*
e1 17 4 15 4 1.0
r6 17 25 400
c3 25 4 1pF
r7 25 18 500
c4 18 4 1pF
*
* Output Stage & Clamp
*
i3 20 4 1.0mA
q3 7 23 20 qn
q4 7 18 19 qn
q5 7 18 21 qn
q6 4 20 22 qp
q7 7 23 18 qn
d1 19 20 da
d2 18 1 da
r8 21 6 2
r9 22 6 2
r10 18 21 10k
r11 7 23 100k
d3 23 24 da
d4 24 4 da
d5 23 18 da
*
* Power Supply Current
*
ips 7 4 3.2mA
*
* Models
*
.model qn npn(is=800e-18 bf=150 tf=0.02nS)
.model qpa pnp(is=810e-18 bf=50 tf=0.02nS)
.model qp pnp(is=800e-18 bf=54 tf=0.02nS)
.model da d(tt=0nS)
.ends
```

EL2257C/EL2357C Macromodel - (one channel) — Contd.


7
VS+
1
CLAMP
i1
i2
r1
10
11
IN-
2
q1
q2
3
IN+
12
13
gm
15
e1
17
r6
25
r7
18
r2
r3
r4
c1
c3
c4
d2
r11
q4
q5
19
21
r10
d5
23
q3
d1
r8
6
V_{OUT}
r9
22
d3
d4
20
q6
i3
VS-
4

2257-33

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2160C
130 MHz Current Feedback Amplifier

Features

- 130 MHz 3 dB bandwidth ($A_V = +2$)
- 180 MHz 3 dB bandwidth ($A_V = +1$)
- 0.01% differential gain, $R_L = 500\Omega$
- 0.01° differential phase, $R_L = 500\Omega$
- Low supply current, 8.5 mA
- Wide supply range, ±2V to ±15V
- 80 mA output current (peak)
- Low cost
- 1500 V/µs slew rate
- Input common mode range to within 1.5V of supplies
- 35 ns settling time to 0.1%

Applications

- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converter

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2160CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2160CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL2160C is a current feedback operational amplifier with −3 dB bandwidth of 130 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, this amplifer uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

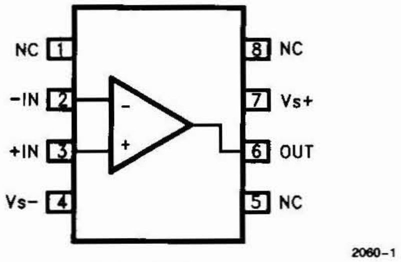
The EL2160C is designed to drive a double terminated 75Ω coax cable to video levels. Differential gain and phase are excellent when driving both loads of 500Ω (<0.01%/<0.01°) and double terminated 75Ω cables (0.025%/0.1°).

The amplifier can operate on any supply voltage from 4V (±2V) to 33V (±16.5V), yet consume only 8.5 mA at any supply voltage. Using industry standard pinouts, the EL2160C is available in 8-pin P-DIP and 8-pin SO packages. For dual and quad applications, please see the EL2260C/EL2460C datasheet.

Elantec's facilities comply with MIL-I-45208A and offer applicable quality specifications. See the Elantec document, QRA-2: *Elantec's Military Processing—Monolithic Products.*

Connection Diagram

EL2160C SO, P-DIP Packages



Top View

December 1995 Rev B

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S−	+33V	Operating Junction Temperature	
Voltage between +IN and −IN	±6V	Plastic Packages	150°C
Current into +IN or −IN	10 mA	Output Current	±50 mA
Internal Power Dissipation	See Curves	Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2160C	
V_{OS}	Input Offset Voltage	V_S = ±5V, ±15V	25°C		2	10	I	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		10		V	μV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		0.5	5	I	μA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		5	25	I	μA
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	25°C	50	55		II	dB
−ICMR	−Input Current Common Mode Rejection (Note 2)	V_S = ±5V, ±15V	25°C		0.2	5	I	μA/V
PSRR	Power Supply Rejection Ratio (Note 3)		25°C	75	95		II	dB
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.2	5	I	μA/V

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 15V$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2160C	
R_{OL}	Transimpedance (Note 4)	$V_S = \pm 15V$ $R_L = 400\Omega$	25°C	500	2000		I	kΩ
		$V_S = \pm 5V$ $R_L = 150\Omega$	25°C	500	1800		I	kΩ
$+R_{IN}$	+ Input Resistance		25°C	1.5	3.0		II	MΩ
$+C_{IN}$	+ Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range	$V_S = \pm 15V$	25°C		±13.5		V	V
		$V_S = \pm 5V$	25°C		±3.5		V	V
V_O	Output Voltage Swing	$R_L = 400\Omega$, $V_S = \pm 15V$	25°C	±12	±13.5		I	V
		$R_L = 150\Omega$, $V_S = \pm 15V$	25°C		±12		V	V
		$R_L = 150\Omega$, $V_S = \pm 5V$	25°C	±3.0	±3.7		I	V
I_{SC}	Output Short Circuit Current (Note 5)	$V_S = \pm 5V$, $V_S = \pm 15V$	25°C	60	100	150	I	mA
I_S	Supply Current	$V_S = \pm 15V$	25°C		8.5	12.0	I	mA
		$V_S = \pm 5V$	25°C		6.4	9.5	I	mA

Closed Loop AC Electrical Characteristics

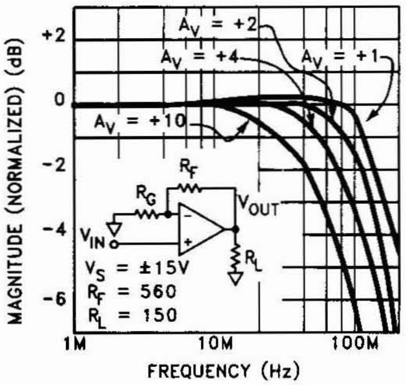
$V_S = \pm 15V, A_V = +2, R_F = 560\Omega, R_L = 150\Omega, T_A = 25°C$ unless otherwise noted

Parameter	Description	Conditions	Limits			Test Level	Units
			Min	Typ	Max	EL2160C	
BW	−3 dB Bandwidth (Note 8)	$V_S = \pm 15V, A_V = +2$		130		V	MHz
		$V_S = \pm 15V, A_V = +1$		180		V	MHz
		$V_S = \pm 5V, A_V = +2$		100		V	MHz
		$V_S = \pm 5V, A_V = +1$		110		V	MHz
SR	Slew Rate (Notes 6, 8)	$R_L = 400\Omega$	1000	1500		IV	V/µs
		$R_F = 1K\Omega, R_G = 110\Omega$ $R_L = 400\Omega$		1500		V	V/µs
t_r, t_f	Rise Time, Fall Time, (Note 8)	$V_{OUT} = \pm 500mV$		2.7		V	ns
t_{pd}	Propagation Delay (Note 8)			3.2		V	ns
OS	Overshoot (Note 8)	$V_{OUT} = \pm 500\ mV$		0		V	%
t_s	0.1% Settling Time (Note 8)	$V_{OUT} = \pm 10V$ $A_V = -1, R_L = 1K$		35		V	ns
dG	Differential Gain (Notes 7, 8)	$R_L = 150\Omega$		0.025		V	%
		$R_L = 500\Omega$		0.006		V	%
dP	Differential Phase (Notes 7, 8)	$R_L = 150\Omega$		0.1		V	deg (°)
		$R_L = 500\Omega$		0.005		V	deg (°)

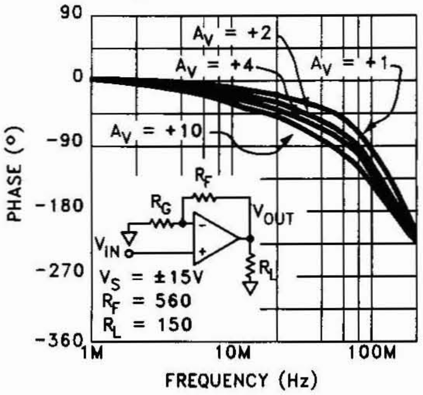
Note 1: Measured from T_{MIN} to T_{MAX}.
Note 2: $V_{CM} = \pm 10V$ for $V_S = \pm 15V$ and $T_A = 25°C$
$V_{CM} = \pm 3V$ for $V_S = \pm 5V$ and $T_A = 25°C$
Note 3: The supplies are moved from ±2.5V to ±15V.
Note 4: $V_{OUT} = \pm 7V$ for $V_S = \pm 15V$, and $V_{OUT} = \pm 2V$ for $V_S = \pm 5V$.
Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 6: Slew Rate is with V_{OUT} from +10V to −10V and measured at the 25% and 75% points.
Note 7: DC offset from −0.714V through +0.714V, AC amplitude 286 mV_{p-p}, f = 3.58 MHz.
Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

Typical Performance Curves

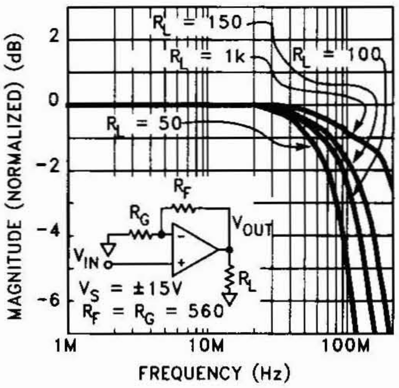
Non-Inverting Frequency Response (Gain)



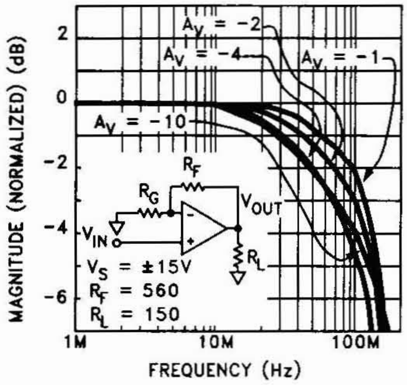
Non-Inverting Frequency Response (Phase)



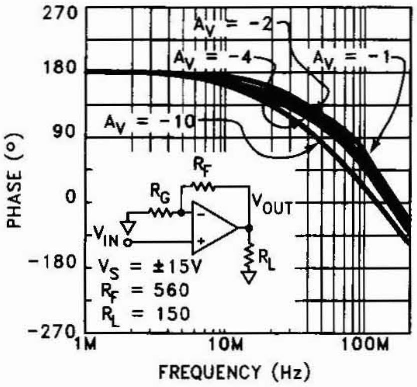
Frequency Response for Various R_L



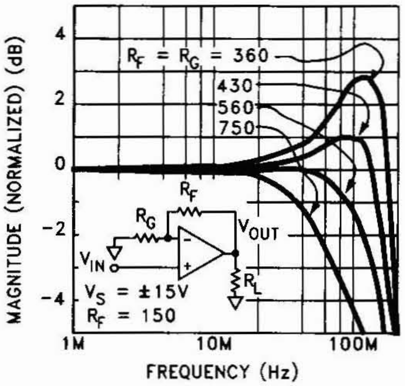
Inverting Frequency Response (Gain)



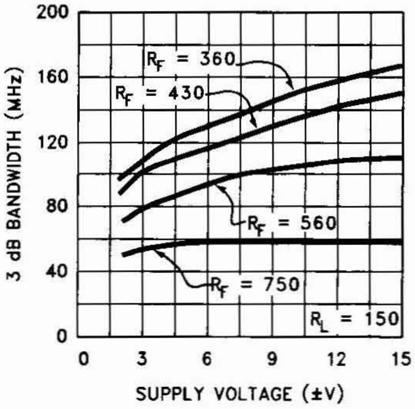
Inverting Frequency Response (Phase)



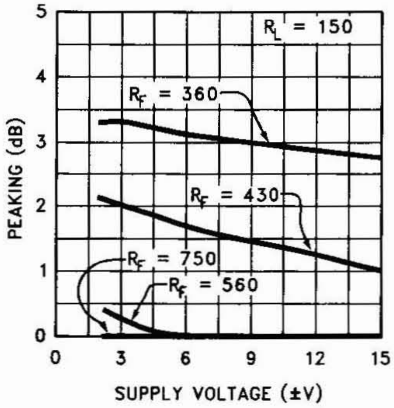
Frequency Response for Various R_F and R_G



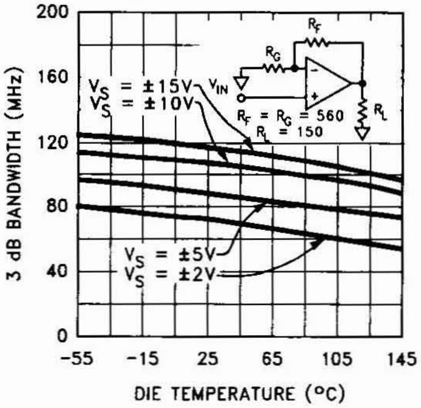
3 dB Bandwidth vs Supply Voltage for A_V = −1



Peaking vs Supply Voltage for A_V = −1



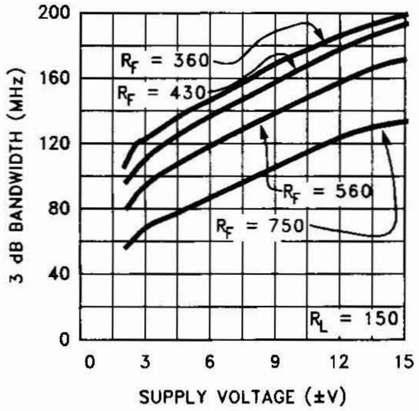
3 dB Bandwidth vs Temperature for A_V = − 1



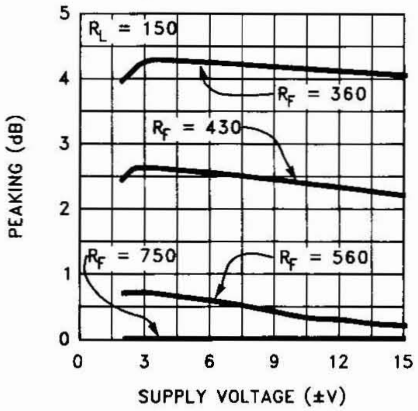
2060-2

Typical Performance Curves — Contd.

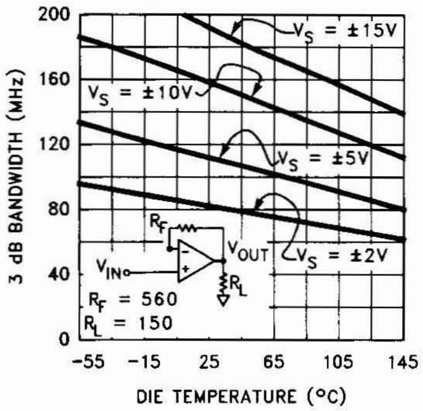
3 dB Bandwidth vs Supply Voltage for $A_V = +1$



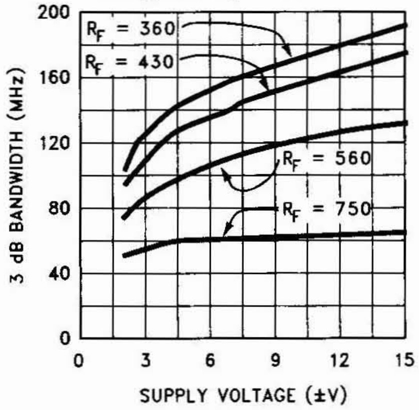
Peaking vs Supply Voltage for $A_V = +1$



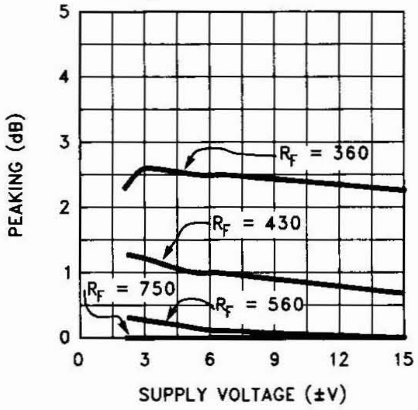
3 dB Bandwidth vs Temperature for $A_V = +1$



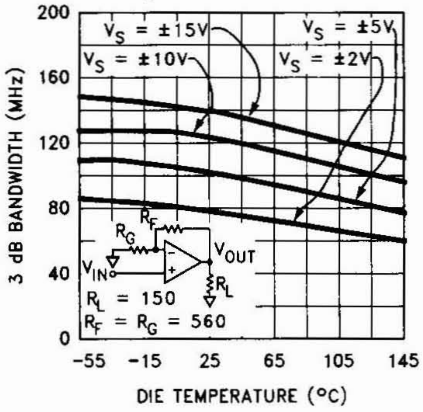
3 dB Bandwidth vs Supply Voltage for $A_V = +2$



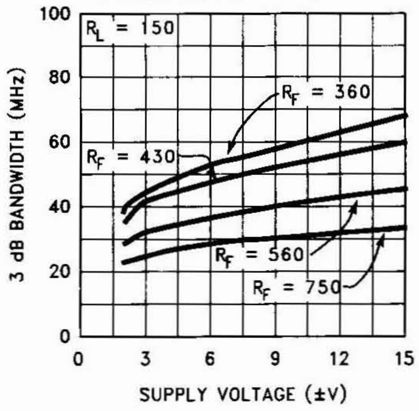
Peaking vs Supply Voltage for $A_V = +2$



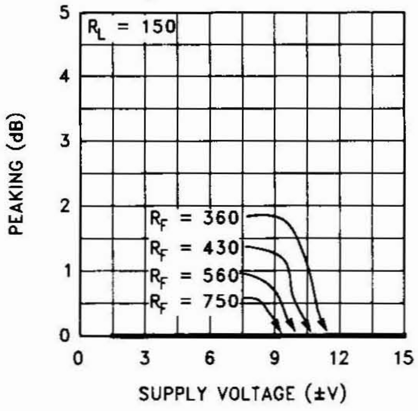
3 dB Bandwidth vs Temperature for $A_V = +2$



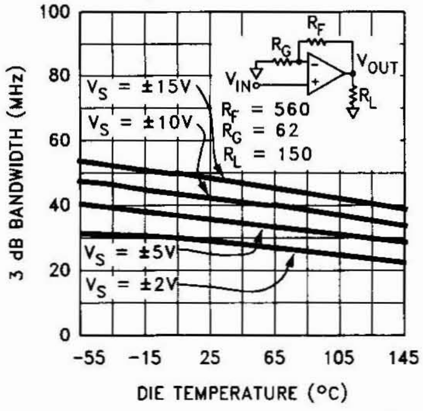
3 dB Bandwidth vs Supply Voltage for $A_V = +10$



Peaking vs Supply Voltage for $A_V = +10$



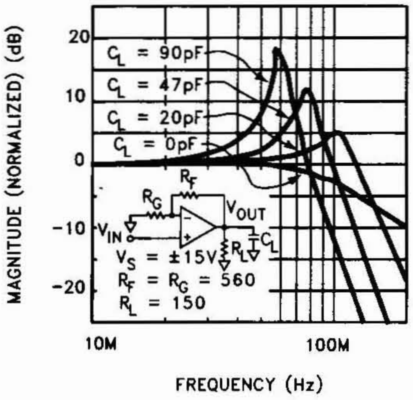
3 dB Bandwidth vs Temperature for $A_V = +10$



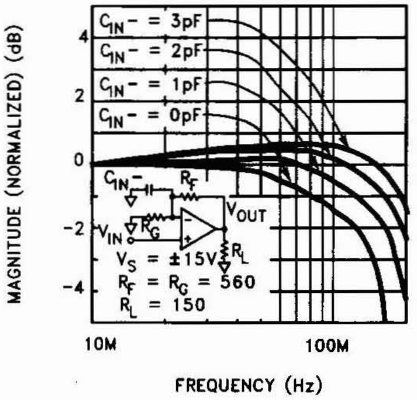
2060-3

Typical Performance Curves — Contd.

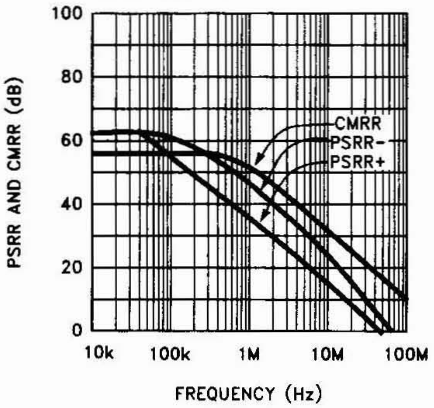
Frequency Response for Various C_L



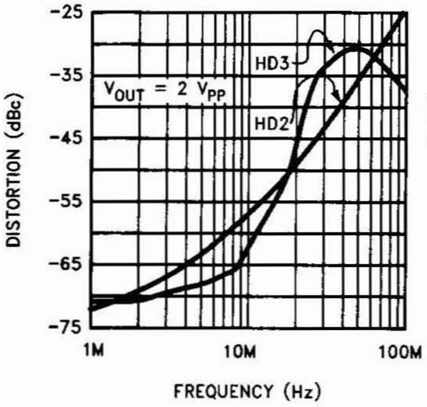
Frequency Response for Various C_{IN-}



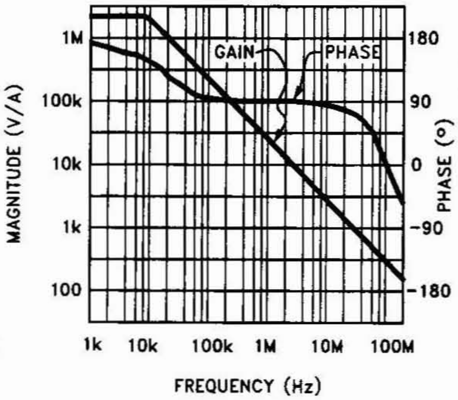
PSRR and CMRR vs Frequency



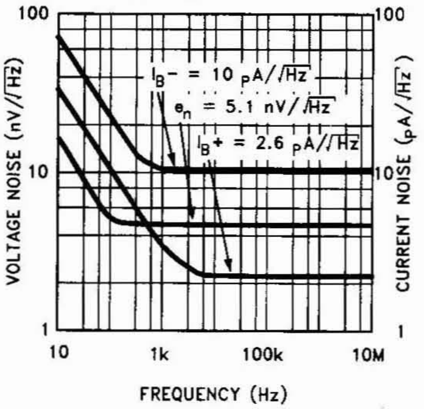
2nd and 3rd Harmonic Distortion vs Frequency



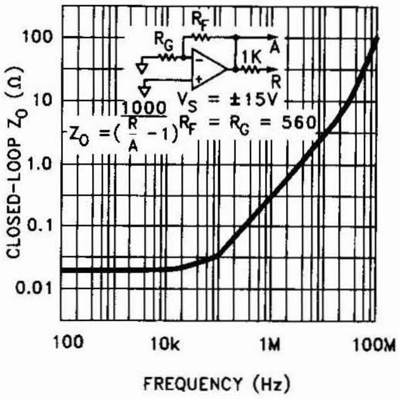
Transimpedance (R_{OL}) vs Frequency



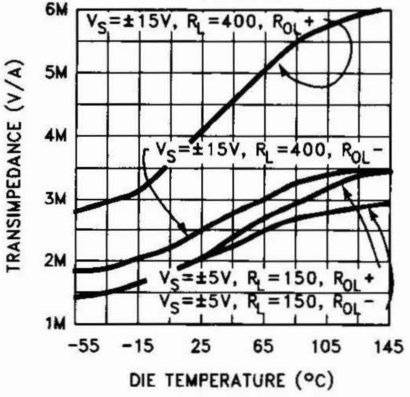
Voltage and Current Noise vs Frequency



Closed-Loop Output Impedance vs Frequency



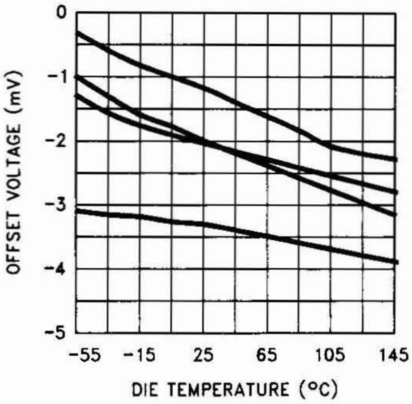
Transimpedance (R_{OL}) vs Die Temperature



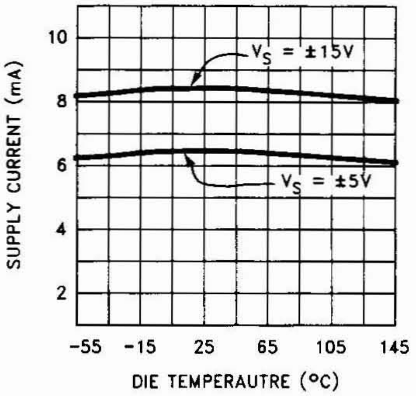
2060-4

Typical Performance Curves — Contd.

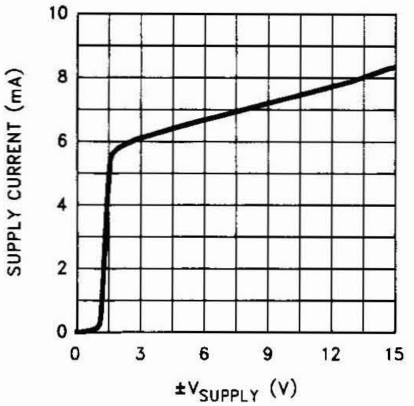
Offset Voltage vs Die Temperature (4 Samples)



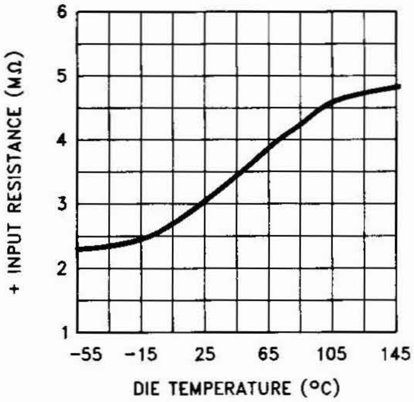
Supply Current vs Die Temperature



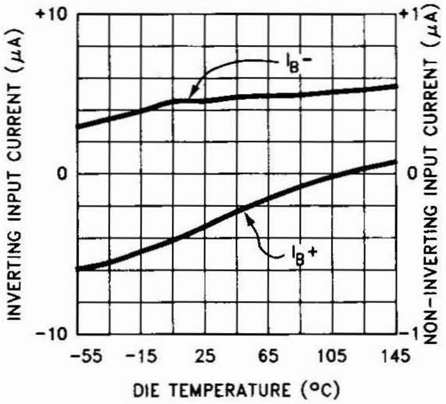
Supply Current vs Supply Voltage



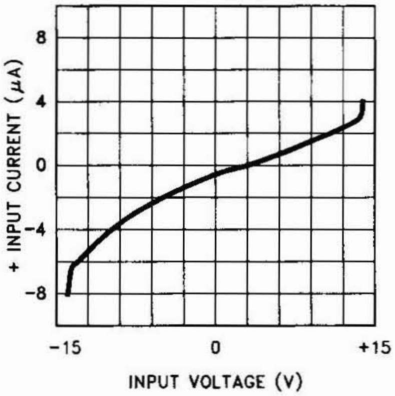
+Input Resistance vs Die Temperature



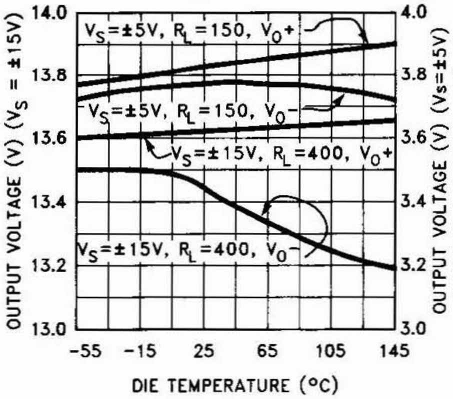
Input Current vs Die Temperature



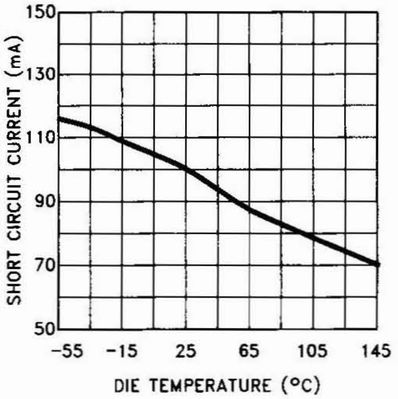
+Input Bias Current vs Input Voltage



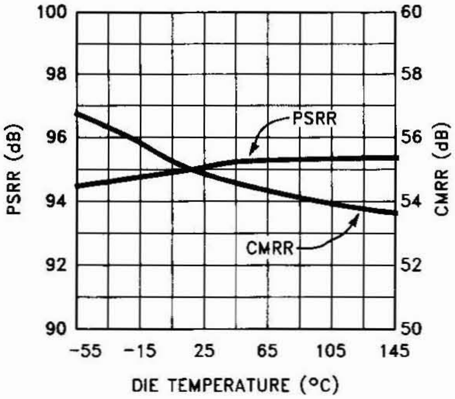
Output Voltage Swing vs Die Temperature



Short Circuit Current vs Die Temperature



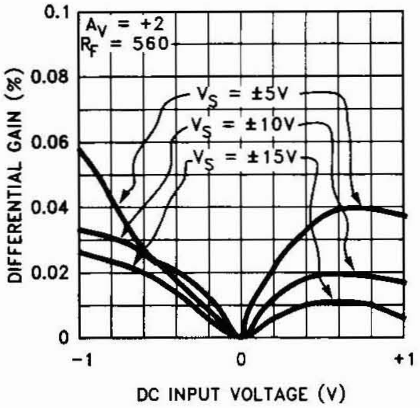
PSRR & CMRR vs Die Temperature



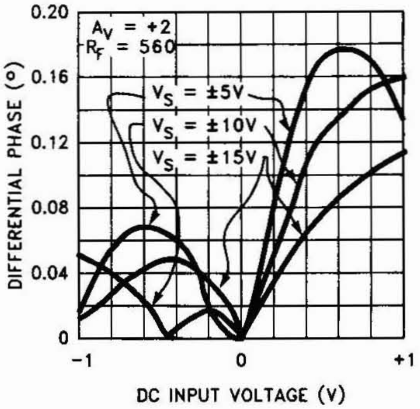
2060-5

Typical Performance Curves — Contd.

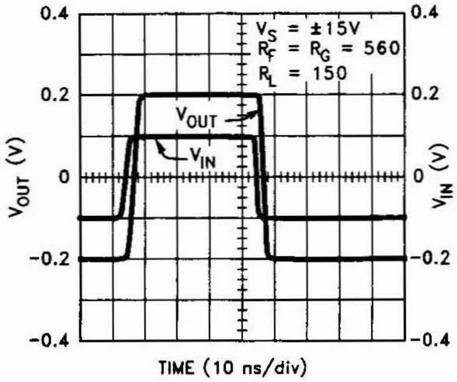
Differential Gain
vs DC Input Voltage,
R_L = 150



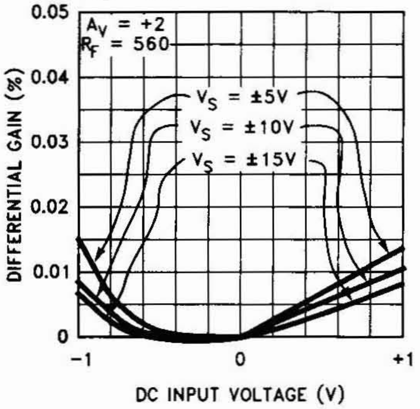
Differential Phase
vs DC Input Voltage,
R_L = 150



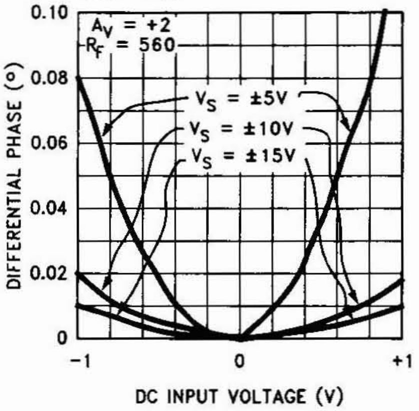
Small Signal
Pulse Response



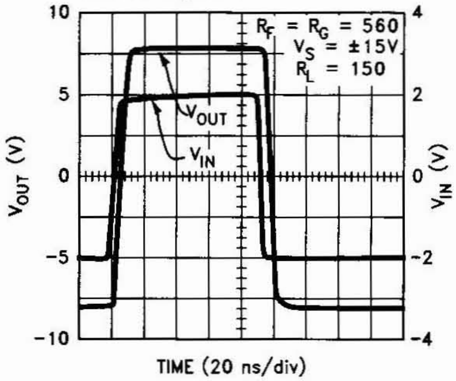
Differential Gain
vs DC Input Voltage,
R_L = 500



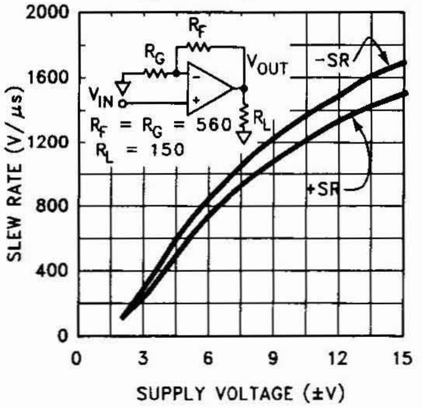
Differential Phase
vs DC Input Voltage,
R_L = 500



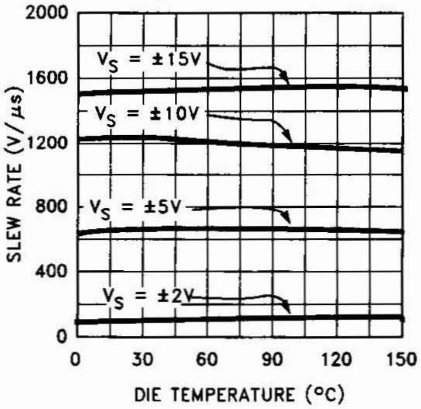
Large Signal
Pulse Response



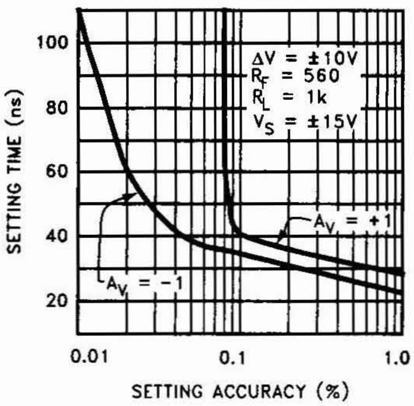
Slew Rate
vs Supply Voltage



Slew Rate
vs Temperature

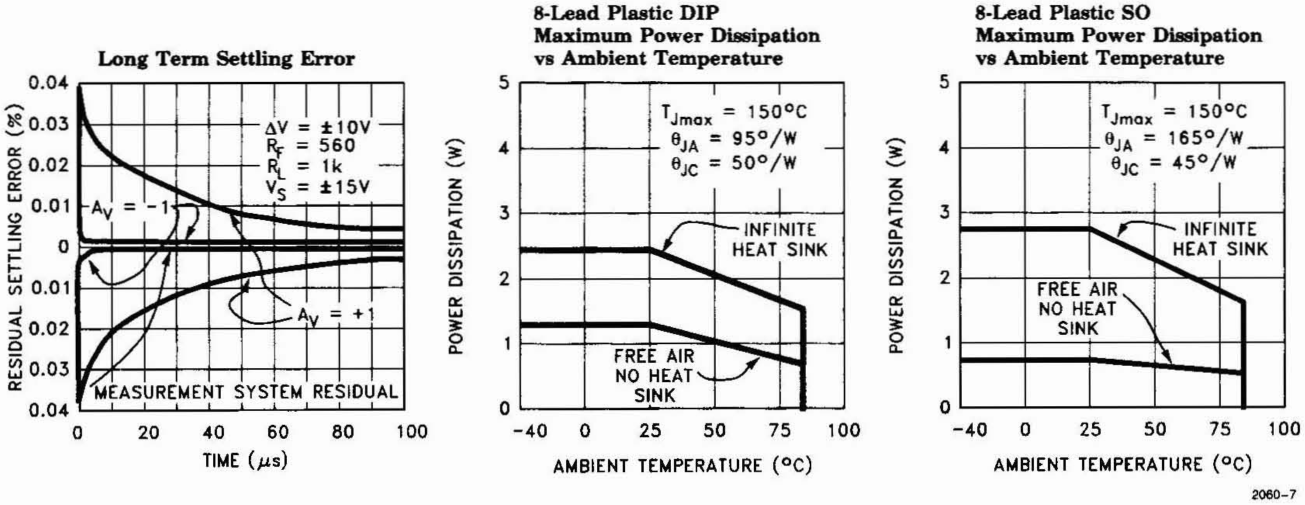


Settling Time
vs Settling Accuracy



2060-6

Typical Performance Curves — Contd.

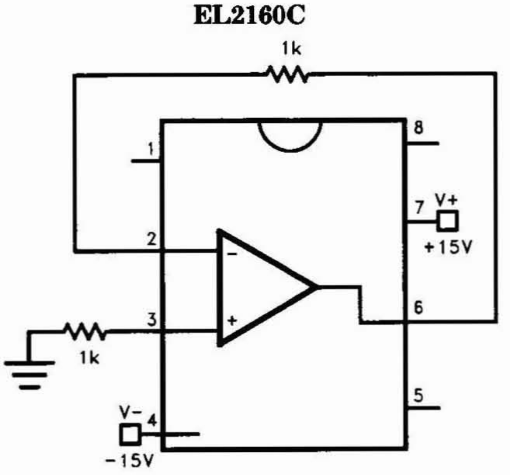

Long Term Settling Error

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature

8-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature

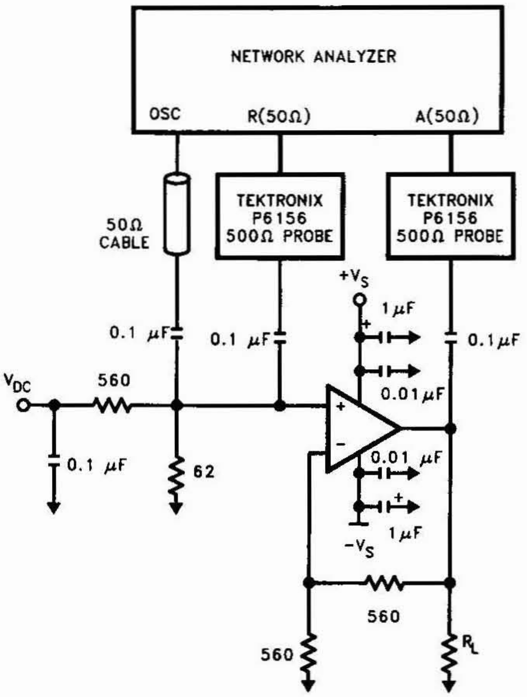
2060-7

Burn-In Circuit


EL2160C
1k
1
2
3
4
5
6
7
8
V+
+15V
V−
−15V
1k
−
+

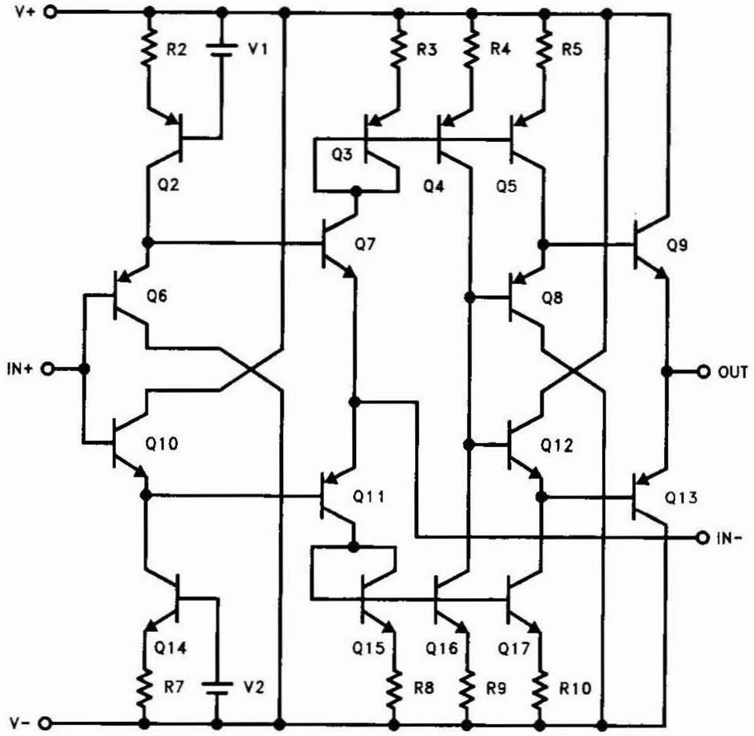
2060-8

Differential Gain and Phase Test Circuit


NETWORK ANALYZER
OSC
R(50Ω)
A(50Ω)
50Ω CABLE
TEKTRONIX P6156 500Ω PROBE
TEKTRONIX P6156 500Ω PROBE
0.1 µF
0.1 µF
0.1 µF
+V_S
1 µF
0.01 µF
V_DC
560
0.1 µF
62
0.01 µF
1 µF
-V_S
560
560
R_L

2060-9

Simplified Schematic (One Amplifier)


V+
R2
V1
R3
R4
R5
Q3
Q2
Q4
Q5
Q7
Q9
Q6
Q8
IN+
OUT
Q10
Q12
Q11
Q13
IN-
Q14
Q15
Q16
Q17
R7
V2
R8
R9
R10
V-

2060-10

Applications Information

Product Description

The EL2160C is a current mode feedback amplifier that offers wide bandwidth and good video specifications at a moderately low supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in industry standard pin-outs. Due to the current feedback architecture, the EL2160C closed-loop 3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3 dB bandwidth is somewhat dependent on the power supply voltage. As the supply voltage is decreased, internal junction capacitances increase, causing a reduction in closed loop bandwidth. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼″. The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO package, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL2160C when operating in the non-inverting configuration. The characteristic curve of gain vs. frequency with variations of $C_{IN}-$ emphasizes this effect. The curve illustrates how the bandwidth can be extended to beyond 200 MHz with some additional peaking with an additional 2 pF of capacitance at the $V_{IN}-$ pin for the case of $A_V = +2$. Higher values of capacitance will be required to obtain similar effects at higher gains.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values

The EL2160C has been designed and specified with $R_F = 560\Omega$ for $A_V = +2$. This value of feedback resistor yields extremely flat frequency response with little to no peaking out to 130 MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing R_F to 430Ω, bandwidth can be extended to 170 MHz with under 1 dB of peaking. Further reduction of R_F to 360Ω increases the bandwidth to 195 MHz with about 2.5 dB of peaking. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

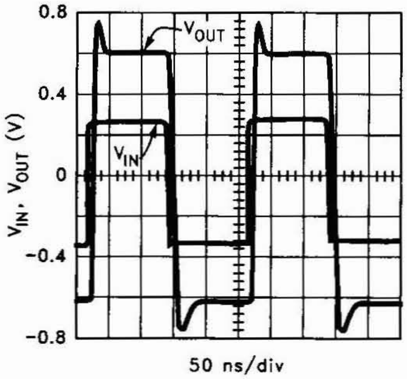
Bandwidth vs Temperature

Whereas many amplifier's supply current and consequently 3 dB bandwidth drop off at high temperature, the EL2160C was designed to have little supply current variations with temperature. An immediate benefit from this is that the 3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth only varies from 150 MHz to 110 MHz over the entire die junction temperature range of $0°C < T < 150°C$.

Applications Information — Contd.

Supply Voltage Range

The EL2160C has been designed to operate with supply voltages from ±2V to ±15V. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages. However, at ±2V supplies, the 3 dB bandwidth at $A_V = +2$ is a respectable 70 MHz. The following figure is an oscilloscope plot of the EL2160C at ±2V supplies, $A_V = +2$, $R_F = R_G = 560\Omega$, driving a load of 150Ω, showing a clean ±600 mV signal at the output.



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If a single supply is desired, values from +4V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2160C.

Settling Characteristics

The EL2160C offers superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2160C is not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for $A_V = +1$, there is approximately a 0.035% residual which tails away to 0.01% in about 40 μs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For $A_V = -1$, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With $A_V = -1$, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation

The EL2160C amplifier combines both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2160C remains within its absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or

$$P_{DMAX} = 2 * V_S * I_S + (V_S - V_{OUT}) * \frac{V_{OUT}}{R_L}$$

where I_S is the supply current. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, the EL2160C maintains almost constant supply

Applications Information — Contd.

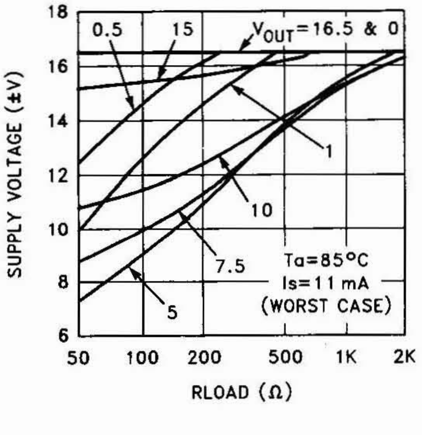
current over temperature so that AC performance is not degraded as much over the entire operating temperature range. Of course, this increase in performance doesn't come for free. Since the current has increased, supply voltages must be limited so that maximum power ratings are not exceeded.

The EL2160C consumes typically 8.5 mA and maximum 11.0 mA. The worst case power in an IC occurs when the output voltage is at half supply, if it can go that far, or its maximum values if it cannot reach half supply. If we set the two P_{DMAX} equations equal to each other, and solve for V_S, we can get a family of curves for various loads and output voltages according to:

$$V_S = \frac{\dfrac{R_L * (T_{JMAX} - T_{AMAX})}{\theta_{JA}} + (V_{OUT})^2}{(2 * I_S * R_L) + V_{OUT}}$$

The following curves show supply voltage ($\pm V_S$) vs R_{LOAD} for various output voltage swings for the 2 different packages. The curves assume worst case conditions of $T_A = +85°C$ and $I_S = 11$ mA.

Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)



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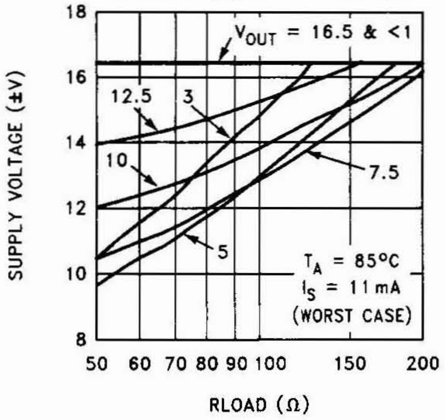
Supply Voltage vs R_{LOAD} for Various V_{OUT} (PDIP Package)



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The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit

The EL2160C has an internal current limit that protects the circuit in the event of the output being shorted to ground. This limit is set at 100 mA nominally and reduces with junction temperature. At a junction temperature of 150°C, the current limits at about 65 mA. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2160C to survive an indefinite short.

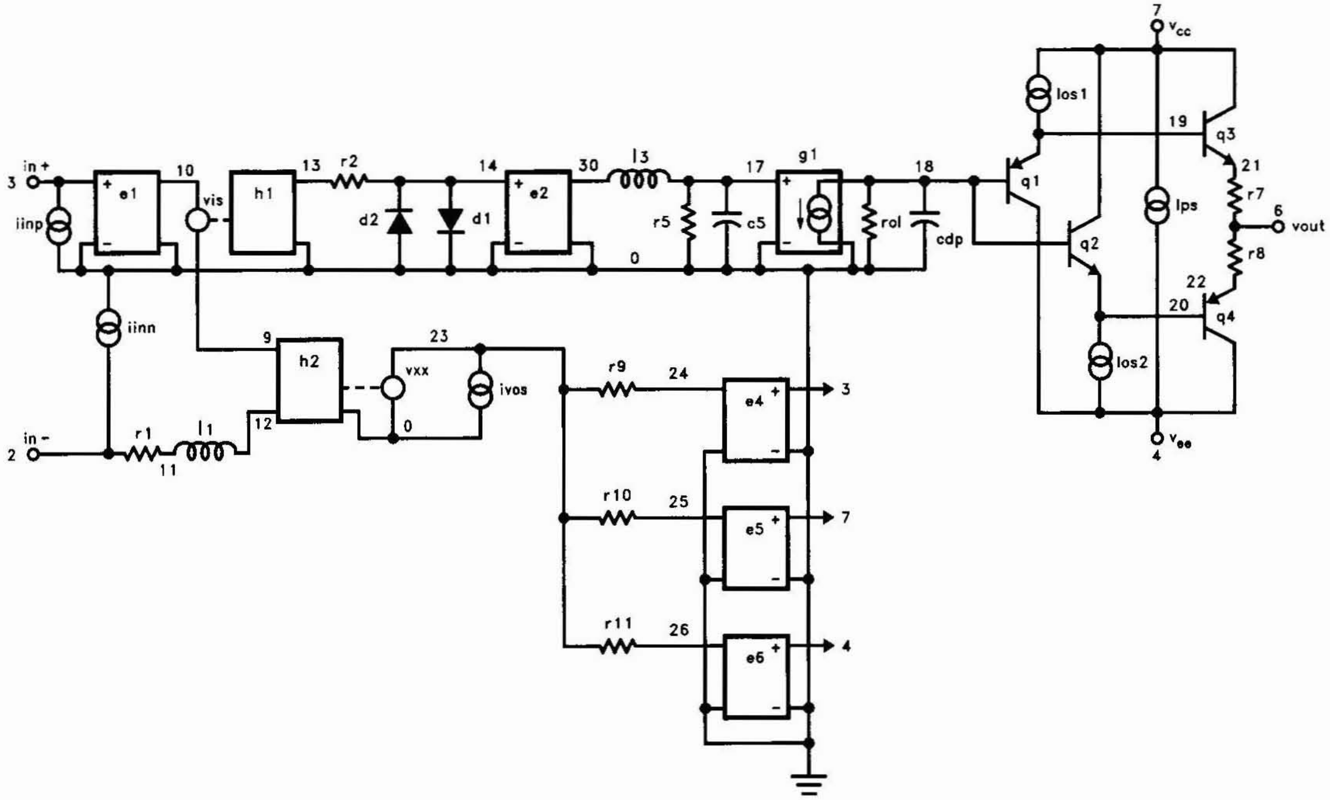
Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2160C from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistor at the output.

EL2160C Macromodel

```
* Revision A, November 1993
* AC Characteristics used CIN- (pin 2) = 1 pF; RF = 560Ω
* Connections:           +input
*                          |    -input
*                          |      |    +Vsupply
*                          |      |      |    -Vsupply
*                          |      |      |      |    output
*                          |      |      |      |      |
.subckt EL2160C/EL         3      2      7      4      6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 130
l1 11 12 25nH
iinp 3 0 0.5μA
iinm 2 0 5μA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.43μH
c5 17 0 0.27pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 2Meg
cdp 18 0 2.285pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2mA
ios2 20 4 2mA
*
* Supply Current
*
ips 7 4 3mA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.1ns)
.model qp pnp (is=5e-15 bf=100 tf=0.1ns)
.model dclamp d (is=1e-30 ibv=0.266 bv=2.24 n=4)
.ends
```

EL2160C Macromodel — Contd.


7
V_{cc}
Ios1
19
q3
in +
3
10
13
r2
14
30
l3
17
g1
18
21
iinp
e1
vis
h1
d2
d1
e2
r5
c5
rol
cdp
q1
Ips
r7
6
vout
0
q2
r8
22
20
q4
iinn
9
h2
23
vxx
ivos
r9
24
e4
3
Ios2
V_{ee}
4
12
0
in -
2
r1
l1
11
r10
25
e5
7
r11
26
e6
4

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élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2260C/EL2460C

Dual/Quad 130 MHz Current Feedback Amplifiers

Features

- 130 MHz 3 dB bandwidth ($A_V = +2$)
- 180 MHz 3 dB bandwidth ($A_V = +1$)
- 0.01% differential gain, $R_L = 500\Omega$
- 0.01° differential phase, $R_L = 500\Omega$
- Low supply current, 7.5 mA per amplifier
- Wide supply range, ±2V to ±15V
- 80 mA output current (peak)
- Low cost
- 1500 V/μs slew rate
- Input common mode range to within 1.5V of supplies
- 35 ns settling time to 0.1%

Applications

- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converter

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2260CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2260CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2460CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL2460CS	−40°C to +85°C	14-Pin SOIC	MDP0027

General Description

The EL2260C/EL2460C are dual/quad current feedback operational amplifiers with −3 dB bandwidth of 130 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, these amplifers use current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

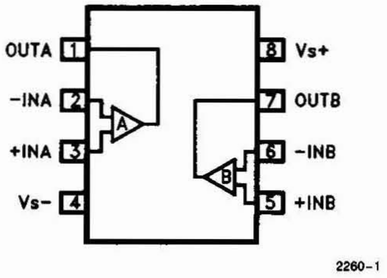
The EL2260C/EL2460C are designed to drive a double terminated 75Ω coax cable to video levels. Differential gain and phase are excellent when driving both loads of 500Ω (<0.01%/<0.01°) and double terminated 75Ω cables (0.025%/0.1°).

The amplifiers can operate on any supply voltage from 4V (±2V) to 33V (±16.5V), yet consume only 7.5 mA per amplifier at any supply voltage. Using industry standard pinouts, the EL2260C is available in 8-pin P-DIP and 8-pin SO packages, while the EL2460C is available in 14-pin P-DIP and 14-pin SO packages.

Elantec's facilities comply with MIL-I-45208A and offer applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing—Monolithic Products.*

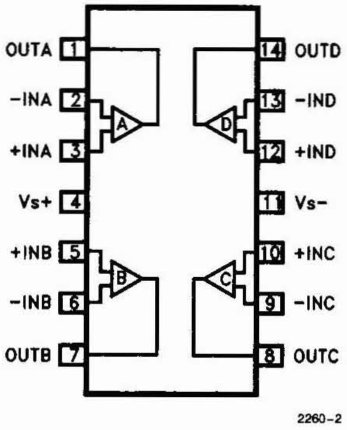
Connection Diagrams

EL2260C SO, P-DIP Packages



Top View

EL2460C SO, P-DIP Packages



Top View

EL2260C/EL2460C

Dual/Quad 130 MHz Current Feedback Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+33V	Operating Ambient Temperature Range	−40°C to +85°C
Voltage between +IN and −IN	±6V	Operating Junction Temperature	
Current into +IN or −IN	10 mA	Plastic Packages	150°C
Internal Power Dissipation	See Curves	Storage Temperature Range	−65°C to +150°C
		Output Current	±50 mA

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2260C EL2460C	
V_{OS}	Input Offset Voltage	V_S = ±5V, ±15V	25°C		2	10	I	mV
			T_{MIN}, T_{MAX}			15	III	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		10		V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		0.5	5	I	µA
			T_{MIN}, T_{MAX}			10	III	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		5	25	I	µA
			T_{MIN}, T_{MAX}			35	III	µA
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	Full	50	55		II	dB
−ICMR	−Input Current Common Mode Rejection (Note 2)	V_S = ±5V, ±15V	25°C		0.2	5	I	µA/V
			T_{MIN}, T_{MAX}			5	III	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		Full	75	95		II	dB
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.2	5	I	µA/V
			T_{MIN}, T_{MAX}			5	III	µA/V

Open Loop DC Electrical Characteristics — Contd.

V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2260C EL2460C	
R_{OL}	Transimpedance (Note 4)	V_S = ±15V R_L = 400Ω	25°C	500	2000		I	kΩ
			T_{MIN}, T_{MAX}	250			III	kΩ
		V_S = ±5V R_L = 150Ω	25°C	500	1800		I	kΩ
			T_{MIN}, T_{MAX}	250			III	kΩ
$+R_{IN}$	+ Input Resistance		Full	1.5	3.0		II	MΩ
$+C_{IN}$	+ Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range	V_S = ±15V	25°C		±13.5		V	V
		V_S = ±5V	25°C		±3.5		V	V
V_O	Output Voltage Swing	R_L = 400Ω, V_S = ±15V	25°C	±12	±13.5		I	V
			T_{MIN}, T_{MAX}	±11			III	V
		R_L = 150Ω, V_S = ±15V	25°C		±12		V	V
		R_L = 150Ω, V_S = ±5V	25°C	±3.0	±3.7		I	V
			T_{MIN}, T_{MAX}	±2.5			III	V
I_{SC}	Output Short Circuit Current (Note 5)	V_S = ±5V, V_S = ±15V	25°C	60	100	150	I	mA
I_S	Supply Current (Per Amplifier)	V_S = ±15V	25°C		7.5	11.0	I	mA
			T_{MIN}, T_{MAX}			11.0	III	mA
		V_S = ±5V	25°C		5.4	8.5	I	mA
			T_{MIN}, T_{MAX}			8.5	III	mA

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +2$, $R_F = 560\Omega$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise noted

Parameter	Description	Test Conditions	Limits			Test Level	Units
			Min	Typ	Max	EL2260C EL2460C	
BW	−3 dB Bandwidth (Note 8)	$V_S = \pm 15V, A_V = +2$		130		V	MHz
		$V_S = \pm 15V, A_V = +1$		180		V	MHz
		$V_S = \pm 5V, A_V = +2$		100		V	MHz
		$V_S = \pm 5V, A_V = +1$		110		V	MHz
SR	Slew Rate (Notes 6, 8)	$R_L = 400\Omega$	1000	1500		IV	V/µs
		$R_F = 1K\Omega, R_G = 110\Omega$ $R_L = 400\Omega$		1500		V	V/µs
t_r, t_f	Rise Time, Fall Time, (Note 8)	$V_{OUT} = \pm 500mV$		2.7		V	ns
t_{pd}	Propagation Delay (Note 8)			3.2		V	ns
OS	Overshoot (Note 8)	$V_{OUT} = \pm 500$ mV		0		V	%
t_s	0.1% Settling Time (Note 8)	$V_{OUT} = \pm 10V$ $A_V = -1, R_L = 1K$		35		V	ns
dG	Differential Gain (Notes 7, 8)	$R_L = 150\Omega$		0.025		V	%
		$R_L = 500\Omega$		0.006		V	%
dP	Differential Phase (Notes 7, 8)	$R_L = 150\Omega$		0.1		V	deg (°)
		$R_L = 500\Omega$		0.005		V	deg (°)

Note 1: Measured from T_{MIN} to T_{MAX}.

Note 2: $V_{CM} = \pm 10V$ for $V_S = \pm 15V$ and $T_A =$ Full
$V_{CM} = \pm 3V$ for $V_S = \pm 5V$ and $T_A = 25°C$
$V_{CM} = \pm 2V$ for $V_S = \pm 5V$ and $T_A = T_{MIN}, T_{MAX}$

Note 3: The supplies are moved from ±2.5V to ±15V.

Note 4: $V_{OUT} = \pm 7V$ for $V_S = \pm 15V$, and $V_{OUT} = \pm 2V$ for $V_S = \pm 5V$.

Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

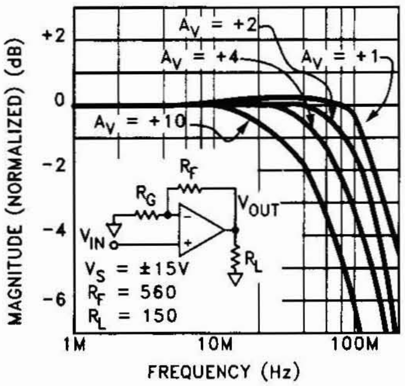
Note 6: Slew Rate is with V_{OUT} from +10V to −10V and measured at the 25% and 75% points.

Note 7: DC offset from −0.714V through +0.714V, AC amplitude 286 mV_{p-p}, f = 3.58 MHz.

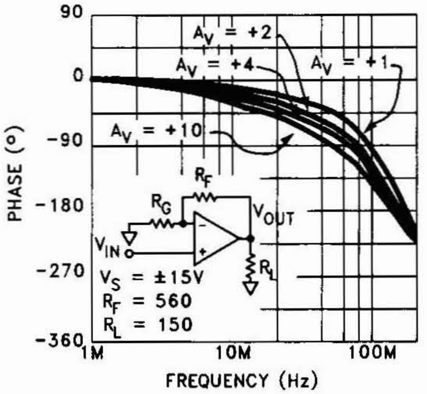
Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

Typical Performance Curves

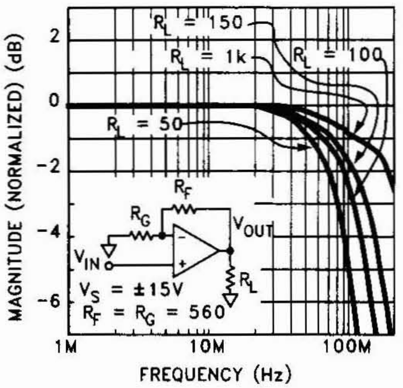
Non-Inverting Frequency Response (Gain)



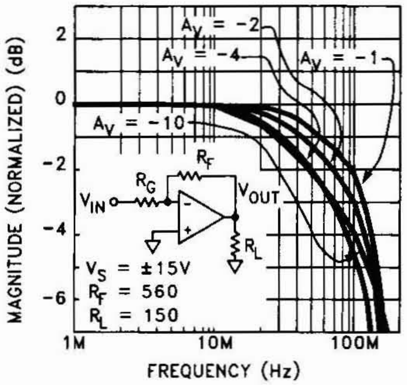
Non-Inverting Frequency Response (Phase)



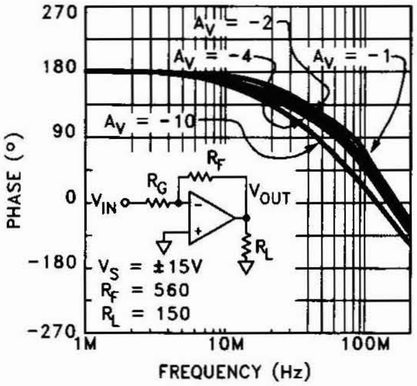
Frequency Response for Various R_L



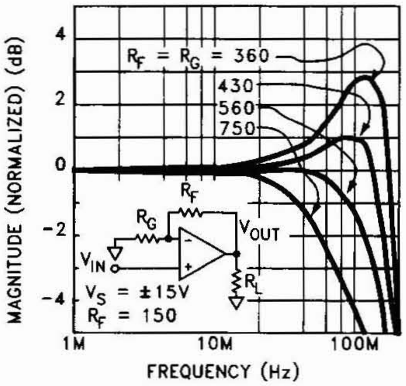
Inverting Frequency Response (Gain)



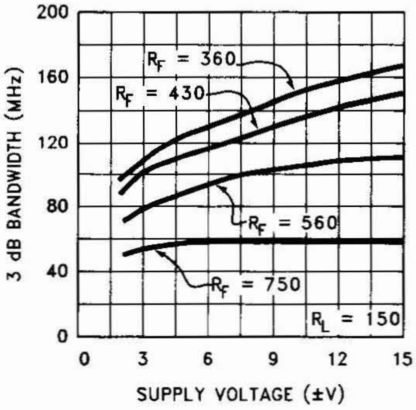
Inverting Frequency Response (Phase)



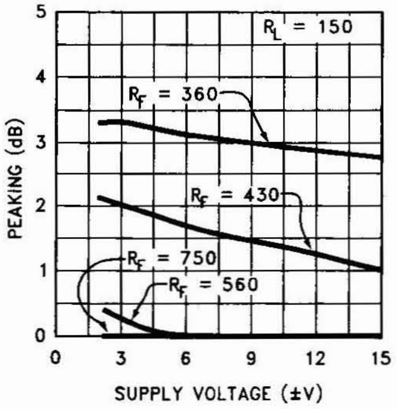
Frequency Response for Various R_F and R_G



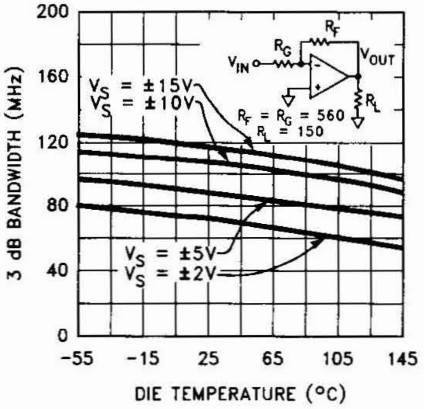
3 dB Bandwidth vs Supply Voltage for $A_V = -1$



Peaking vs Supply Voltage for $A_V = -1$



3 dB Bandwidth vs Temperature for $A_V = -1$



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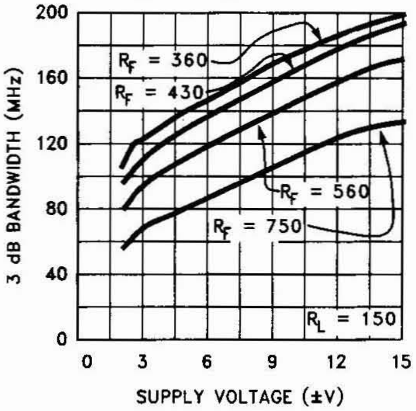
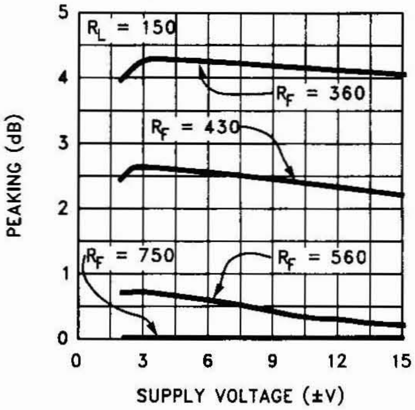
Typical Performance Curves — Contd.

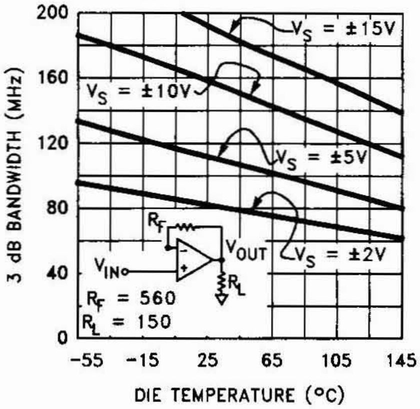
3 dB Bandwidth vs Supply Voltage for $A_V = +1$



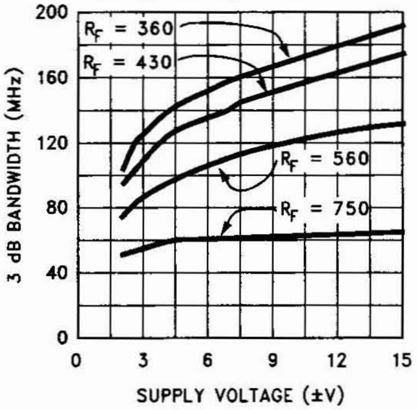
Peaking vs Supply Voltage for $A_V = +1$



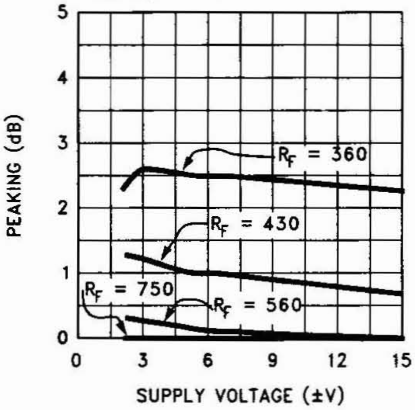
3 dB Bandwidth vs Temperature for $A_V = +1$



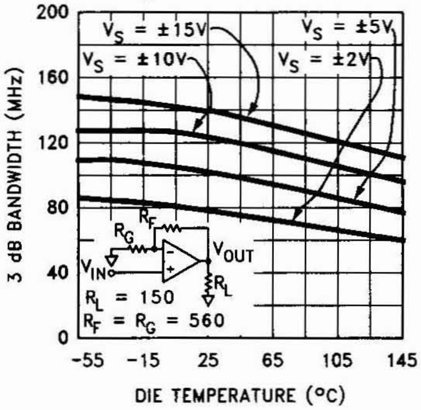
3 dB Bandwidth vs Supply Voltage for $A_V = +2$



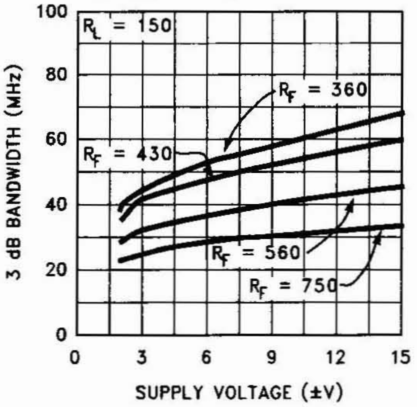
Peaking vs Supply Voltage for $A_V = +2$



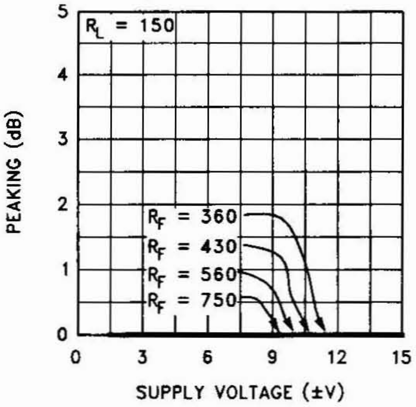
3 dB Bandwidth vs Temperature for $A_V = +2$



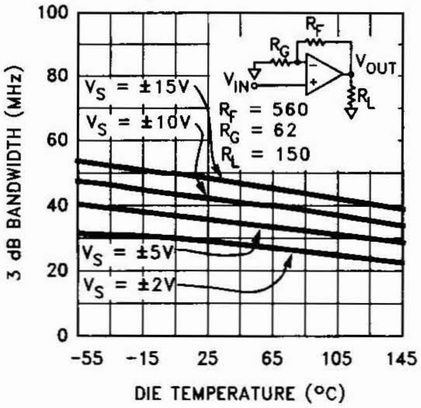
3 dB Bandwidth vs Supply Voltage for $A_V = +10$



Peaking vs Supply Voltage for $A_V = +10$



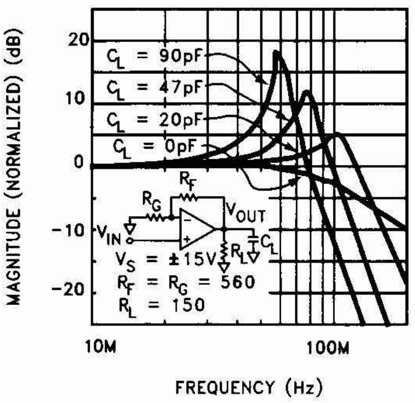
3 dB Bandwidth vs Temperature for $A_V = +10$



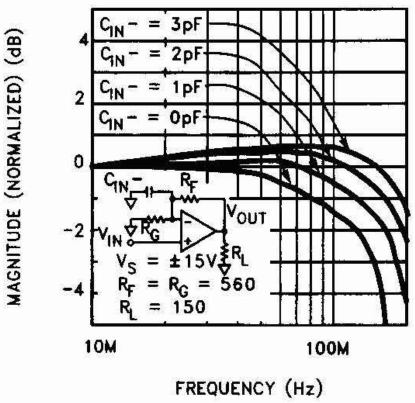
2260-4

Typical Performance Curves — Contd.

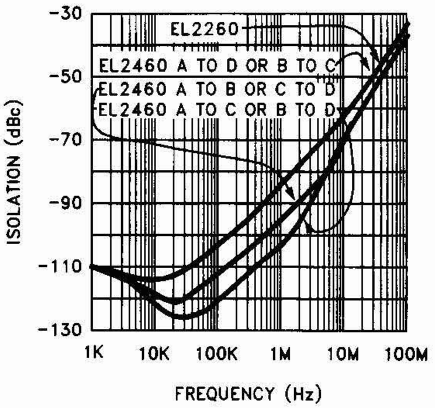
Frequency Response for Various C_L



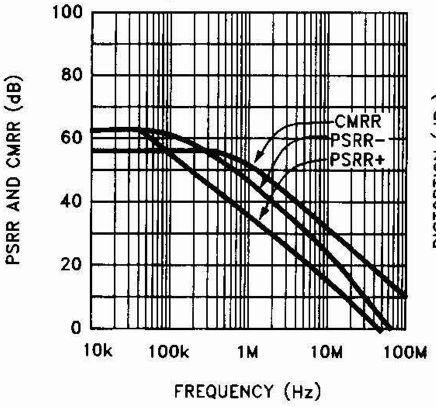
Frequency Response for Various C_{IN-}



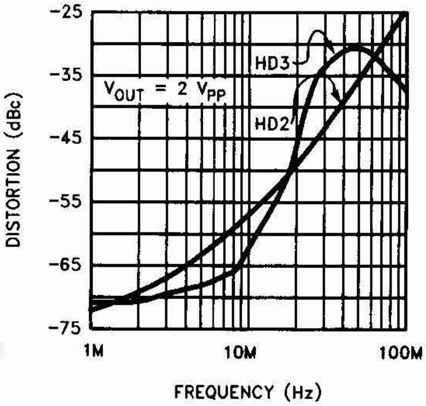
Channel to Channel Isolation vs Frequency



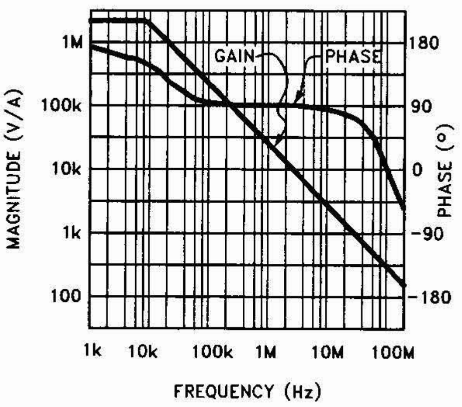
PSRR and CMRR vs Frequency



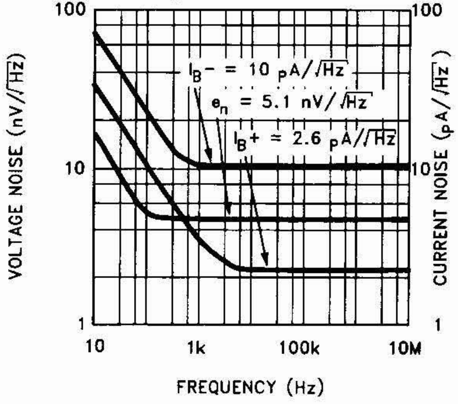
2nd and 3rd Harmonic Distortion vs Frequency



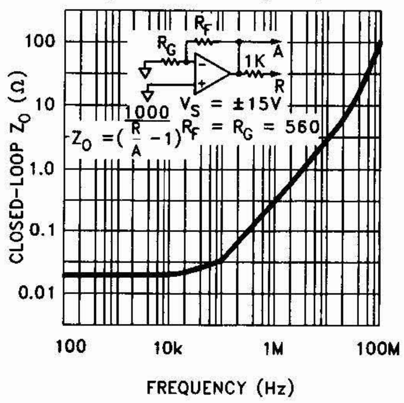
Transimpedance (R_{OL}) vs Frequency



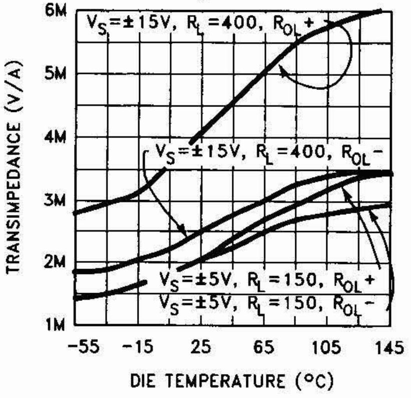
Voltage and Current Noise vs Frequency



Closed-Loop Output Impedance vs Frequency



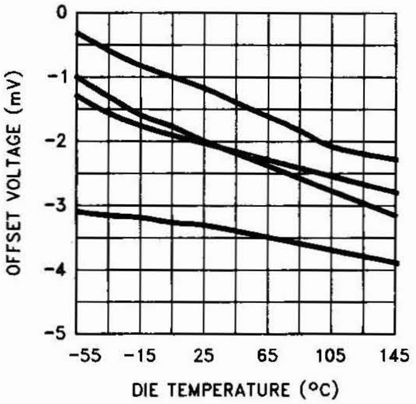
Transimpedance (R_{OL}) vs Die Temperature



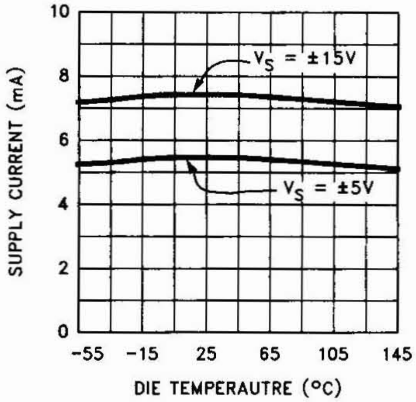
2260-5

Typical Performance Curves — Contd.

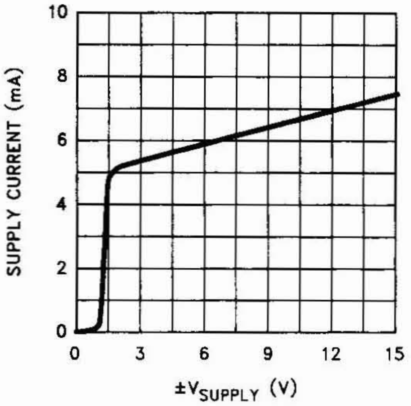
Offset Voltage vs Die Temperature (4 Samples)



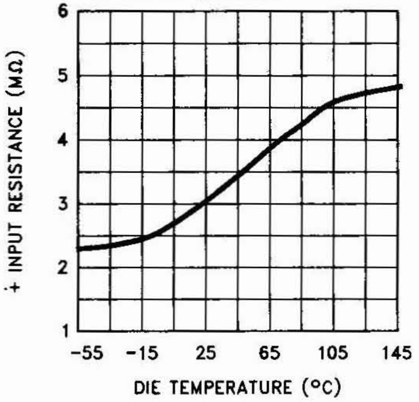
Supply Current vs Die Temperature (Per Amplifier)



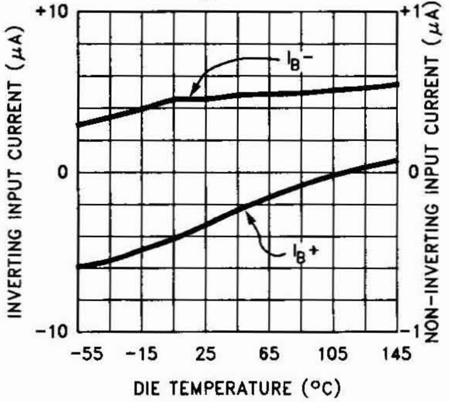
Supply Current vs Supply Voltage (Per Amplifier)



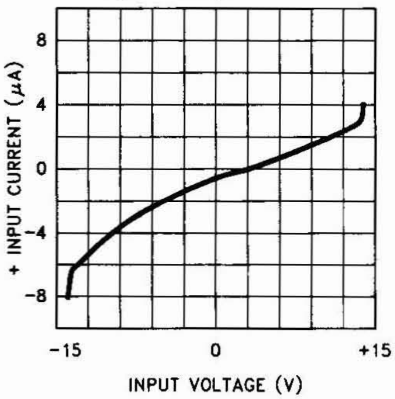
+Input Resistance vs Die Temperature



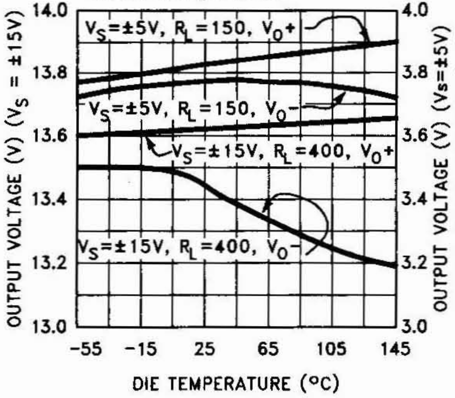
Input Current vs Die Temperature



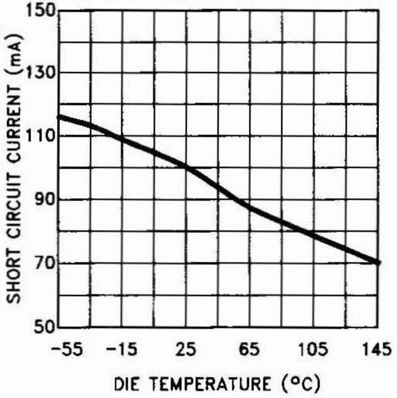
+Input Bias Current vs Input Voltage



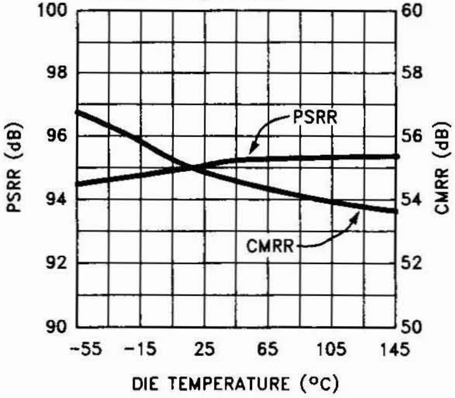
Output Voltage Swing vs Die Temperature



Short Circuit Current vs Die Temperature



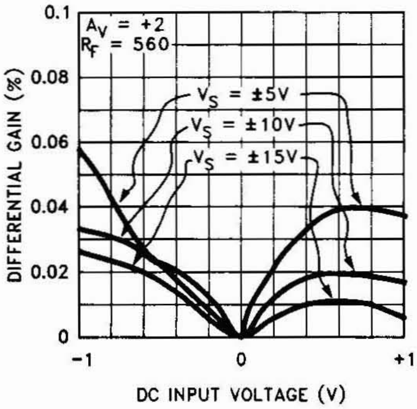
PSRR & CMRR vs Die Temperature



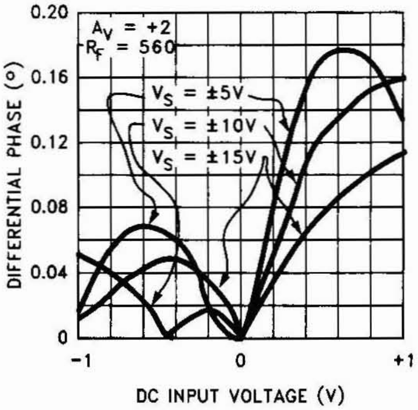
2260-6

Typical Performance Curves — Contd.

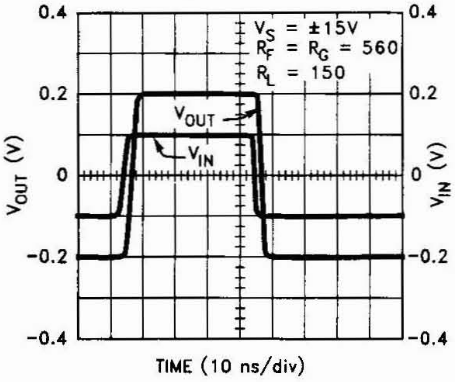
Differential Gain vs DC Input Voltage, R_L = 150



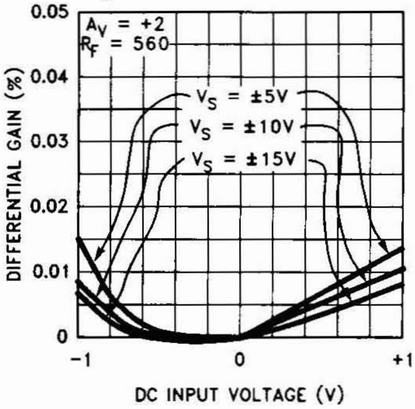
Differential Phase vs DC Input Voltage, R_L = 150



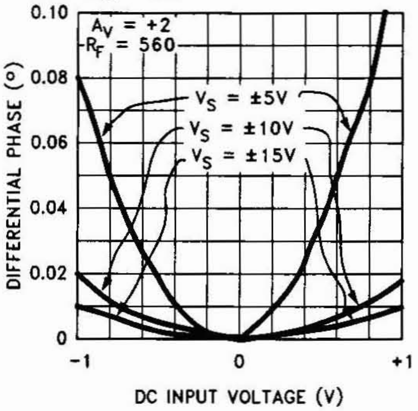
Small Signal Pulse Response



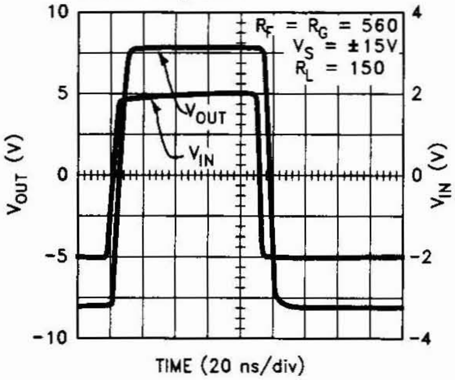
Differential Gain vs DC Input Voltage, R_L = 500



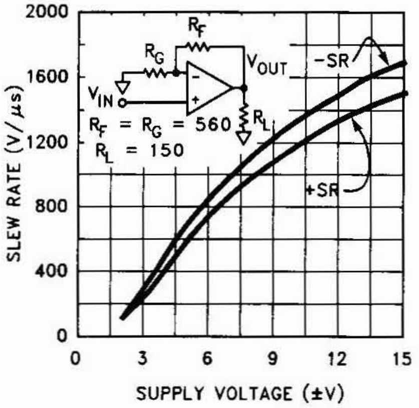
Differential Phase vs DC Input Voltage, R_L = 500



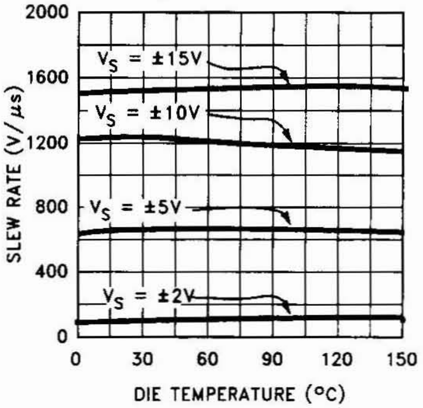
Large Signal Pulse Response



Slew Rate vs Supply Voltage



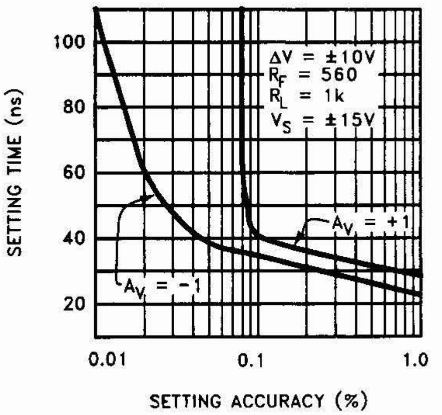
Slew Rate vs Temperature



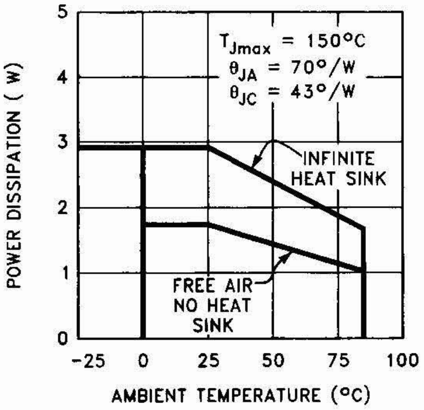
2260-7

Typical Performance Curves — Contd.

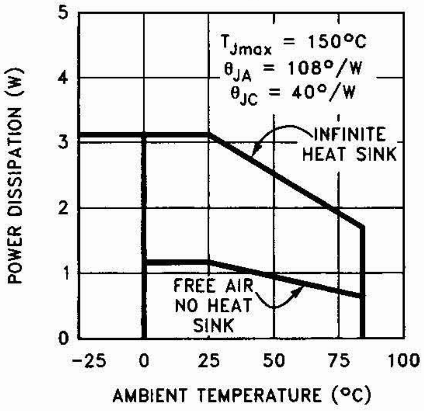
Settling Time vs Settling Accuracy



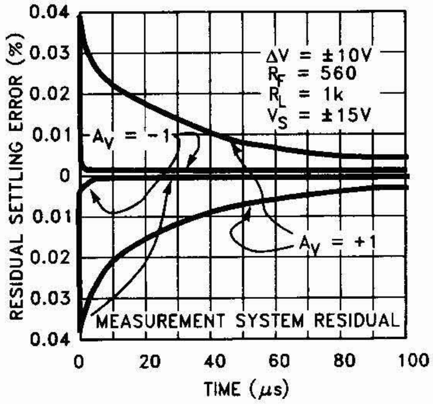
14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



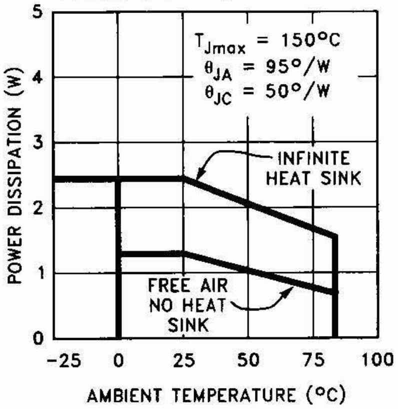
14-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature



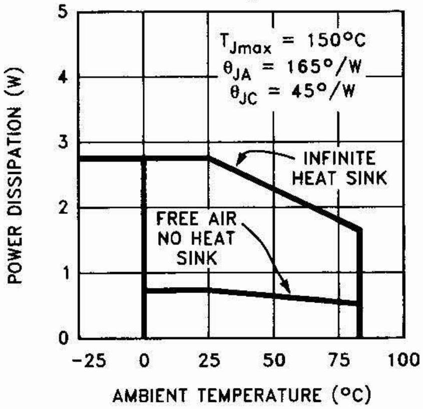
Long Term Settling Error



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



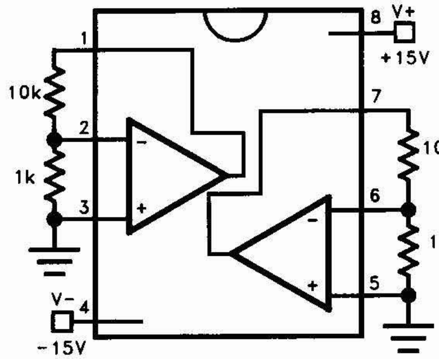
8-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature



2260-8

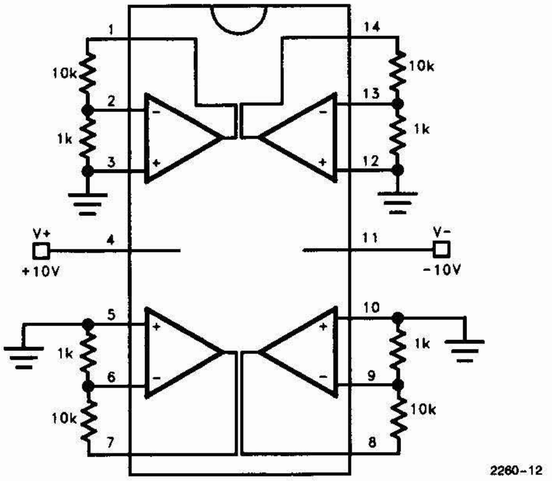
Burn-In Circuits

EL2260C


1
2
3
4
5
6
7
8
V+
+15V
V−
−15V
10k
1k
10k
1k

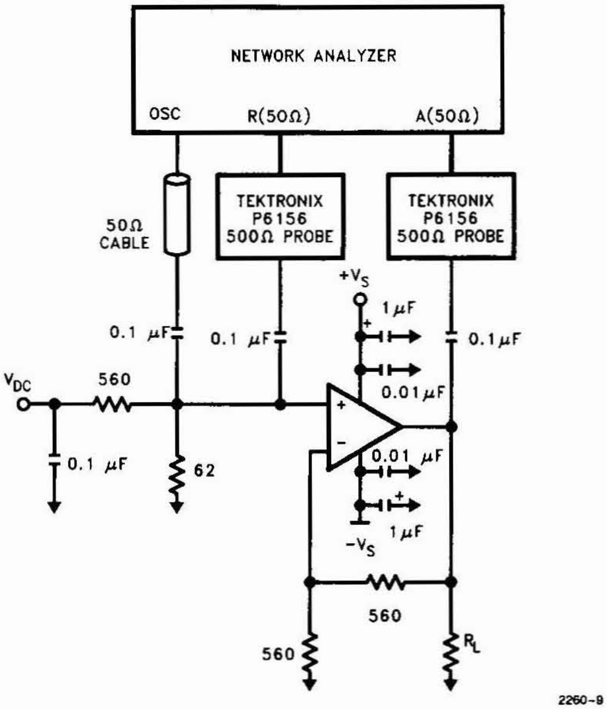
2260-11

EL2460C

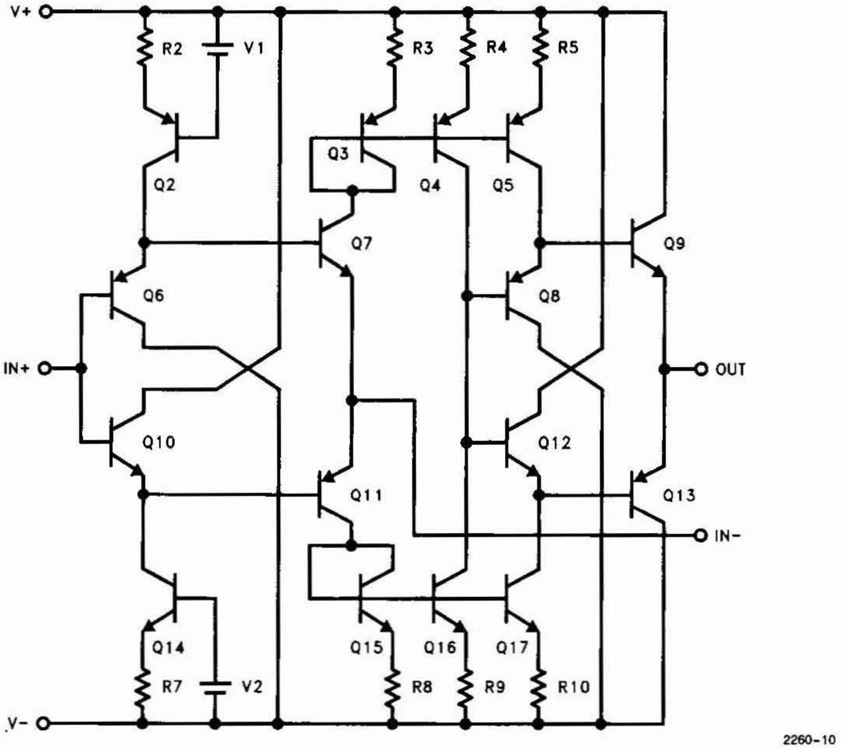

1
2
3
4
5
6
7
8
9
10
11
12
13
14
10k
1k
1k
10k
10k
1k
1k
10k
V+
+10V
V−
−10V

2260-12

Differential Gain and Phase Test Circuit


NETWORK ANALYZER
OSC
R(50Ω)
A(50Ω)
TEKTRONIX P6156 500Ω PROBE
TEKTRONIX P6156 500Ω PROBE
50Ω CABLE
0.1 µF
0.1 µF
0.1 µF
+V_S
1 µF
0.01 µF
V_DC
560
0.1 µF
62
0.01 µF
1 µF
−V_S
560
560
R_L
2260-9

Simplified Schematic (One Amplifier)


V+
R2
V1
R3
R4
R5
Q3
Q2
Q4
Q5
Q7
Q9
Q6
Q8
IN+
OUT
Q10
Q12
Q11
Q13
IN−
Q14
Q15
Q16
Q17
R7
V2
R8
R9
R10
V−
2260-10

Applications Information

Product Description

The EL2260C/EL2460C are dual and quad current mode feedback amplifiers that offer wide bandwidths and good video specifications at moderately low supply currents. They are built using Elantec's proprietary complimentary bipolar process and are offered in industry standard pin-outs. Due to the current feedback architecture, the EL2260C/EL2460C closed-loop 3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3 dB bandwidth is somewhat dependent on the power supply voltage. As the supply voltage is decreased, internal junction capacitances increase, causing a reduction in closed loop bandwidth. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼". The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0 µF tantalum capacitor in parallel with a 0.01 µF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO packages, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL2260C/EL2460C when operating in the non-inverting configuration. The characteristic curve of gain vs. frequency with variations of $C_{IN}-$ emphasizes this effect. The curve illustrates how the bandwidth can be extended to beyond 200 MHz with some additional peaking with an additional 2 pF of capacitance at the $V_{IN}-$ pin for the case of $A_V = +2$. Higher values of capacitance will be required to obtain similar effects at higher gains.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values

The EL2260C and EL2460C have been designed and specified with $R_F = 560\Omega$ for $A_V = +2$. This value of feedback resistor yields extremely flat frequency response with little to no peaking out to 130 MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing R_F to 430Ω, bandwidth can be extended to 170 MHz with under 1 dB of peaking. Further reduction of R_F to 360Ω increases the bandwidth to 195 MHz with about 2.5 dB of peaking. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

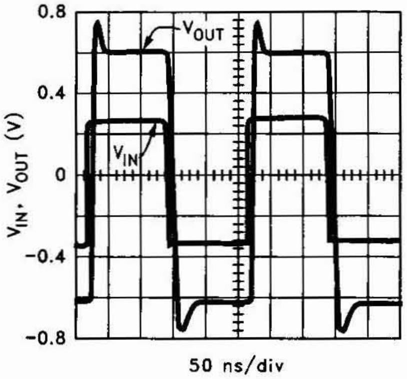
Bandwidth vs Temperature

Whereas many amplifier's supply current and consequently 3 dB bandwidth drop off at high temperature, the EL2260C/EL2460C were designed to have little supply current variations with temperature. An immediate benefit from this is that the 3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth only varies from 150 MHz to 110 MHz over the entire die junction temperature range of $0°C < T < 150°C$.

Applications Information — Contd.

Supply Voltage Range

The EL2260C/EL2460C has been designed to operate with supply voltages from ±2V to ±15V. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages. However, at ±2V supplies, the 3 dB bandwidth at $A_V = +2$ is a respectable 70 MHz. The following figure is an oscilloscope plot of the EL2260C at ±2V supplies, $A_V = +2$, $R_F = R_G = 560\Omega$, driving a load of 150Ω, showing a clean ±600 mV signal at the output.



2260-13

If a single supply is desired, values from +4V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2260C/EL2460C.

Settling Characteristics

The EL2260C/EL2460C offer superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2260/EL2460 are not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for $A_V = +1$, there is approximately a 0.035% residual which tails away to 0.01% in about 40 μs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For $A_V = -1$, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With $A_V = -1$, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation

The EL2260C/EL2460C amplifiers combine both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2260C/EL2460C remain within their absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or

$$P_{DMAX} = N * \left(2 * V_S * I_S + (V_S - V_{OUT}) * \frac{V_{OUT}}{R_L} \right)$$

where N is the number of amplifiers per package, and I_S is the current per amplifier. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, such as the LT1229 and LT1230, the EL2260C/EL2460C

Applications Information — Contd.

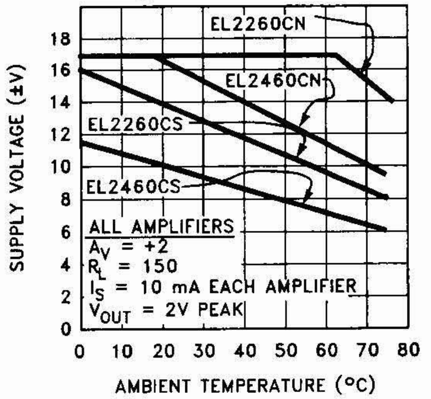
maintain almost constant supply current over temperature so that AC performance is not degraded as much over the entire operating temperature range. Of course, this increase in performance doesn't come for free. Since the current has increased, supply voltages must be limited so that maximum power ratings are not exceeded.

Each amplifier in the EL2260C/EL2460C consume typically 7.5 mA and maximum 10.0 mA. The worst case power in an IC occurs when the output voltage is at half supply, if it can go that far, or its maximum value if it cannot reach half supply. If we assume that the EL2260C/EL2460C is used for double terminated video cable driving applications ($R_L = 150\Omega$), and the gain $= +2$, then the maximum output voltage is 2V, and the average output voltage is 1.4V. If we set the two P_{Dmax} equations equal to each other, and solve for V_S, we can get a family of curves for various packages and conditions according to:

$$V_S = \frac{\dfrac{R_L * (T_{JMAX} - T_{AMAX})}{N * \theta_{JA}} + (V_{OUT})^2}{(2 * I_S * R_L) + V_{OUT}}$$

The following curve shows supply voltage ($\pm V_S$) vs. temperature for the various packages assuming $A_V = +2$, $R_L = 150$, and V_{OUT} peak $= 2V$. The curves include worst case conditions ($I_S = 10$ mA and all amplifiers operating at V_{OUT} peak $= 2V$).

Supply Voltage vs Ambient Temperature for All Packages of EL2260C/EL2460C



2260-14

The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit

The EL2260C/EL2460C have internal current limits that protect the circuit in the event of the output being shorted to ground. This limit is set at 100 mA nominally and reduces with junction temperature. At a junction temperature of 150°C, the current limits at about 65 mA. If any one output is shorted to ground, the power dissipation could be well over 1W, and much greater if all outputs are shorted. Heat removal is required in order for the EL2260C/EL2460C to survive an indefinite short.

Channel to Channel Isolation

Due to careful biasing connections within the internal circuitry of the EL2260C/EL2460C, exceptionally good channel to channel isolation is obtained. Isolation is over 70 dB at video frequencies of 4 MHz, and over 65 dB up to 10 MHz. The EL2460C isolation is improved an additional 10 dB, up to about 5 MHz, for amplifiers A to B and amplifiers C to D. Isolation is improved another 8 dB for amplifiers A to C and amplifiers B to D. See the curve in the Typical Performance Curves section for more detail.

Driving Cables and Capacitive Loads

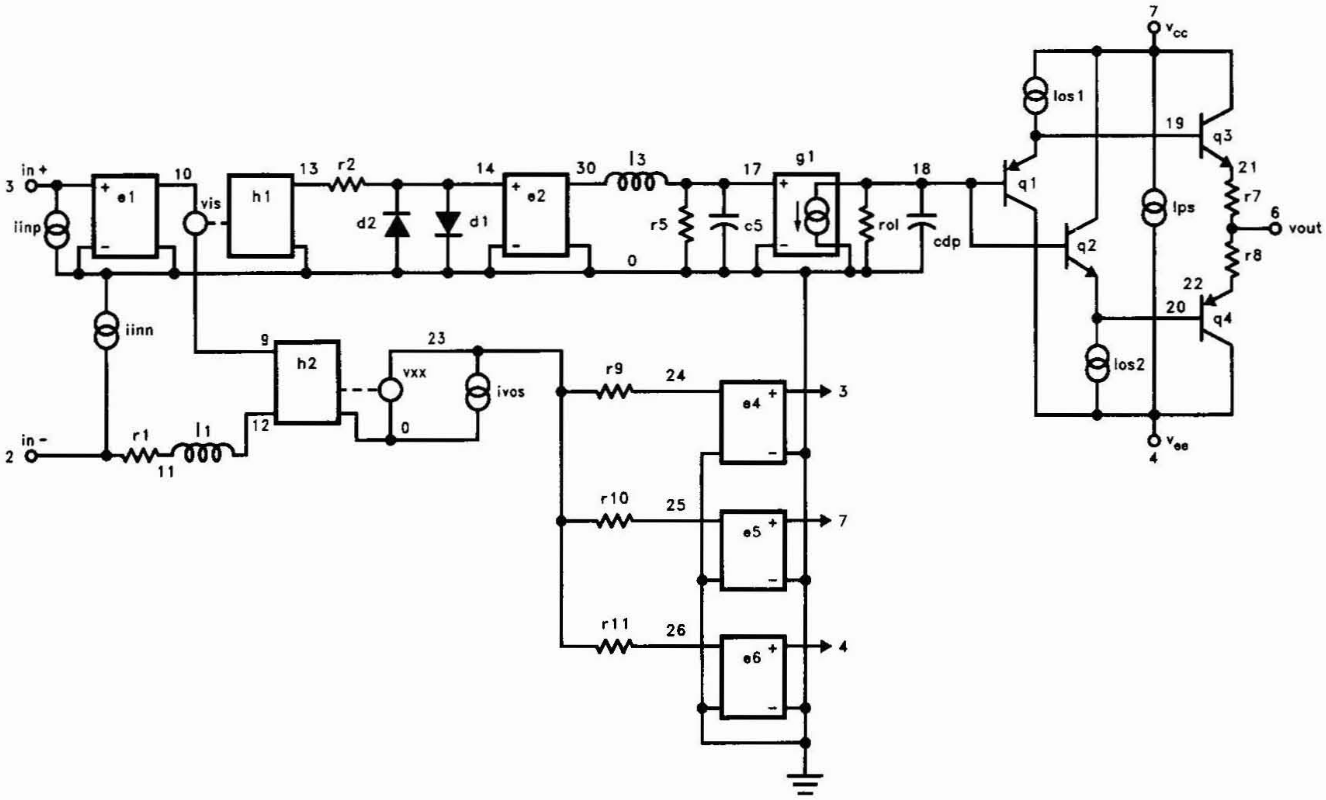
When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2260C and EL2460C from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. In these applications, an additional small value ($5\Omega - 50\Omega$) resistor in series with the output will eliminate most peaking. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistor at the output.

EL2260C/EL2460C Macromodel

```
* Revision A, March 1993
* AC Characteristics used CIN- (pin 2) = 1 pF; RF = 560Ω
* Connections:      +input
*                   |    -input
*                   |    |    +Vsupply
*                   |    |    |    -Vsupply
*                   |    |    |    |    output
*                   |    |    |    |    |
.subckt EL2260C/EL  3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 130
l1 11 12 25nH
iinp 3 0 0.5µA
iinm 2 0 5µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.43µH
c5 17 0 0.27pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 2Meg
cdp 18 0 2.285pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2mA
ios2 20 4 2mA
*
```

EL2260C/EL2460C Macromodel — Contd.

```
* Supply Current
*
ips 7 4 2mA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.1ns)
.model qp pnp (is=5e-15 bf=100 tf=0.1ns)
.model dclamp d (is=1e-30 ibv=0.266 bv=2.24 n=4)
.ends
```


in +
3
iinp
e1
10
vis
h1
13
r2
d2
d1
14
e2
30
l3
r5
c5
0
17
g1
rol
18
cdp
7
Vcc
Ios1
19
q3
q1
21
r7
Ips
6
vout
q2
r8
22
20
q4
Ios2
Vee
4
iinn
9
h2
23
vxx
ivos
0
12
in -
2
r1
l1
11
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4

2260-15

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2360C
Triple 130 MHz Current Feedback Amplifier

Features

- Triple amplifier topology
- 130 MHz −3 dB bandwidth ($A_V = +2$)
- 180 MHz −3 dB bandwidth ($A_V = +1$)
- Wide supply range, ±2V to ±15V
- 80 mA output current (peak)
- Low cost
- 1500 V/µs slew rate
- Input common mode range to within 1.5V of supplies
- 35 ns settling time to 0.1%
- Available in single (EL2160C), dual (EL2260C), and quad (EL2460C) form

Applications

- RGB amplifiers
- Video amplifiers
- Cable driver
- Test equipment amplifiers
- Current to voltage converters
- Video broadcast equipment

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2360CN	−40°C to +85°C	16−Pin PDIP	MDP0031
EL2360CS	−40°C to +85°C	16−Pin SOIC	MDP0027

General Description

The EL2360C is a triple current-feedback operational amplifier which achieves a −3 dB bandwidth of 130 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, these amplifiers use current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback amplifier.

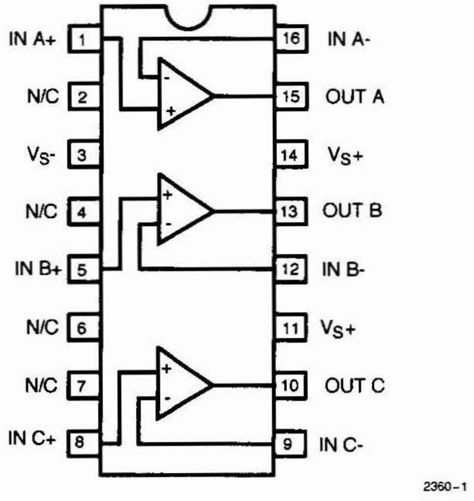
The EL2360C is designed to drive a double terminated 75Ω coax cable to video levels. It's fast slew rate of 1500 V/µs, combined with the triple amplifier topology, makes its ideal for RGB video applications.

This amplifier can operate on any supply voltage from 4V (±2V) to 33V (±16.5V), yet consume only 8 mA per amplifier at any supply voltage. The EL2360C is available in 16-pin PDIP and SOIC packages.

For Single, Dual, or Quad applications, consider the EL2160C, EL2260C, or EL2460C all in industry standard pin outs. For Single applications with a power down feature, consider the EL2166C.

Connection Diagram

EL2360C SOIC, P-DIP Packages



Top View

June 1996 Rev A

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+33V	Output Current (continuous)	±50 mA
Common-Mode Input Voltage	V_S- to V_S+	Operating Ambient Temperature Range	−40°C to +85°C
Differential Input Voltage	±6V	Operating Junction Temperature	150°C
Current into +IN or −IN	±10 mA	Storage Temperature Range	−65°C to +150°C
Internal Power Dissipation	See Curves		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±5V, ±15V		2	10	I	mV
TCV_{OS}	Average Input Offset Voltage Drift, (Note 1)			10		V	μV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V		0.5	3	I	μA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V		5	25	I	μA
CMRR	Common Mode Rejection Ratio, (Note 2)	V_S = ±5V, ±15V	50	55		I	dB
−ICMR	−Input Current Common Mode Rejection, (Note 2)	V_S = ±5V, ±15V		0.2	5	I	μA/V
PSRR	Power Supply Rejection Ratio, (Note 3)		75	95		I	dB
−IPSR	−Input Current Power Supply Rejection, (Note 3)			0.2	5	I	μA/V
R_{OL}	Transimpedance, (Note 4)	V_S = ±15V, R_L = 400Ω	500	2000		I	kΩ
		V_S = ±15V, R_L = 150Ω	500	1800		I	kΩ
$+R_{IN}$	+ Input Resistance		1.5	3		I	MΩ
$+C_{IN}$	+ Input Capacitance	PDIP package		1.5		V	pF
		SOIC package		1		V	pF
CMIR	Common Mode Input Range	V_S = ±15V		±13.5		V	V
		V_S = ±5V		±3.5		V	V

Note 1: Measured from T_{MIN} to T_{MAX}.
Note 2: V_{CM} = ±10V for V_S = ±15V, V_{CM} = ±3V for V_S = ±5V.
Note 3: The supplies are moved from ±2.5V to ±15V.
Note 4: V_{OUT} = ±7V for V_S = ±15V, V_{OUT} = ±2V for V_S = ±5V.

DC Electrical Characteristics $V_S = \pm 15V, R_L = 150\Omega, T_A = 25°C$ unless otherwise specified — Contd.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	$V_S = \pm 15V, R_L = 400\Omega$	±12	±13.5		I	V
		$V_S = \pm 15V, R_L = 150\Omega$		±12		V	V
		$V_S = \pm 5V, R_L = 150\Omega$	±3.0	±3.7		I	V
I_{SC}	Output Short Circuit Current, (Note 5)	$V_S = \pm 5V, \pm 15V$	60	100	150	I	mA
I_S	Supply Current (per amplifier)	$V_S = \pm 15V$		8.0	11.3	I	mA
		$V_S = \pm 5V$		5.7	8.8	I	mA

Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

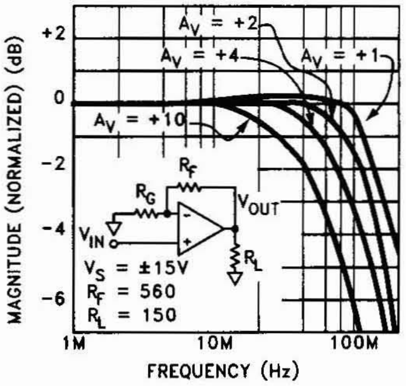
AC Electrical Characteristics (Note 8), $V_S = \pm 15V, A_V = +2, R_F = R_G = 560\Omega, R_L = 150\Omega, T_A = 25°C$ unless otherwise specified.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth	$V_S = \pm 15V, A_V = +2$		130		V	MHz
		$V_S = \pm 15V, A_V = +1$		180		V	MHz
		$V_S = \pm 5V, A_V = +2$		100		V	MHz
		$V_S = \pm 5V, A_V = +1$		110		V	MHz
SR	Slew Rate (Note 6)	$R_L = 400\Omega$	1000	1500		IV	V/µs
		$R_F = 1 k\Omega, R_G = 110\Omega, R_L = 400\Omega$		1500		V	V/µs
t_r, t_f	Rise Time, Fall Time	$V_{OUT} = \pm 500 mV$		2.7		V	ns
t_{PD}	Propagation Delay	$V_{OUT} = \pm 500 mV$		3.2		V	ns
OS	Overshoot	$V_{OUT} = \pm 500 mV$		0		V	%
t_S	0.1% Settling Time	$V_{OUT} = \pm 2.5V, A_V = -1$		35		V	ns
dG	Differential Gain (Note 7)	$R_L = 150\Omega$		0.025		V	%
		$R_L = 500\Omega$		0.006		V	%
dP	Differential Phase (Note 7)	$R_L = 150\Omega$		0.1		V	°
		$R_L = 500\Omega$		0.005		V	°

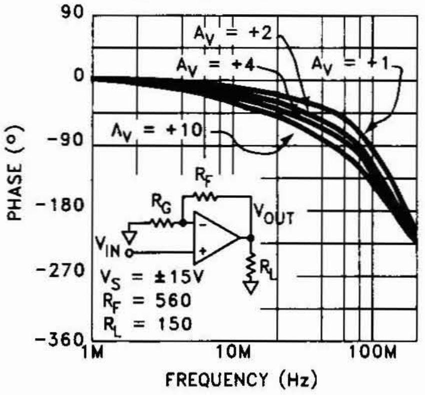
Note 6: Slew Rate is with V_{OUT} from +10V to −10V and measured at +5V and −5V.
Note 7: DC offset from −0.714V to +0.714V, AC amplitude 286 mV_{P-P}, f = 3.58 MHz.
Note 8: All AC tests are performed on a "warmed up" part, except Slew Rate, which is pulse tested.

Typical Performance Curves

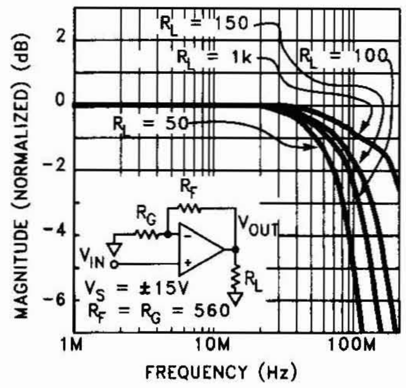
Non-Inverting Frequency Response (Gain)



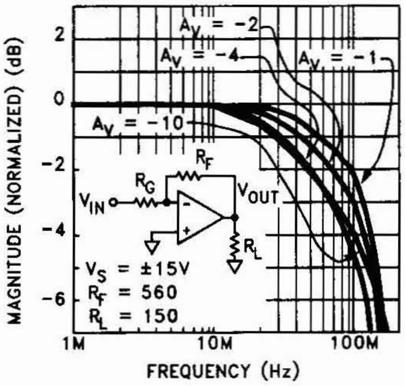
Non-Inverting Frequency Response (Phase)



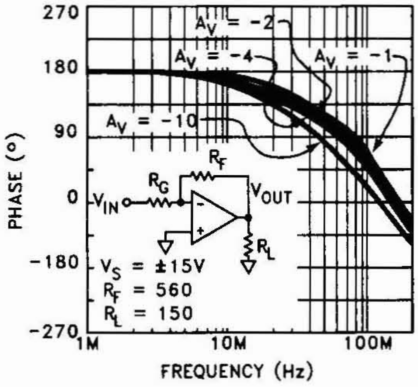
Frequency Response for Various R_L



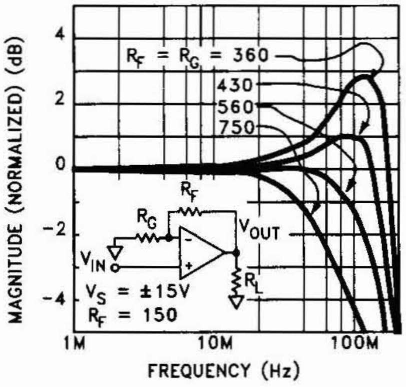
Inverting Frequency Response (Gain)



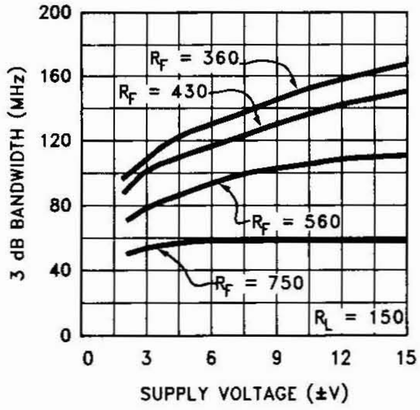
Inverting Frequency Response (Phase)



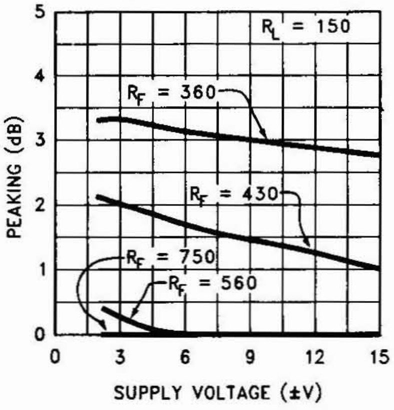
Frequency Response for Various R_F and R_G



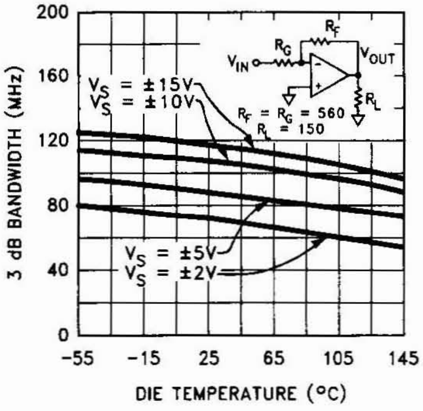
3 dB Bandwidth vs Supply Voltage for $A_V = -1$



Peaking vs Supply Voltage for $A_V = -1$



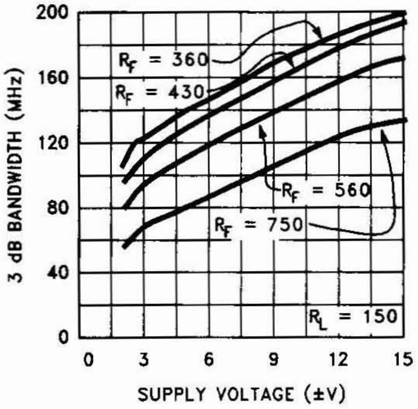
3 dB Bandwidth vs Temperature for $A_V = -1$



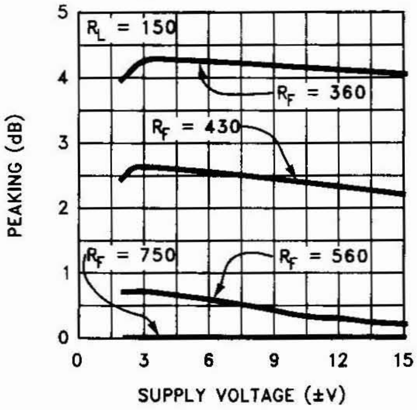
2360-2

Typical Performance Curves — Contd.

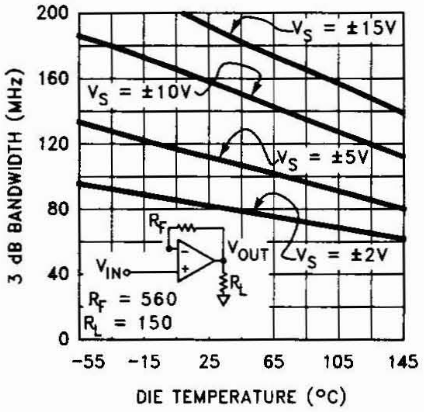
3 dB Bandwidth vs Supply Voltage for $A_V = +1$



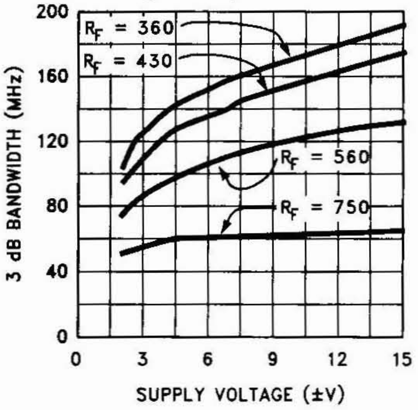
Peaking vs Supply Voltage for $A_V = +1$



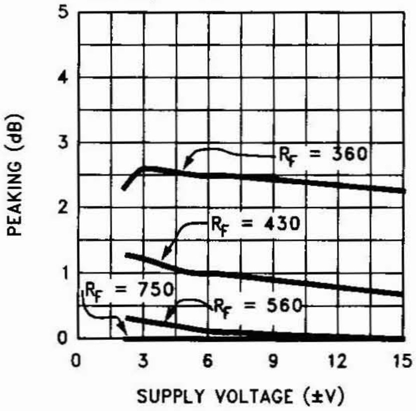
3 dB Bandwidth vs Temperature for $A_V = +1$



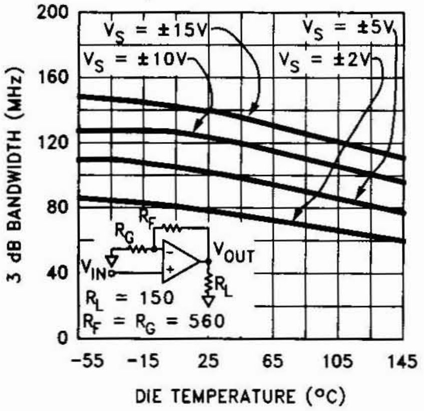
3 dB Bandwidth vs Supply Voltage for $A_V = +2$



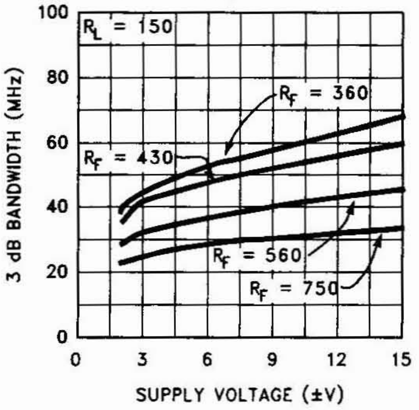
Peaking vs Supply Voltage for $A_V = +2$



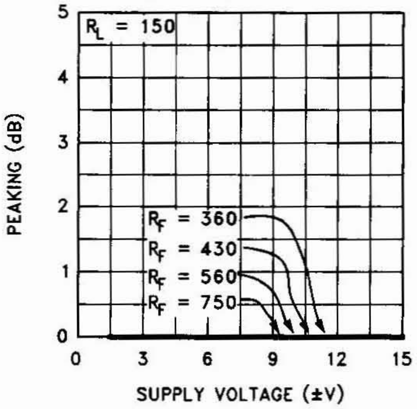
3 dB Bandwidth vs Temperature for $A_V = +2$



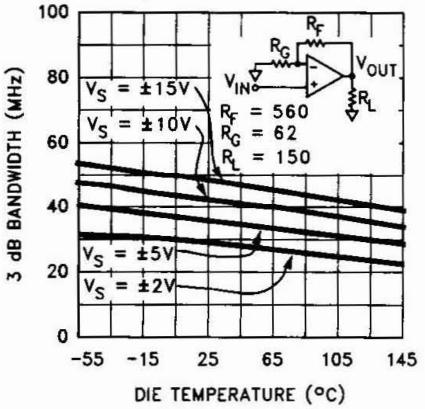
3 dB Bandwidth vs Supply Voltage for $A_V = +10$



Peaking vs Supply Voltage for $A_V = +10$



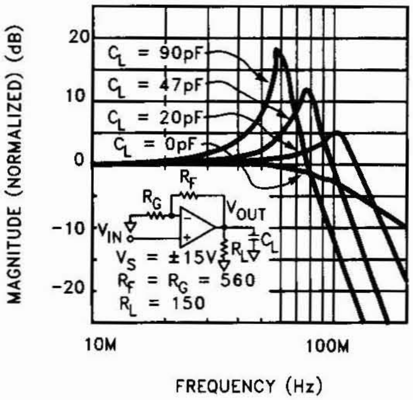
3 dB Bandwidth vs Temperature for $A_V = +10$



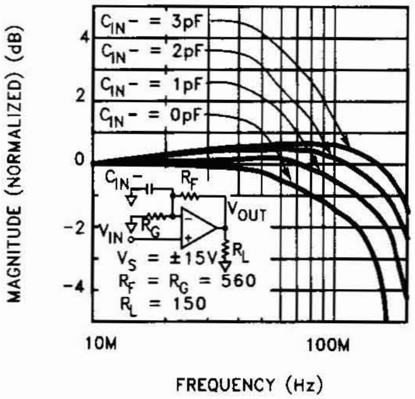
2360-3

Typical Performance Curves — Contd.

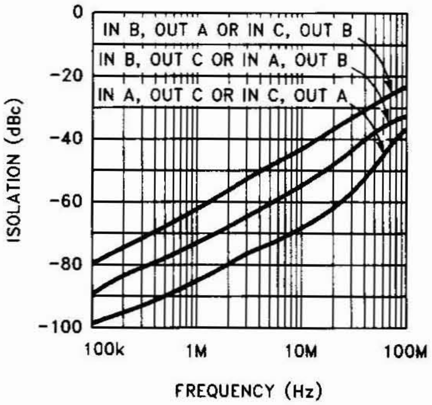
Frequency Response for Various C_L



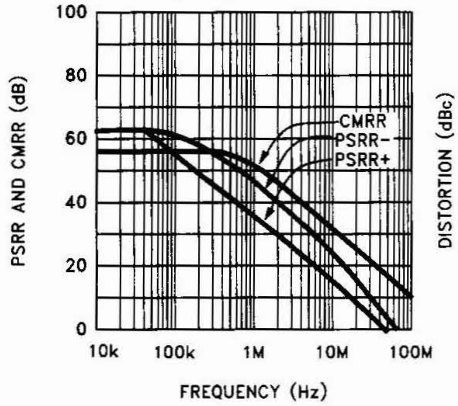
Frequency Response for Various C_{IN-}



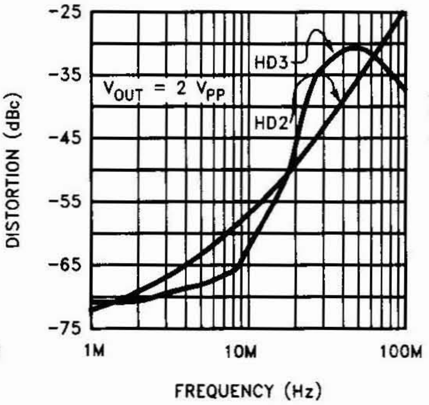
Channel to Channel Isolation vs Frequency



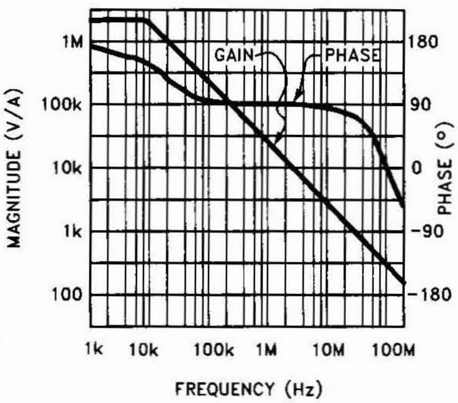
PSRR and CMRR vs Frequency



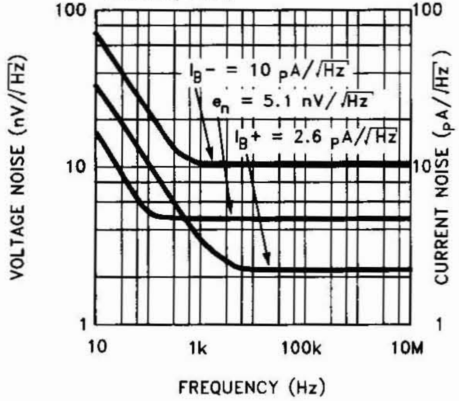
2nd and 3rd Harmonic Distortion vs Frequency



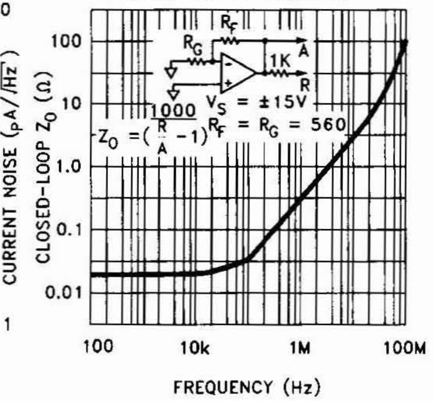
Transimpedance (R_{OL}) vs Frequency



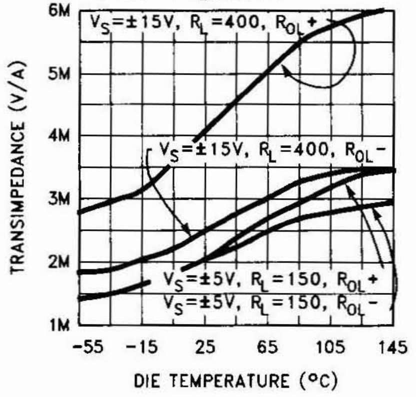
Voltage and Current Noise vs Frequency



Closed-Loop Output Impedance vs Frequency

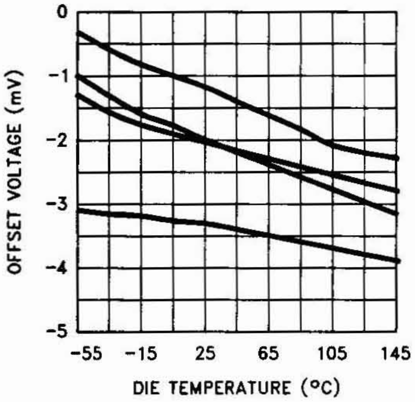


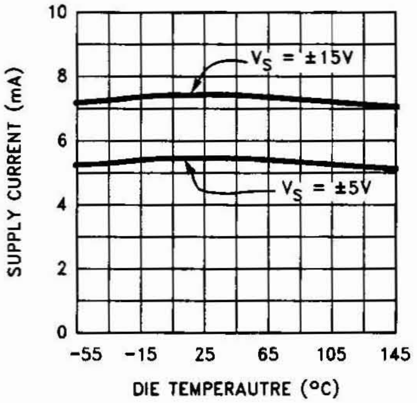
Transimpedance (R_{OL}) vs Die Temperature

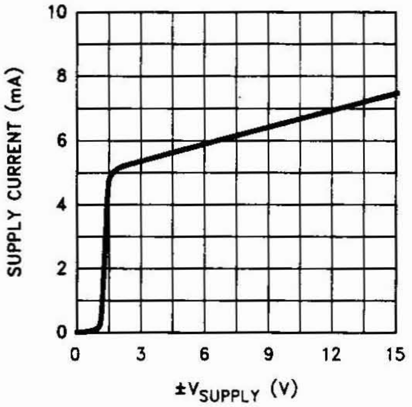


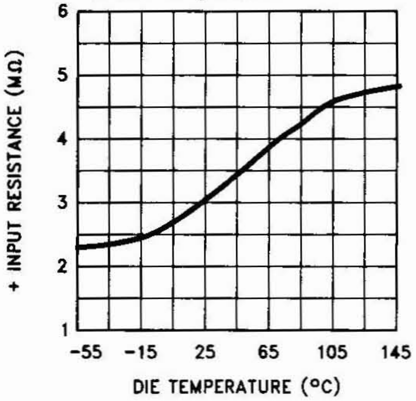
2360-4

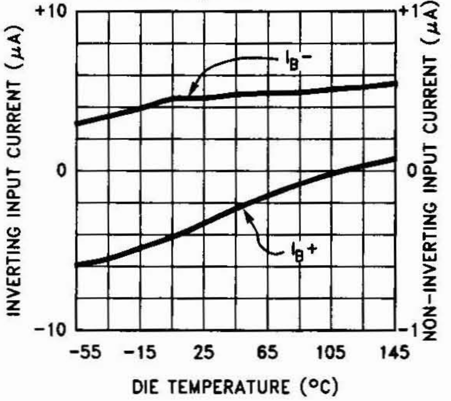
Typical Performance Curves — Contd.

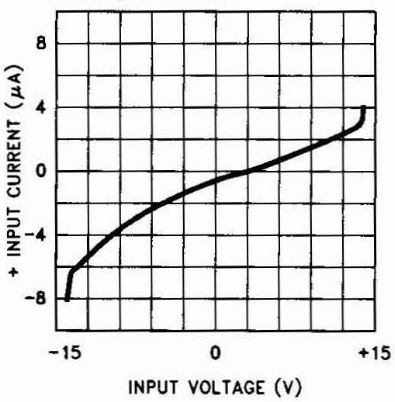

Offset Voltage vs Die Temperature (4 Samples)

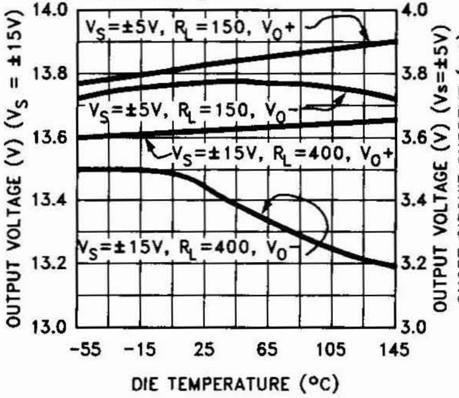

Supply Current vs Die Temperature (Per Amplifier)

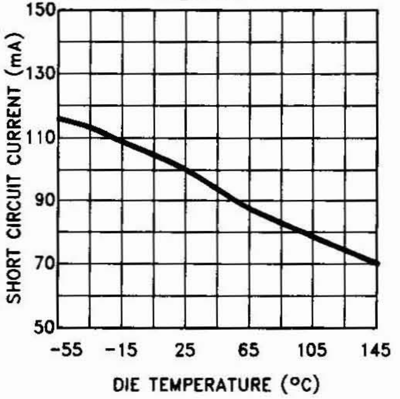

Supply Current vs Supply Voltage (Per Amplifier)

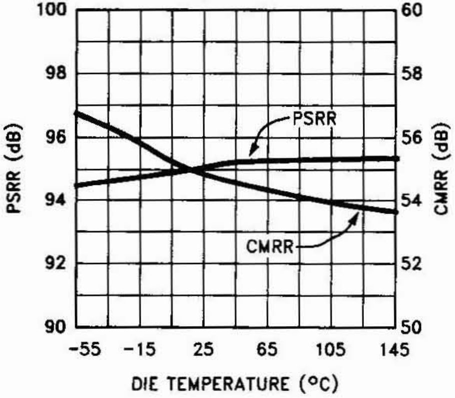

+Input Resistance vs Die Temperature


Input Current vs Die Temperature


+Input Bias Current vs Input Voltage


Output Voltage Swing vs Die Temperature

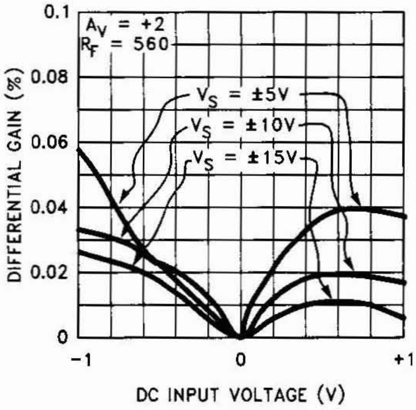

Short Circuit Current vs Die Temperature


PSRR & CMRR vs Die Temperature

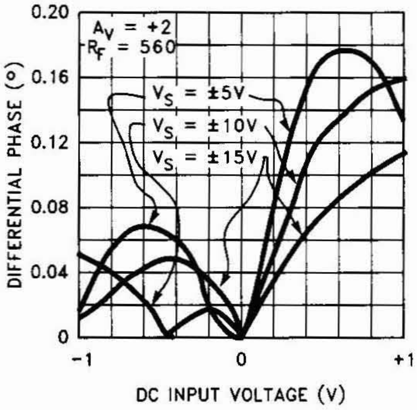
2360-5

Typical Performance Curves — Contd.

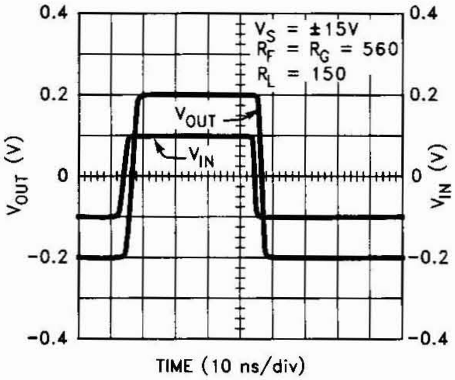
Differential Gain vs DC Input Voltage, R_L = 150



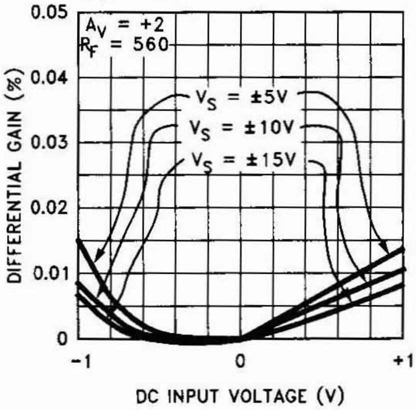
Differential Phase vs DC Input Voltage, R_L = 150



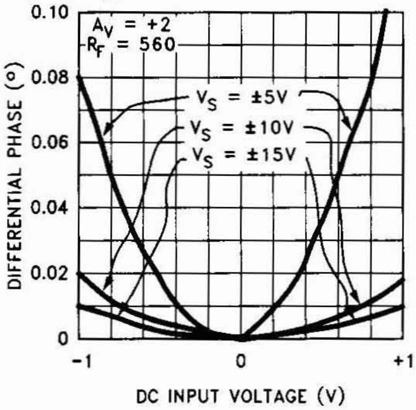
Small Signal Pulse Response



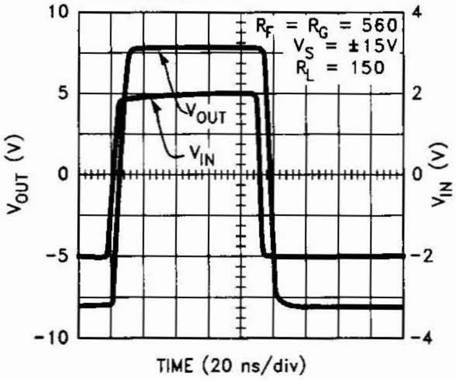
Differential Gain vs DC Input Voltage, R_L = 500



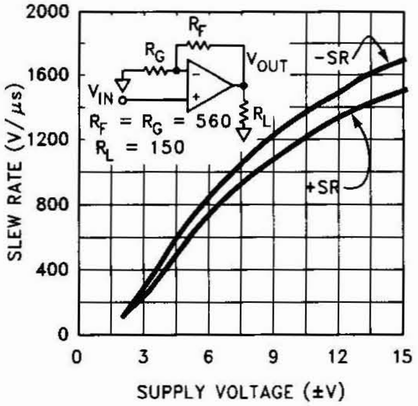
Differential Phase vs DC Input Voltage, R_L = 500



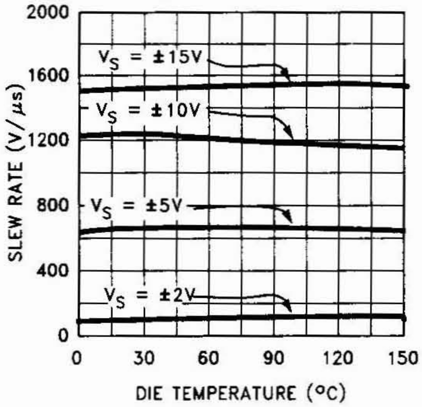
Large Signal Pulse Response



Slew Rate vs Supply Voltage



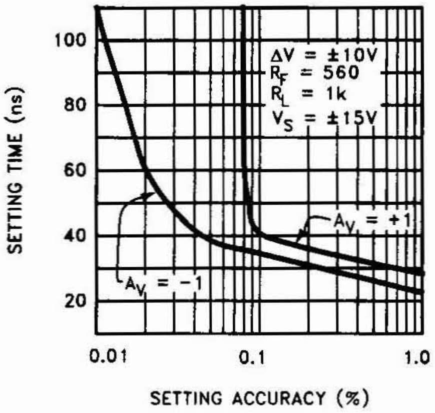
Slew Rate vs Temperature



2360-6

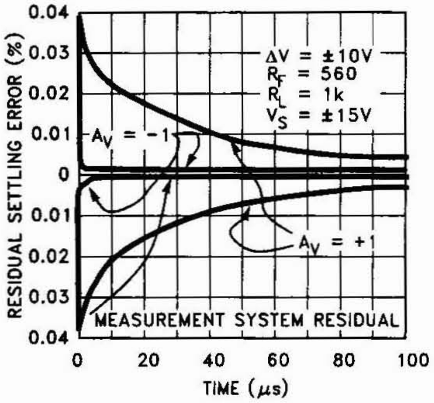
Typical Performance Curves — Contd.

Settling Time vs Settling Accuracy



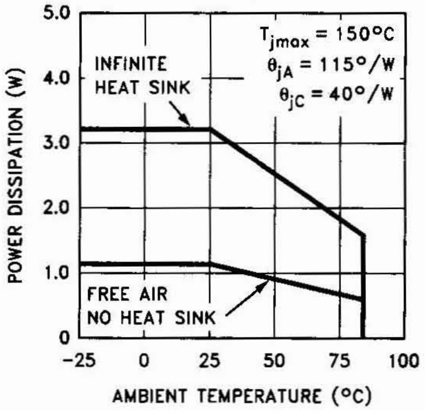
2360-15

Long Term Settling Error



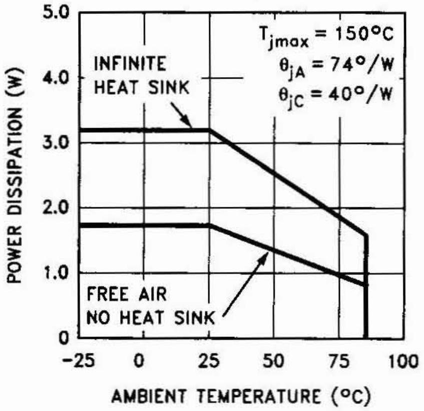
2360-16

16-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature



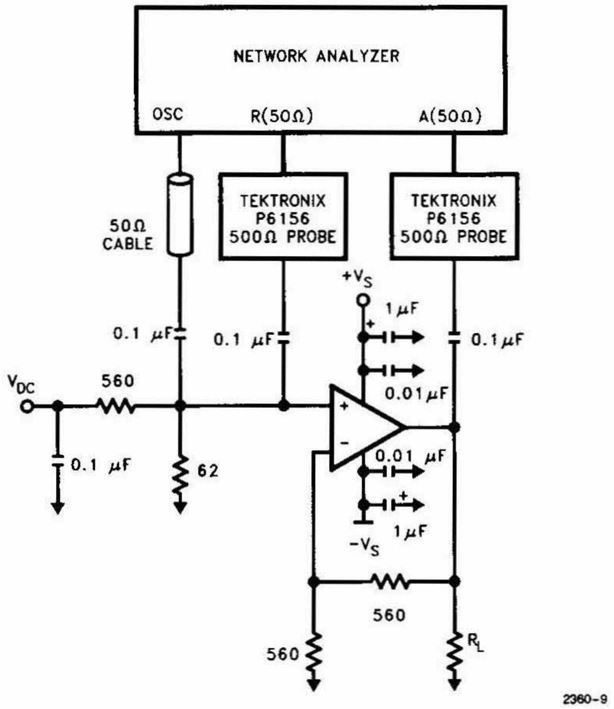
2360-7

16-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature

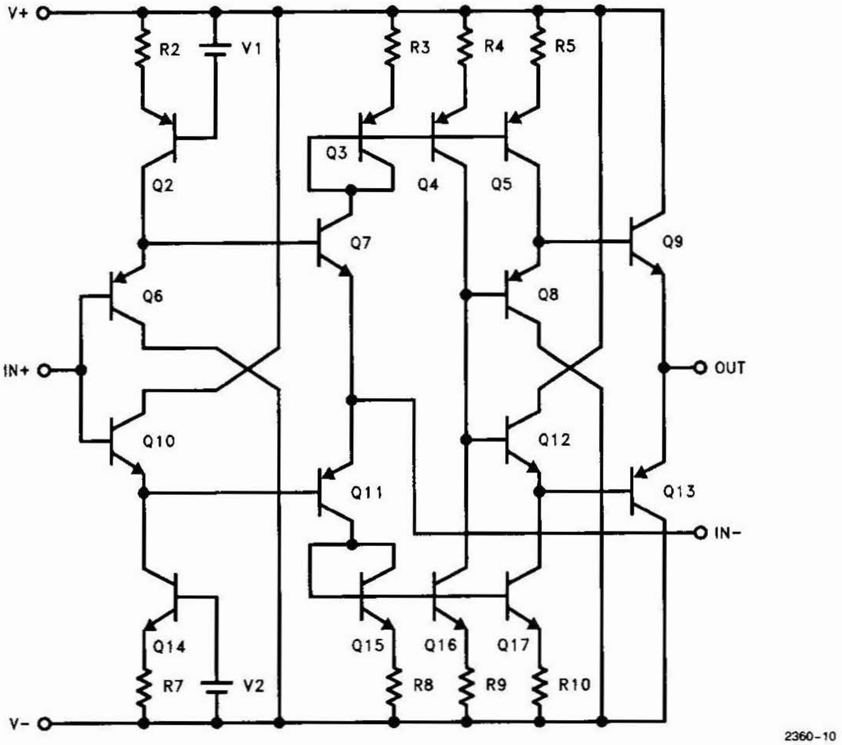


2360-8

Differential Gain And Phase Test Circuit


NETWORK ANALYZER
OSC
R(50Ω)
A(50Ω)
TEKTRONIX P6156 500Ω PROBE
TEKTRONIX P6156 500Ω PROBE
50Ω CABLE
+VS
1 μF
0.1 μF
0.1 μF
0.1 μF
0.01 μF
VDC
560
0.1 μF
62
0.01 μF
1 μF
−VS
560
560
RL
2360-9

Simplified Schematic (One Amplifier)


V+
R2
V1
R3
R4
R5
Q3
Q2
Q4
Q5
Q7
Q9
Q6
Q8
IN+
OUT
Q10
Q12
Q11
Q13
IN−
Q14
Q15
Q16
Q17
R7
V2
R8
R9
R10
V−
2360-10

Applications Information

Product Description

The EL2360C is a triple current feedback amplifier that offers wide bandwidth and good video specifications at moderately low supply currents. It is built using Elantec's proprietary complimentary bipolar process and is offered in both a 16 pin PDIP and SOIC packages. Due to the current feedback architecture, the EL2360C closed−loop −3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking a gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The −3 dB bandwidth is somewhat dependent on the power supply voltage. As the supply voltage is decreased, internal junction capacitances increase, causing a reduction in the closed loop bandwidth. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, preferably below ¼". The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. The characteristic curve of gain vs. frequency with variations in C_{IN-} emphasizes this effect. The curve illustrates how the bandwidth can be extended to beyond 200 MHz with some additional peaking with an additional 2pF of capacitance at the V_{IN-} pin. For inverting gains, this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains, this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.

Feedback Resistor Values

The EL2360C has been designed and specified at a gain of +2 with $R_F = 560\Omega$. This value of feedback resistor yields relatively flat frequency response with little to no peaking out to 130 MHz. Since the EL2360C is a current-feedback amplifier, it is also possible to change the value of R_F to get more bandwidth. As seen in the curve of Frequency Response For Various R_F and R_G, bandwidth and peaking can be easily modified by varying the value of the feedback resistor. For example, by reducing R_F to 430Ω, bandwidth can be extended to 170 MHz with under 1 dB of peaking. Further reduction of R_F to 360Ω increases the bandwidth to 195 MHz with about 2.5 dB of peaking.

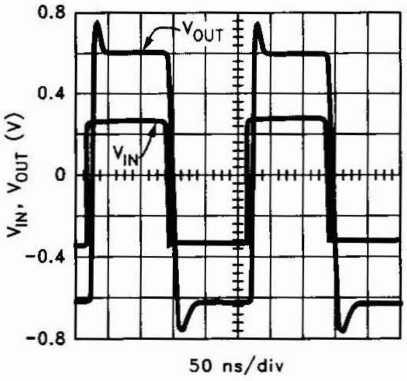
Bandwidth vs Temperature

Whereas many amplifier's supply current and consequently −3 dB bandwidth drop off at high temperature, the EL2360C was designed to have little supply current variation with temperature. An immediate benefit from this is that the −3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth varies only from 150 MHz to 110 MHz over the entire die junction temperature range of $-50°C < T < 150°C$.

Applications Information — Contd.

Supply Voltage Range and Single Supply Operation

The EL2360C has been designed to operate with supply voltages from ±2V to ±15V. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages. However, at ±2V supplies, the −3 dB bandwidth at $A_V = +2$ is a respectable 70 MHz. The following figure is an oscilloscope plot of the EL2360C at ±2V supplies, $A_V = +2$, $R_F = R_G = 560\Omega$, driving a load of 150Ω, showing a clean ±600 mV signal at the output.



2360-11

If a single supply is desired, values from +4V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2360C, which is typically 1.5V from each supply rail.

Settling Characteristics

The EL2360C offers superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2360C is not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for $A_V = +1$, there is approximately a 0.035% residual which tails away to 0.01% in about 40 μs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For $A_V = -1$, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With $A_V = -1$, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation

The EL2360C amplifier combines both high speed and large output current capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2360C remains within it's absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined according to [1]:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \qquad [1]$$

where:

T_{JMAX} = Maximum Junction Temperature
T_{AMAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
PD_{MAX} = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or [2]

$$PD_{MAX} = N^{*}(V_S * I_{SMAX} + (V_S - V_{OUT}) * \frac{V_{OUT}}{RL}) \qquad [2]$$

where:

N = Number of amplifiers
V_S = Total Supply Voltage
I_{SMAX} = Maximum Supply Current per amplifier
V_{OUT} = Maximum Output Voltage of the Application
R_L = Load Resistance tied to Ground

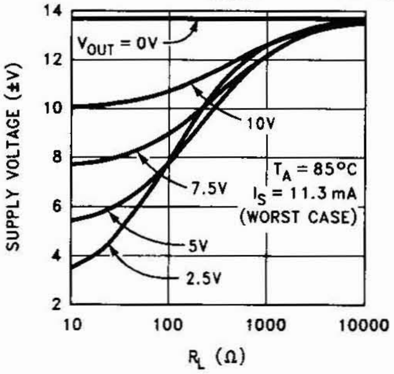
Applications Information — Contd.

If we set the two PD_{MAX} equations, [1] and [2], equal to each other, and solve for V_S, we can get a family of curves for various loads and output voltages according to [3]:

$$V_S = \frac{\dfrac{R_L{}^*(T_{JMAX} - T_{AMAX})}{N^*\theta_{JA}} + (V_{OUT})^2}{(I_S{}^*R_L) + V_{OUT}} \qquad [3]$$

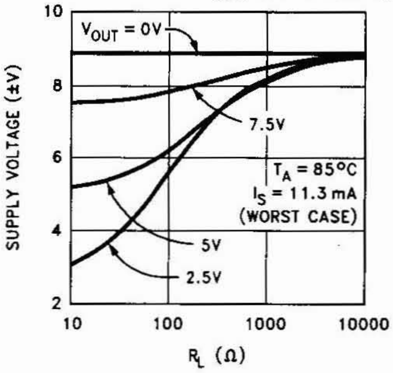
The figures below show total supply voltage V_S vs R_L for various output voltage swings for the PDIP and SOIC packages. The curves assume WORST CASE conditions of $T_A = +85°C$ and $I_S = 11.3$ mA per amplifier. The curves do not include heat removal or forcing air, or the simple fact that the package will be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Supply Voltage vs R_L for Various V_{OUT} (PDIP Package)



2360-12

Supply Voltage vs R_L for Various V_{OUT} (SOIC Package)



2360-13

Current Limit

The EL2360C has internal current limits that protect the circuit in the event of an output being shorted to ground. This limit is set at 100 mA nominally and reduces with the junction temperature. At $T_J = 150°C$, the current limits at about 65 mA. If any one output is shorted to ground, the power dissipation could be well over 1W, and much greater if all outputs are shorted. Heat removal is required in order for the EL2360C to survive an indefinite short.

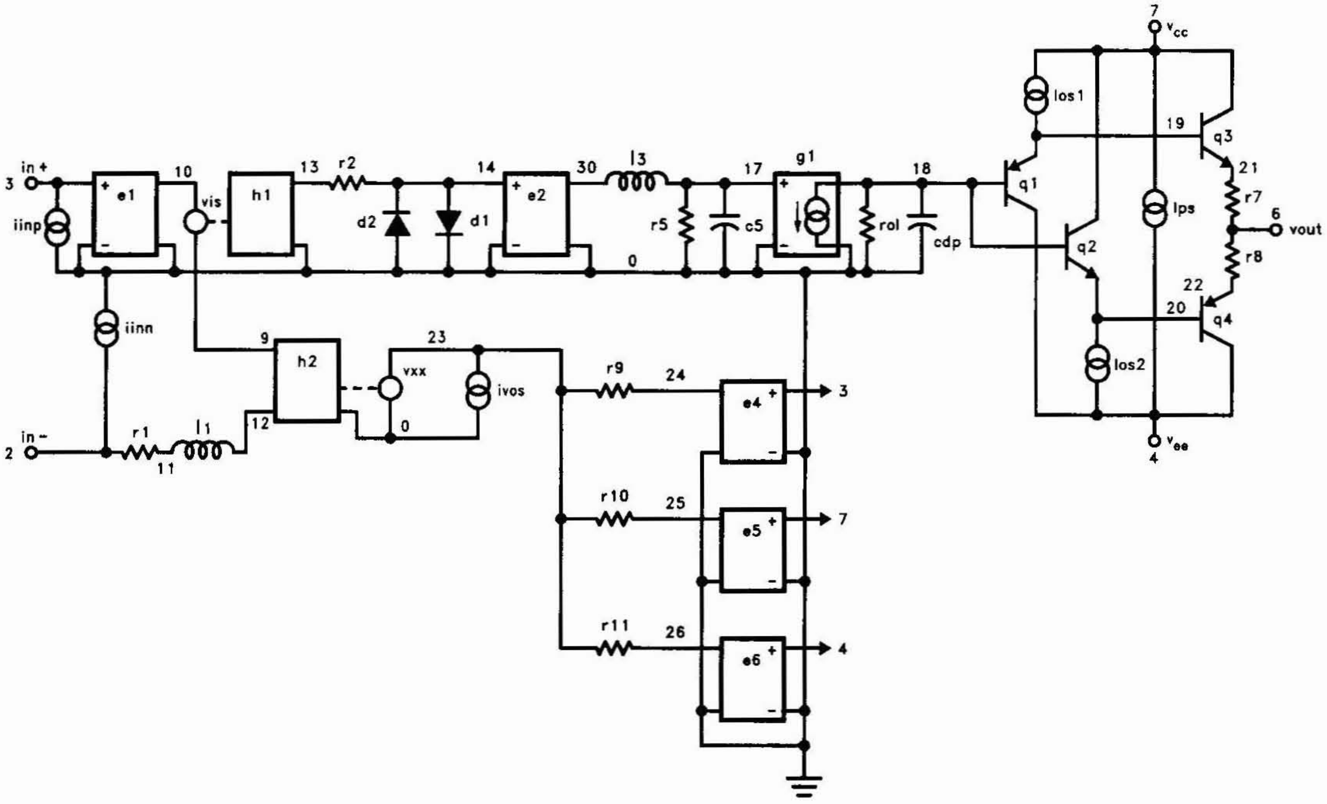
Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will de-couple the EL2360C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (R_F) to reduce the peaking.

EL2360C Macromodel

```
*     EL2360C Macromodel
*     Revision A, June 1996
*     AC characteristics used: Rf = Rg = 560 ohms
*     Pin numbers reflect a standard single opamp
*     Connections:        +input
*                          |      -input
*                          |       |      +Vsupply
*                          |       |       |       -Vsupply
*                          |       |       |       |      output
*                          |       |       |       |       |
.subckt EL2360/EL          3       2       7       4       6
*
*     Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 130
l1 11 12 25nH
iinp 3 0 0.5µA
iinm 2 0 5µA
r12 3 0 2 Meg
*
*     Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
*     High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 0.43µH
c5 17 0 0.27pF
r5 17 0 500
*
*     Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 2Meg
cdp 18 0 2.285pF
*
*     Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2mA
ios2 20 4 2mA
*
*     Supply Current
*
ips 7 4 2.5mA
*
*     Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 -1.0
r9 24 23 562
r10 25 23 1K
r11 26 23 1K
*
*     Models
*
.model qn npn(is=5e-15 bf=100 tf=0.1 ns)
.model qp pnp(is=5e-15 bf=100 tf=0.1 ns)
.model dclamp d(is=1e-30 ibv=0.266
+ bv=2.24v n=4)
.ends
```

EL2360C Macromodel — Contd.


in +
3
iinp
e1
10
vis
h1
13
r2
d2
d1
14
e2
30
l3
17
r5
c5
g1
18
rol
cdp
0
iinn
9
h2
23
vxx
ivos
0
12
in −
2
r1
l1
11
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4
7
v_{cc}
los1
19
q3
q1
21
r7
lps
6
vout
q2
r8
22
20
q4
los2
4
v_{ee}

2360–14

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2165C

30 MHz Precision Current Mode Feedback Amplifier

Features

- 35 MΩ transimpedance
- 30 MHz −3dB bandwidth (A_V = +1)
- 30 MHz −3dB bandwidth (A_V = +2)
- 1 mV input offset voltage
- 2 μA negative input bias current
- 86 dB common mode rejection ratio
- 92 dB power supply rejection ratio
- Low supply current, 4 mA
- Wide supply range, ±4.5V to ±16.5V
- 55 mA output peak current
- High capacitive load toleration
- Low cost
- Input/output compliance to ±2V of supplies
- 500 V/μs slew rate
- 65 ns settling to 0.1%
- 110 ns settling to 0.01%
- −68 dBc distortion @ 1 MHz

Applications

- Instrumentation circuitry
- Current to voltage convertors
- DAC/ADC output amplifier/ buffer
- Cable drivers
- Low distortion communications
- Medical imaging
- CCD imaging
- Infrared image enhancement

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2165CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2165CS	−40°C to +85°C	8-Lead SOIC	MDP0027

General Description

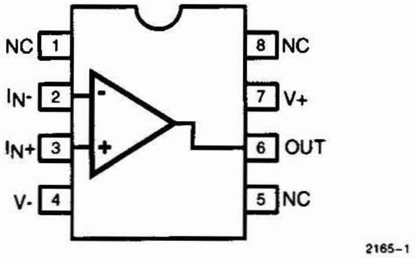
The EL2165C is a low offset, high transimpedance current mode feedback amplifier with a −3 dB bandwidth of 30 MHz at a gain of +2. Built on Elantec's proprietary monolithic complementary bipolar process, this amplifier uses current feedback to achieve more bandwidth at a given gain than conventional voltage feedback amplifiers.

The high 35 MΩ transimpedance gain and low input referred offset of the EL2165 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

In addition, the common-mode and power supply rejection have been greatly improved over earlier current mode feedback amplifiers and the input offset voltage and current have been trimmed to rival that of good conventional voltage feedback amplifiers. The part has a typical slew rate of 500 V/μs and a 0.01% settling time of less than 110ns in inverting mode. At a gain of +2 and an output signal level of 2 Vp-p, the total harmonic distortion is only −68 dB at 1 MHz.

The amplifier can operate on any supply from 9V (±4.5V) to 33V (±16.5V), yet consumes only 4 mA at any supply voltage. Using the industry standard 8-pin pinout, the EL2165C is available in both P-DIP and SO packages.

Connection Diagram



Manufactured under U.S. Patent No. 5,418,495, 5,420,542, 5,479,133

December 1995 Rev B

EL2165C
30 MHz Precision Current Mode Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+33V	Operating Junction Temperature	
Voltage between I_N+ and I_N-	±6V	Plastic Package	150°
Current into I_N+ and I_N-	4 mA	Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	See Curves		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics
(V_S = ±15V, R_L = 500Ω, T_A = 25°C unless otherwise specified)

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		25°C		1	3	I	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		2		V	μV/°C
$I_{IN}+$	+ Input Current		25°C		−1	±6	I	μA
$I_{IN}-$	− Input Current		25°C		±2	±7	I	μA
CMRR	Common Mode Rejection Ratio (Note 2)		25°C	79	86		I	dB
ICMR−	− Input Current Common Mode Rejection (Note 2)		25°C		23	100	I	nA/V
PSRR	Power Supply Rejection Ratio (Note 3)		25°C	84	93		I	dB
IPSR−	− Input Current Power Supply Rejection (Note 3)		25°C		75	225	I	nA/V
R_{OL}	Transimpedance (Note 4)	V_S = ±15V R_L = 500Ω	25°C		35		V	MΩ
		V_S = ±5V R_L = 150Ω	25°C	5.0	12.4		I	MΩ
$R_{IN}+$	+ Input Resistance			18	36		I	MΩ
$C_{IN}+$	+ Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range (Note 2)	V_S = ±15V	25°C	±12	±12.5		I	V
		V_S = ±5V	25°C	±2.0	±2.5		I	V

Open Loop DC Electrical Characteristics

(V_S = ±15V, R_L = 500Ω, T_A = 25°C unless otherwise specified) — Contd.

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	R_L = 500Ω V_S = ±15V	25°C	±12.3	±13		I	V
		R_L = 150Ω V_S = ±15V	25°C		±11.6		V	V
		R_L = 150Ω V_S = ±5V	25°C	±2.7	±3.0		I	V
I_{SC}	Output Short Circuit Current (Note 4 and 5)		25°C	55	80		I	mA
I_S	Supply Current		25°C		4.0	5.25	I	mA

Closed Loop AC Electrical Characteristics

(V_S = ±15V, A_V = +2, R_F = 1KΩ, R_L = 500Ω, T_A = 25°C unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
BW	−3dB (Note 8)	V_S = ±15V, A_V = +2, R_F = 1K		30		V	MHz
		V_S = ±15V, A_V = +1, R_F = 1.3K		28		V	MHz
		V_S = ±5V, A_V = +2, R_F = 1K		30		V	MHz
		V_S = ±5V, A_V = +1, R_F = 1.3K		30		V	MHz
SR	Slew Rate (Notes 6 and 8)	R_L = 500Ω	250	500		I	V/μS
		R_F = 1 KΩ, R_G = 110Ω R_L = 400Ω		500		V	V/μS
t_r, t_f	Rise Time, Fall Time (Note 8)	V_{OUT} = ±500 mV		14		V	nS
t_{pd}	Propagation Delay (Note 8)			12		V	nS
O_S	Overshoot (Note 8)	V_{OUT} = ±500 mV		2		V	%
t_s	0.1% Settling Time (Note 8)	V_{OUT} = ±10V A_V = 1		120		V	nS
		A_V = −1		65			
		A_V = 2		100			
t_s	0.01% Settling Time (Note 8)	V_{OUT} = ±10V A_V = 1		750		V	nS
		A_V = −1		110			
		A_V = 2		500			

Note 1: Measured from T_{MIN} to T_{MAX}

Note 2: V_{CM} = ±12V for V_S = ±15V and T_A = 25°C
V_{CM} = ±2V for V_S = ±5V and T_A = 25°C
CMIR is guaranteed by the part passing CMRR at the rated common-mode swing.

Note 3: The supplies are moved from ±4.5V to ±15V.

Note 4: V_{OUT} = ±10V for V_S = ±15V, and V_{OUT} = ±2V for V_S = ±5V.

Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

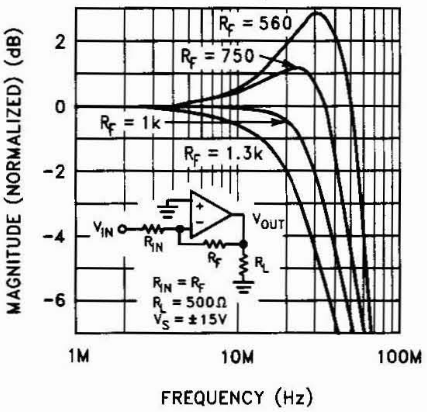
Note 6: Slew Rate is with V_{OUT} from +10V to −10V and measured at the 25% and 75% points.

Note 7: DC offset from −0.714V through +0.714V, AC amplitude 286 mV_{p-p}, f = 3.58 MHz.

Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

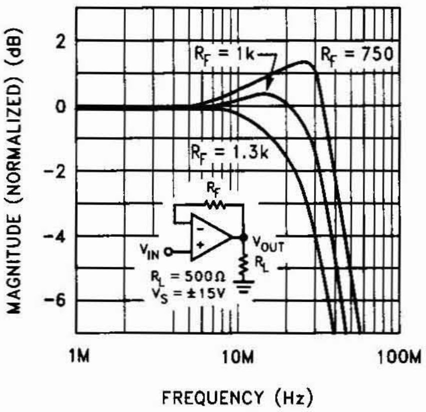
Typical Performance Curves

Frequency Response for $A_V = -1$ and for Various R_F Values



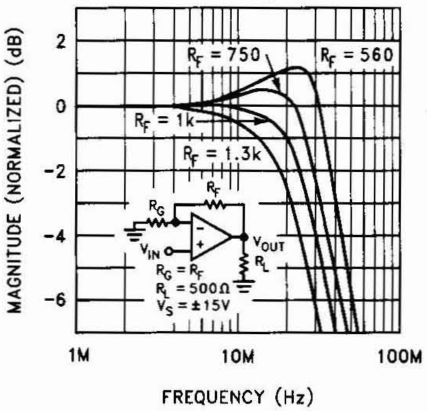
2165-2

Frequency Response for $A_V = +1$ and for Various R_F Values



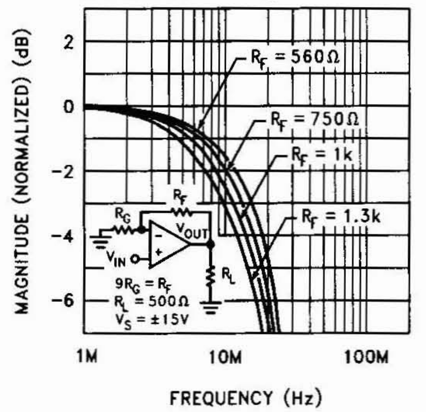
2165-3

Frequency Response for $A_V = +2$ and for Various R_F Values



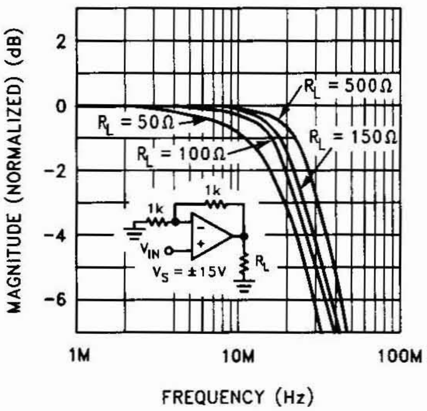
2165-4

Frequency Response for $A_V = +10$ and for Various R_F Values



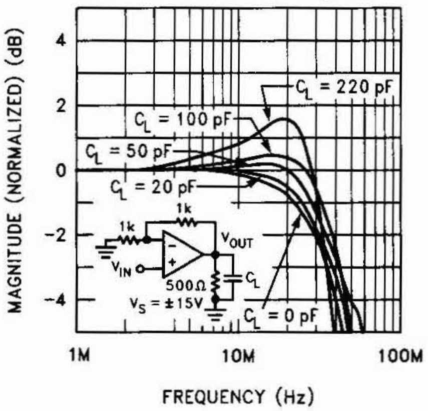
2165-5

Frequency Response for Various Values of R_L



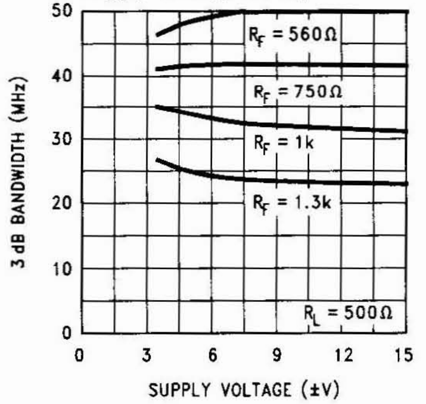
2165-6

Frequency Response for Various Values of C_L



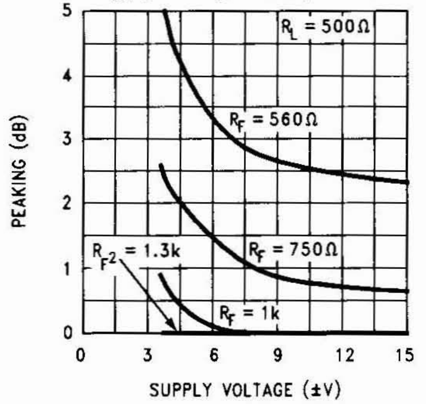
2165-7

3 dB Bandwidth vs Supply Voltage for $A_V = -1$



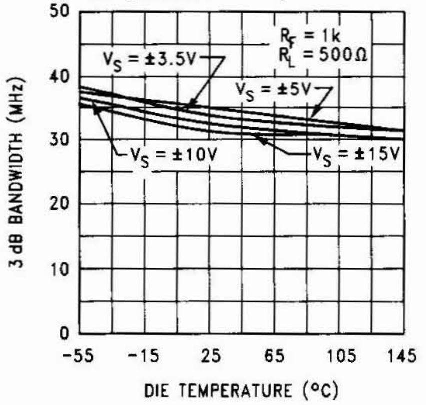
2165-8

Peaking vs Supply Voltage for $A_V = -1$



2165-9

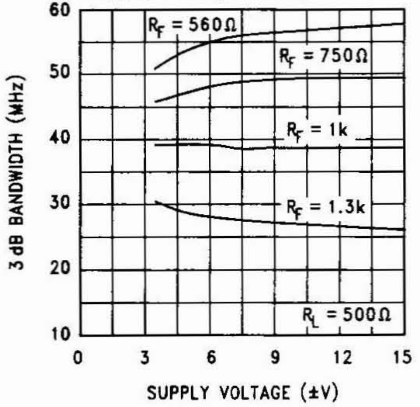
3 dB Bandwidth vs Temperature for $A_V = -1$



2165-10

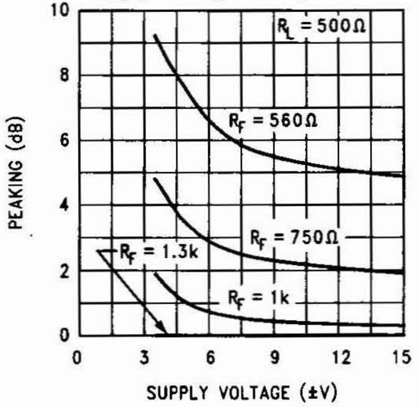
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for $A_V = +1$



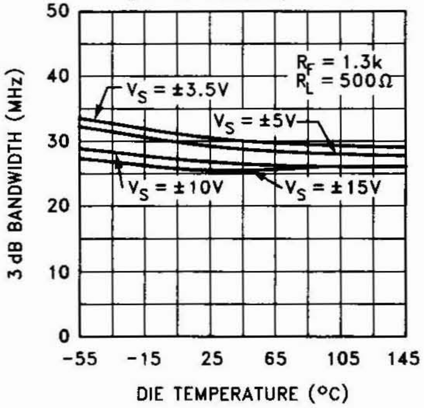
2165-11

Peaking vs Supply Voltage for $A_V = +1$



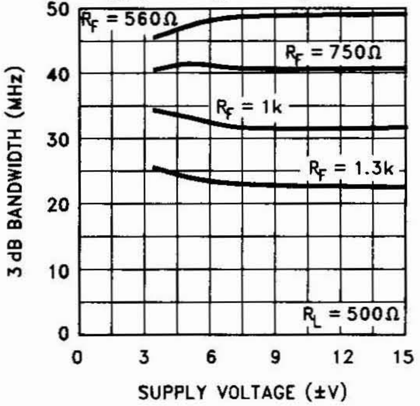
2165-12

3 dB Bandwidth vs Temperature for $A_V = +1$



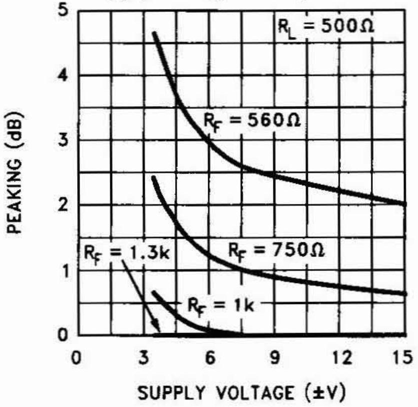
2165-13

3 dB Bandwidth vs Supply Voltage for $A_V = +2$



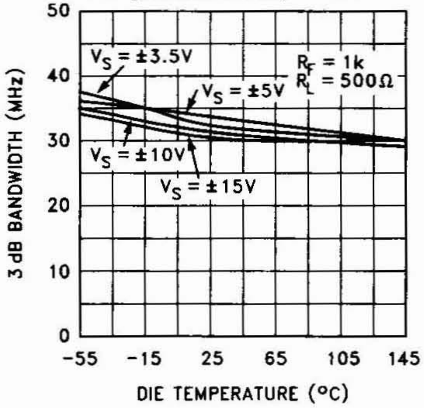
2165-14

Peaking vs Supply Voltage for $A_V = +2$



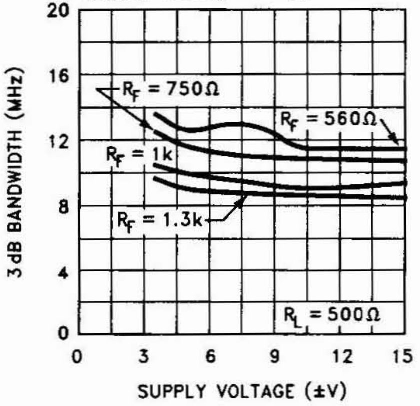
2165-15

3 dB Bandwidth vs Temperature for $A_V = +2$



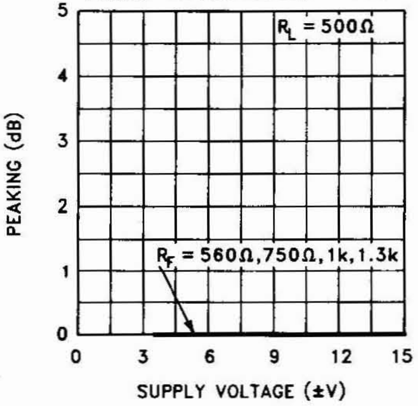
2165-16

3 dB Bandwidth vs Supply Voltage for $A_V = +10$



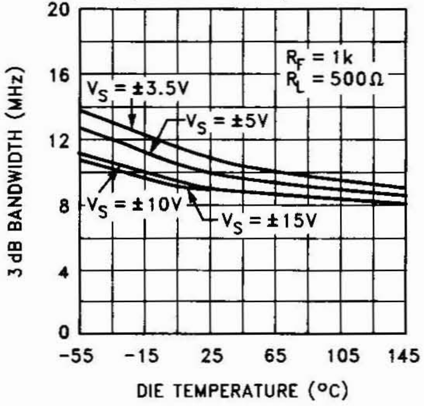
2165-17

Peaking vs Supply Voltage for $A_V = +10$



2165-18

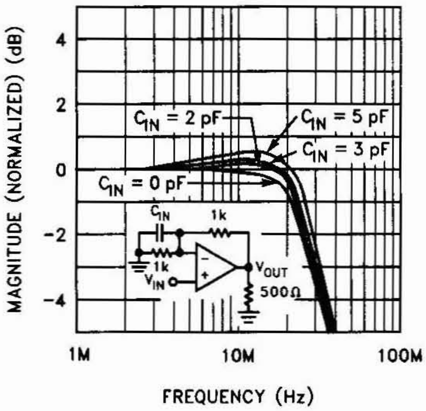
3 dB Bandwidth vs Temperature for $A_V = +10$



2165-19

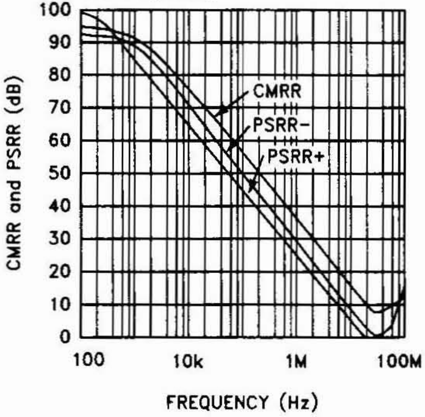
Typical Performance Curves — Contd.

Frequency Response for Various Values of C_{IN}



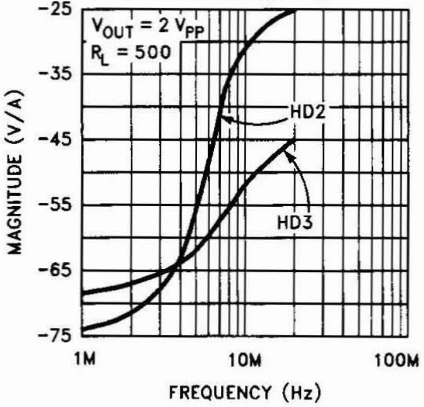
2165-20

PSRR and CMRR vs Frequency



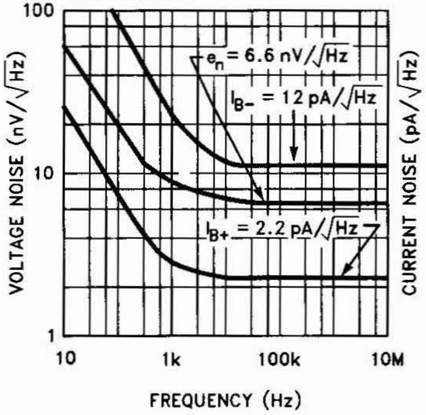
2165-21

Second and Third Hormonic Distortion vs Frequency



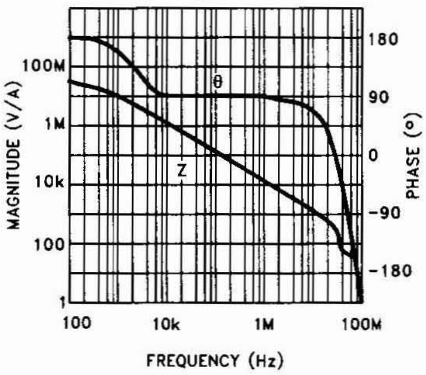
2165-41

Voltage and Current Noise vs Frequency



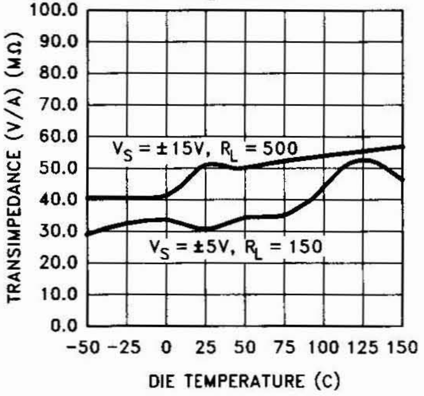
2165-22

Transimpedance (R_{OL}) vs Frequency



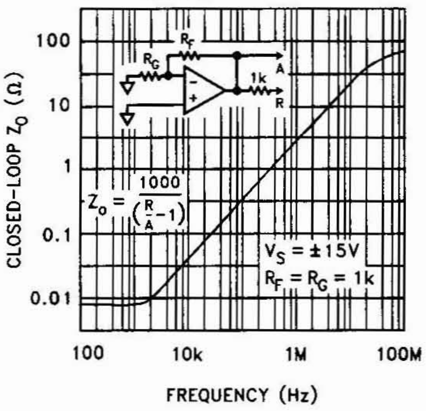
2165-23

Transimpedance (R_{OL}) vs Die Temperature



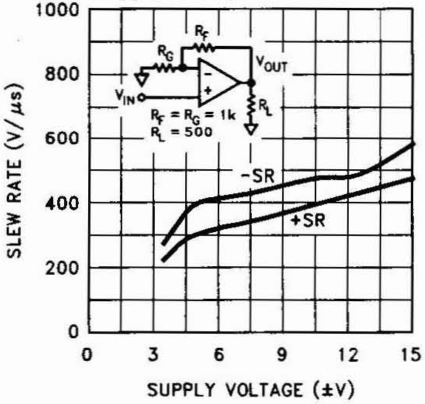
2165-24

Closed-Loop Output Impedance vs Frequency



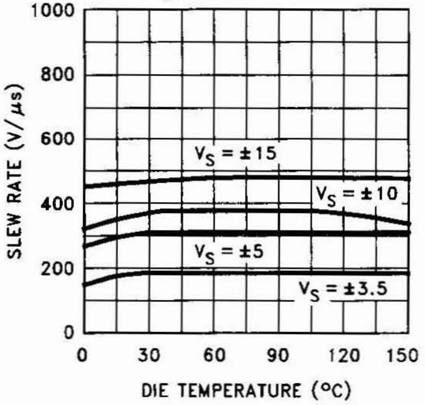
2165-25

Slew Rate vs Supply Voltage



2165-26

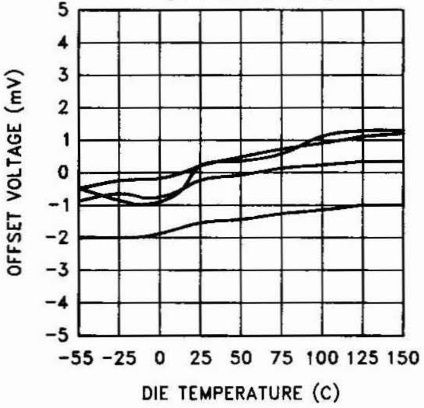
Slew Rate vs Temperature



2165-27

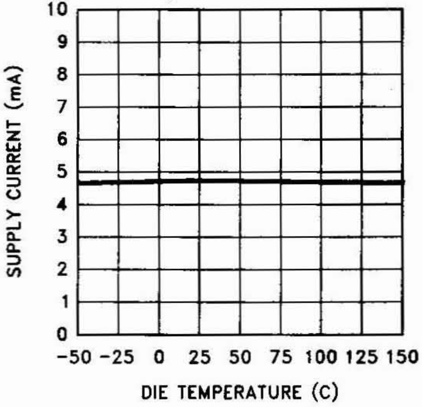
Typical Performance Curves — Contd.

Offset Voltage vs Die Temperature (4 Samples)



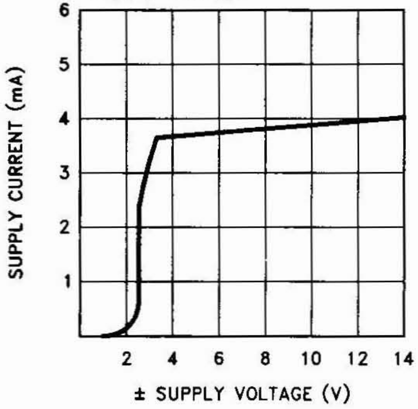
2165-28

Supply Current vs Die Temperature



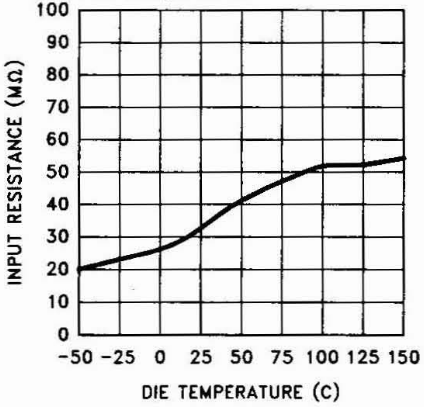
2165-29

Supply Current vs Supply Voltage



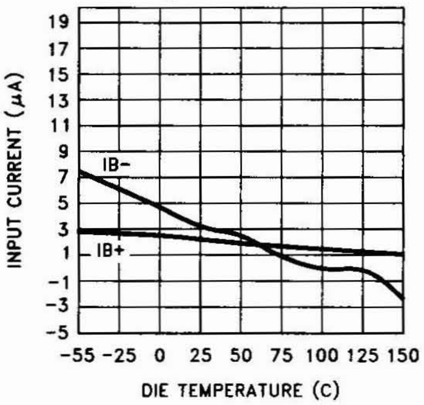
2165-30

Input Resistance vs Die Temperature



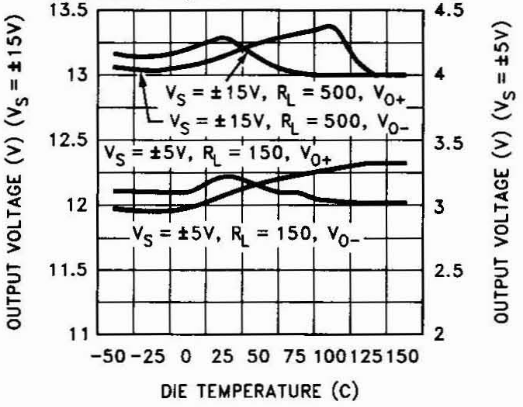
2165-31

Input Current vs Die Temperature



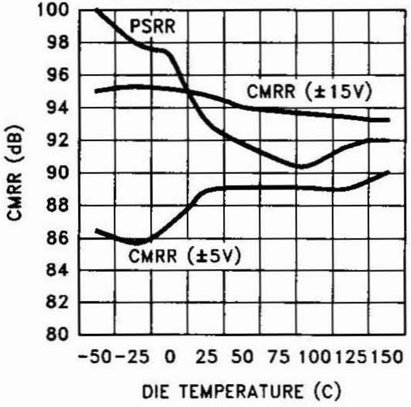
2165-32

Output Voltage Swing vs Die Temperature



2165-33

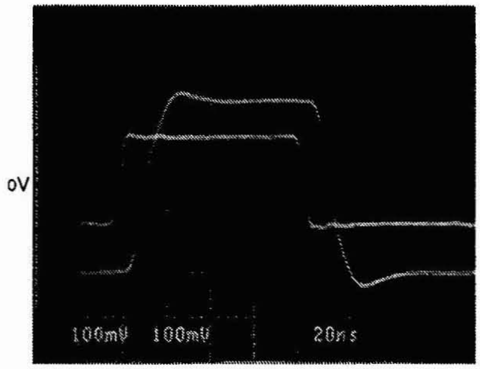
PSRR and CMRR vs Die Temperature



2165-34

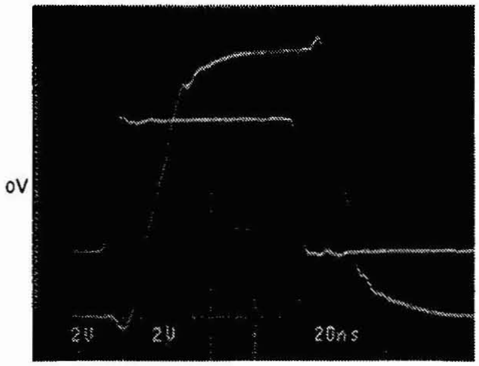
Typical Performance Curves — Contd.

Small Signal Pulse Response



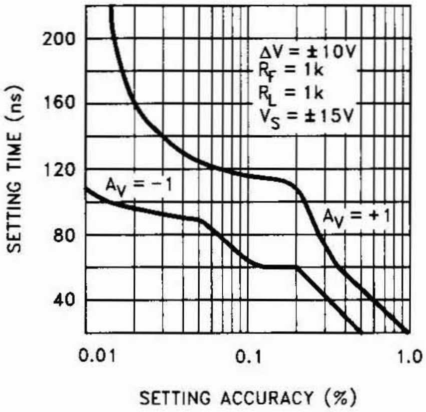
2165-35

Large Signal Pulse Response



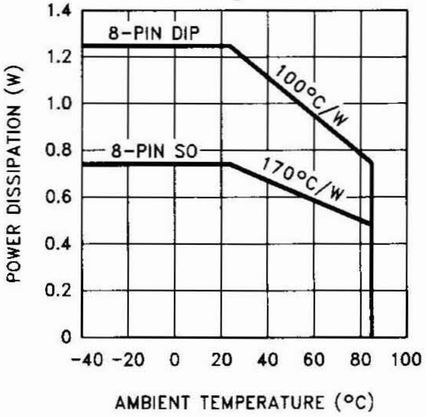
2165-36

Settling Time vs Settling Accuracy



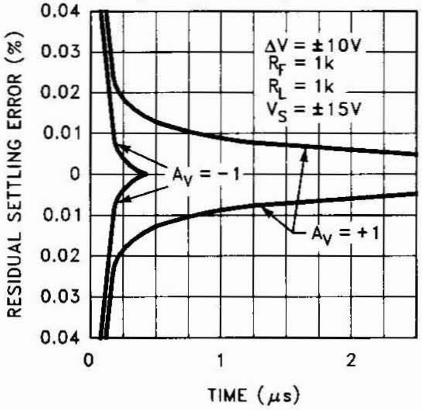
2165-37

8-Pin Package Power Dissipation vs Ambient Termperature



2165-38

Long Term Settling Error



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Applications Information

Product Description

The EL2165C is a single current mode feedack amplifier that offers wide bandwidth, high gain, low distortion and exceptional DC specifications for a CMF type amplifier at moderate supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in the industry standard pin-out. Due to the current feedback architecture, the EL2165 closed loop 3 dB bandwidth is dependent on the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain set resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3 dB bandwidth is significantly less dependent on supply voltage than earlier CMF amplifiers where increasing junction capacitances with decreasing supply voltage caused a much larger reduction in bandwidth. To compensate for the remaining effect, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼". The power supply pins must be well bypassed to ensure stability. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should have low inductance for best performance. Use of sockets, particularly for SO packages, should be avoided. Sockets have parasitic inductance and capacitance which will cause peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the conventional current feedback amplifiers, stray capacitance at the inverting input will affect their AC and transient performance when operating in the non-inverting configuration. This may cause design, development and production difficulties. The EL2165 has been designed in such a way as to largely ignore such strays. The characteristic curves of gain vs. frequency with varying values of C_{IN-} illustrate this effect which produces only a slight increase in peaking with C_{IN-} values up to 5 pF with almost no change in 3 dB bandwidth.

In the inverting gain mode, added capacitance at the inverting input has almost no effect at all. This is because the inverting input is now a virtual ground and the stray capacitance is not therefore "seen" by the amplifier.

Feedback Resistors Values

The EL2165 has been designed and specified with $R_F = 1\ K\Omega$ for $A_V = +2$. This value of feedback resistor yields an extremely flat frequency response with little or no peaking out to 30 MHz. As is the case with all CMF amplifiers, wider bandwidth, at the expense of peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at lower frequency. For example, the 3 dB bandwidth of the EL2165 connected for $A_V = -1$ and $R_F = 1\ K\Omega$ is about 34 MHz. If R_F is reduced to 750Ω the bandwidth increases to 48 MHz. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors, supply voltages and temperature.

Bandwidth vs. Temperature

The supply current of many amplifiers, and consequently their 3 dB bandwidths, drop off significantly with increasing temperature. The EL2165 was designed to have nearly constant supply current over temperature resulting in a part with much less bandwidth vs. temperature sensitivity. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth only varies from 38 MHz to 29 MHz over the entire die temperature range of $0°C < T < 150°C$.

Applications Information — Contd.

Supply Voltage Range

The EL2165 has been designed to operate comfortably with supply voltages from ±5V to ±15V. AC characterization has been conducted down to supply voltages of ±3.5V. However, this low value will not allow the part to power up and function properly at the lowest portion of the part's operating temperature range (−40°C to +85°C). In general, bandwidth, slew rate and video characteristics will tend to improve with increasing supply voltages.

If a single supply is desired, values from +9V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and DC couple the signal, or 2) ensure the driving a signal is within the input common mode range of the EL2165.

Settling Characteristics

The EL2165 offers superb settling characteristics to 0.1%, typically 65 ns operating in inverting mode. The inverting 0.01% settling time is about 110 ns. The EL2165 is not slew rate limited, therefore a step size up to ±10V gives the same settling time. The high 35 MΩ transimpedance gain and low input referred offsets of the EL2165 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

The noninverting ($A_V = +1$) 0.1% settling time is about 120 ns. As can be seen from the Long Term Settling Error graph, for $A_V = +1$, there is approximately a 0.04% residual which tails away to 0.01% in about 750 ns. This is a thermal settling error caused by a power dissipation change in the input stage devices (before and after the voltage step). All others CMF amplifier exhibit 0.01% thermal settling tails of several tens of microseconds under the same conditions. The input stage of the EL2165 has been designed to greatly reduce this effect. For $A_V = -1$, the inverting input is a virtual ground, therefore this tail does not appear even in conventional CMF amplifiers since the input stage does not experience the large voltage change that it does in non-inverting mode.

Distortion Performance

The distortion performance of all high frequency amplifiers degrade with increasing frequency. The EL2165 is no exception. However, due to the part's high transimpedance, its distortion performance at a given frequency can be 4 dB–8 dB better than other high speed amplifiers available, with the same power dissipation.

Power Dissipation

The EL2165 amplifier combines both high speed and large output drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature and loading conditions. To ensure that the EL2165 remains within it's absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by it's thermal resistance and the amount of temperature rise according to:

$$P_{Dmax} = (TJ_{MAX} - TA_{MAX})/\theta_{JA}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power dissipated in the IC due to the load, or:

$$P_{Dmax} = N \times (2 \times V_S \times I_{S} + (V_S - V_{OUT}) \times V_{OUT}/R_L)$$

where N is the number of amplifiers per package, and I_S is the current per amplifier. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term when the output is driving a load. That is to say, due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher temperatures and lower supply current. Unlike some amplifiers, the EL2165 and many other Elantec amplifiers maintain almost constant supply current over temperature so that

Applications Information — Contd.

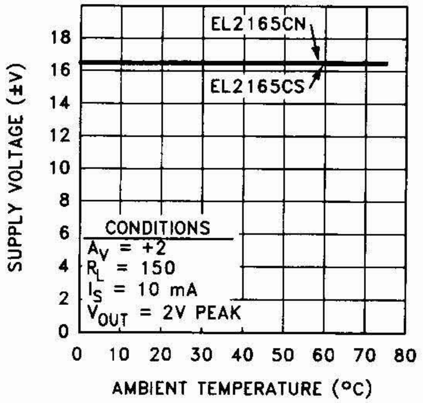
the AC performance is not degraded as much at the upper end of the operating temperature range.

The EL2165 consumes typically 4 mA and a maximum of 5 mA. The worst case power dissipated in a IC amplifier operating from split supplies with a grounded load occurs when the output is between ground and half of one of its supplies or, if it can't go that far due to drive limitations, at its maximum value. If we assume that the EL2165 is used for double terminated cable driving application ($R_L = 150\Omega$), and $A_V = +2$, then the maximum output voltage is 2V, and the average output voltage is 1.4V. If we set the two P_{Dmax} equations equal to each other, and solve for V_S, we get a family of curves for various packages options according to :

$$V_S = \frac{R_L \times (TJ_{MAX} - TA_{MAX}) / N \times \theta_{JA} + (V_{OUT}) \times (V_{OUT})}{(2 \times I_S \times R_L) + (V_{OUT})}$$

The following curve shows supply voltage ($\pm V_S$) vs. temperature for the EL2165's two packages assuming $A_V = +2$, $R_L = 150$, and V_{OUT} (peak) = 2V. The curves include the worst case supply specification ($I_S = 5$ mA).

Supply Voltage vs Ambient Temperature



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The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the device.

Output Current Drive

The EL2165 does not have output short circuit protection. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2165 to survive an indefinite short.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For these applications, the back termination series resistor will decouple the EL2165 from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. The EL2165 has particularly high capacitive load toleration and can drive a 50 pF load with only 0.3 dB of peaking and a 100 pF load with only 0.5 dB of peaking and without any instability. If higher capacitive loads must be driven or if little or no peaking is required, an additional small value ($5\Omega-50\Omega$) resistor can be placed in series with the output. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistance at the output.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2166C

110 MHz Current Feedback Amplifier with Disable

Features

- 110 MHz 3 dB bandwidth ($A_V = +2$)
- 115 MHz 3 dB bandwidth ($A_V = +1$)
- 0.01% differential gain, $R_L = 500\Omega$
- 0.01° differential phase, $R_L = 500\Omega$
- Low supply current, 7.5 mA
- Fast disable < 75 ns
- Low cost
- 1500 V/μs slew rate

Applications

- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters
- Broadcast equipment
- High speed communications
- Video multiplexing

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL2166CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2166CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

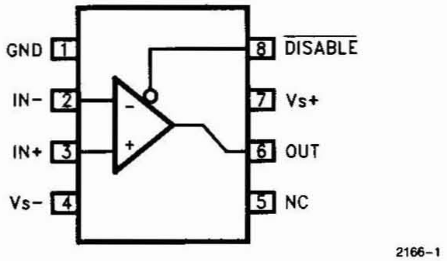
The EL2166C is a current feedback operational amplifier with −3 dB bandwidth of 110 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, this amplifer uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

The EL2166C is designed to drive a double terminated 75Ω coax cable to video levels. Differential gain and phase are excellent when driving both loads of 500Ω (<0.01%/<0.01°) and double terminated 75Ω cables (0.025%/0.05° @ $V_S = \pm 15V$, 0.04%/0.02° @ $V_S = \pm 5V$).

The EL2166C has a superior output disable function. Time to enable or disable is < 75 ns. The $\overline{\text{DISABLE}}$ pin is TTL/CMOS compatible. In disable mode, the amplifier can withstand over 1500 V/μs signals at their outputs. The amplifier can operate on any supply voltage from 10V (±5V) to 33V (±16.5V), yet consume only 7.5 mA at any supply voltage. The EL2166C is available in 8-pin P-DIP and 8-pin SO packages.

Connection Diagram

EL2166C SO, P-DIP
Packages



Top View

Manufactured under U.S. Patent No. 5,420,542, 4,893,091

December 1995 Rev C

EL2166C

110 MHz Current Feedback Amplifier with Disable

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+33V
Voltage between +IN and −IN	±6V
Current into +IN or −IN	10 mA
Output Current	±50 mA
Current into $\overline{\text{DISABLE}}$ Pin	±5 mA
Voltage between $\overline{\text{DISABLE}}$ Pin and GND Pin	±7V

Voltage at IN+, IN−, V_{OUT}, $\overline{\text{DISABLE}}$, GND Pins	$(V_{S-}) - 0.5V$ to $(V_{S+}) + 0.5V$
Internal Power Dissipation	See Curves
Operating Ambient Temperature Range	−40°C to +85°C
Operating Junction Temperature Plastic Packages	150°C
Storage Temperature Range	−65°C to +150°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2166C	
V_{OS}	Input Offset Voltage	V_S = ±5V, ±15V	25°C		2	10	I	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		10		V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		0.5	5	I	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		5	20	I	µA
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	25°C	55	62		II	dB
−ICMR	−Input Current Common Mode Rejection (Note 2)	V_S = ±5V, ±15V	25°C		0.1	2	I	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		25°C	65	72		II	dB
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.1	2	I	µA/V

Open Loop DC Electrical Characteristics — Contd.

V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2166C	
R_{OL}	Transimpedance (Note 4)	V_S = ±15V R_L = 400Ω	25°C	500	2000		I	kΩ
		V_S = ±5V R_L = 150Ω	25°C	500	1200		I	kΩ
$+R_{IN}$	+ Input Resistance		25°C	2.0	5.0		I	MΩ
$+C_{IN}$	+ Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range	V_S = ±15V	25°C	±12.6	±13.2		I	V
		V_S = ±5V	25°C	±2.6	±3.2		I	V
V_O	Output Voltage Swing	R_L = 400Ω, V_S = ±15V	25°C	±12	±13.5		I	V
		R_L = 150Ω, V_S = ±15V	25°C		±11.4		V	V
		R_L = 150Ω, V_S = ±5V	25°C	±3.0	±3.7		I	V
I_{SC}	Output Short Circuit Current (Note 5)	V_S = ±5V, V_S = ±15V	25°C	50	80	130	I	mA
I_S	Supply Current	V_S = ±15V V_S = ±5V	25°C		7.5	10.0	I	mA
I_S, OFF	Supply Current Disabled, Pin 8 = 0V		25°C		7.3	10.0	I	mA
I_{OUT}, OFF	Output Current Disabled, Pin 8 = 0V	A_V = +1	25°C		2.0	50.0	I	μA
V_{IH}	$\overline{\text{DISABLE}}$ Pin Voltage for Output Enabled (Note 9)		25°C	2.0			I	V
V_{IL}	$\overline{\text{DISABLE}}$ Pin Threshold for Output Disabled		25°C			0.8	I	V
I_{DIS}, ON	$\overline{\text{DISABLE}}$ Pin Input Current, Pin 8 = +5V		25°C		70	150	I	μA
I_{DIS}, OFF	$\overline{\text{DISABLE}}$ Pin Input Current, Pin 8 = 0V		25°C	−150	−60		I	μA

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V, A_V = +2, R_F = 560\Omega, R_L = 150\Omega, T_A = 25^\circ C$ unless otherwise noted

Parameter	Description	Conditions	Limits			Test Level	Units
			Min	Typ	Max	EL2166C	
BW	−3 dB Bandwidth (Note 8)	$V_S = \pm 15V, A_V = +2$		110		V	MHz
		$V_S = \pm 15V, A_V = +1$		115		V	MHz
		$V_S = \pm 5V, A_V = +2$		95		V	MHz
		$V_S = \pm 5V, A_V = +1$		100		V	MHz
SR	Slew Rate (Notes 6, 8)	$R_L = 400\Omega$	1000	1500		IV	V/µs
t_r, t_f	Rise Time, Fall Time, (Note 8)	$V_{OUT} = \pm 500mV$		3.2		V	ns
t_{pd}	Propagation Delay (Note 8)			4.3		V	ns
OS	Overshoot (Note 8)	$V_{OUT} = \pm 500\ mV$		7		V	%
t_s	0.1% Settling Time (Note 8)	$V_{OUT} = \pm 10V$ $A_V = \pm 1, R_L = 1K$		35		V	ns
dG	Differential Gain (Notes 7, 8)	$R_L = 150\Omega, V_S = \pm 15V$		0.025		V	%
		$R_L = 150\Omega, V_S = \pm 5V$		0.05		V	%
		$R_L = 500\Omega, V_S = \pm 15V$		0.01		V	%
		$R_L = 500\Omega, V_S = 5V$		0.01		V	%
dP	Differential Phase (Notes 7, 8)	$R_L = 150\Omega, V_S = \pm 15V$		0.04		V	deg (°)
		$R_L = 150\Omega, V_S = \pm 5V$		0.02		V	deg (°)
		$R_L = 500\Omega, V_S = \pm 15V$		0.01		V	deg (°)
		$R_L = 500\Omega, V_S = 5V$		0.01		V	deg (°)
t_{DIS}	Disable/Enable Time (Note 10)			75		V	ns

Note 1: Measured from T_{MIN} to T_{MAX}.

Note 2: $V_{CM} = \pm 12.6V$ for $V_S = \pm 15V$ and $T_A = 25^\circ C$
$V_{CM} = \pm 2.6V$ for $V_S = \pm 5V$ and $T_A = 25^\circ C$

Note 3: The supplies are moved from ±5V to ±15V.

Note 4: $V_{OUT} = \pm 7V$ for $V_S = \pm 15V$, and $V_{OUT} = \pm 2V$ for $V_S = \pm 5V$.

Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

Note 6: Slew Rate is with V_{OUT} from +10V to −10V and measured at the 25% and 75% points.

Note 7: DC offset from −0.714V through +0.714V, AC amplitude 286 $mV_{p\text{-}p}$, f = 3.58 MHz.

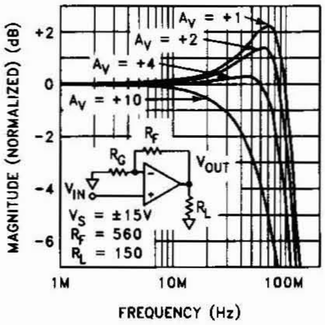
Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

Note 9: The EL2166C will remain ENABLED if pin 8 is either left unconnected or V_{IH} is applied to pin 8.

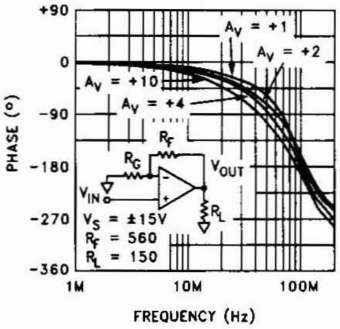
Note 10: Disable/Enable time is defined as the time from when the logic signal is applied to the $\overline{\text{DISABLE}}$ pin to when the output voltage has gone 50% of the way from its initial to its final value.

Typical Performance Curves

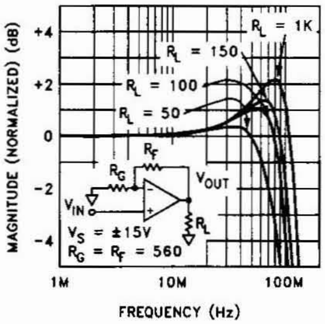
Non-Inverting Frequency Response (Gain)



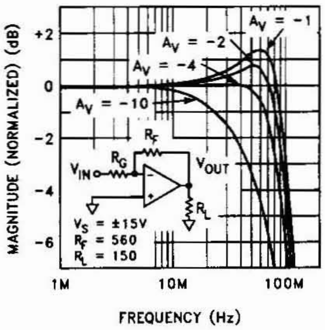
Non-Inverting Frequency Response (Phase)



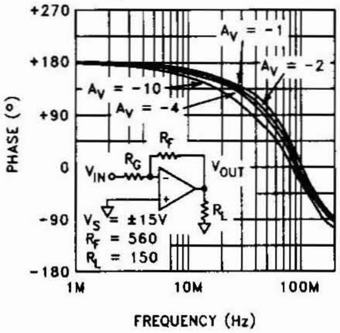
Frequency Response for Various R_L



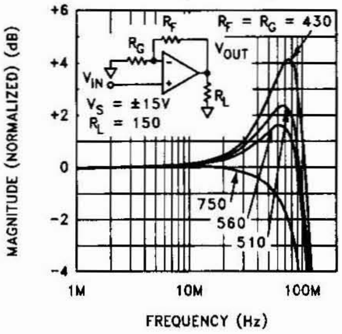
Inverting Frequency Response (Gain)



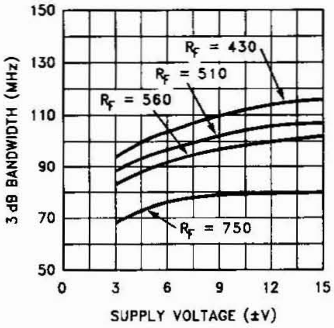
Inverting Frequency Response (Phase)



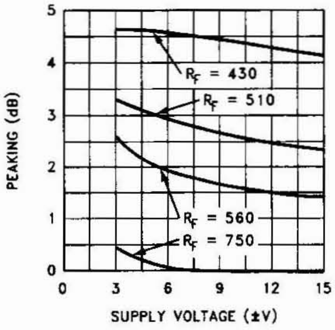
Frequency Response for Various R_F and R_G



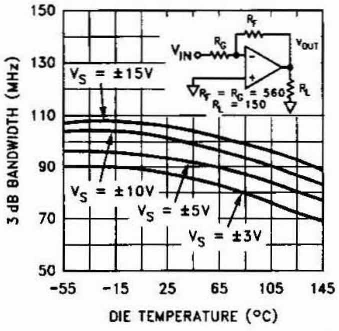
3 dB Bandwidth vs Supply Voltage for A_V = −1



Peaking vs Supply Voltage for A_V = −1



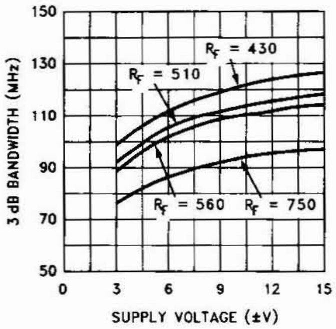
3 dB Bandwidth vs Temperature for A_V = − 1



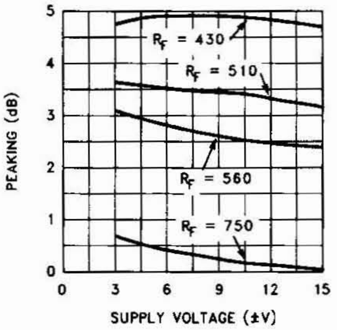
2166-2

Typical Performance Curves — Contd.

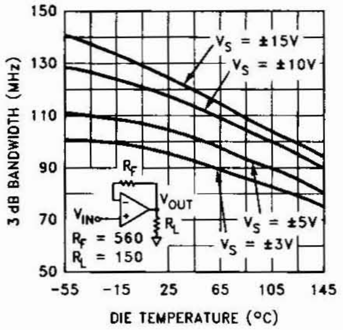
3 dB Bandwidth vs Supply Voltage for $A_V = +1$



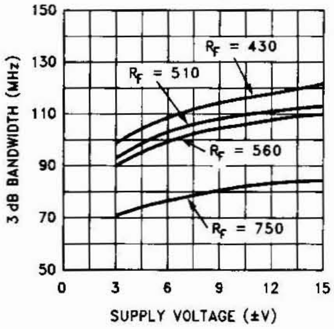
Peaking vs Supply Voltage for $A_V = +1$



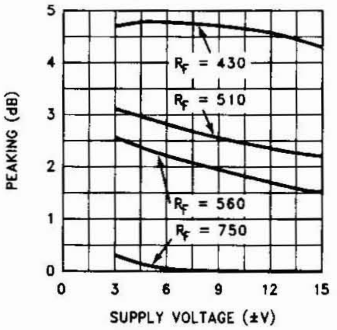
3 dB Bandwidth vs Temperature for $A_V = +1$



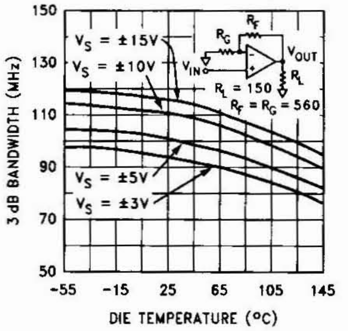
3 dB Bandwidth vs Supply Voltage for $A_V = +2$



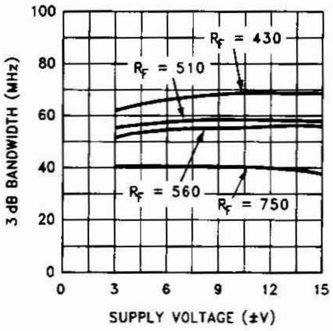
Peaking vs Supply Voltage for $A_V = +2$



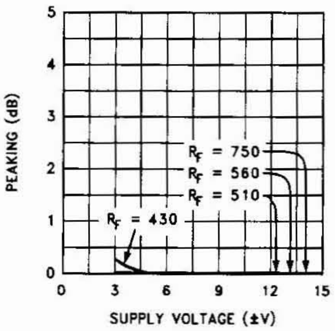
3 dB Bandwidth vs Temperature for $A_V = +2$



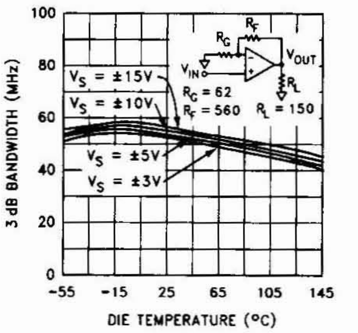
3 dB Bandwidth vs Supply Voltage for $A_V = +10$



Peaking vs Supply Voltage for $A_V = +10$



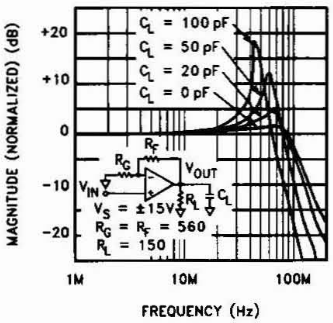
3 dB Bandwidth vs Temperature for $A_V = +10$



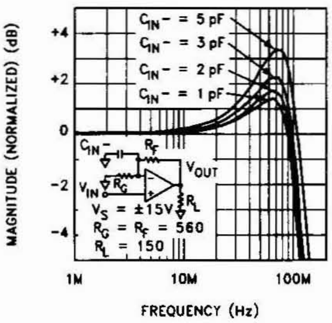
2166-3

Typical Performance Curves — Contd.

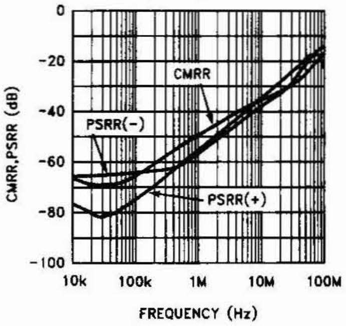
Frequency Response for Various C_L



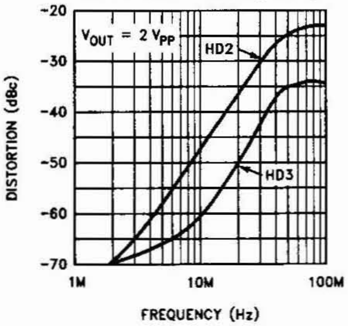
Frequency Response for Various C_{IN-}



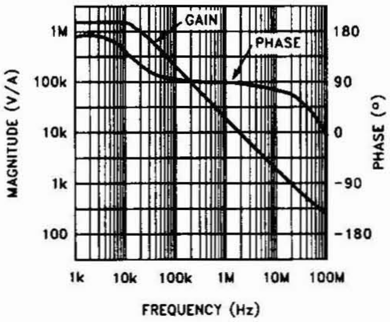
PSRR and CMRR vs Frequency



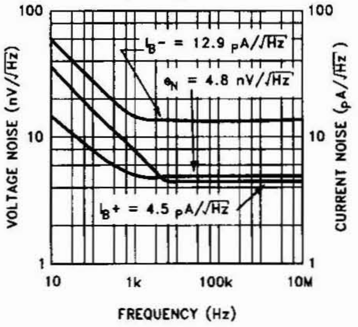
2nd and 3rd Harmonic Distortion vs Frequency



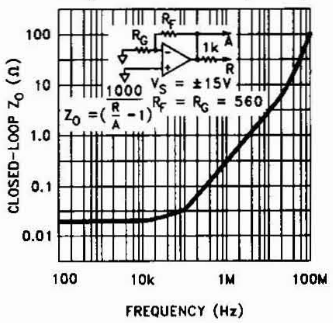
Transimpedance (R_{OL}) vs Frequency



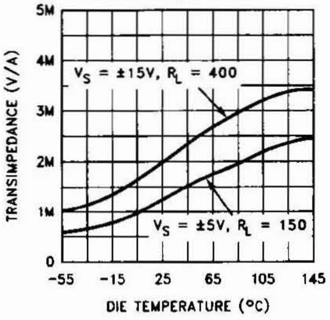
Voltage and Current Noise vs Frequency



Closed-Loop Output Impedance vs Frequency



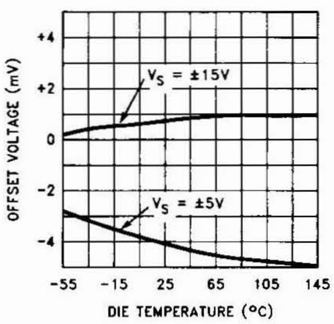
Transimpedance (R_{OL}) vs Die Temperature



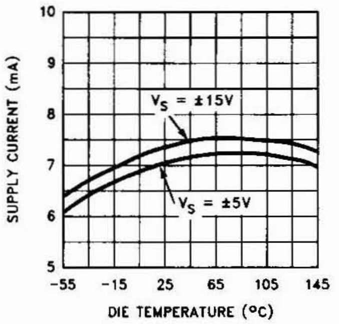
2166-4

Typical Performance Curves — Contd.

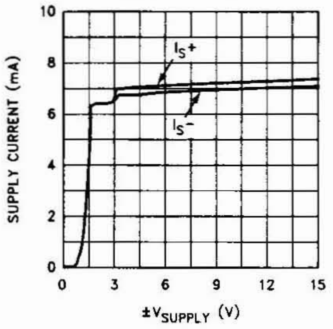
Offset Voltage vs Die Temperature



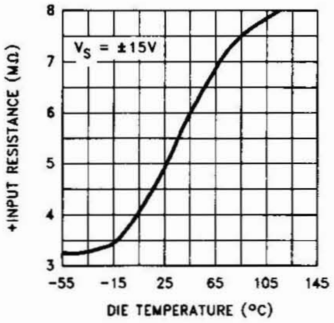
Supply Current vs Die Temperature



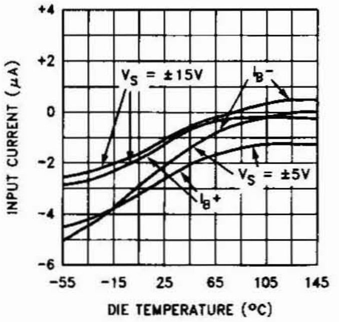
Supply Current vs Supply Voltage



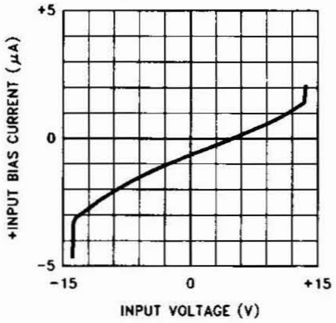
+Input Resistance vs Die Temperature



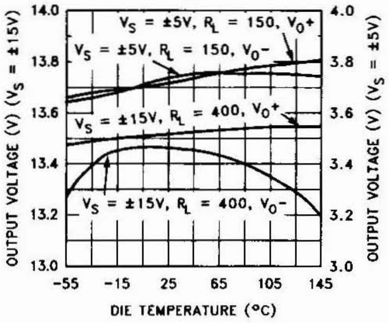
Input Current vs Die Temperature



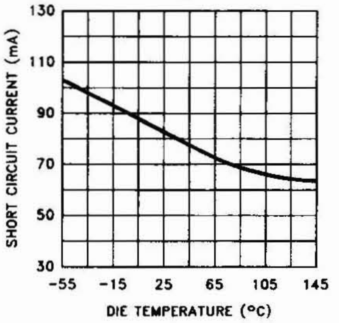
+Input Bias Current vs Input Voltage



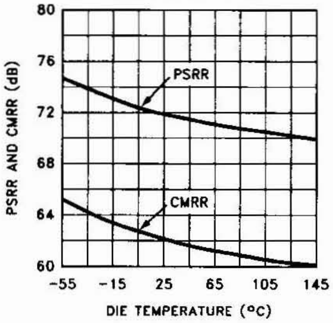
Output Voltage Swing vs Die Temperature



Short Circuit Current vs Die Temperature



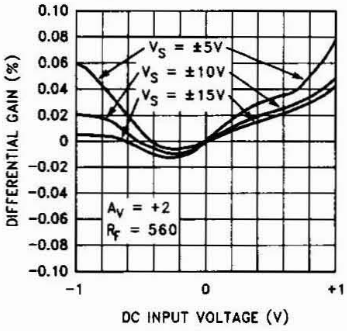
PSRR & CMRR vs Die Temperature



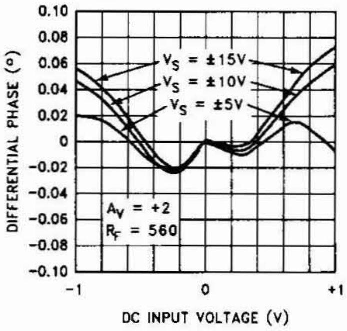
2166-5

Typical Performance Curves — Contd.

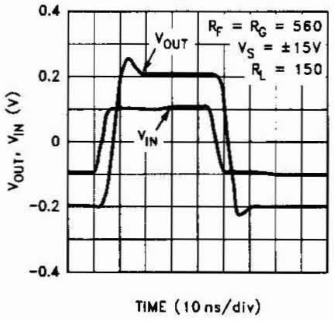
Differential Gain vs DC Input Voltage, R_L = 150



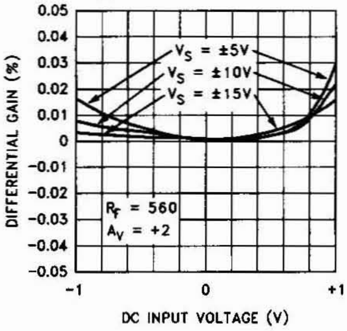
Differential Phase vs DC Input Voltage, R_L = 150



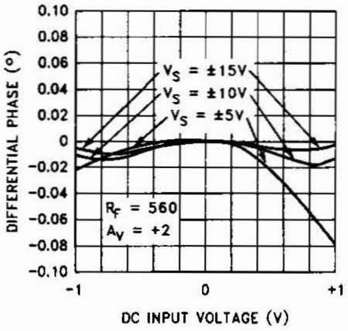
Small Signal Pulse Response



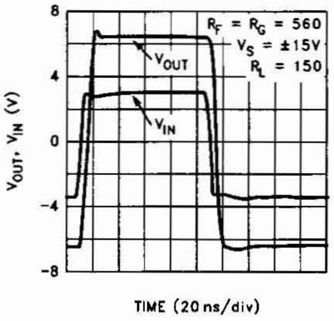
Differential Gain vs DC Input Voltage, R_L = 500



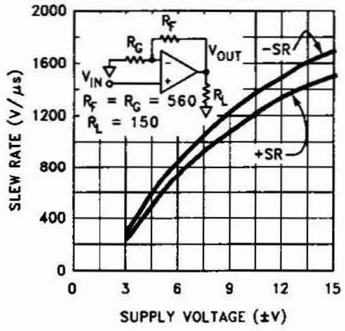
Differential Phase vs DC Input Voltage, R_L = 500



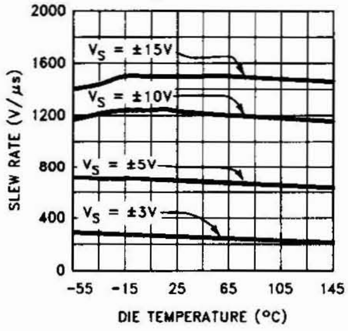
Large Signal Pulse Response



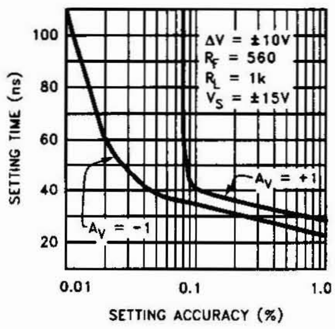
Slew Rate vs Supply Voltage



Slew Rate vs Temperature

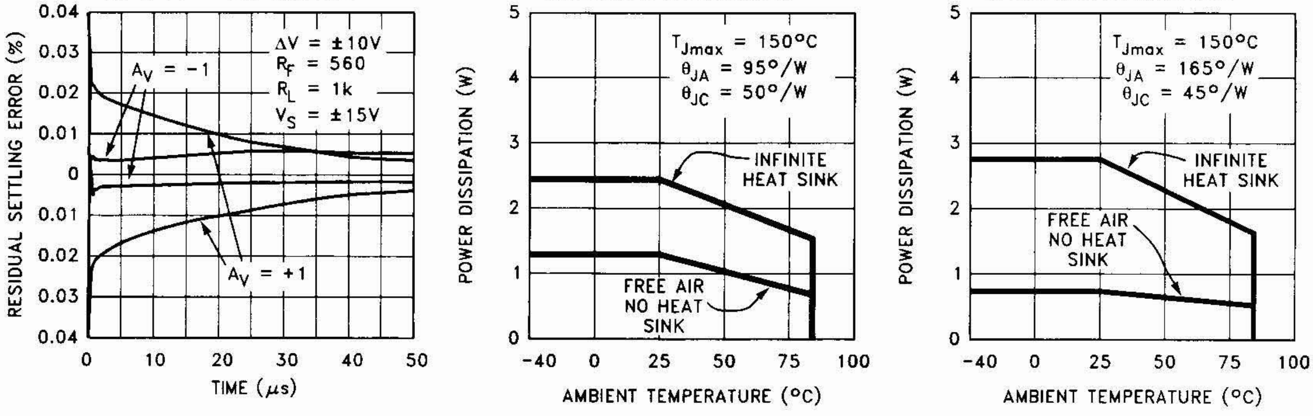


Settling Time vs Settling Accuracy



2166-6

Typical Performance Curves — Contd.



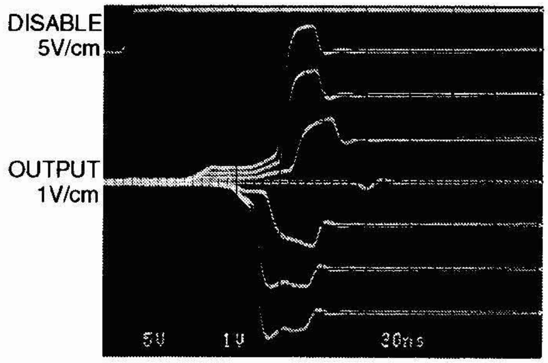
Long Term Settling Error

8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature

8-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature

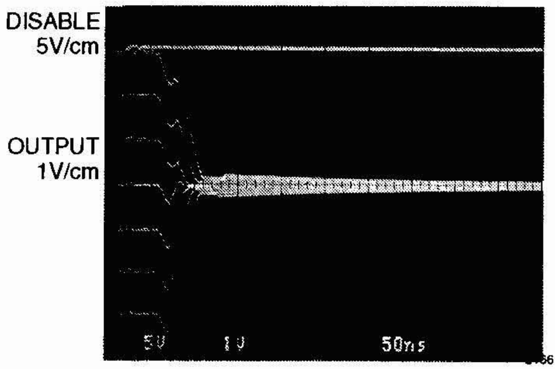
2166-7

ENABLE Response for a Family of D.C. Inputs



$A_V = +2, R_L = 150, V_S = \pm 15V$ 2166-8

DISABLE Response for a Family of D.C. Inputs

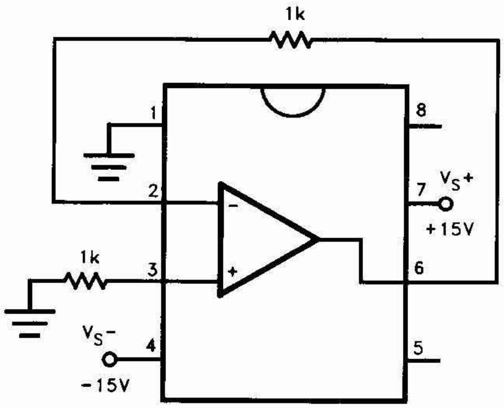


2166-9

$A_V = +2, R_L = 150, V_S = \pm 15V$

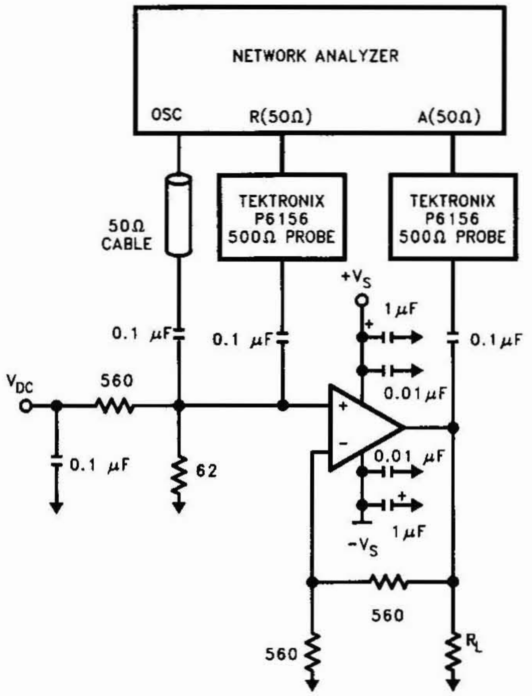
Burn-In Circuit

EL2166C



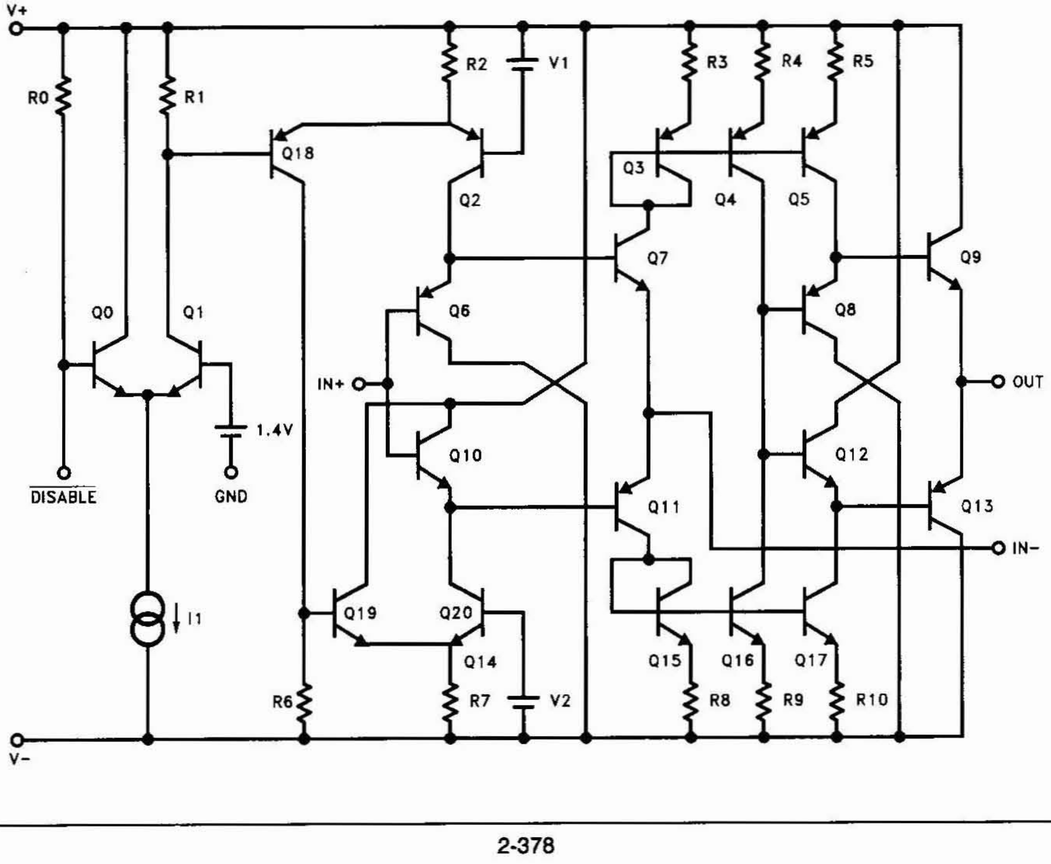
2166-10

Differential Gain and Phase Test Circuit


NETWORK ANALYZER
OSC
R(50Ω)
A(50Ω)
50Ω CABLE
TEKTRONIX P6156 500Ω PROBE
TEKTRONIX P6156 500Ω PROBE
+V_S
1 μF
0.1 μF
0.1 μF
0.1 μF
0.01 μF
V_DC
560
0.1 μF
62
0.01 μF
1 μF
-V_S
560
560
R_L

2166-11

Simplified Schematic


V+
R0
R1
R2
V1
R3
R4
R5
Q18
Q2
Q3
Q4
Q5
Q7
Q9
Q0
Q1
Q6
Q8
IN+
OUT
1.4V
Q10
Q12
DISABLE
GND
Q11
Q13
IN-
I1
Q19
Q20
Q14
Q15
Q16
Q17
R6
R7
V2
R8
R9
R10
V-

2166-12

Applications Information

Product Description

The EL2166C is a current mode feedback amplifier that offers wide bandwidth and good video specifications at a moderately low supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in industry standard pin-outs. Due to the current feedback architecture, the EL2166C closed-loop 3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3 dB bandwidth is only slightly dependent on the power supply voltage. The bandwidth reduces from 110 MHz to 95 MHz as supplies are varied from ±15V to ±5V. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼″. The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO package, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL2166C when operating in the non-inverting configuration. The characteristic curve of gain vs. frequency with variations of $C_{IN}-$ emphasizes this effect. The curve illustrates how the bandwidth can be extended over 30 MHz with some additional peaking with an additional 5 pF of capacitance at the $V_{IN}-$ pin for the case of $A_V = +2$. Higher values of capacitance will be required to obtain similar effects at higher gains.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values

The EL2166C has been designed and specified with $R_F = 560\Omega$ for $A_V = +2$. This value of feedback resistor yields relatively flat frequency response with <1.5 dB peaking out to 110 MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing R_F to 430Ω, bandwidth can be extended to 120 MHz with 4.5 dB of peaking. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature

Whereas many amplifier's supply current and consequently 3 dB bandwidth drop off at high temperature, the EL2166C was designed to have little supply current variations with temperature. An immediate benefit from this is that the 3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth only varies from 115 MHz to 95 MHz over the entire die junction temperature range of $0°C < T < 150°C$.

Applications Information — Contd.

Supply Voltage Range

The EL2166C has been designed to operate with supply voltages from ±5V to ±15V. AC performance, including −3 dB bandwidth and differential gain and phase, shows little degradation as the supplies are lowered to ±5V. For example, as supplies are lowered from ±15V to ±5V, −3 dB bandwidth reduces only 15 MHz, and differential gain and phase remain less than 0.05%/ 0.02° respectively.

If a single supply is desired, values from +10V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2166C.

Disable Function

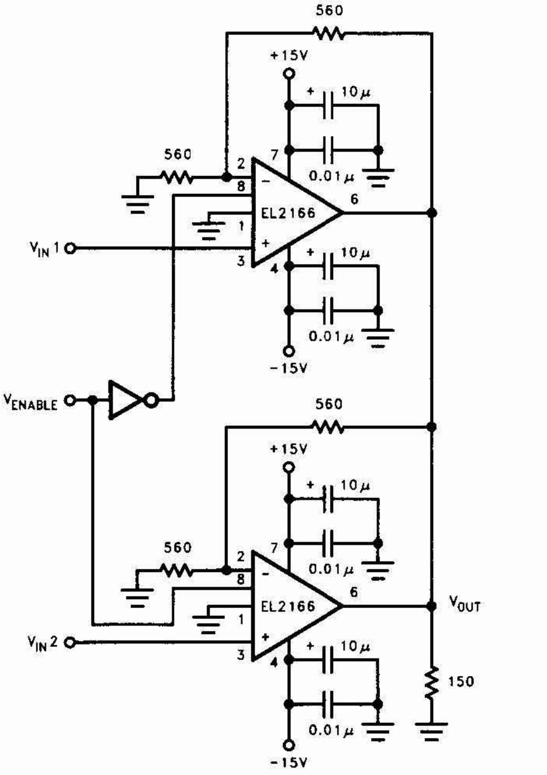
The EL2166C has a superior disable function that has been optimized for video performance. Time to disable/enable is around 75 ns.

During disable, the output of the EL2166C can withstand over 1500 V/µs slew rate signals at its output and the output does not draw excessive currents. The feed-through can be modeled as a 1.5 pF capacitor from $V_{IN}+$ to the output, and the output impedance can be modeled as 4.4 pF in parallel with 180 kΩ to ground when disabled. Consequently, multiplexing with the EL2166C is very easy. Simply tie the outputs of multiple EL2166Cs together and drive the /DISABLE pins with standard TTL or CMOS signals. The disable signal applied to the /DISABLE pin is referenced to the GND pin. The GND pin can be tied as low as the V_S- pin. This allows the EL2166C to be operated on a single supply. For example, one could tie the V_S- and GND pins to 0V and V_S+ to +10V, and then use standard TTL or CMOS to drive the /DISABLE pin. Remember to keep the inputs of the EL2166C within their common mode range.

Multiplexing with the EL2166C

An example of multiplexing with the EL2166C and its response curve is shown below. Always be sure that no more than ±5V is applied between $V_{IN}+$ and $V_{IN}-$, which is compatible with standard video signals. This usually becomes an issue only when using the disable feature and amplifying large voltages.

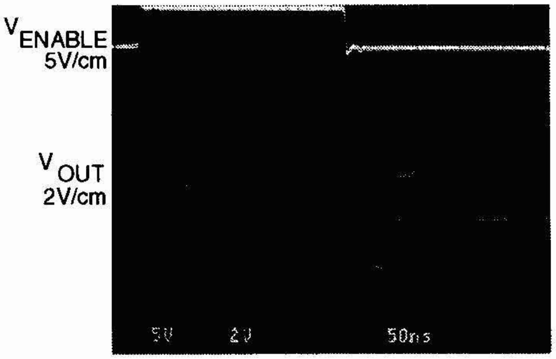
Dual EL2166C Multiplexer



2166-15

In the multiplexer above, suppose one amp is disabled and the other has amplified a signal to +10V at V_{OUT}. The voltage at pin 2 of the dis-

Dual EL2166C Multiplexer Switching 4 Vpp Uncorrelated Sinewaves to 2 Vpp Uncorrelated Sinewaves



2166-16

Applications Information — Contd.

abled amplifier will now be +5V due to the resistor divider action. Therefore, any applied voltage at pin 3 of the disabled amplifier must remain above 0V if the voltage between pins 2 and 3 of the disabled amplifier is to remain less than 5V. Also keep in mind that each disabled amplifier adds more capacitance to the bus, as discussed above. See Disable Function, and Driving Cables and Capacitive Loads in this section, and the Frequency Response for Various C_L curves in the Typical Performance Curve section.

Settling Characteristics

The EL2166C offers superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2166C is not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for $A_V = +1$, there is approximately a 0.02% residual which tails away to 0.01% in about 20 µs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For $A_V = -1$, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With $A_V = -1$, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation

The EL2166C amplifier combines both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2166C remains within its absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or

$$P_{DMAX} = 2 * V_S * I_S + (V_S - V_{OUT}) * \frac{V_{OUT}}{R_L}$$

where I_S is the supply current. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, the EL2166C maintains almost constant supply current over temperature so that AC performance is not degraded as much over the entire operating temperature range. Of course, this increase in performance doesn't come for free. Since the current has increased, supply voltages must be limited so that maximum power ratings are not exceeded.

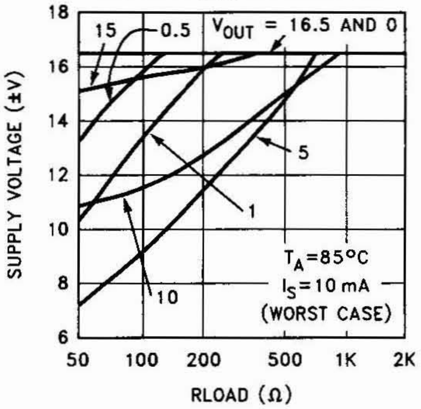
The EL2166C consumes typically 7.5 mA and maximum 10.0 mA. The worst case power in an IC occurs when the output voltage is at half supply, if it can go that far, or its maximum values if it cannot reach half supply. If we set the two P_{DMAX} equations equal to each other, and solve for V_S, we can get a family of curves for various loads and output voltages according to:

$$V_S = \frac{\dfrac{R_L * (T_{JMAX} - T_{AMAX})}{\theta_{JA}} + (V_{OUT})^2}{(2 * I_S * R_L) + V_{OUT}}$$

Applications Information — Contd.

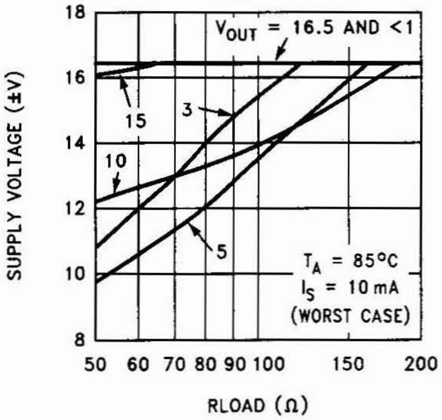
The following curves show supply voltage ($\pm V_S$) vs R_{LOAD} for various output voltage swings for the 2 different packages. The curves assume worst case conditions of $T_A = +85°C$ and $I_S = 10$ mA.

Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)



2166-13

Supply Voltage vs R_{LOAD} for Various V_{OUT} (PDIP Package)



2166-14

The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit

The EL2166C has an internal current limit that protects the circuit in the event of the output being shorted to ground. This limit is set at 80 mA nominally and reduces with junction temperature. At a junction temperature of 150°C, the current limits at about 50 mA. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2166C to survive an indefinite short.

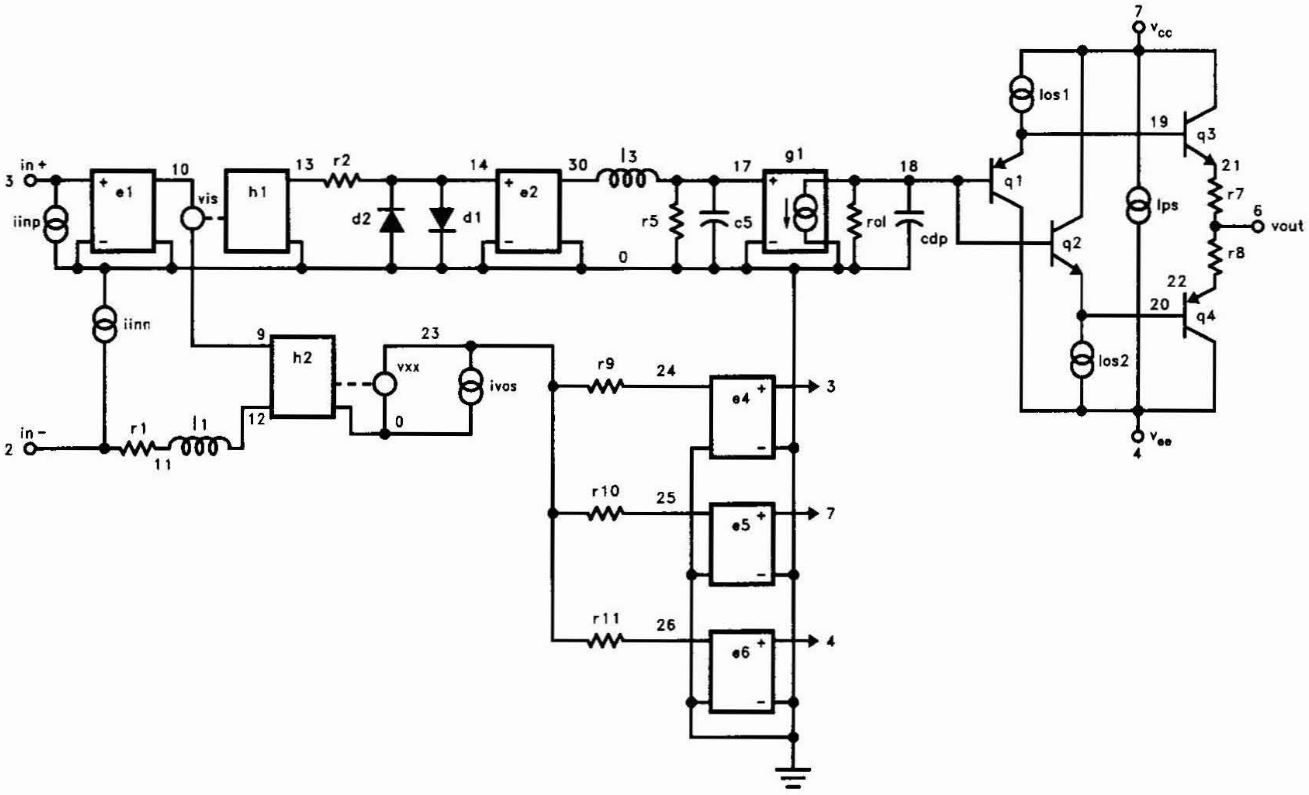
Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2166C from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistor at the output.

EL2166C Macromodel

```
* Revision A, May 1994
* AC Characteristics used CIN− (pin 2) = 1 pF; RF = 560Ω
* Connections:          +input
*                       |    −input
*                       |    |    +Vsupply
*                       |    |    |    −Vsupply
*                       |    |    |    |    output
*                       |    |    |    |    |
.subckt EL2166C/EL      3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 130
l1 11 12 25nH
iinp 3 0 0.5μA
iinm 2 0 5μA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.8μH
c5 17 0 1.25pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
ro1 18 0 2Meg
cdp 18 0 2.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2mA
ios2 20 4 2mA
*
* Supply Current
*
ips 7 4 2mA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.35K
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e−15 bf=200 tf=0.1ns)
.model qp pnp (is=5e−15 bf=200 tf=0.1ns)
.model dclamp d (is=1e−30 ibv=0.266 bv=2.8 n=4)
.ends
```

EL2166C Macromodel — Contd.


7
vcc
Ios1
19
q3
21
r7
6
vout
r8
22
20
q4
Ios2
Ips
q1
q2
vee
4
in+
3
iinp
e1
10
vis
h1
13
r2
d2
d1
14
e2
30
l3
r5
c5
17
g1
rol
18
cdp
0
iinn
9
h2
23
vxx
ivos
0
12
in−
2
r1
l1
11
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4

2166-17

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2170C/EL2270C/EL2470C

70 MHz/1 mA Current Mode Feedback Amplifiers

Features

- Single (EL2170C), dual (EL2270C) and quad (EL2470C) topologies
- 1 mA supply current (per amplifier)
- 70 MHz −3 dB bandwidth
- Tiny SOT23-5 Package (EL2170C)
- Low cost
- Single- and dual-supply operation down to ±1.5V
- 0.15%/0.15° diff. gain/diff. phase into 150Ω
- 800 V/µs slew rate
- Large output drive current:
  100 mA (EL2170C)
  55 mA (EL2270C)
  55 mA (EL2470C)
- Also available with disable in single (EL2176C) and dual (EL2276C)
- Higher speed EL2180C/EL2186C family also available (3 mA/ 250 MHz) in single, dual and quad

Applications

- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2170CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2170CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2170CW	−40°C to +85°C	5-Pin SOT23*	MDP0038
EL2270CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2270CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2470CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL2470CS	−40°C to +85°C	14-Pin SOIC	MDP0027

*See Ordering Information section of databook.

General Description

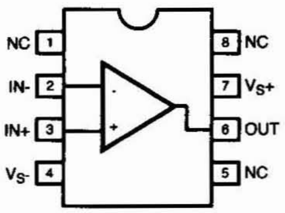
The EL2170C/EL2270C/EL2470C are single/dual/quad current-feedback operational amplifiers which achieve a −3 dB bandwidth of 70 MHz at a gain of +1 while consuming only 1 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from +3V to +12V. In spite of their low supply current, the EL2270C and the EL2470C can output 55 mA while swinging to ±4V on ±5V supplies. The EL2170C can output 100 mA with similar output swings. These attributes make the EL2170C/EL2270C/EL2470C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

For applications where board space is extremely critical, the EL2170C is available in the tiny 5-Lead SOT23 package, which has a footprint 28% the size of an 8-Lead SOIC. The EL2170C/ EL2270C/EL2470C are each also available in industry standard pinouts in PDIP and SOIC packages.

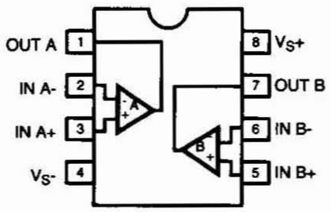
For Single and Dual applications with disable, consider the EL2176C (8-Pin Single) or EL2276C (14-Pin Dual). For higher speed applications where power is still a concern, consider the EL2180C/El2186C family which also comes in similar Single, Dual, Triple and Quad configurations. The EL2180C/EL2186C family provides a −3 dB bandwidth of 250 MHz while consuming 3 mA of supply current per amplifier.

Connection Diagrams

EL2170C SO, P-DIP

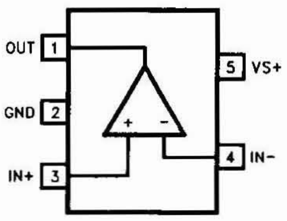


EL2270C SO, P-DIP



2170-1

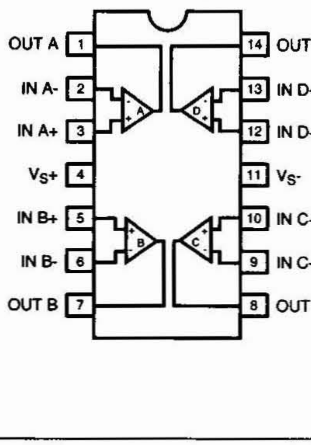
EL2170C SOT23-5



2170-46

Top View

EL2470C SO, P-DIP



2170-2

EL2170C/EL2270C/EL2470C

70 MHz/1 mA Current Mode Feedback Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_{S+} and V_{S-}	+12.6V	Operating Junction Temperature	
Common-Mode Input Voltage	V_{S-} to V_{S+}	Plastic Packages	150°C
Differential Input Voltage	±6V	Output Current (EL2170C)	±120 mA
Current into +IN or −IN	±7.5 mA	Output Current (EL2270C)	±60 mA
Internal Power Dissipation	See Curves	Output Current (EL2470C)	±60 mA
Operating Ambient Temperature Range	−40°C to +85°C	Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±5V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			2.5	15	I	mV
TCV_{OS}	Average Input Offset Voltage Drift	Measured from T_{MIN} to T_{MAX}		5		V	μV/°C
dV_{OS}	V_{OS} Matching	EL2270C, EL2470C only		0.5		V	mV
$+I_{IN}$	+ Input Current			0.5	5	I	μA
$d+I_{IN}$	$+I_{IN}$ Matching	EL2270C, EL2470C only		20		V	nA
$-I_{IN}$	− Input Current			4	15	I	μA
$d-I_{IN}$	$-I_{IN}$ Matching	EL2270C, EL2470C only		1.5		V	μA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	45	50		I	dB
−ICMR	− Input Current Common Mode Rejection	V_{CM} = ±3.5V		4	10	I	μA/V
PSRR	Power Supply Rejection Ratio	V_S is moved from ±4V to ±6V	60	70		I	dB
−IPSR	− Input Current Power Supply Rejection	V_S is moved from ±4V to ±6V		0.5	5	I	μA/V
R_{OL}	Transimpedance	V_{OUT} = ±2.5V	150	400		I	kΩ
$+R_{IN}$	+ Input Resistance	V_{CM} = ±3.5V	1	4		I	MΩ
$+C_{IN}$	+ Input Capacitance			1.2		V	pF
CMIR	Common Mode Input Range		±3.5	±4.0		I	V

DC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	$V_S = \pm 5$	±3.5	±4.0		I	V
		$V_S = +5$ Single-Supply, High		4.0		V	V
		$V_S = +5$ Single-Supply, Low		0.3		V	V
I_O	Output Current	EL2170C only	80	100		I	mA
		EL2270C only, per Amplifier	50	55		I	mA
		EL2470C only, per Amplifier	50	55		I	mA
I_S	Supply Current	Per Amplifier		1	2	I	mA

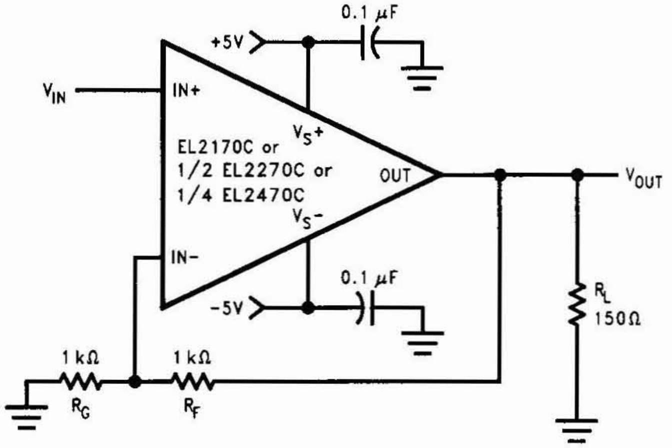
AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = R_G = 1\ k\Omega$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
−3 dB BW	−3 dB Bandwidth	$A_V = +1$		70		V	MHz
−3 dB BW	−3 dB Bandwidth	$A_V = +2$		60		V	MHz
SR	Slew Rate	$V_{OUT} = \pm 2.5V$, $A_V = +2$	400	800		IV	V/µs
t_r, t_f	Rise and Fall Time	$V_{OUT} = \pm 500$ mV		4.5		V	ns
t_{pd}	Propagation Delay	$V_{OUT} = \pm 500$ mV		4.5		V	ns
OS	Overshoot	$V_{OUT} = \pm 500$ mV		3.0		V	%
t_s	0.1% Settling	$V_{OUT} = \pm 2.5V$, $A_V = -1$		40		V	ns
dG	Differential Gain	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.15		V	%
dP	Differential Phase	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.15		V	°
dG	Differential Gain	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.02		V	%
dP	Differential Phase	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.01		V	°
C_S	Channel Separation	EL2270C, EL2470C only, f = 5 MHz		85		V	dB

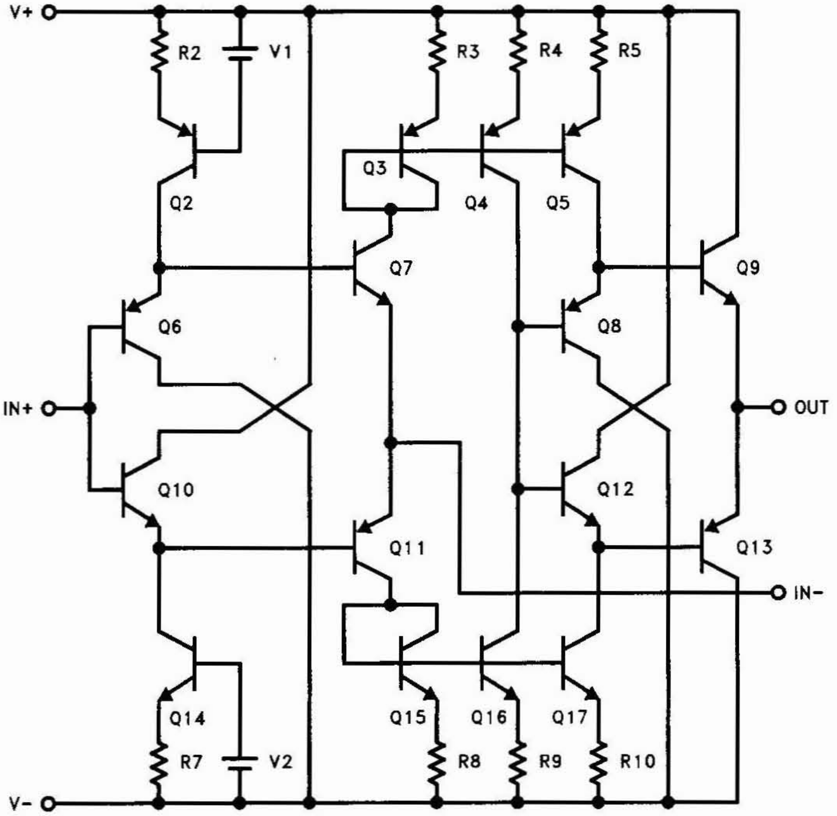
Note 1: DC offset from 0V to 0.714V, AC amplitude 286 $mV_{P\text{-}P}$, f = 3.58 MHz.

Test Circuit (per Amplifier)


V_{IN}
IN+
+5V
0.1 μF
EL2170C or
1/2 EL2270C or
1/4 EL2470C
V_S+
OUT
V_S-
IN-
-5V
0.1 μF
V_{OUT}
R_L
150Ω
1 kΩ
R_G
1 kΩ
R_F

2170-3

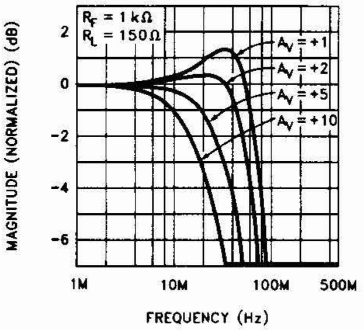
Simplified Schematic (per Amplifer)


V+
R2
V1
R3
R4
R5
Q2
Q3
Q4
Q5
Q7
Q9
Q6
Q8
IN+
OUT
Q10
Q12
Q11
Q13
IN-
Q14
Q15
Q16
Q17
R7
V2
R8
R9
R10
V-

2170-4

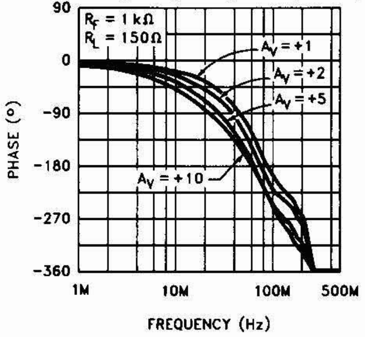
Typical Performance Curves

Non-Inverting Frequency Response (Gain)



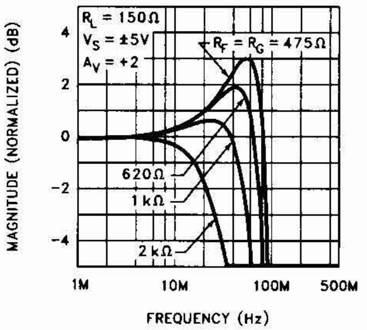
2170-5

Non-Inverting Frequency Response (Phase)



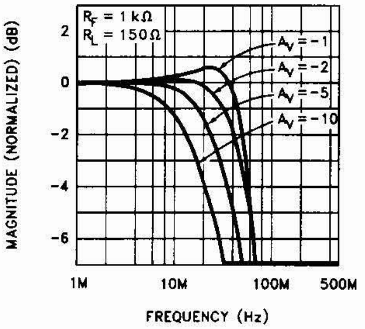
2170-6

Frequency Response for Various R_F and R_G



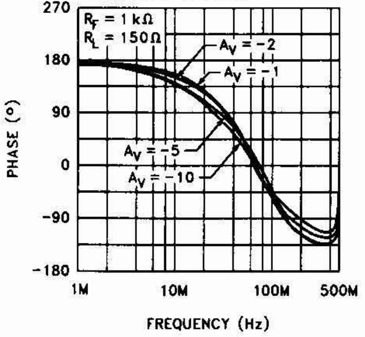
2170-7

Inverting Frequency Response (Gain)



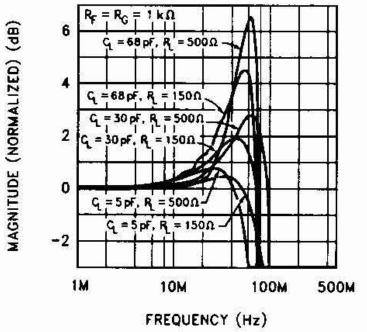
2170-8

Inverting Frequency Response (Phase)



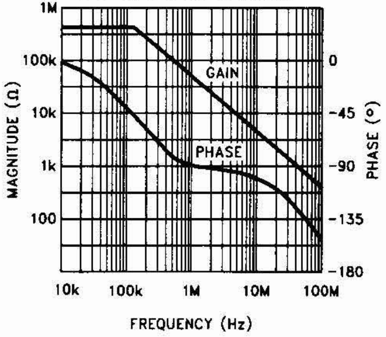
2170-9

Frequency Response for Various R_L and C_L



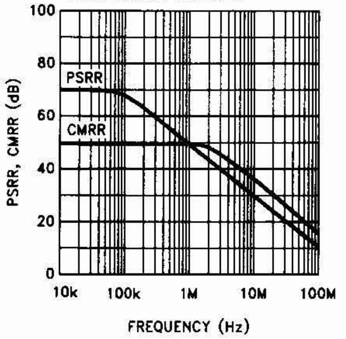
2170-10

Transimpedance (R_{OL})



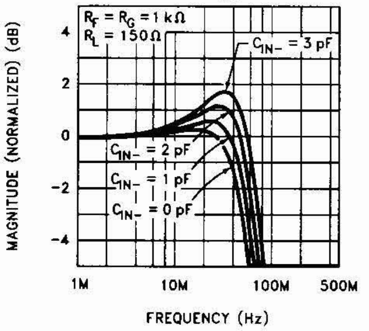
2170-11

PSRR and CMRR



2170-12

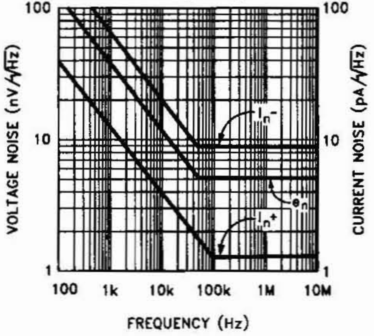
Frequency Response for Various C_{IN-}



2170-13

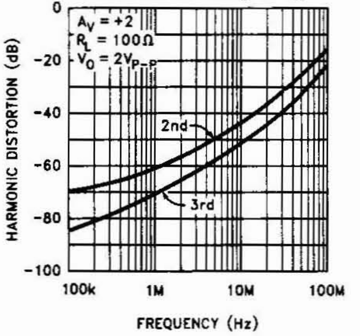
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency



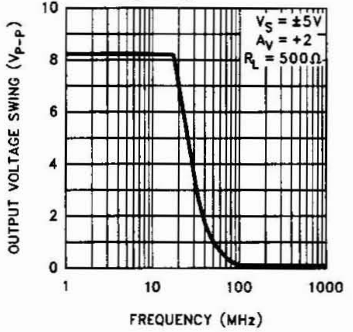
2170-14

2nd and 3rd Harmonic Distortion vs Frequency



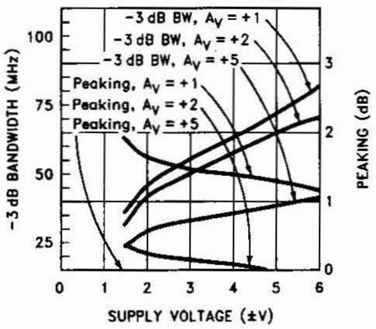
2170-15

Output Voltage vs Frequency



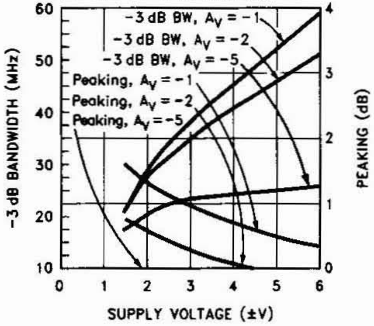
2170-16

−3 dB Bandwith and Peaking vs Supply Voltage for Various Non-Inverting Gains



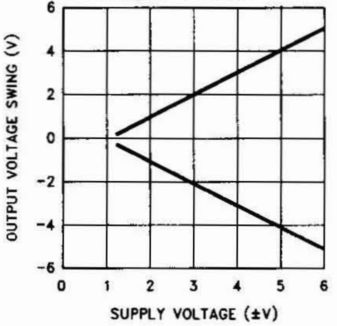
2170-17

−3 dB Bandwith and Peaking vs Supply Voltage for Various Inverting Gains



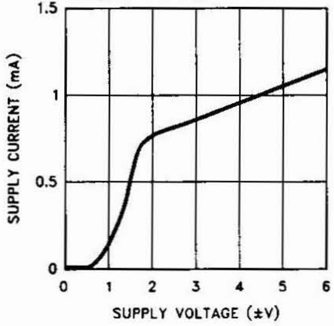
2170-18

Output Voltage Swing vs Supply Voltage



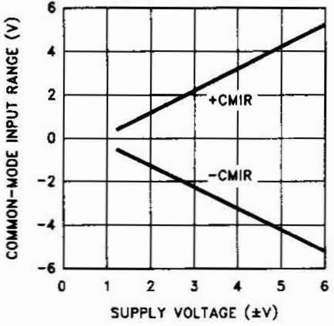
2170-19

Supply Current vs Supply Voltage



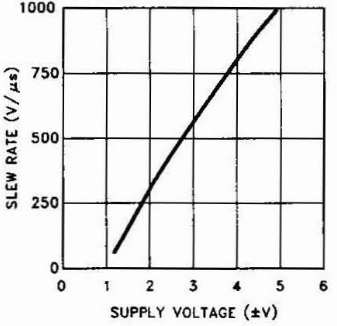
2170-20

Common-Mode Input Range vs Supply Voltage



2170-21

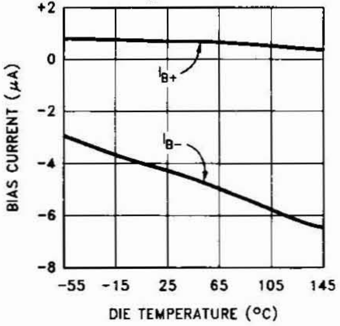
Slew Rate vs Supply Voltage



2170-22

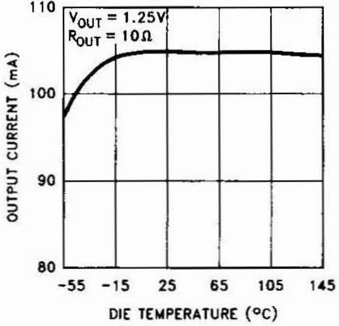
Typical Performance Curves — Contd.

Input Bias Current vs Die Temperature



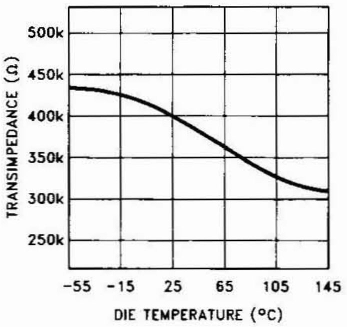
2170-23

Short-Circuit Current vs Die Temperature



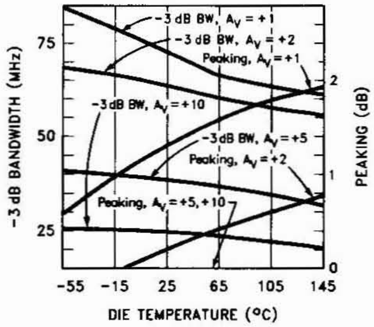
2170-24

Transimpedance (R_{OL}) vs Die Temperature



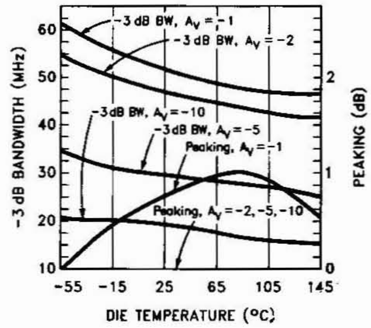
2170-25

−3 dB Bandwith and Peaking vs Die Temperature for Various Non-Inverting Gains



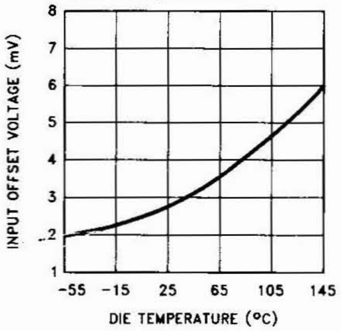
2170-26

−3 dB Bandwith and Peaking vs Die Temperature for Various Inverting Gains



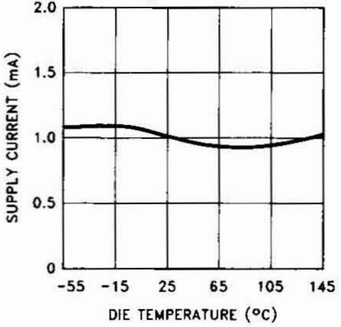
2170-27

Input Offset Voltage vs Die Temperature



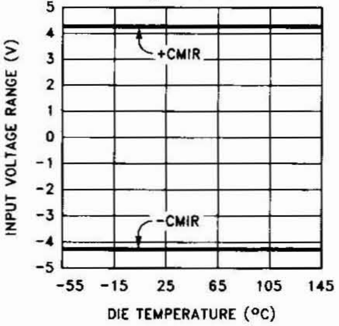
2170-28

Supply Current vs Die Temperature



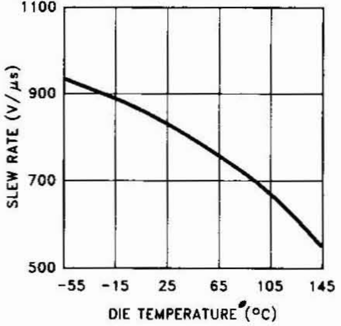
2170-29

Input Voltage Range vs Die Temperature



2170-30

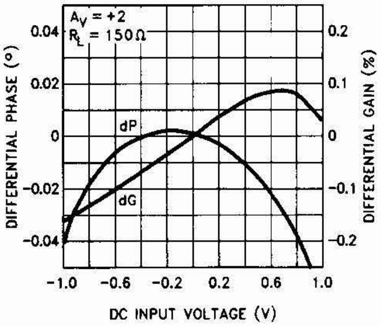
Slew Rate vs Die Temperature



2170-31

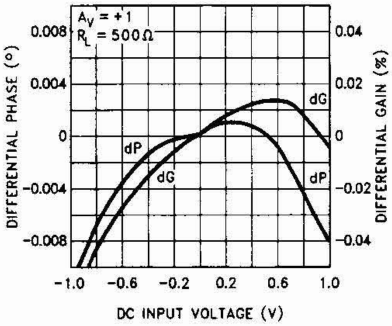
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz/A_V = +2



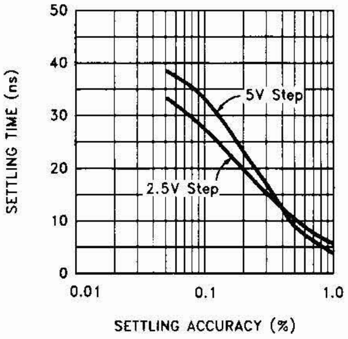
2170-32

Differential Gain and Phase vs DC Input Offset at 3.58 MHz/A_V = +1



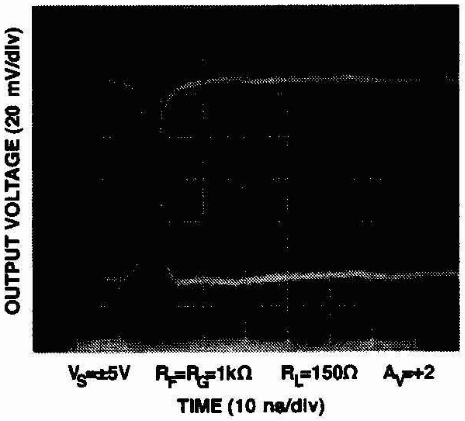
2170-33

Settling Time vs Settling Accuracy



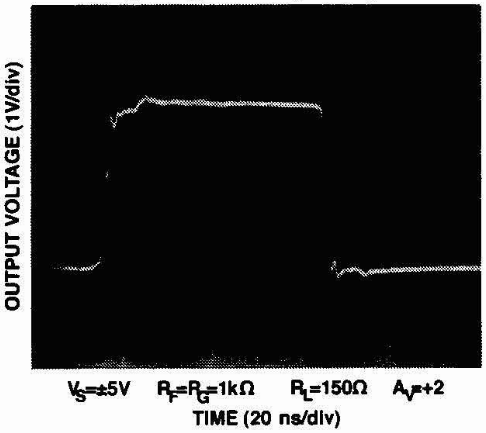
2170-34

Small-Signal Step Response



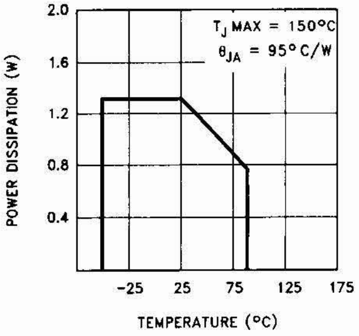
2170-35

Large-Signal Step Response



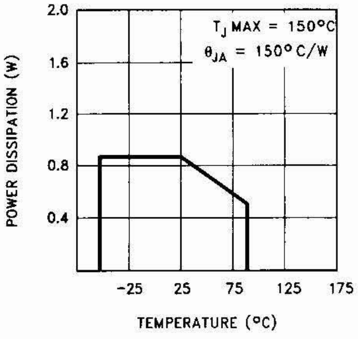
2170-36

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2170-37

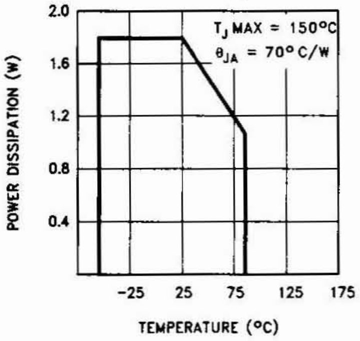
8-Lead SO Maximum Power Dissipation vs Ambient Temperature



2170-38

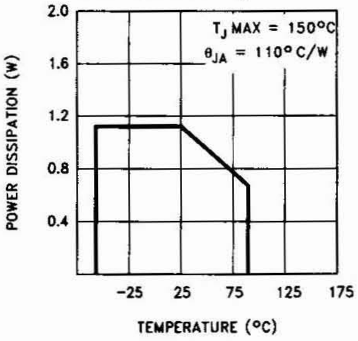
Typical Performance Curves — Contd.

14-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



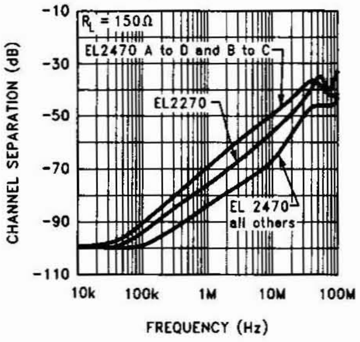
2170-39

14-Lead SO Maximum Power Dissipation vs Ambient Temperature



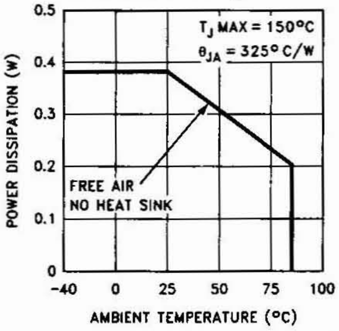
2170-40

Channel Separation vs Frequency



2170-41

5-Lead Plastic SOT23 Maximum Power Dissipation vs Ambient Temperature



2170-47

Applications Information

Product Description

The EL2170C/EL2270C/EL2470C are current-feedback operational amplifiers that offer a wide −3 dB bandwidth of 70 MHz and a low supply current of 1 mA per amplifier. All of these products also feature high output current drive. The EL2170C can output 100 mA, while the EL2270C and the EL2470C can output 55 mA per amplifier. The EL2170C/EL2270C/EL2470C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to within 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2170C/EL2270C/EL2470C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their −3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2170C/EL2270C/EL2470C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For applications where board space is extremely critical, the EL2170C is available in the tiny 5-Lead SOT23 package, which has a footprint 28% the size of an 8-Lead SOIC. The EL2170C/EL2270C/EL2470C are each also available in industry standard pinouts in PDIP and SOIC packages.

For Single and Dual applications with disable, consider the EL2176C (8-Pin Single) and EL2276C (14-Pin Dual). If higher speed is required, refer to the EL2180C/EL2186C family which provides Singles, Duals, Triples, and Quads with 250 MHz of bandwidth while consuming 3 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.

Applications Information — Contd.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2170C/EL2270C/EL2470C have less bandwidth than expected. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e. g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various R_F and R_G, and Frequency Response for Various C_{IN-}.

Feedback Resistor Values

The EL2170C/EL2270C/EL2470C have been designed and specified at gains of +1 and +2 with $R_F = 1\ k\Omega$. This value of feedback resistor gives 70 MHz of −3 dB bandwidth at $A_V = +1$ with about 1.5 dB of peaking, and 60 MHz of −3 dB bandwidth at $A_V = +2$ with about 0.5 dB of peaking. Since the EL2170C/EL2270C/EL2470C are current-feedback amplifiers, it is also possible to change the value of R_F to get more bandwidth. As seen in the curve of Frequency Response For Various R_F and R_G, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2170C/EL2270C/EL2470C are current-feedback amplifiers, their gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2170C/EL2270C/EL2470C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases. Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of R_F below the specified 1 kΩ and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2170C/EL2270C/EL2470C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2170C/EL2270C/EL2470C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2170C/EL2270C/EL2470C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2170C/EL2270C/EL2470C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2170C/EL2270C/EL2470C have an input range which spans from 1V to 4V. The output range of the EL2170C/EL2270C/EL2470C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2170C/EL2270C/EL2470C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically more than the entire 1 mA supply current of each EL2170C/EL2270C/EL2470C amplifier! Special circuitry has been incorporated in the EL2170C/EL2270C/EL2470C to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.15% and 0.15° while driving 150Ω at a gain of +2.

Applications Information — Contd.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2170C/EL2270C/EL2470C have dG and dP specifications of 0.01% and 0.02° respectively while driving 500 Ω at $A_V = +1$.

Output Drive Capability

In spite of its low 1 mA of supply current, the EL2170C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2270C and the EL2470C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2170C is capable of driving 50Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2270C and EL2470C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2170C/EL2270C/EL2470C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (R_F) to reduce the peaking.

Current Limiting

The EL2170C/EL2270C/EL2470C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2170C/EL2270C/EL2470C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when R_L falls below about 25Ω, it is important to calculate the maximum junction temperature (T_{JMAX}) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2170C/EL2270C/EL2470C to remain in the safe operating area. These parameters are calculated as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} * n * PD_{MAX}) \qquad [1]$$

where:

T_{MAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
n = Number of Amplifiers in the Package
PD_{MAX} = Maximum Power Dissipation of Each Amplifier in the Package.

PD_{MAX} for each amplifier can be calculated as follows:

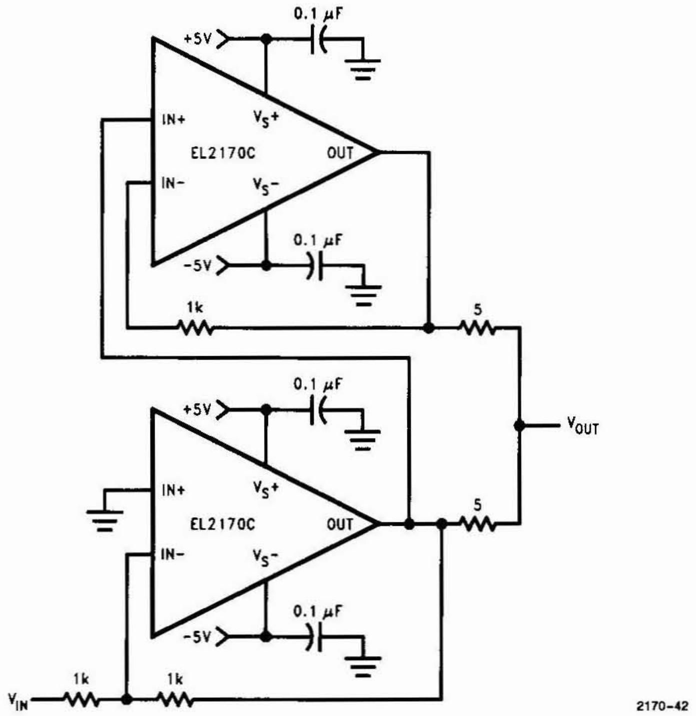
$$PD_{MAX} = (2 * V_S * I_{SMAX}) + (V_S - V_{OUTMAX}) * (V_{OUTMAX}/R_L)) \qquad [2]$$

where:

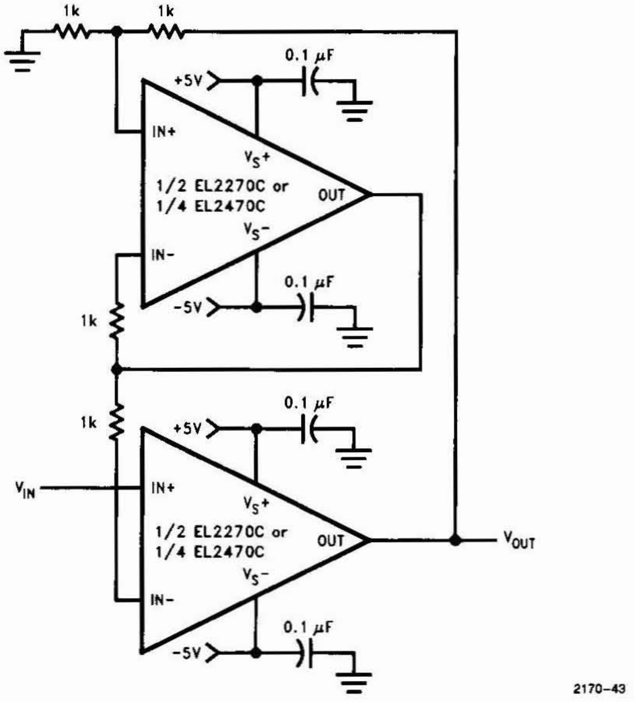
V_S = Supply Voltage
I_{SMAX} = Maximum Supply Current of 1 Amplifier
V_{OUTMAX} = Max. Output Voltage of the Application
R_L = Load Resistance

Typical Application Circuits

Inverting 200 mA Output Current Distribution Amplifier

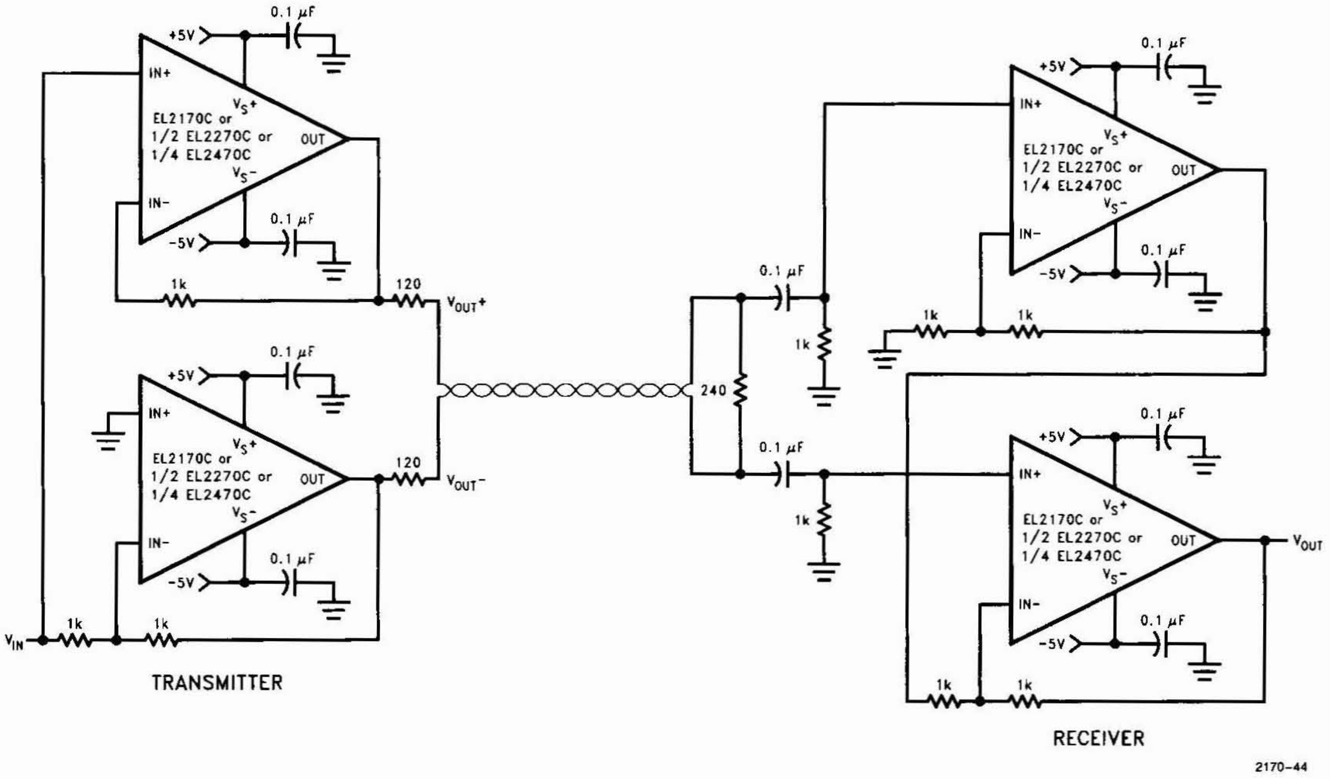

+5V
0.1 µF
IN+
V_S+
EL2170C
OUT
IN−
V_S−
−5V
0.1 µF
1k
5
V_{OUT}
+5V
0.1 µF
IN+
V_S+
EL2170C
OUT
IN−
V_S−
5
−5V
0.1 µF
V_{IN}
1k
1k
2170-42

Fast-Settling Precision Amplifier


1k
1k
0.1 µF
+5V
IN+
V_S+
1/2 EL2270C or
1/4 EL2470C
OUT
V_S−
IN−
0.1 µF
−5V
1k
1k
0.1 µF
+5V
V_{IN}
IN+
V_S+
1/2 EL2270C or
1/4 EL2470C
OUT
V_{OUT}
V_S−
IN−
0.1 µF
−5V
2170-43

Typical Application Circuits — Contd.

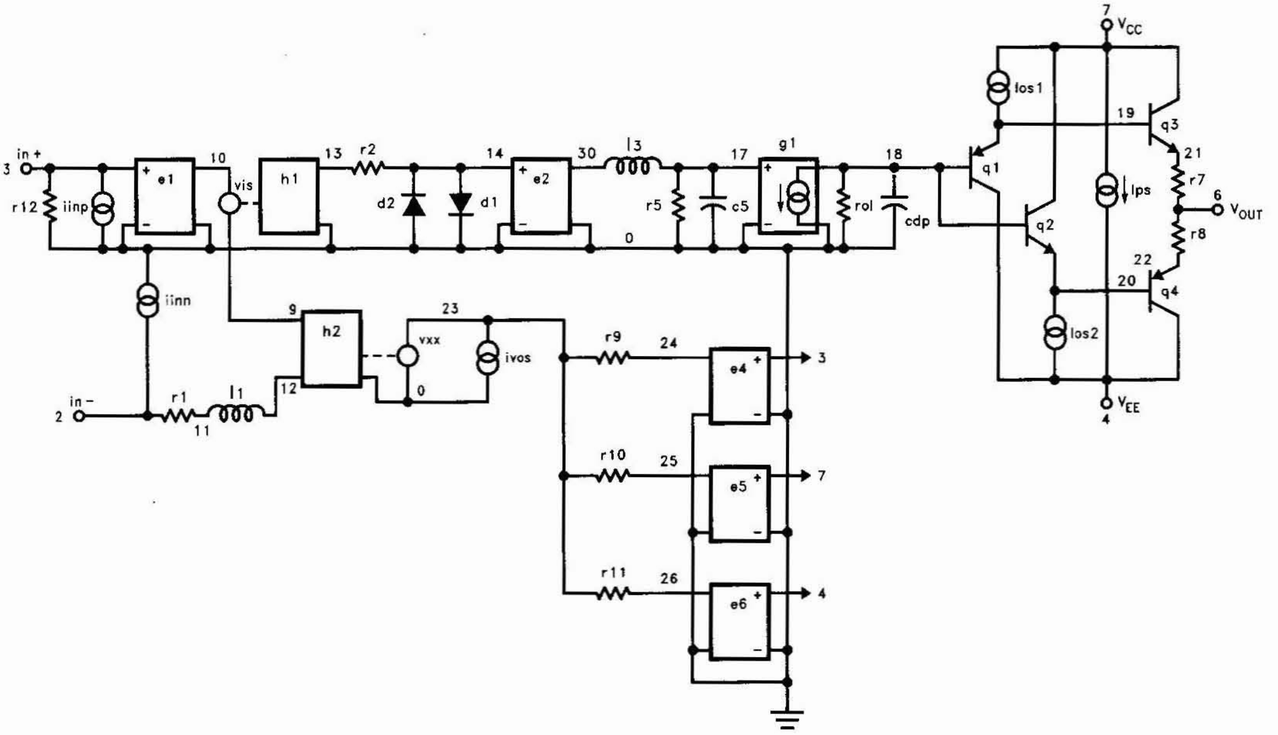
Differential Line-Driver/Receiver


+5V
0.1 µF
IN+
V_S+
EL2170C or
1/2 EL2270C or
1/4 EL2470C
OUT
V_S-
IN−
−5V
1k
120
$V_{OUT}+$
$V_{OUT}-$
240
V_{IN}
TRANSMITTER
RECEIVER
V_{OUT}
2170-44

EL2170C/EL2270C/EL2470C Macromodel

```
* Revision A, March 1995
* AC characteristics used Rf=Rg=1KΩ, RL=150Ω
* Connections:       +input
*                      |    -input
*                      |     |    +Vsupply
*                      |     |     |    -Vsupply
*                      |     |     |     |    output
*                      |     |     |     |     |
.subckt EL2170/el      3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 165
l1 11 12 25nH
iinp 3 0 0.5uA
iinm 2 0 4uA
r12 3 0 4Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 0.5uH
c5 17 0 0.69pF
r5 17 0 300
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 400K
cdp 18 0 1.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 0.4mA
ios2 20 4 0.4mA
*
* Supply Current
*
ips 7 4 1nA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 -1.0
r9 24 23 0.316K
r10 25 23 3.2K
r11 26 23 3.2K
*
* Models
*
.model qn npn(is=5e-15 bf=200 tf=0.01nS)
.model qp pnp(is=5e-15 bf=200 tf=0.01nS)
.model dclamp d(is=1e-30 ibv=0.266
+ bv=1.3v n=4)
.ends
```

EL2170C/EL2270C/EL2470C Macromodel — Contd.


in+
3
r12
iinp
e1
10
vis
h1
13
r2
d2
d1
14
e2
30
l3
17
r5
c5
g1
rol
18
cdp
0
iinn
9
h2
23
vxx
ivos
0
12
in−
2
r1
l1
11
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4
7
VCC
Ios1
19
q3
q1
21
r7
q2
Ips
6
VOUT
r8
22
20
q4
Ios2
VEE
4

2170-45

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2175C

120 MHz Precision Current Mode Feedback Amplifier

Features

- 30 MΩ transimpedance
- 142 MHz − 3 dB bandwidth (A_V = +1)
- 120 MHz − 3 dB bandwidth (A_V = +2)
- 1 mV input offset voltage
- 2 μA negative input bias current
- 86 dB common-mode rejection ratio
- 92 dB power supply rejection ratio
- Low supply current, 8.5 mA
- Wide supply range, ±4.5V to ±16.5V
- 80 mA peak output current
- High capacitive load toleration
- Input/output compliance to ±2V of supplies
- 1,000 V/μs slew rate
- 50 ns settling to 0.1%
- 90 ns settling to 0.01%
- −70 dB distortion @ 4 MHz
- Low cost

Applications

- Instrumentation circuitry
- Current to voltage convertors
- RGB amplifiers
- DAC/ADC output amplifier/buffer
- Cable drivers
- Low distortion communications
- Medical imaging
- CCD imaging
- Infrared image enhancement

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2175CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2175CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

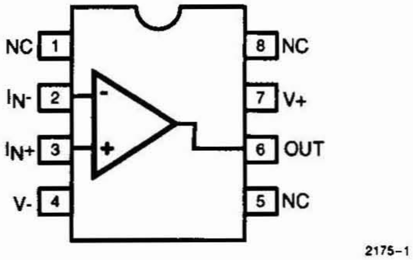
The EL2175C is a low offset, high transimpedance current mode feedback amplifier with a −3 dB bandwidth of 120 MHz at a gain of +2. Built on Elantec's proprietary monolithic complementary bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a give gain than conventional voltage feedback amplifiers.

The high 30 MΩ transimpedance gain and low input referred offset of the EL2175 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

In addition, the common-mode and power supply rejection have been greatly improved over earlier current mode feedback amplifiers and the input offset voltage and current have been trimmed to rival that of good conventional voltage feedback amplifiers. The part has a typical slew rate of 1,000 V/μs and a 0.01% settling time of less than 90 ns in inverting mode. At a gain of +2 and an output signal level of 2 V_{P-P} the total harmonic distortion is only −70 dB at 4 MHz.

The amplifier can operate on any supply from 9V (±4.5V) to 33V (±16.5V), yet consumes only 8.5 mA at any supply voltage. Using the industry standard pinout, the EL2175C is available in both P-DIP and SO packages.

Connection Diagram



Manufactured under U.S. Patent No. 5,418,495

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+33V	Operating Junction Temperature	
Voltage between I_N+ and I_N-	±6V	Plastic Package	150°C
Current into I_N+ and I_N-	4 mA	Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	See Curves		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 500Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		25°C		1	3	I	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		2		V	μV/°C
$I_{IN}+$	+ Input Current		25°C		−2.5	±6	I	μA
$I_{IN}-$	− Input Current		25°C		±2	±7	I	μA
CMRR	Common Mode Rejection Ratio (Note 2)		25°C	79	86		II	dB
ICMR−	−Input Current Common Mode Rejection (Note 2)		25°C		27	100	I	nA/V
PSRR	Power Supply Rejection Ratio (Note 3)		25°C	84	92		II	dB
IPSR−	−Input Current Power Supply Rejection (Note 3)		25°C		28	225	I	nA/V
R_{OL}	Transimpedance (Note 4)	V_S = ±15V R_L = 500Ω	25°C		30		I	MΩ
		V_S = ±5V R_L = 150Ω	25°C	5	25		I	MΩ
$R_{IN}+$	+ Input Resistance		25°C	18	25		II	MΩ
$C_{IN}+$	+ Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range (Note 2)	V_S = ±15V	25°C	±12	±12.5		I	V
		V_S = ±5V	25°C	±2.0	±2.5		I	V

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 500Ω, T_A = 25°C unless otherwise specified — Contd.

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Levels	Units
V_O	Output Voltage Swing	R_L = 500Ω V_S = ±15V	25°C	±12, 3	±13		I	I
		R_L = 150Ω V_S = ±15V	25°C		±11.7		V	V
		R_L = 150Ω V_S = ±5V	25°C	±2.7	±3.0		I	I
I_{SC}	Output Short Circuit Current (Note 4)	V_S = ±5V V_S = ±15V	25°C	55 80	90 135		I	mA
I_S	Supply Current	V_S = ±15V	25°C		8.5	10.25	I	mA

Closed Loop AC Electrical Characteristics

V_S = ±15V, A_V = +2, R_F = 750Ω, R_L = 500Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
BW	−3 dB (Note 8) BDWH	V_S = ±15V, A_V = +2, R_F = 750Ω		120		V	MHz
		V_S = ±15V, A_V = +1, R_F = 1KΩ		142		V	MHz
		V_S = ±5V, A_V = +2, R_F = 750Ω		98		V	MHz
		V_S = ±5V, A_V = +1, R_F = 1KΩ		113		V	MHz
SR	Slew Rate (Notes 6, 8)	R_L = 500Ω	500	1000		I	V/μs
		R_F = 1 KΩ, R_G = 110Ω R_L = 500Ω		1000		V	V/μs
t_r, t_f	Rise Time, Fall Time (Note 8)	V_{OUT} = ±500 mV		3.7		V	ns
t_{pd}	Propagation Delay			7.7		V	ns
O_S	Overshoot (Note 8)	V_{OUT} = ±500 mV		6		V	%
t_s	0.1% Settling Time (Note 8)	ΔV_{OUT} = ±10V A_V = 1		70		V	ns
		A_V = −1		50			
		A_V = 2		60			
t_s	0.01% Settling Time	ΔV_{OUT} = ±10V A_V = 1		900		V	ns
		A_V = −1		90			
		A_V = 2		500			
dG	Differential Gain (Notes 7, 8)	R_L = 150Ω		0.09		V	%
		R_L = 500Ω		0.02		V	%
dP	Differential Phase (Notes 7, 8)	R_L = 150Ω		0.5		V	deg (°)
		R_L = 500Ω		0.16		V	deg (°)

Note 1: Measured from T_{MIN} to T_{MAX}

Note 2: V_{CM} = ±12V for V_S = ±15V and T_A = 25°C
V_{CM} = ±2V for V_S = ±5V and T_A = 25°C
CMIR is guaranteed by the part passing CMRR at the rated common-mode swing.

Note 3: The supplies are moved from ±4.5V to ±15V.

Note 4: V_{OUT} = ±10V for V_S = ±15V, and V_{OUT} = ±2V for V_S = ±5V.

Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.

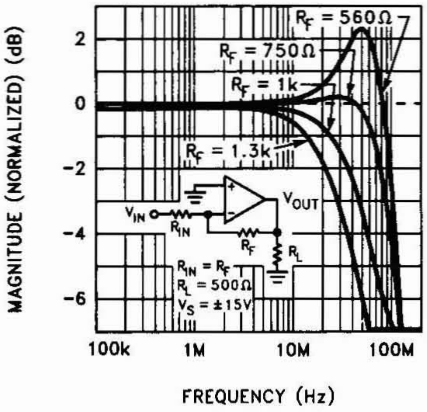
Note 6: Slew Rate is with V_{OUT} from +10V to −10V and measured at the 25% and 75% points.

Note 7: DC offset from −0.714V through +0.714V, AC amplitude 286 mV_{p-p}, f = 3.58 MHz.

Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

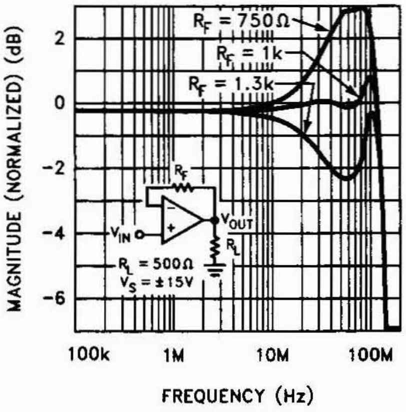
Typical Performance Curves

Frequency Response for $A_V = -1$ and for Various R_F Values



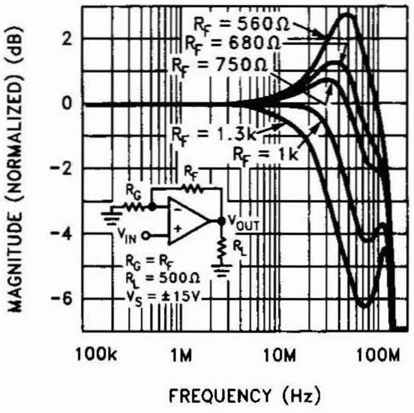
2175-2

Frequency Response for $A_V = +1$ and for Various R_F Values



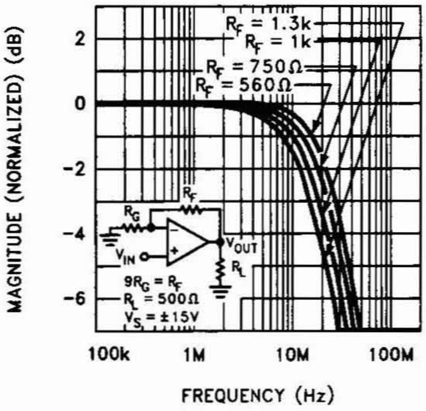
2175-3

Frequency Response for $A_V = +2$ and for Various R_F Values



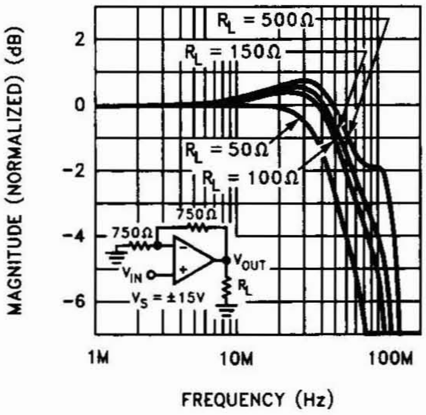
2175-4

Frequency Response for $A_V = +10$ and for Various R_F Values



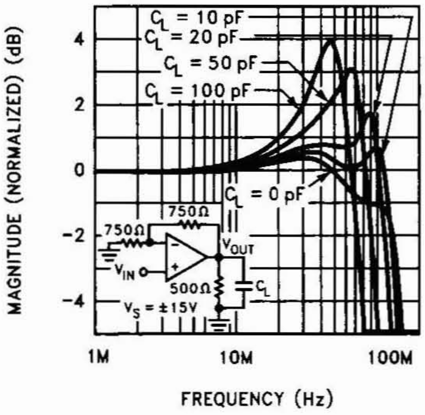
2175-5

Frequency Response for Various Values of R_L



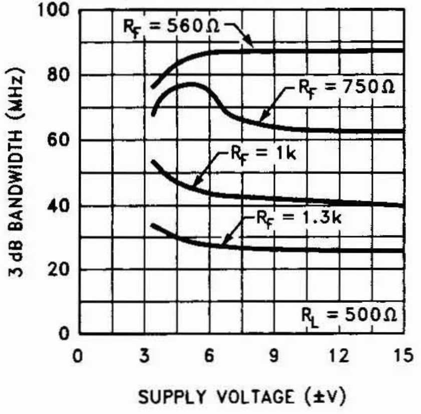
2175-6

Frequency Response for Various Values of C_L



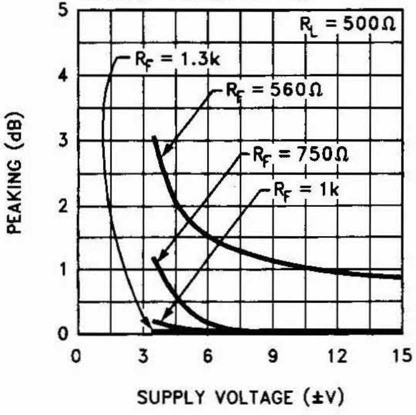
2175-7

3 dB Bandwidth vs Supply Voltage for $A_V = -1$



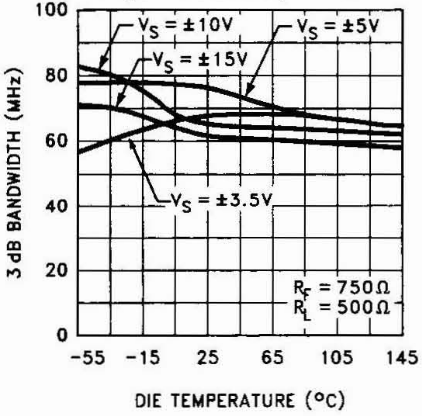
2175-8

Peaking vs Supply Voltage for $A_V = -1$



2175-9

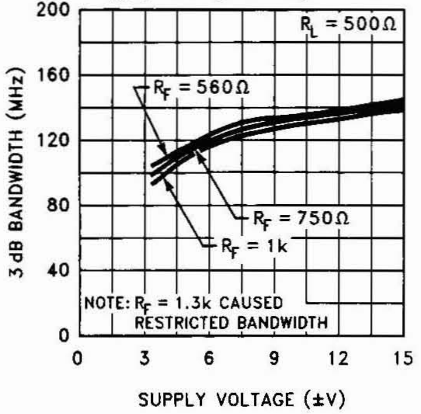
3 dB Bandwidth vs Temperature for $A_V = -1$



2175-10

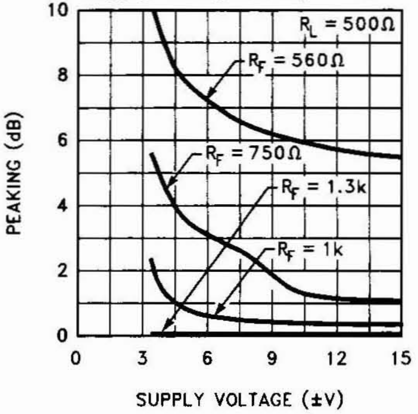
Typical Performance Curves — Contd.

3 dB Bandwidth vs Supply Voltage for $A_V = +1$



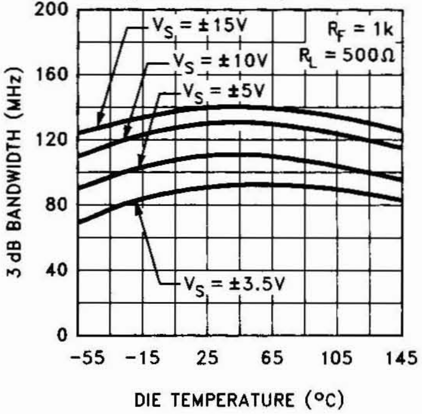
2175-11

Peaking vs Supply Voltage for $A_V = +1$



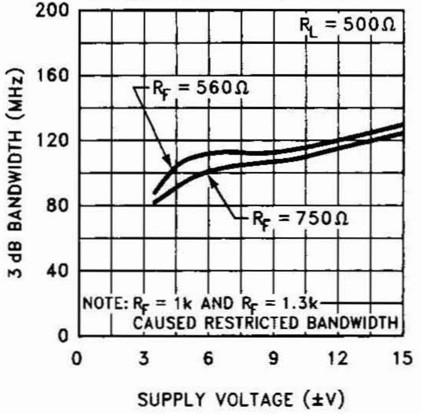
2175-12

3 dB Bandwidth vs Temperature for $A_V = +1$



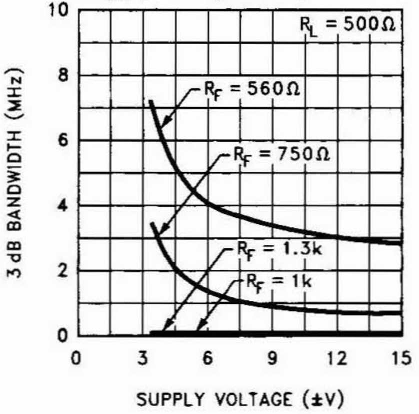
2175-13

3 dB Bandwidth vs Temperature for $A_V = +2$



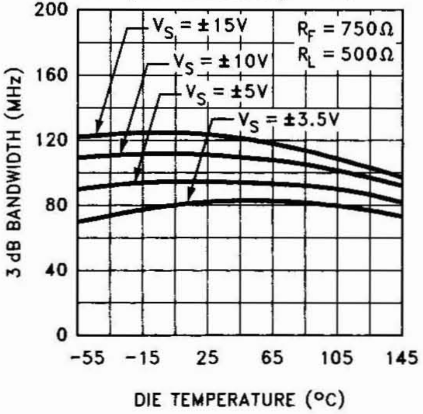
2175-14

Peaking vs Supply Voltage for $A_V = +2$



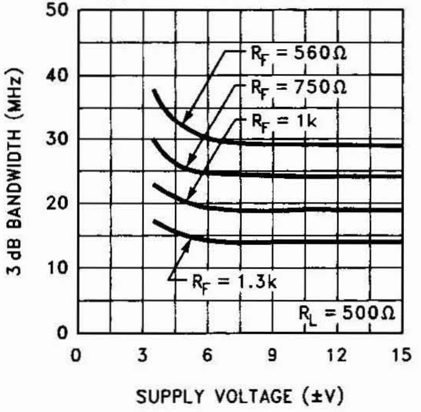
2175-15

3 dB Bandwidth vs Temperature for $A_V = +2$



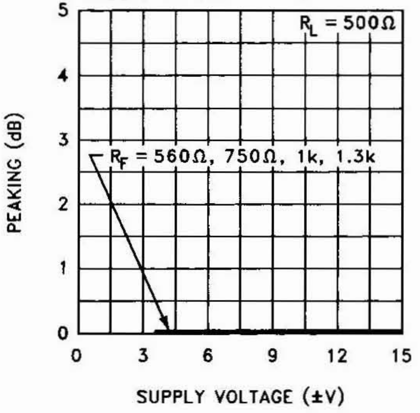
2175-16

3 dB Bandwidth vs Supply Voltage for $A_V = +10$



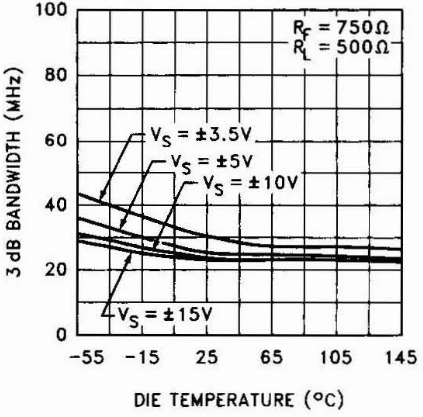
2175-17

Peaking vs Supply Voltage for $A_V = +10$



2175-18

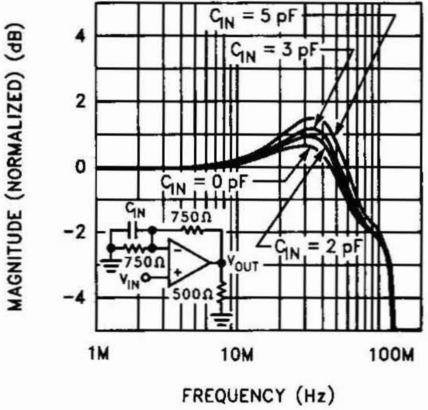
3 dB Bandwidth vs Temperature for $A_V = +10$



2175-19

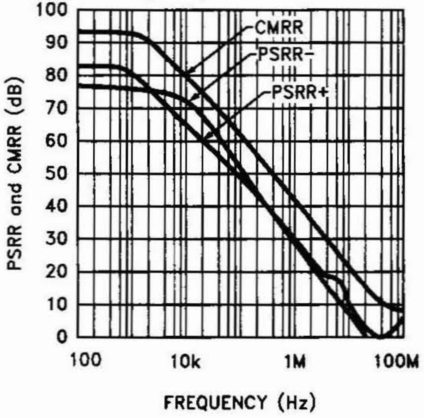
Typical Performance Curves — Contd.

Frequency Response for Various Values of C_{IN}



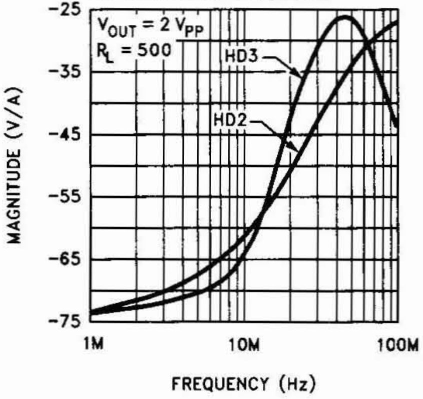
2175-20

PSRR and CMRR vs Frequency



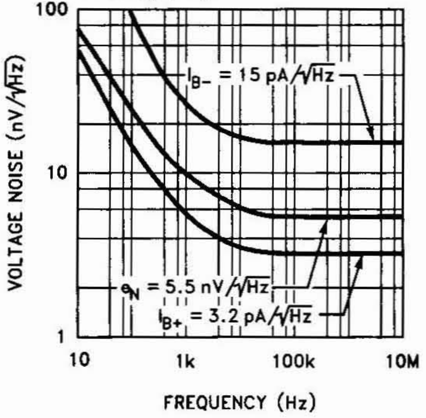
2175-21

Second and Third Harmonic Distortion vs Frequency



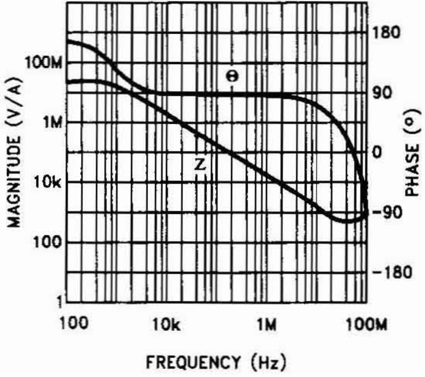
2175-45

Voltage and Current Noise vs Frequency



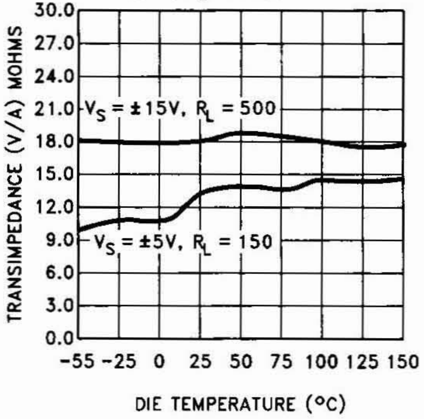
2175-22

Transimpedance (R_{OL}) vs Frequency



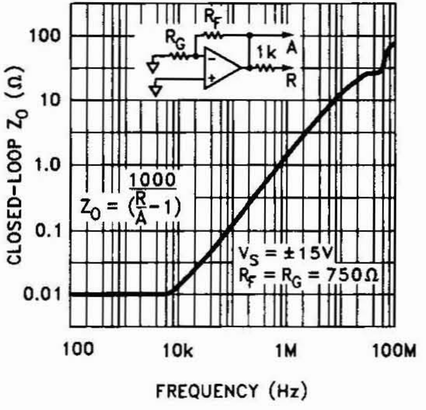
2175-23

Transimpedance (R_{OL}) vs Die Temperature



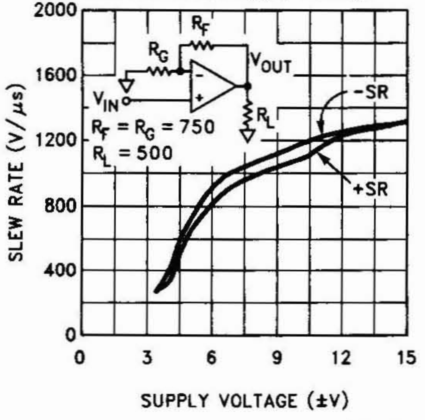
2175-24

Closed-Loop Output Impedance vs Frequency



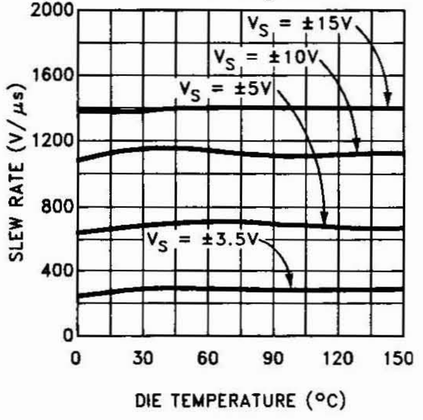
2175-25

Slew Rate vs Supply Voltage



2175-26

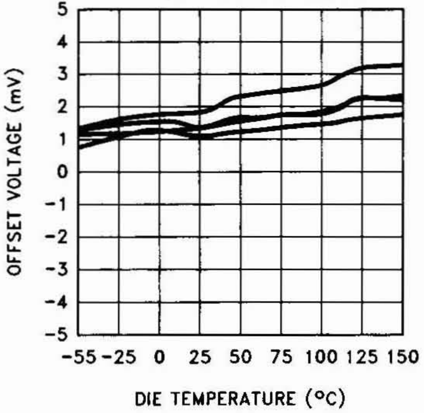
Slew Rate vs Temperature



2175-27

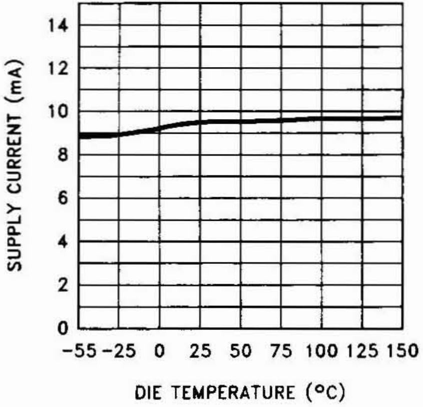
Typical Performance Curves — Contd.

Offset Voltage vs Die Temperature (4 Samples)



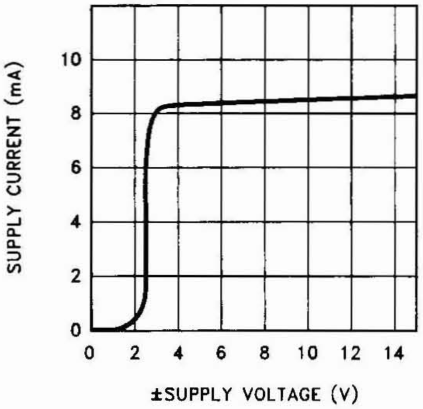
2175-28

Supply Current vs Die Temperature



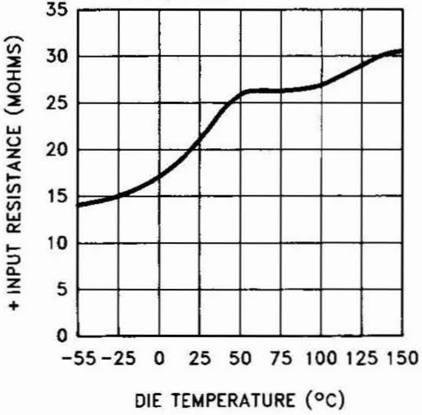
2175-29

Supply Current vs Supply Voltage



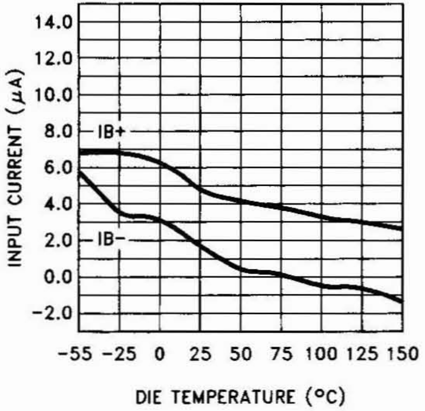
2175-30

+Input Resistance vs Die Temperature



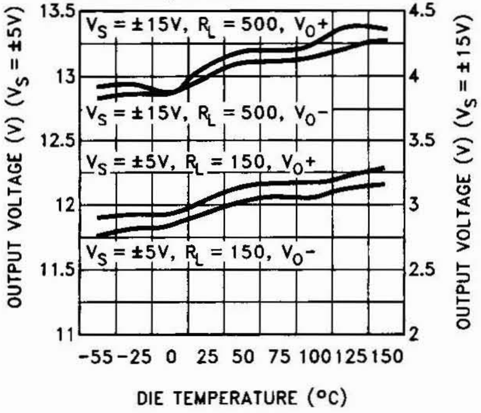
2175-31

Input Current vs Die Temperature



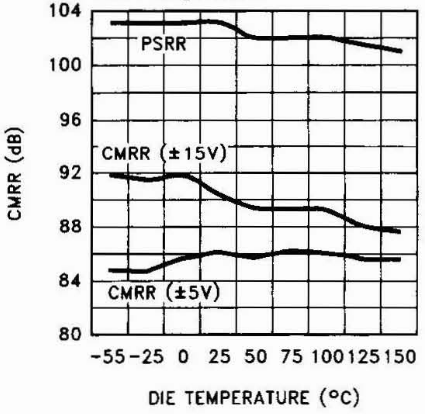
2175-32

Output Voltage Swing vs Die Temperature



2175-33

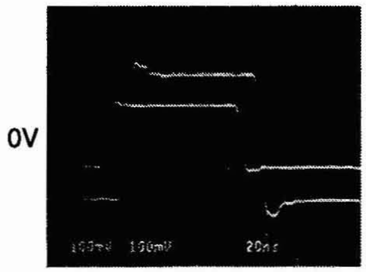
PSRR and CMRR vs Die Temperature



2175-34

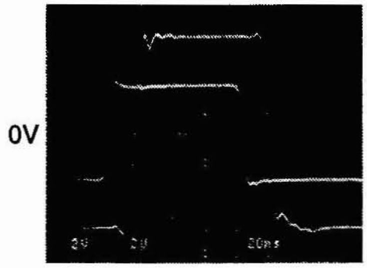
Typical Performance Curves — Contd.

Small Signal Pulse Response



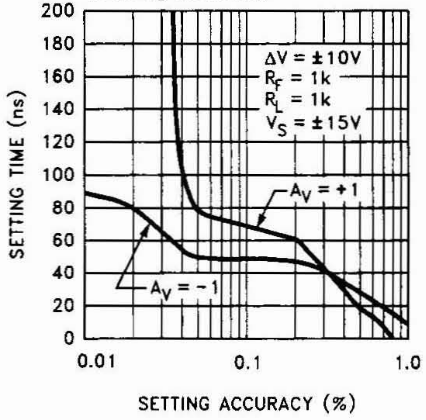
2175-35

Large Signal Pulse Response



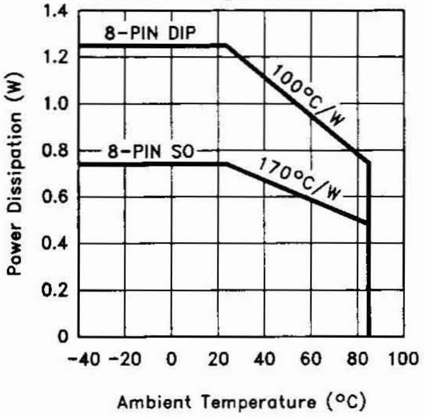
2175-36

Settling Time vs Settling Accuracy



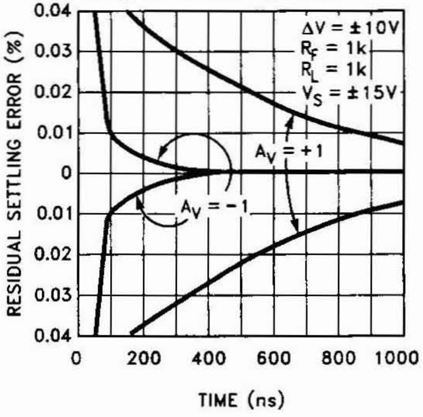
2175-37

8-Pin Package Power Dissipation vs Ambient Termperature



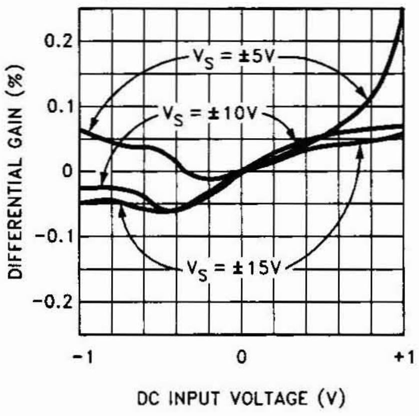
2175-38

Long Term Settling Error



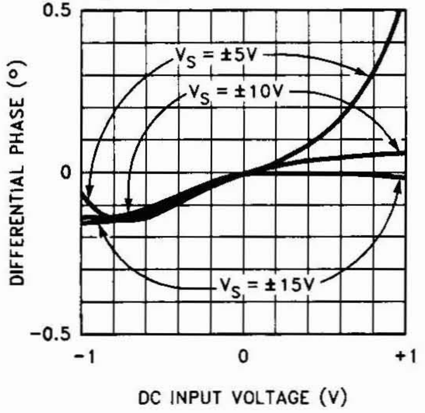
2175-39

Differential Gain vs DC Input Voltage R_L = 150



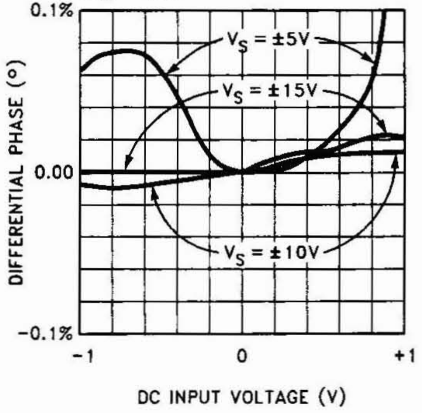
2175-40

Differential Phase vs DC Input Voltage R_L = 500



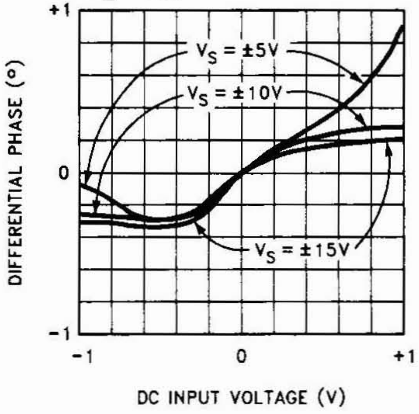
2175-41

Differential Gain vs DC Input Voltage R_L = 500



2175-42

Differential Phase vs DC Input Voltage R_L = 150



2175-43

EL2175C

120 MHz Precision Current Mode Feedback Amplifier

Applications Information

Product Description

The EL2175 is a single current mode feedback amplifier that offers wide bandwidth, high gain, low distortion and exceptional DC specifications for a CMF type amplifier at moderate supply current. Due to the current feedback architecture, the closed loop 3 dB bandwidth is dependent on the feedback resistor, R_F, and then the gain is set by picking the gain set resistor, R_G. The curves at the beginning of the "Typical Performance Curves" section show the effect of varying both R_F and R_G. The 3 dB bandwidth is significantly less dependent on supply voltage than earlier CMF amplifiers where increasing junction capacitance's with decreasing supply voltage caused a much larger reduction in bandwidth. To compensate for the remaining effect, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing And Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼″. The power supply pins must be well bypassed to ensure stability. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should have low inductance for best performance. Use of sockets, particularly for SO packages, should be avoided. Sockets have parasitic inductance and capacitance which will cause peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the conventional current feedback amplifiers, stray capacitance at the inverting input will affect their AC and transient performance when operating in the non-inverting configuration. This may cause design, development and production difficulties. The EL2175 has been designed in such a way as to largely ignore such strays. The characteristic curves of gain vs. frequency with varying values of $C_{IN}-$ illustrate this effect which produces only a slight increase in peaking with $C_{IN}-$ values up to 5 pF with almost no change in 3 dB bandwidth.

In the inverting gain mode, added capacitance at the inverting input has almost no effect at all. This is because the inverting input is now a virtual ground and the stray capacitance is not therefore "seen" by the amplifier.

Feedback Resistor Values

The EL2175 has been designed and specified with $R_F = 750\Omega$ for $A_V = +2$. This value of feedback resistor yields an extremely flat frequency response with little or no peaking out to 120 MHz. As is the case with all CMF amplifiers, wider bandwidth, at the expense of peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause roll-off to occur at lower frequency. This dependence of bandwidth on feedback resistance value is not as pronounced with the EL2175 at low non-inverting gains as with other CMF amplifiers. However, it is at all other gain conditions. For example, the 3 dB bandwidth of the EL2175 connected for $A_V = -1$ and $R_F = 750\Omega$ is about 65 MHz. If R_F is reduced to 560Ω, the bandwidth increases to about 88 MHz. See "Typical Performance Curves" section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistor, supply voltages and temperatures.

Bandwidth vs Temperature

The supply currents of many amplifiers and consequently their 3 dB bandwidths drop off significantly with increasing temperature. The EL2175 was designed to have nearly constant supply current over temperature resulting in a device with much less bandwidth vs. temperature sensitivity. With $V_S = +15V$ and $A_V = +2$, the bandwidth only varies from 123 MHz to 96 MHz over the entire die temperature range of $0°C < T < 150°C$.

Applications Information — Contd.

Supply Voltage Range

The EL2175 has been designed to operate comfortably with supply voltages from ±5V to ±15V. AC characterization has been conducted down to supply voltages of ±3.5V. However, this low value will not allow the part to power up and function properly at the lowest portion of the part's operating temperature range (−40°C to +85°C). In general, bandwidth, slew rate and video characteristics will tend to improve with increasing supply voltages.

If a single supply is desired, values from +9V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the input common mode range of the EL2175.

Settling Characteristics

The EL2175 offers superb settling characteristics to 0.1%, typically 50 ns operating in inverting mode. The inverting 0.01% settling time is about 90 ns. The EL2175 is not slew rate limited, therefore step size up to ±10V gives approximately the same settling time. The high 30 MΩ transimpedance gain and low input referred offsets of the EL2175 will also bring the final settled output much closer to its ideal value than is possible with earlier CMF designs.

The non-inverting ($A_V = +1$) 0.1% settling time is about 70 ns. As can be seen from the Long Term Settling Error graph, for $A_V = +1$, there is approximately a 0.04% residual which tails away to 0.01% in about 900 ns. This is a thermal settling error caused by a power dissipation change in the input stage devices (before and after the voltage step). All other CMF amplifiers exhibit 0.01% thermal settling tails of several tens of microseconds under the same conditions. The input stage of the EL2175 has been designed to greatly reduce this effect. For $A_V = -1$, because the inverting input is then a virtual ground, this tail does not appear even in conventional CMF amplifiers since the input stage does not experience the large voltage change that it does in non-inverting mode.

Distortion Performance

The distortion performance of all high frequency amplifiers degrade with increasing frequency. The EL2175 is no exception. However, due to it's high transimpedance, it's distortion performance at a given frequency can be 10–14 dB better than other high speed amplifiers available.

Power Dissipation

The EL2175 combines both high speed and large output drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature and loading conditions. To ensure that the EL2175 remains within it's absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by it's thermal resistance and the amount of temperature rise according to:

$$P_{DMAX} = (T_{JMAX} - T_{AMAX}) / \theta_{JA}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power dissipated in the IC due to the load, or:

$$P_{DMAX} = N \times (2 \times V_S \times I_S + (V_S - V_{OUT}) \times V_{OUT} / R_L)$$

where N is the number of amplifiers per package, and I_S is the current per amplifier. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term when the output is driving a load. That is to say, due to the class AB nature of the output stage, the output driver current is now included in the second term.) In general, an amplifier's AC performance degrades at higher temperatures and lower supply current. Unlike some amplifiers, the EL2175 and many other Elantec amplifiers maintain almost constant supply current over temperature so that the AC performance is not degraded as much at the upper end of the operating temperature range.

The EL2175 consumes typically 8.5 mA and a maximum of 10 mA. The worst case power in an amplifier operating from split supplies with a grounded load occurs when the output is between ground and half of one of it's supplies or, if it can't go that far due to drive limitations, at it's

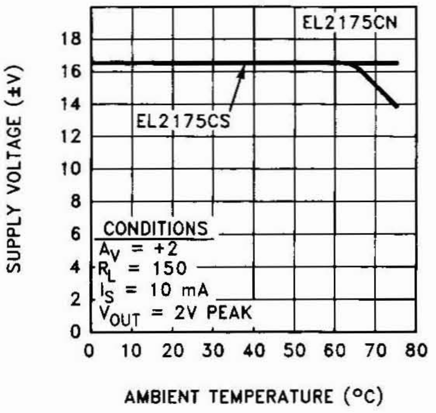
Applications Information — Contd.

maximum value. If we assume that the EL2175 is used for double terminate video cable driving applications ($R_L = 150\Omega$), and $A_V = +2$, then the maximum output voltage is 2V, and the average output voltage is 1.4V. If we set the two P_{DMAX} equations equal to each other, and solve for V_S, we get a family of curves for various package options according to:

$$V_S = \frac{R_L \times (T_{JMAX} - T_{AMAX}) / N \times \theta_{JA} + (V_{OUT}) \times (V_{OUT})}{(2 \times I_S \times R_L) + (V_{OUT})}$$

The following curve shows supply voltage ($\pm V_S$) vs. temperature for the EL2175's two packages, assuming $A_V = +2$, $R_L = 150\Omega$, and V_{OUT} (peak) = 2V. the curves include the worst case supply specification (I_S = 10 mA)

Supply Voltage
vs Ambient Temperature



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The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the device.

Output Current Drive

The EL2175 does not have output short circuit protection. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2175 to survive a continuous short.

Driving Cables And Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For these applications, the back termination series resistor will decouple the EL2175 from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. The EL2175 has particularly high capacitive load toleration and can drive a 50 pF load with only 3 dB of peaking and a 100 pF load with only 4 dB of peaking and without any instability. If higher capacitive loads must be driven or if little or no peaking is required, an additional small value (5Ω–50Ω) resistor can be placed in series with the output. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistance at the output.

EL2176C/EL2276C

70 MHz/1 mA Current Mode Feedback Amp w/Disable

Features

- Single (EL2176C) and dual (EL2276C) topologies
- 1 mA supply current (per amplifier)
- 70 MHz −3 dB bandwidth
- Low cost
- Fast disable
- Powers down to 0 mA
- Single- and dual-supply operation down to ±1.5V
- 0.15%/0.15° diff. gain/diff. phase into 150Ω
- 800V/μs slew rate
- Large output drive current:
  100 mA (EL2176C)
  55 mA (EL2276C)
- Also available without disable in single (EL2170C), dual (EL2270C) and quad (EL2470C)
- Higher speed EL2180C/EL2186C family also available (3 mA/250 MHz) in single, dual and quad

Applications

- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2176CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2176CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2276CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL2276CS	−40°C to +85°C	14-Pin SOIC	MDP0027

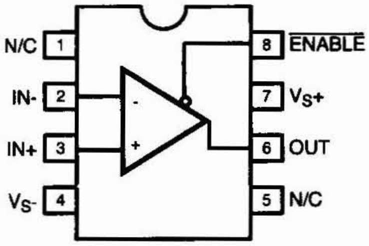
General Description

The EL2176C/EL2276C are single/dual current-feedback operational amplifiers which achieve a −3 dB bandwidth of 70 MHz at a gain of +1 while consuming only 1 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from +3V to +12V. The EL2176C/EL2276C also include a disable/power-down feature which reduces current consumption to 0 mA while placing the amplifier output in a high impedance state. In spite of its low supply current, the EL2276C can output 55 mA while swinging to ±4V on ±5V supplies. The EL2176C can output 100 mA with similar output swings. These attributes make the EL2176C/EL2276C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

For Single, Dual and Quad applications without disable, consider the EL2170C (8-Pin Single), EL2270C (8-Pin Dual) or EL2470C (14-Pin Quad). For higher bandwidth applications where low power is still a concern, consider the EL2180C/El2186C family which also comes in similar Single, Dual and Quad configurations. The EL2180C/EL2186C family provides a −3 dB bandwidth of 250 MHz while consuming 3 mA of supply current per amplifier.

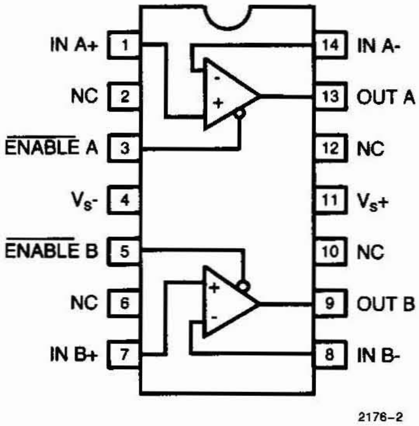
Connection Diagrams

EL2176C SO, P-DIP



2176-1

EL2276C SO, P-DIP



2176-2

Manufactured under U.S. Patent No. 5,352,989, 5,351,012, 5,418,495

EL2176C/EL2276C

70 MHz/1 mA Current Mode Feedback Amp w/Disable

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+12.6V	Operating Junction Temperature	
Common-Mode Input Voltage	V_S- to V_S+	Plastic Packages	150°C
Differential Input Voltage	±6V	Output Current (EL2176C)	±120 mA
Current into +IN or −IN	±7.5 mA	Output Current (EL2276C)	±60 mA
Internal Power Dissipation	See Curves	Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±5V, R_L = 150Ω, $\overline{\text{ENABLE}}$ = 0V, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			2.5	15	I	mV
TCV_{OS}	Average Input Offset Voltage Drift	Measured from T_{MIN} to T_{MAX}		5		V	µV/°C
dV_{OS}	V_{OS} Matching	EL2276C only		0.5		V	mV
$+I_{IN}$	+ Input Current			0.5	5	I	µA
$d+I_{IN}$	$+I_{IN}$ Matching	EL2276C only		20		V	nA
$-I_{IN}$	− Input Current			4	15	I	µA
$d-I_{IN}$	$-I_{IN}$ Matching	EL2276C only		1.5		V	µA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5 V	45	50		I	dB
−ICMR	− Input Current Common Mode Rejection	V_{CM} = ±3.5V		4	10	I	µA/V
PSRR	Power Supply Rejection Ratio	V_S is moved from ±4V to ±6V	60	70		I	dB
−IPSR	− Input Current Power Supply Rejection	V_S is moved from ±4V to ±6V		0.5	5	I	µA/V
R_{OL}	Transimpedance	V_{OUT} = ±2.5V	150	400		I	kΩ
$+R_{IN}$	+ Input Resistance	V_{CM} = ±3.5V	1	4		I	MΩ
$+C_{IN}$	+ Input Capacitance			1.2		V	pF
CMIR	Common Mode Input Range		±3.5	±4.0		I	V

DC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_L = 150\Omega$, $\overline{ENABLE} = 0V$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	$V_S = \pm 5$	±3.5	±4.0		I	V
		$V_S = +5$ Single-Supply, High		4.0		V	V
		$V_S = +5$ Single-Supply, Low		0.3		V	V
I_O	Output Current	EL2176C only	80	100		I	mA
		EL2276C only, per Amplifier	50	55		I	mA
I_S	Supply Current	$\overline{ENABLE}$ = 2.0V, per Amplifier		1	2	I	mA
$I_{S(DIS)}$	Supply Current (Disabled)	$\overline{ENABLE}$ = 4.5V		0	20	I	μA
$C_{OUT(DIS)}$	Output Capacitance (Disabled)	$\overline{ENABLE}$ = 4.5V		4.4		V	pF
R_{EN}	Enable Pin Input Resistance	Measured at $\overline{ENABLE}$ = 2.0V, 4.5V	45	85		I	kΩ
I_{IH}	Logic "1" Input Current	Measured at $\overline{ENABLE}$, $\overline{ENABLE}$ = 4.5V		−0.04		V	μA
I_{IL}	Logic "0" Input Current	Measured at $\overline{ENABLE}$, $\overline{ENABLE}$ = 0V		−53		V	μA
V_{DIS}	Minimum Voltage at $\overline{ENABLE}$ to Disable		4.5			I	V
V_{EN}	Maximum Voltage at $\overline{ENABLE}$ to Enable				2.0	I	V

AC Electrical Characteristics

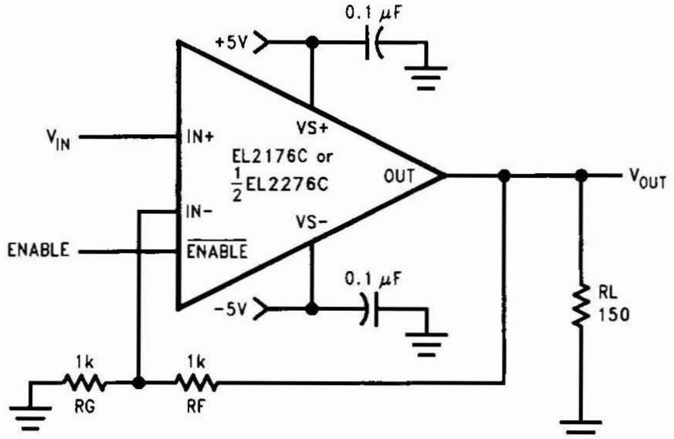
$V_S = \pm 5V$, $R_F = R_G = 1.0\ k\Omega$, $R_L = 150\Omega$, $\overline{ENABLE} = 0V$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
−3 dB BW	−3 dB Bandwidth	$A_V = +1$		70		V	MHz
−3 dB BW	−3 dB Bandwidth	$A_V = +2$		60		V	MHz
SR	Slew Rate	$V_{OUT} = \pm 2.5V$, $A_V = +2$	400	800		IV	V/μs
t_r, t_f	Rise and Fall Time	$V_{OUT} = \pm 500$ mV		4.5		V	ns
t_{pd}	Propagation Delay	$V_{OUT} = \pm 500$ mV		4.5		V	ns
OS	Overshoot	$V_{OUT} = \pm 500$ mV		3.0		V	%
ts	0.1% Settling	$V_{OUT} = \pm 2.5V$, $A_V = -1$		40		V	ns
dG	Differential Gain	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.15		V	%
dP	Differential Phase	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.15		V	°
dG	Differential Gain	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.02		V	%
dP	Differential Phase	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.01		V	°
t_{ON}	Turn-On Time	$A_V = +2$, $V_{IN} = +1V$, $R_L = 150\Omega$ (Note 2)		40	100	I	ns
t_{OFF}	Turn-Off Time	$A_V = +2$, $V_{IN} = +1V$, $R_L = 150\Omega$ (Note 2)		1500	2000	I	ns
CS	Channel Separation	EL2276C only, f = 5 MHz		85		V	dB

Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mV_{P-P}, f = 3.58 MHz.

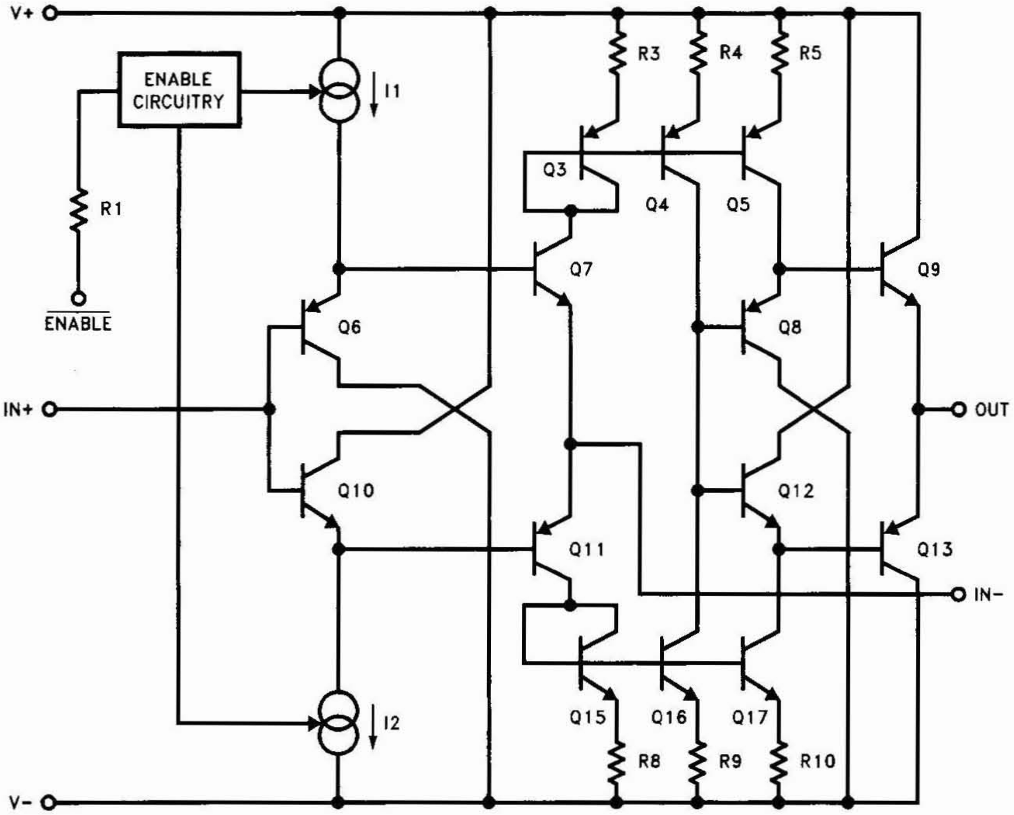
Note 2: Measured from the application of the logic signal until the output voltage is at the 50% point between initial and final values.

Test Circuit (per Amplifier)


+5V
0.1 µF
VS+
V_{IN}
IN+
EL2176C or
$\frac{1}{2}$EL2276C
OUT
V_{OUT}
IN-
VS-
ENABLE
$\overline{ENABLE}$
0.1 µF
-5V
RL
150
1k
RG
1k
RF

2176-3

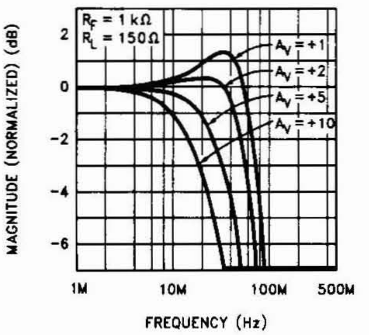
Simplified Schematic (per Amplifer)


V+
ENABLE CIRCUITRY
I1
R1
$\overline{ENABLE}$
R3
R4
R5
Q3
Q4
Q5
Q7
Q9
Q6
Q8
IN+
OUT
Q10
Q12
Q11
Q13
IN-
Q15
Q16
Q17
I2
R8
R9
R10
V-

2176-4

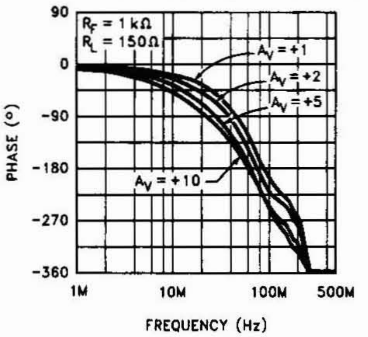
Typical Performance Curves

Non-Inverting Frequency Response (Gain)



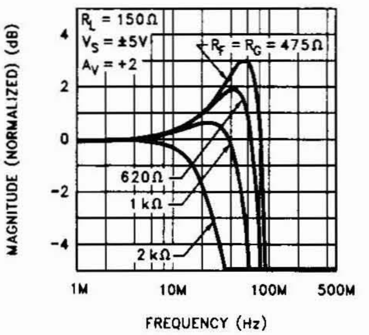
2176-5

Non-Inverting Frequency Response (Phase)



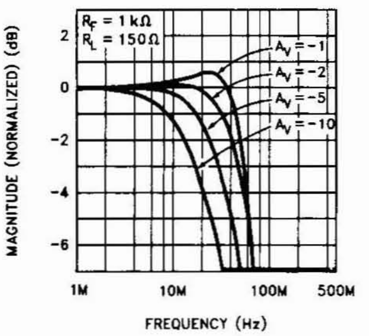
2176-6

Frequency Response for Various R_F and R_G



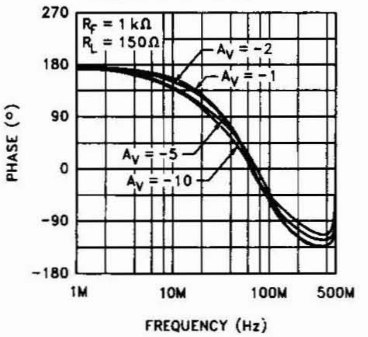
2176-7

Inverting Frequency Response (Gain)



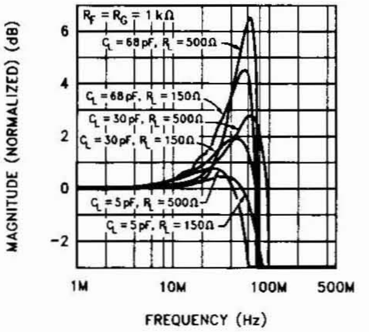
2176-8

Inverting Frequency Response (Phase)



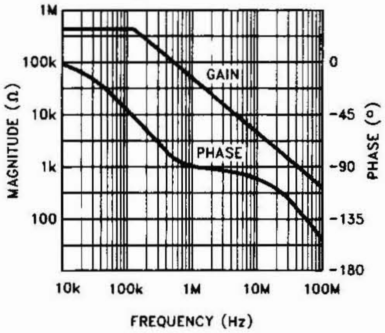
2176-9

Frequency Response for Various R_L and C_L



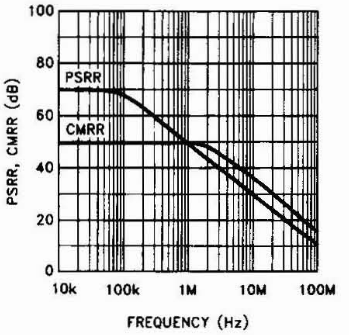
2176-10

Transimpedance (R_{OL})



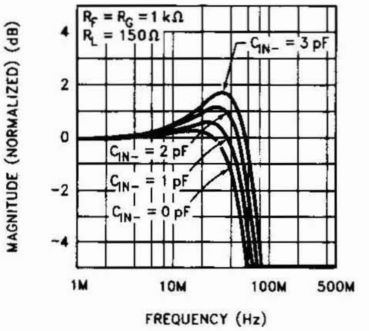
2176-11

PSRR and CMRR



2176-12

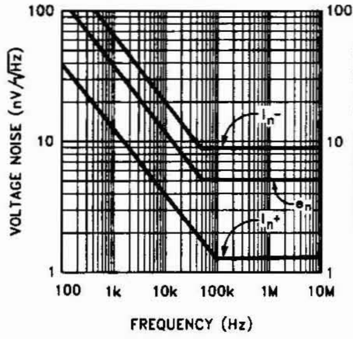
Frequency Response for Various C_{IN-}



2176-13

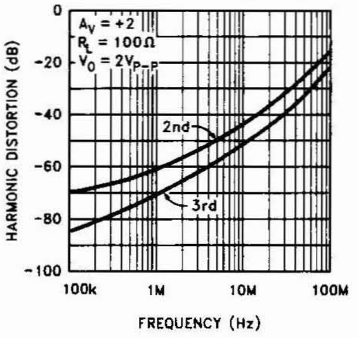
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency



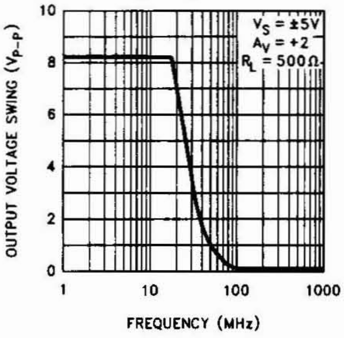
2176-14

2nd and 3rd Harmonic Distortion vs Frequency



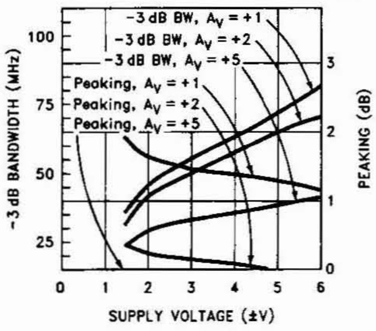
2176-15

Output Voltage vs Frequency



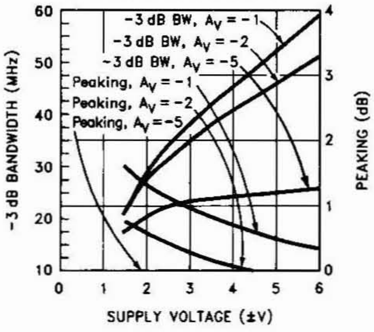
2176-16

−3 dB Bandwith and Peaking vs Supply Voltage for Various Non-Inverting Gains



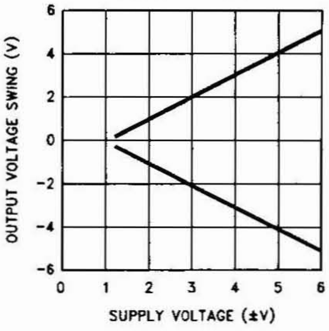
2176-17

−3 dB Bandwith and Peaking vs Supply Voltage for Various Inverting Gains



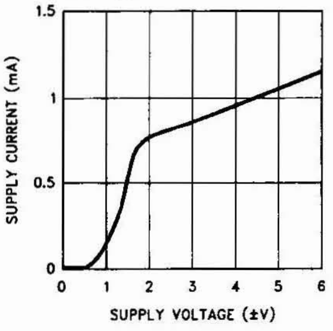
2176-18

Output Voltage Swing vs Supply Voltage



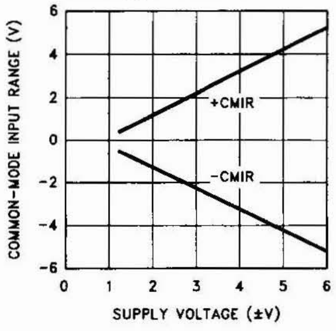
2176-19

Supply Current vs Supply Voltage



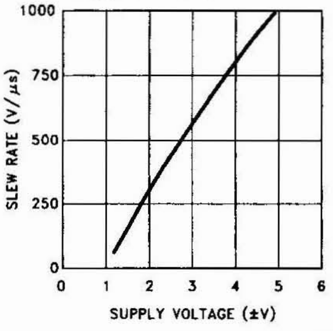
2176-20

Common-Mode Input Range vs Supply Voltage



2176-21

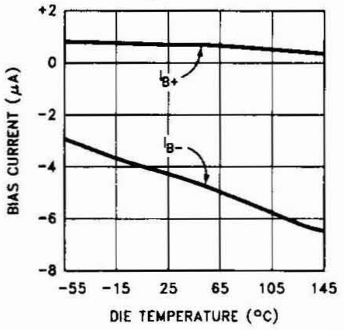
Slew Rate vs Supply Voltage



2176-22

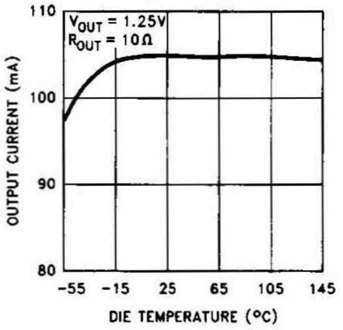
Typical Performance Curves — Contd.

Input Bias Current vs Die Temperature



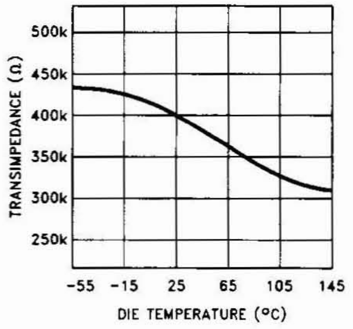
2176-23

Short-Circuit Current vs Die Temperature



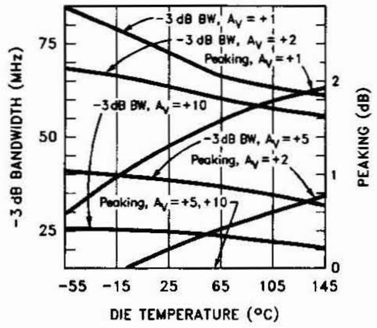
2176-24

Transimpedance (R_{OL}) vs Die Temperature



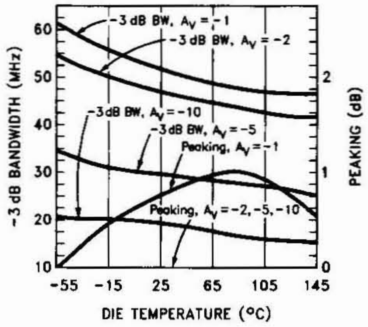
2176-25

−3 dB Bandwith and Peaking vs Die Temperature for Various Non-Inverting Gains



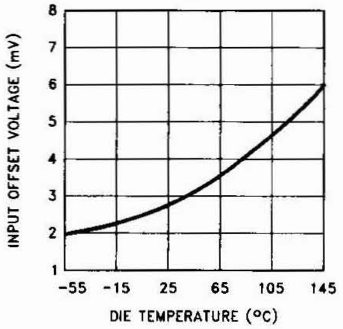
2176-26

−3 dB Bandwith and Peaking vs Die Temperature for Various Inverting Gains



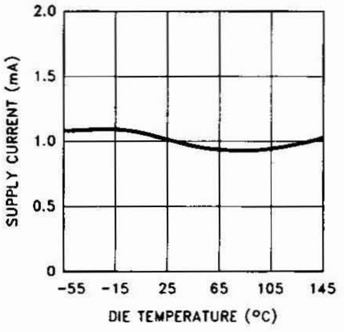
2176-27

Input Offset Voltage vs Die Temperature



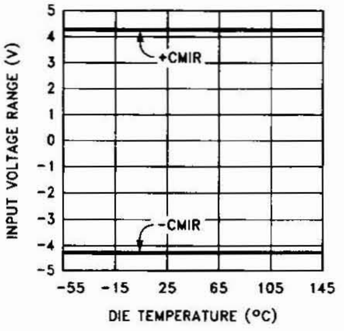
2176-28

Supply Current vs Die Temperature



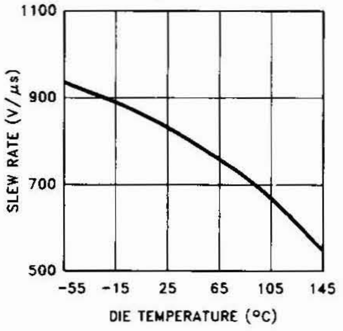
2176-29

Input Voltage Range vs Die Temperature



2176-30

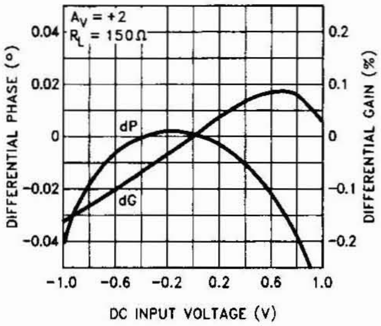
Slew Rate vs Die Temperature



2176-31

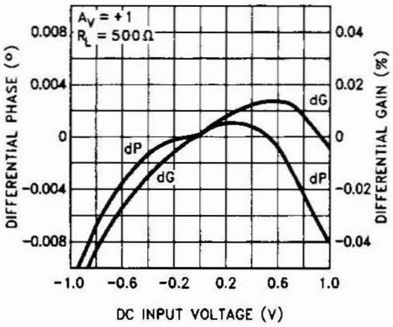
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz/A_V = +2



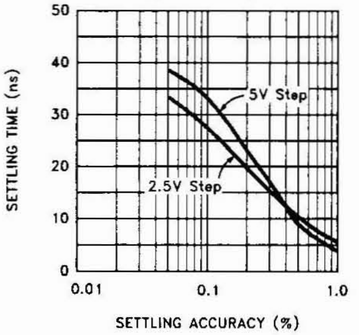
2176-32

Differential Gain and Phase vs DC Input Offset at 3.58 MHz/A_V = +1



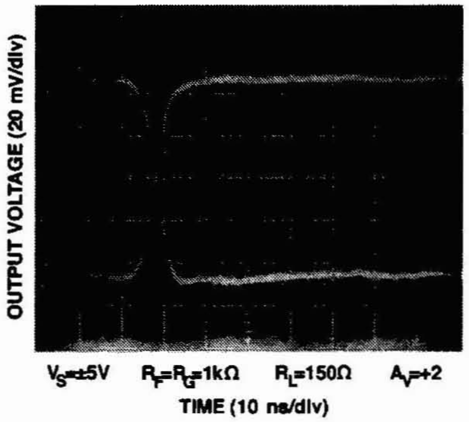
2176-33

Settling Time vs Settling Accuracy



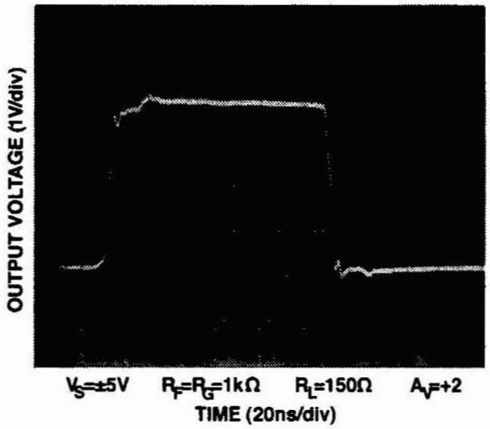
2176-34

Small-Signal Step Response



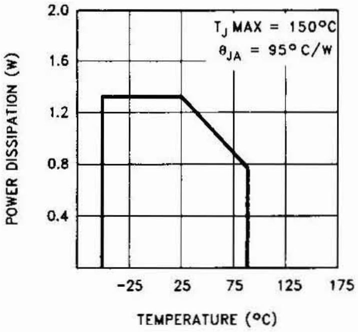
2176-35

Large-Signal Step Response



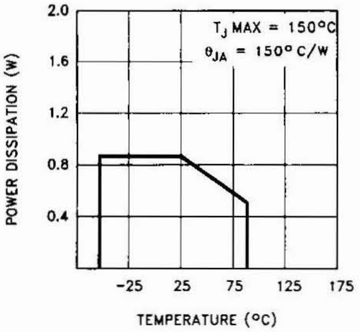
2176-36

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2176-37

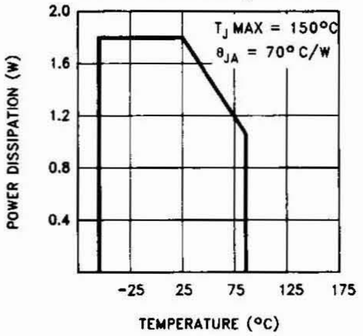
8-Lead SO Maximum Power Dissipation vs Ambient Temperature



2176-38

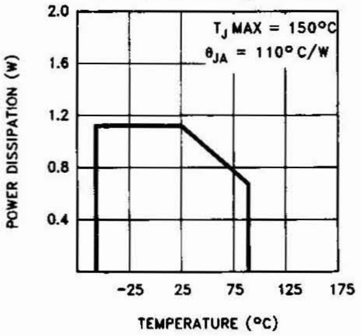
Typical Performance Curves — Contd.

14-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



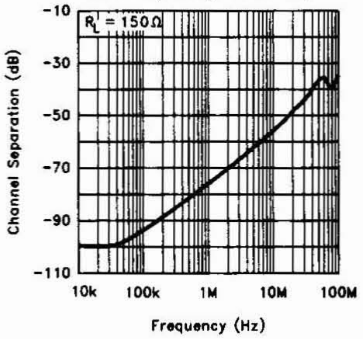
2176-39

14-Lead SO Maximum Power Dissipation vs Ambient Temperature



2176-40

Channel Separation vs Frequency (EL2276)



2176-41

Applications Information

Product Description

The EL2176C/EL2276C are current-feedback operational amplifiers that offer a wide −3 dB bandwidth of 70 MHz, a low supply current of 1 mA per amplifier and the ability to disable to 0 mA. Both products also feature high output current drive. The EL2176C can output 100 mA, while the EL2276C can output 55 mA per amplifier. The EL2176C/EL2276C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to with in 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2176C/EL2276C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their −3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2176C/EL2276C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For Single, Dual and Quad applications without disable, consider the EL2170C (8-Pin Single), EL2270C (8-Pin Dual) and EL2470C (14-Pin Quad). If more AC performance is required, refer to the EL2180C/EL2186C family which provides Singles, Duals, and Quads with 250 MHz of bandwidth while consuming 3 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Disable/Power-Down

The EL2176C/EL2276C amplifiers can be disabled, placing their output in a high-impedance state. When disabled, each amplifier's supply current is reduced to 0 mA. Each EL2176C/EL2276C amplifier is disabled when its $\overline{\text{ENABLE}}$ pin is floating or pulled up to within 0.5V of the positive supply. Similarly, each amplifier is enabled by pulling its $\overline{\text{ENABLE}}$ pin at least 3V below the positive supply. For ±5V supplies, this means that an EL2176C/EL2276C amplifier will be enabled when $\overline{\text{ENABLE}}$ is at 2V or less, and disabled when $\overline{\text{ENABLE}}$ is above 4.5V. Although the logic levels are not standard TTL, this choice of logic voltages allows the EL2176C/EL2276C to be enabled by tying $\overline{\text{ENABLE}}$ to ground, even in +3V single-supply applications. The $\overline{\text{ENABLE}}$ pin can be driven from CMOS outputs or open-collector TTL.

When enabled, supply current does vary somewhat with the voltage applied at $\overline{\text{ENABLE}}$. For example, with the supply voltages of the EL2176C at ±5V, if $\overline{\text{ENABLE}}$ is tied to −5V (rather than ground) the supply current will increase about 15% to 1.15 mA.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feed-

Applications Information — Contd.

back and gain resistors further exacerbates the problem by further lowering the pole frequency.

The EL2176C/EL2276C have been specially designed to reduce power dissipation in the feedback network by using large 1.0 kΩ feedback and gain resistors. With the high bandwidths of these amplifiers, these large resistor values would normally cause stability problems when combined with parasitic capacitance, but by internally canceling the effects of a nominal amount of parasitic capacitance, the EL2176C/EL2276C remain very stable. For less experienced users, this feature makes the EL2176C/EL2276C much more forgiving, and therefore easier to use than other products not incorporating this proprietary circuitry.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2176C/EL2276 C have less bandwidth than expected. In this case, the inverting input may have less parasitic capacitance than expected by the internal compensation circuitry of the EL2176C/EL2276C. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g., 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various R_F and R_G, and Frequency Response for Various C_{IN-}.

Feedback Resistor Values

The EL2176C/EL2276C have been designed and specified at gains of +1 and +2 with R_F = 1.0 kΩ. This value of feedback resistor gives 70 MHz of −3 dB bandwidth at A_V = +1 with about 1.5 dB of peaking, and 60 MHz of −3 dB bandwidth at A_V = +2 with about 0.5 dB of peaking. Since the EL2176C/EL2276C are current-feedback amplifiers, it is also possible to change the value of R_F to get more bandwidth. As seen in the curve of Frequency Response For Various R_F and R_G, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2176C is a current-feedback amplifier, the gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2176C/EL2276C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases.

Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of R_F below the specified 1.0 kΩ and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2176C/EL2276C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2176C/EL2276C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2176C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2176C/EL2276C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2176C/EL2276C have an input range which spans from 1V to 4V. The output range of the EL2176C /EL2276C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2176C/EL2276C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically in excess of the

Applications Information — Contd.

entire 1 mA supply current of each EL2176C/EL2276C amplifier! Special circuitry has been incorporated in the EL2176C/EL2276C to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.15% and 0.15° while driving 150Ω at a gain of +2.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2176C/EL2276C have dG and dP specifications of 0.01% and 0.02° respectively while driving 500Ω at $A_V = +1$.

Output Drive Capability

In spite of its low 1 mA of supply current, the EL2176C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2276C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2176C is capable of driving 50Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2276C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2176C/EL2276C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (R_F) to reduce the peaking.

Current Limiting

The EL2176C/EL2276C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2176C/EL2276C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when R_L falls below about 25Ω, it is important to calculate the maximum junction temperature (T_{Jmax}) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2176C/EL2276C to remain in the safe operating area. These parameters are calculated as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} * n * PD_{MAX}) \qquad [1]$$

where:

T_{MAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
n = Number of Amplifiers in the Package
PD_{MAX} = Maximum Power Dissipation of Each Amplifier in the Package.

PD_{MAX} for each amplifier can be calculated as follows:

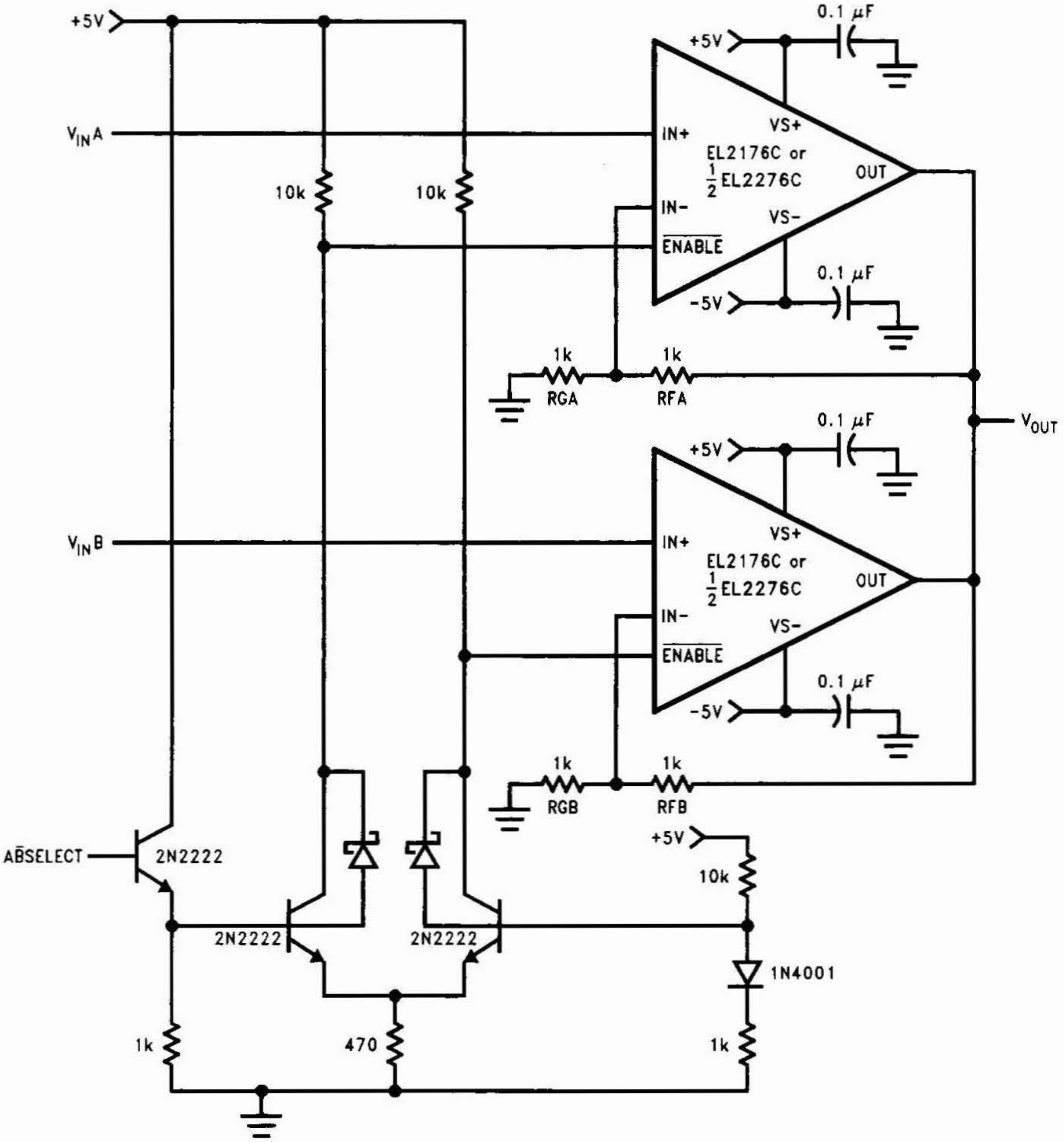
$$PD_{MAX} = (2 * V_S * I_{SMAX}) + (V_S - V_{OUTMAX}) * (V_{OUTMAX}/R_L)) \qquad [2]$$

where:

V_S = Supply Voltage
I_{SMAX} = Maximum Supply Current of 1 Amplifier
V_{OUTMAX} = Max. Output Voltage of the Application
R_L = Load Resistance

Typical Application Circuits

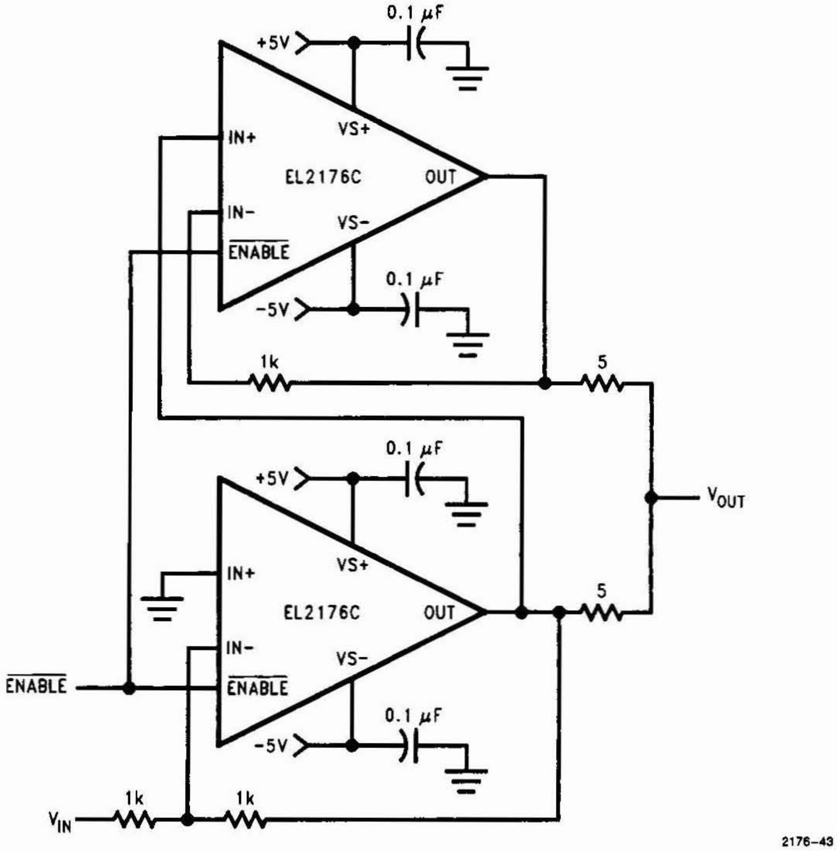
Low Power Multiplexer with Single-Ended TTL Input


+5V
V_{IN}A
V_{IN}B
10k
10k
0.1 μF
+5V
IN+
VS+
EL2176C or
$\frac{1}{2}$ EL2276C
OUT
IN-
VS-
ENABLE
-5V
1k
RGA
1k
RFA
V_{OUT}
RGB
RFB
AB̄SELECT
2N2222
1N4001
470
1k

2176-42

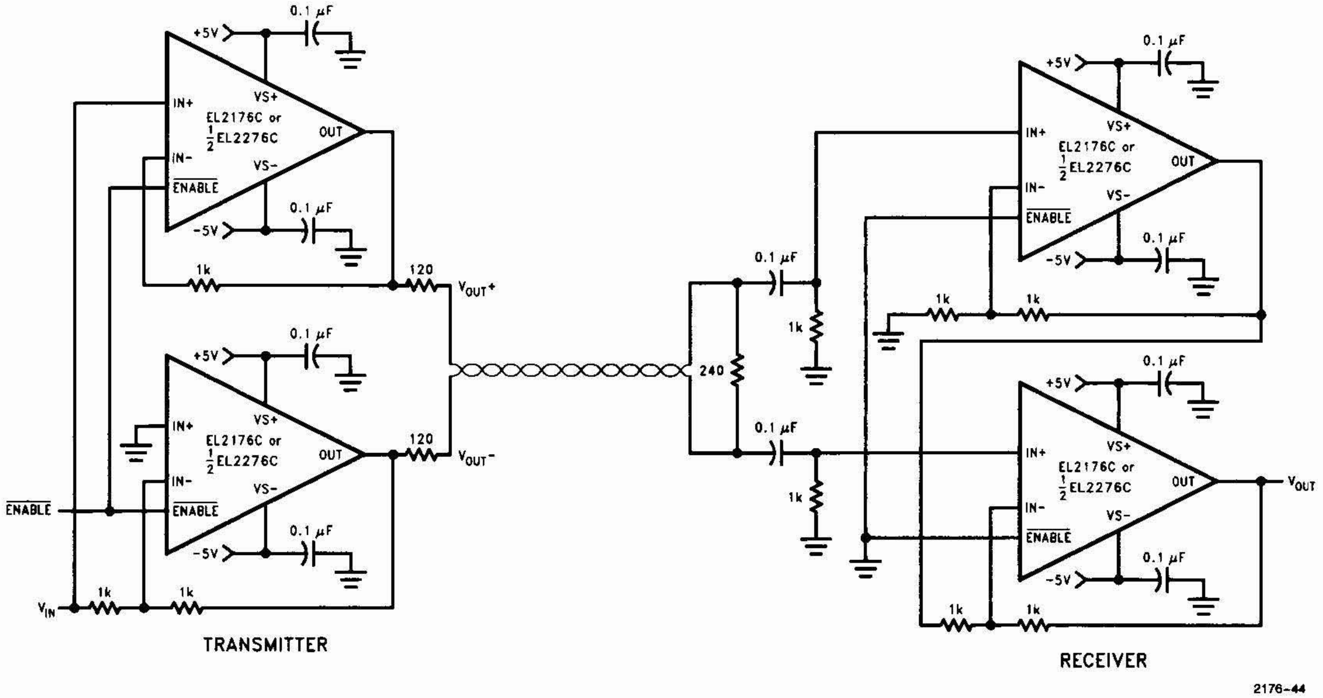
Typical Application Circuits — Contd.

Inverting 200 mA Output Current Distribution Amplifier


0.1 μF
+5V
IN+
VS+
EL2176C
OUT
IN-
VS-
ENABLE
0.1 μF
-5V
1k
5
0.1 μF
+5V
VOUT
IN+
VS+
EL2176C
OUT
5
IN-
VS-
ENABLE
ENABLE
0.1 μF
-5V
VIN
1k
1k
2176-43

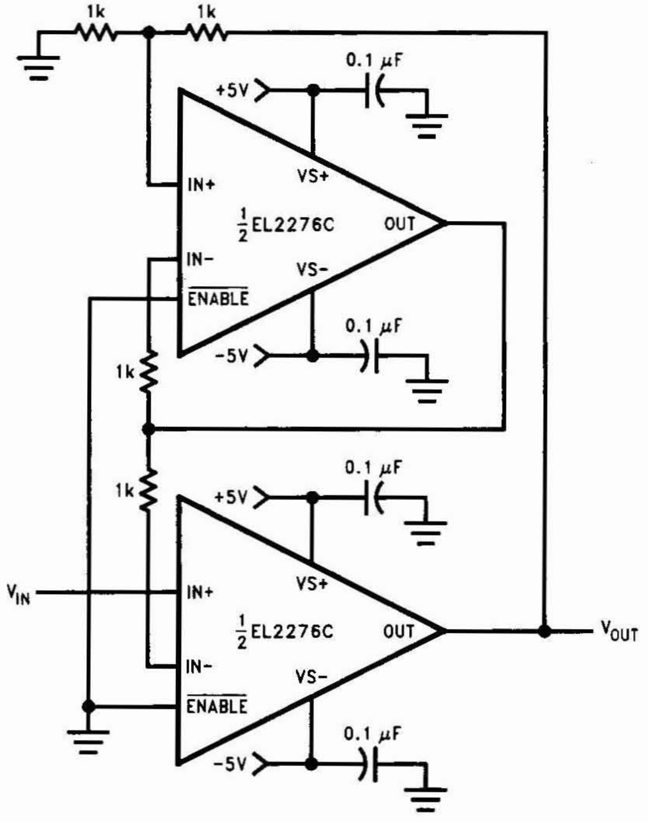
Typical Application Circuits — Contd.

Differential Line-Driver/Receiver


+5V
0.1 μF
IN+
VS+
EL2176C or
$\frac{1}{2}$ EL2276C
OUT
IN−
VS−
$\overline{\text{ENABLE}}$
−5V
1k
120
$V_{OUT}+$
$V_{OUT}-$
$\overline{\text{ENABLE}}$
V_{IN}
TRANSMITTER
240
1k
V_{OUT}
RECEIVER
2176-44

Typical Application Circuits — Contd.

Fast-Settling Precision Amplifier

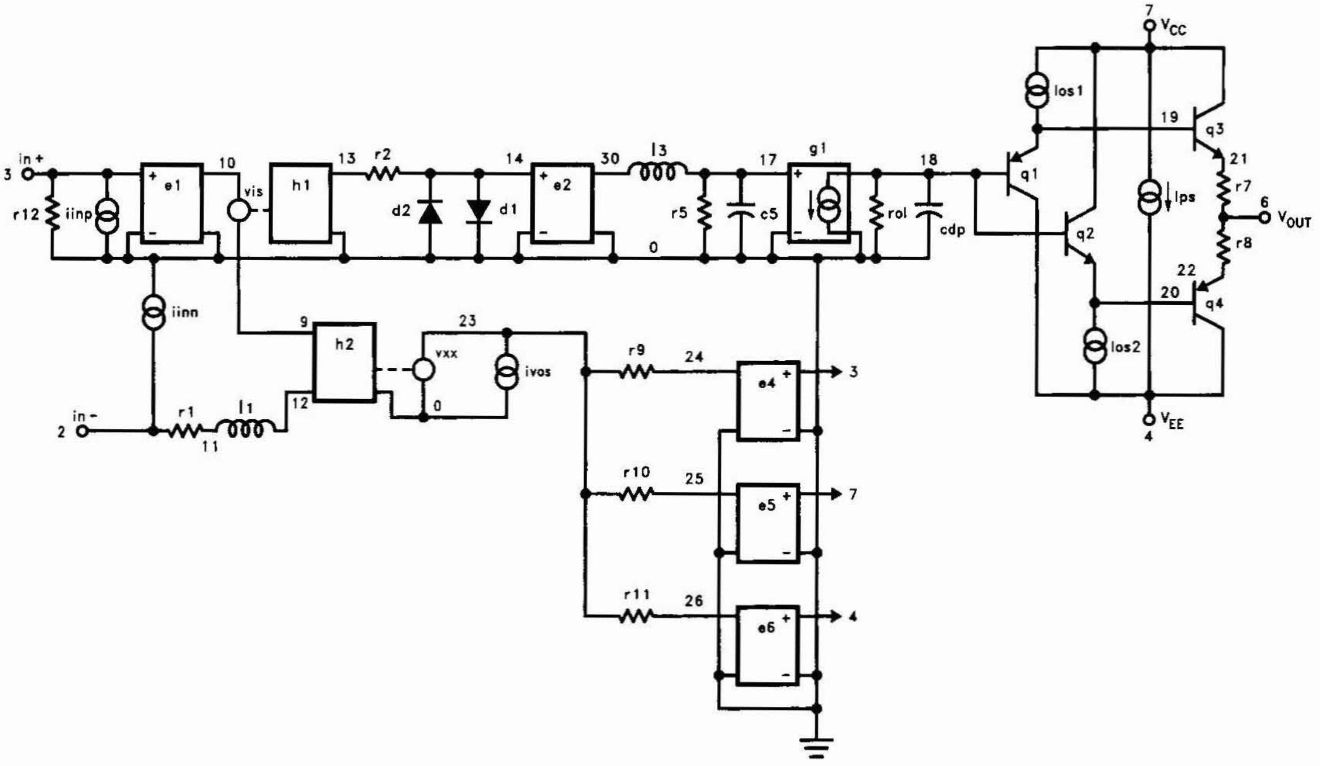

1k
1k
0.1 μF
+5V
IN+
VS+
$\frac{1}{2}$EL2276C
OUT
IN−
VS−
ENABLE
0.1 μF
−5V
1k
1k
0.1 μF
+5V
V_{IN}
IN+
VS+
$\frac{1}{2}$EL2276C
OUT
V_{OUT}
IN−
VS−
ENABLE
0.1 μF
−5V

2176-45

EL2176C/EL2276C Macromodel

```
* Revision A, March 1995
* AC characteristics used Rf = Rg = 1KΩ, RL = 150Ω
* Connections:      +input
*                   |   -input
*                   |   |   +Vsupply
*                   |   |   |   -Vsupply
*                   |   |   |   |   output
*                   |   |   |   |   |
.subckt EL2176/el   3   2   7   4   6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 165
l1 11 12 25nH
iinp 3 0 0.5uA
iinm 2 0 4uA
r12 3 0 4Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 0.5uH
c5 17 0 0.69pF
r5 17 0 300
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 400K
cdp 18 0 1.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 0.4mA
ios2 20 4 0.4mA
*
* Supply Current
*
ips 7 4 1nA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 -1.0
r9 24 23 0.316K
r10 25 23 3.2K
r11 26 23 3.2K
*
* Models
*
.model qn npn(is = 5e-15 bf = 200 tf = 0.01nS)
.model qp pnp(is = 5e-15 bf = 200 tf = 0.01nS)
.model dclamp d(is = 1e-30 ibv = 0.266
+ bv = 1.3v n = 4)
.ends
```

EL2176C/EL2276C Macromodel — Contd.


7
VCC
Ios1
19
q3
21
r7
6
VOUT
r8
22
20
q4
Ios2
VEE
4
q1
q2
Ips
in+
3
r12
iinp
e1
10
vis
h1
13
r2
d2
d1
14
e2
30
l3
r5
c5
0
17
g1
rol
18
cdp
iinn
9
h2
23
vxx
ivos
0
12
in−
2
r1
l1
11
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4

2176–46

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2180C/EL2280C/EL2480C

250 MHz/3 mA Current Mode Feedback Amplifiers

Features

- Single (EL2180C), dual (EL2280C) and quad (EL2480C) topologies
- 3 mA supply current (per amplifier)
- 250 MHz −3 dB bandwidth
- Tiny SOT23-5 Package (EL2180C)
- Low cost
- Single- and dual-supply operation down to ±1.5V
- 0.05%/0.05° diff. gain/diff. phase into 150Ω
- 1200 V/μs slew rate
- Large output drive current:
  100 mA (EL2180C)
  55 mA (EL2280C)
  55 mA (EL2480C)
- Also available with disable in single (EL2186C), dual (EL2286C), and triple (EL2386C)
- Lower power EL2170C/EL2176C family also available (1 mA/ 70 MHz) in single, dual and quad

Applications

- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2180CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2180CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2180CW	−40°C to +85°C	5-Pin SOT23*	MDP0038
EL2280CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2280CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2480CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL2480CS	−40°C to +85°C	14-Pin SOIC	MDP0027

*See Ordering Information section of databook.

General Description

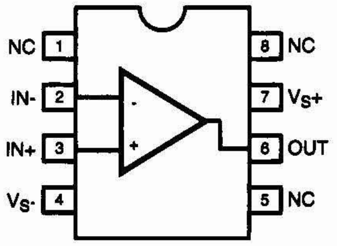
The EL2180C/EL2280C/EL2480C are single/dual/quad current-feedback operational amplifiers which achieve a −3 dB bandwidth of 250 MHz at a gain of +1 while consuming only 3 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from +3V to +12V. In spite of their low supply current, the EL2480C and the EL2280C can output 55 mA while swinging to ±4V on ±5V supplies. The EL2180C can output 100 mA with similar output swings. These attributes make the EL2180C/EL2280C/EL2480C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

For applications where board space is extremely critical, the EL2180C is available in the tiny 5-lead SOT23 package, which has a footprint 28% the size of an 8-lead SOIC.

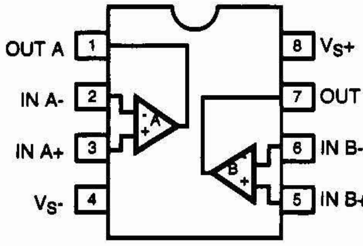
For Single, Dual, and Triple applications with disable, consider the EL2186C (8-Pin Single), EL2286C (14-Pin Dual) or EL2386C (16-Pin Triple). For lower power applications where speed is still a concern, consider the EL2170C/El2176C family which also comes in similar Single, Dual and Quad configurations. The EL2170C/EL2176C family provides a −3 dB bandwidth of 70 MHz while consuming 1 mA of supply current per amplifier.

Connection Diagrams

EL2180C SO, P-DIP

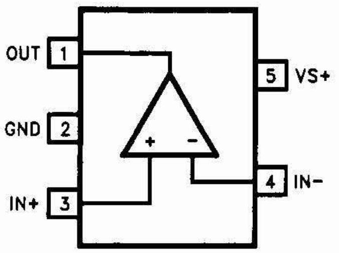


EL2280C SO, P-DIP



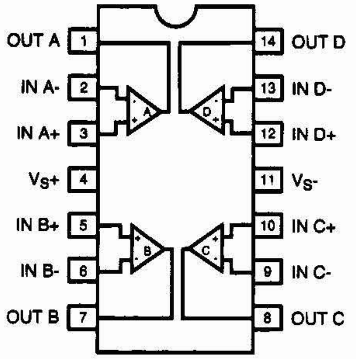
2180-1

EL2180C SOT23-5



2180-46

EL2480C SO, P-DIP



2180-2

EL2180C/EL2280C/EL2480C

250 MHz/3 mA Current Mode Feedback Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+12.6V	Operating Junction Temperature	
Common-Mode Input Voltage	V_S- to V_S+	Plastic Packages	150°C
Differential Input Voltage	±6V	Output Current (EL2180C)	±120 mA
Current into +IN or −IN	±7.5 mA	Output Current (EL2280C)	±60 mA
Internal Power Dissipation	See Curves	Output Current (EL2480C)	±60 mA
Operating Ambient Temperature Range	−40°C to +85°C	Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±5V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			2.5	15	I	mV
TCV_{OS}	Average Input Offset Voltage Drift	Measured from T_{MIN} to T_{MAX}		5		V	µV/°C
dV_{OS}	V_{OS} Matching	EL2280C, EL2480C only		0.5		V	mV
$+I_{IN}$	+ Input Current			1.5	15	I	µA
$d+I_{IN}$	$+I_{IN}$ Matching	EL2280C, EL2480C only		20		V	nA
$-I_{IN}$	− Input Current			16	40	I	µA
$d-I_{IN}$	$-I_{IN}$ Matching	EL2280C, EL2480C only		2		V	µA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	45	50		I	dB
−ICMR	− Input Current Common Mode Rejection	V_{CM} = ±3.5V		5	30	I	µA/V
PSRR	Power Supply Rejection Ratio	V_S is moved from ±4V to ±6V	60	70		I	dB
−IPSR	− Input Current Power Supply Rejection	V_S is moved from ±4V to ±6V		1	15	I	µA/V
R_{OL}	Transimpedance	V_{OUT} = ±2.5V	120	300		I	kΩ
$+R_{IN}$	+ Input Resistance	V_{CM} = ±3.5V	0.5	2		I	MΩ
$+C_{IN}$	+ Input Capacitance			1.2		V	pF
CMIR	Common Mode Input Range		±3.5	±4.0		I	V

DC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	$V_S = \pm 5$	±3.5	±4.0		I	V
		$V_S = +5$ Single-Supply, High		4.0		V	V
		$V_S = +5$ Single-Supply, Low		0.3		V	V
I_O	Output Current	EL2180C only	80	100		I	mA
		EL2280C only, per Amplifier	50	55		I	mA
		EL2480C only, per Amplifier	50	55		I	mA
I_S	Supply Current	Per Amplifier		3	6	I	mA

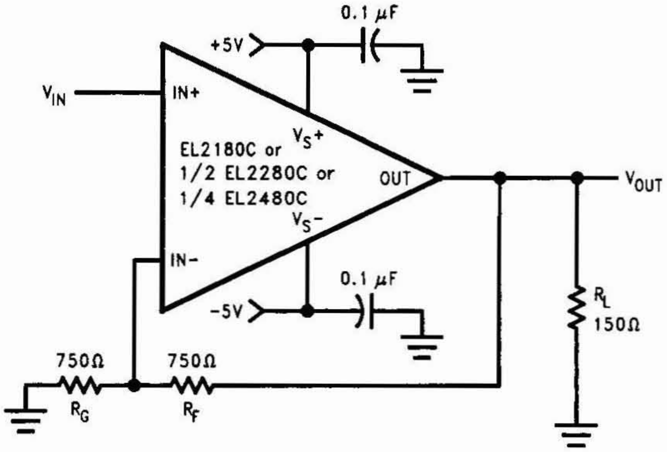
AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = R_G = 750\Omega$ for PDIP and SOIC packages, $R_F = R_G = 560\Omega$ for SOT23-5 package, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
−3 dB BW	−3 dB Bandwidth	$A_V = +1$		250		V	MHz
−3 dB BW	−3 dB Bandwidth	$A_V = +2$		180		V	MHz
0.1 dB BW	0.1 dB Bandwidth	$A_V = +2$		50		V	MHz
SR	Slew Rate	$V_{OUT} = \pm 2.5V$, $A_V = +2$	600	1200		IV	V/µs
t_r, t_f	Rise and Fall Time	$V_{OUT} = \pm 500$ mV		1.5		V	ns
t_{pd}	Propagation Delay	$V_{OUT} = \pm 500$ mV		1.5		V	ns
OS	Overshoot	$V_{OUT} = \pm 500$ mV		3.0		V	%
t_s	0.1% Settling	$V_{OUT} = \pm 2.5V$, $A_V = -1$		15		V	ns
dG	Differential Gain	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.05		V	%
dP	Differential Phase	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.05		V	°
dG	Differential Gain	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.01		V	%
dP	Differential Phase	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.01		V	°
C_S	Channel Separation	EL2280C, EL2480C only, f = 5 MHz		85		V	dB

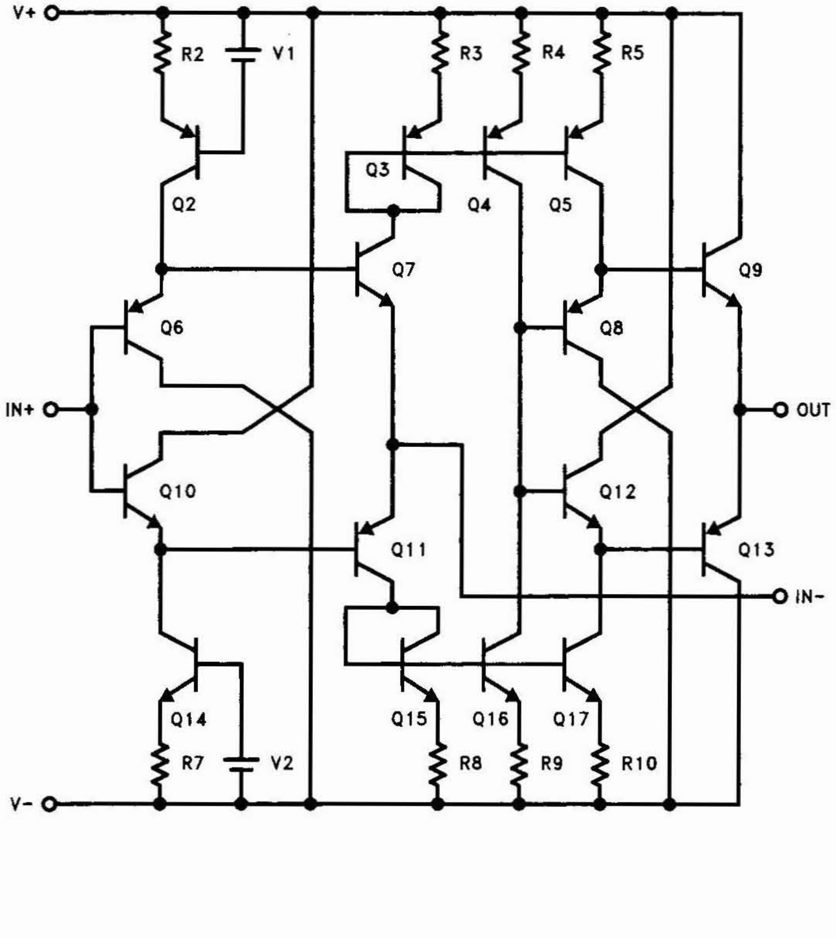
Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mV_{P-P}, f = 3.58 MHz.

Test Circuit (per Amplifier)


0.1 μF
+5V
V_IN
IN+
V_S+
EL2180C or
1/2 EL2280C or
1/4 EL2480C
OUT
V_OUT
V_S-
IN-
0.1 μF
-5V
R_L
150Ω
750Ω
750Ω
R_G
R_F

2180-3

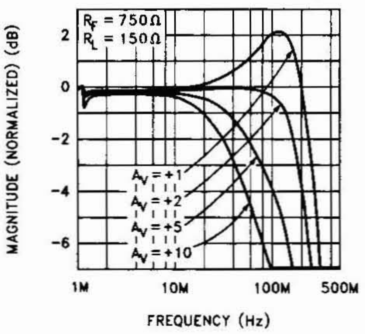
Simplified Schematic (per Amplifer)


V+
R2
V1
R3
R4
R5
Q3
Q2
Q4
Q5
Q7
Q9
Q6
Q8
IN+
OUT
Q10
Q12
Q11
Q13
IN-
Q14
Q15
Q16
Q17
R7
V2
R8
R9
R10
V-

2180-4

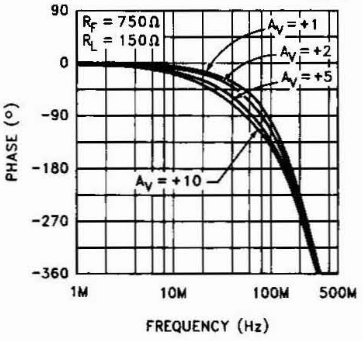
Typical Performance Curves

Non-Inverting Frequency Response (Gain) (PDIP and SOIC Packages)



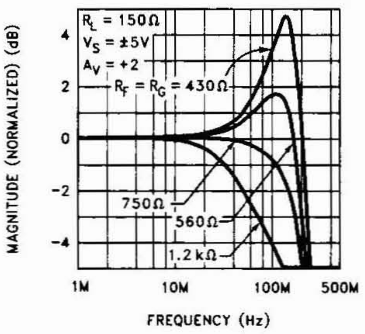
2180-5

Non-Inverting Frequency Response (Phase) (PDIP and SOIC Packages)



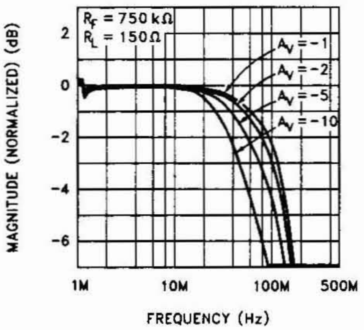
2180-6

Frequency Response for Various R_F and R_G (PDIP and SOIC Packages)



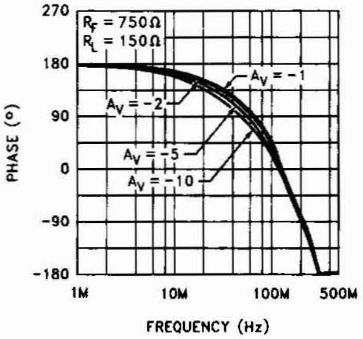
2180-7

Inverting Frequency Response (Gain) (PDIP and SOIC Packages)



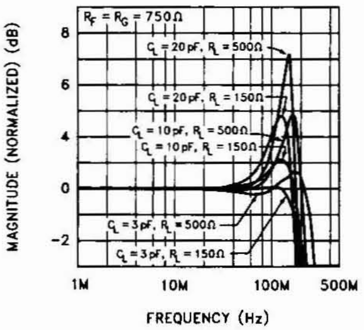
2180-8

Inverting Frequency Response (Phase) (PDIP and SOIC Packages)



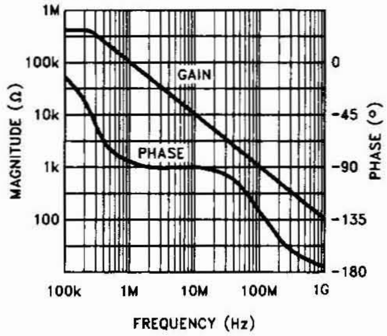
2180-9

Frequency Response for Various R_L and R_L (PDIP and SOIC Packages)



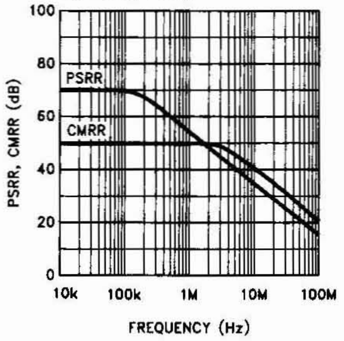
2180-10

Transimpedance (R_{OL}) vs Frequency



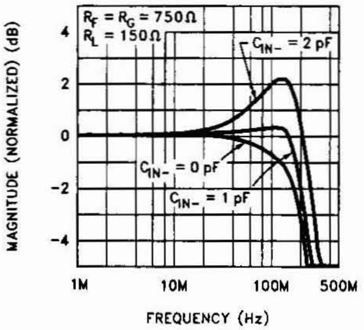
2180-11

PSRR and CMRR vs Frequency



2180-12

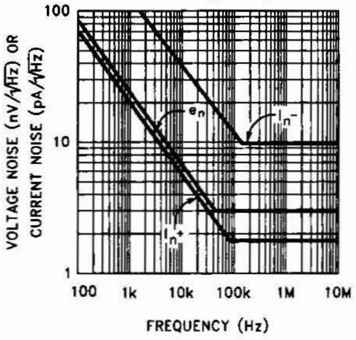
Frequency Response for Various C_{IN-}



2180-13

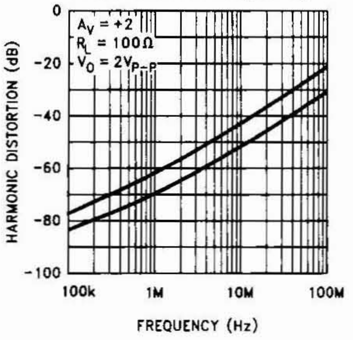
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency



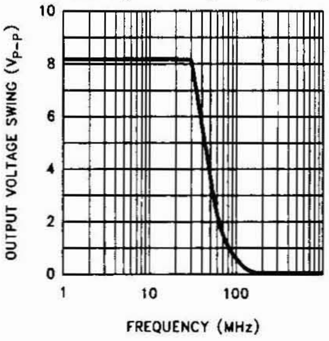
2180-14

2nd and 3rd Harmonic Distortion vs Frequency



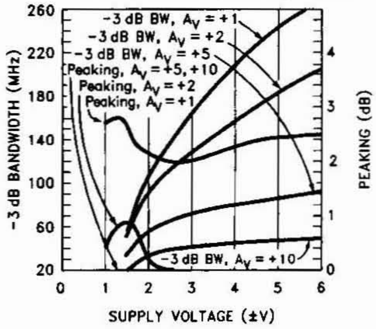
2180-15

Output Voltage Swing vs Frequency



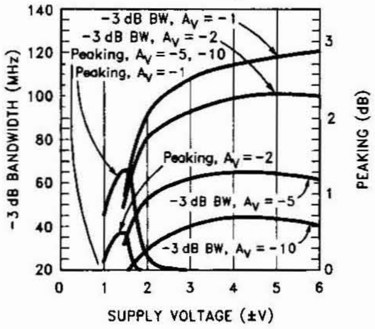
2180-16

−3 dB Bandwidth and Peaking vs Supply Voltage for Various Non-Inverting Gains



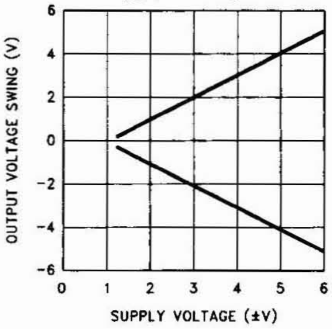
2180-17

−3 dB Bandwidth and Peaking vs Supply Voltage for Various Inverting Gains



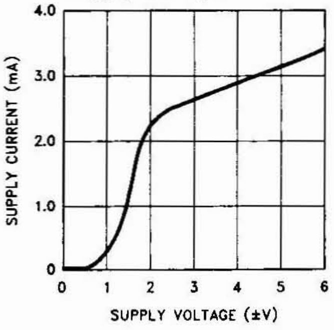
2180-18

Output Voltage Swing vs Supply Voltage



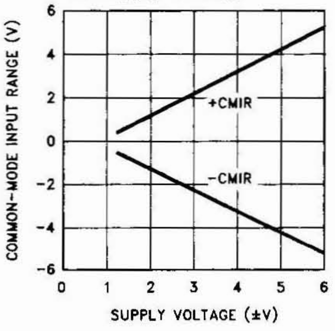
2180-19

Supply Current vs Supply Voltage



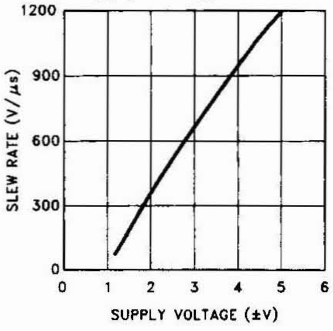
2180-20

Common-Mode Input Range vs Supply Voltage



2180-21

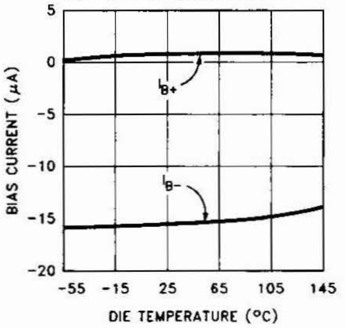
Slew Rate vs Supply Voltage



2180-22

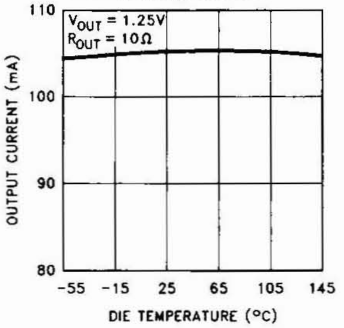
Typical Performance Curves — Contd.

Input Bias Current vs Die Temperature



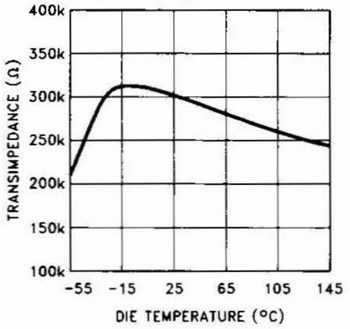
2180-23

Short-Circuit Current vs Die Temperature



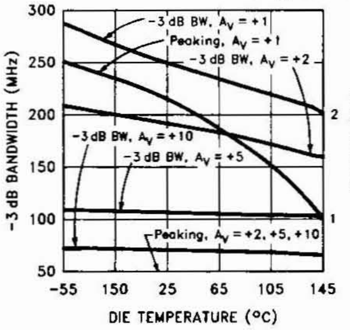
2180-24

Transimpedance (R_{OL}) vs Die Temperature



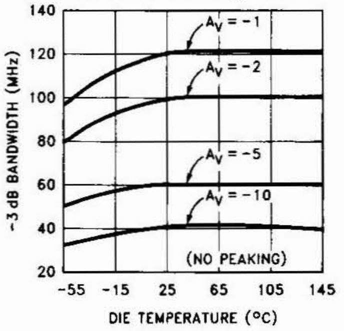
2180-25

−3 dB Bandwidth and Peaking vs Die Temperature for Various Non-Inverting Gains



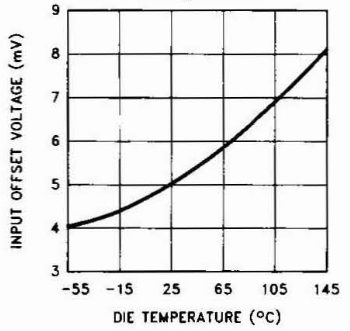
2180-26

−3 dB Bandwidth vs Die Temperature for Various Inverting Gains



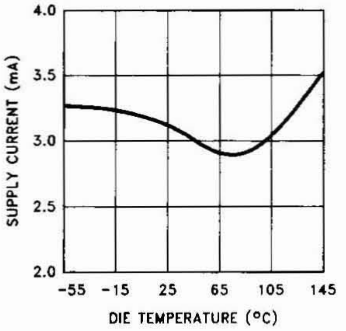
2180-27

Input Offset Voltage vs Die Temperature



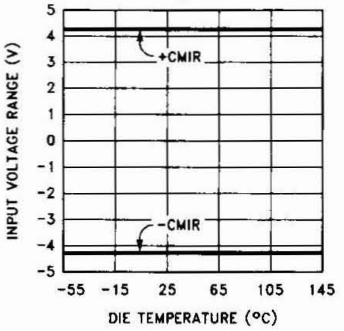
2180-28

Supply Current vs Die Temperature



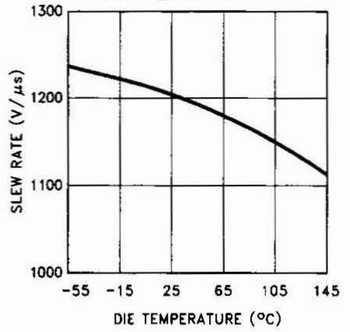
2180-29

Input Voltage Range vs Die Temperature



2180-30

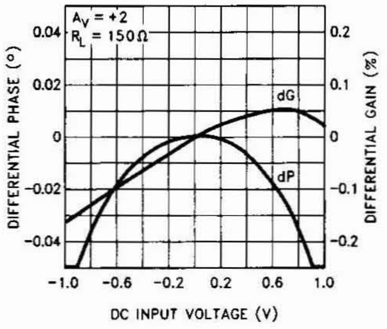
Slew Rate vs Die Temperature



2180-31

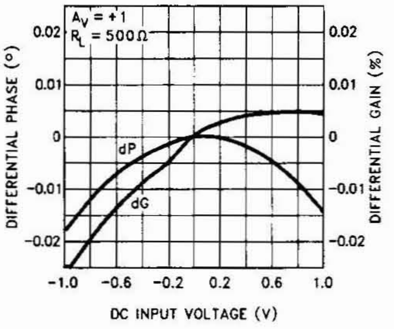
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



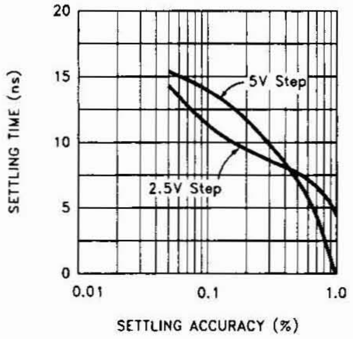
2180-32

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



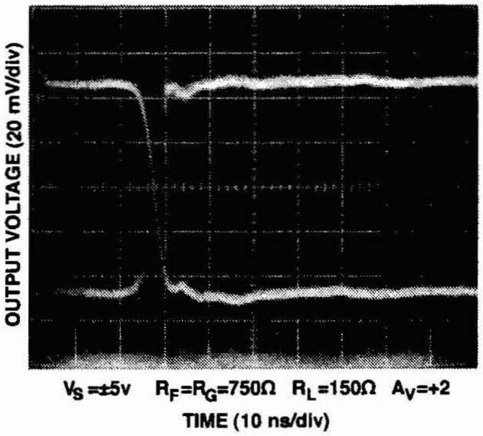
2180-33

Settling Time vs Settling Accuracy



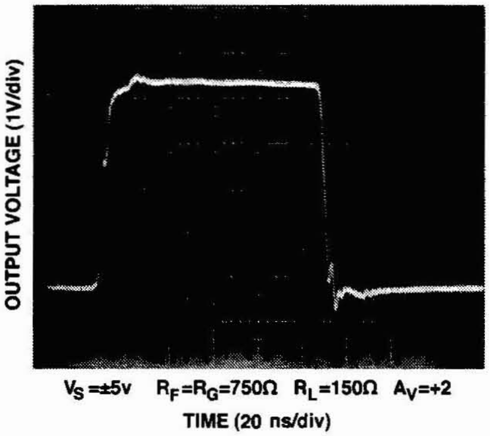
2180-34

Small-Signal Step Response



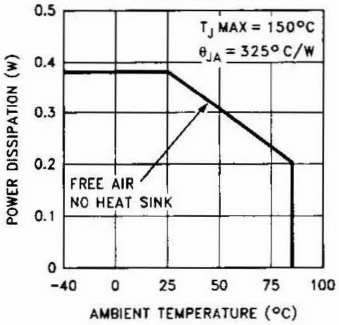
2180-35

Large-Signal Step Response



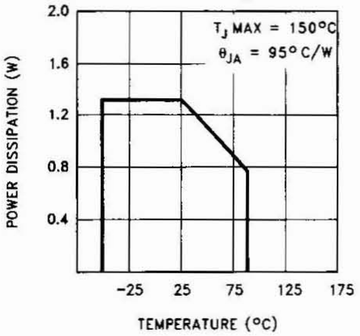
2180-36

5-Lead Plastic SOT23 Maximum Power Dissipation vs Ambient Temperature



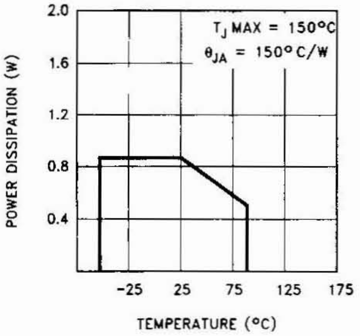
2180-47

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2180-37

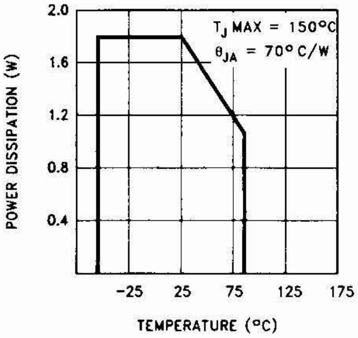
8-Lead SO Maximum Power Dissipation vs Ambient Temperature



2180-38

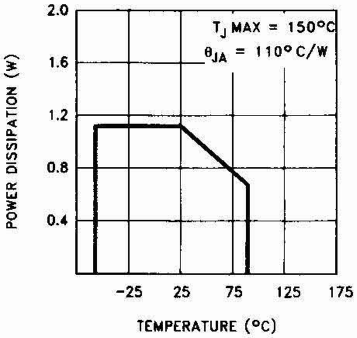
Typical Performance Curves — Contd.

14-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



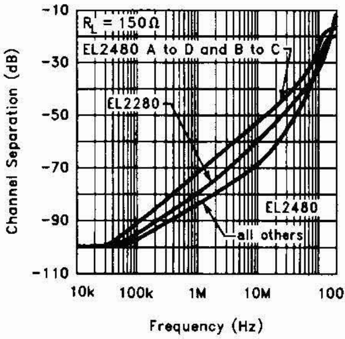
2180-39

14-Lead SO Maximum Power Dissipation vs Ambient Temperature



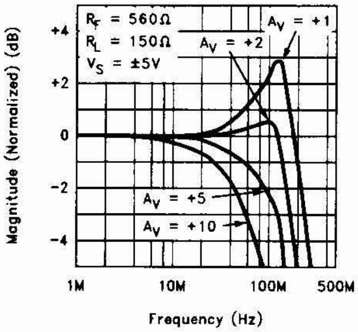
2180-40

Channel Separation vs Frequency



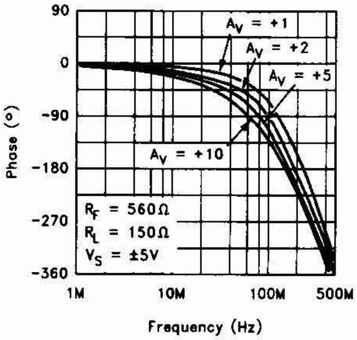
2180-41

Non-Inverting Frequency Response (Gain) (SOT23-5 Package)



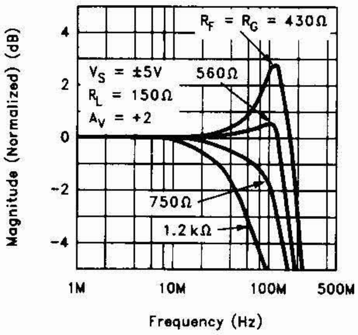
2180-48

Non-Inverting Frequency Response (Phase) (SOT23-5 Package)



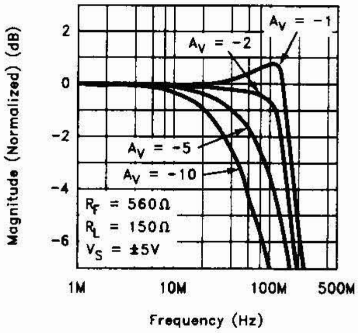
2180-49

Frequency Response for Various R_F and R_G (SOT23-5 Package)



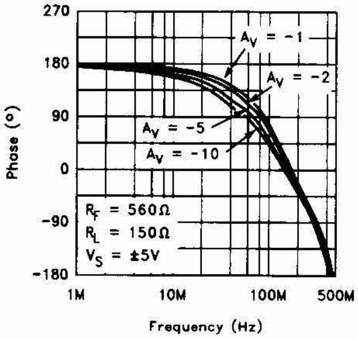
2180-50

Inverting Frequency Response (Gain) (SOT23-5 Package)



2180-51

Inverting Frequency Response (Phase) (SOT23-5 Package)



2180-52

Applications Information

Product Description

The EL2180C/EL2280C/EL2480C are current-feedback operational amplifiers that offer a wide −3 dB bandwidth of 250 MHz and a low supply current of 3 mA per amplifier. All of these products also feature high output current drive. The EL2180C can output 100 mA, while the EL2280C and the EL2480C can output 55 mA per amplifier. The EL2180C/EL2280C/EL2480C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to within 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2180C/EL2280C/EL2480C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their −3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2180C/EL2280C/EL2480C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For applications where board space is extremely critical, the EL2180C is available in the tiny 5-lead SOT23 package, which has a footprint 28% the size of an 8-lead SOIC. The EL2180C/EL2280C/EL2480C are each also available in industry standard pinouts in PDIP and SOIC packages.

For Single, Dual and Triple applications with disable, consider the EL2186C (8-Pin Single), EL2286C (14-Pin Dual) and EL2386C (16-Pin Triple). If lower power is required, refer to the EL2170C/EL2176C family which provides Singles, Duals, and Quads with 70 MHz of bandwidth while consuming 1 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.

Applications Information — Contd.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2180C/EL2280C/EL2480C have less bandwidth than expected.

The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various R_F and R_G, and Frequency Response for Various C_{IN-}.

Feedback Resistor Values

The EL2180C/EL2280C/EL2480C have been designed and specified at gains of +1 and +2 with $R_F = 750\Omega$ in PDIP and SOIC packages and $R_F = 560\Omega$ in SOT23-5 package. These values of feedback resistors give 250 MHz of −3 dB bandwidth at $A_V = +1$ with about 2.5 dB of peaking, and 180 MHz of −3 dB bandwidth at $A_V = +2$ with about 0.1 dB of peaking. The SOT23-5 package is characterized with a smaller value of feedback resistor, for a given bandwidth, to compensate for lower parasitics within both the package itself and the printed circuit board where it will be placed. Since the EL2180C/EL2280C/EL2480C are current-feedback amplifiers, it is also possible to change the value of R_F to get more bandwidth. As seen in the curve of Frequency Response For Various R_F and R_G, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2180C/EL2280C/EL2480C are current-feedback amplifiers, their gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2180C/EL2280C/EL2480C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases. Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of R_F below the specified 560Ω and 750Ω and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2180C/EL2280C/EL2480C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2180C/EL2280C/EL2480C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2180C/EL2280C/EL2480C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2180C/EL2280C/EL2480C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2180C/EL2280C/EL2480C have an input range which spans from 1V to 4V. The output range of the EL2180C/EL2280C/EL2480C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2180C/EL2280C/EL2480C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically comparable to the entire 3 mA supply current of each EL2180C/EL2280C/EL2480C amplifier! Special circuitry has been incorporated in the EL2180C/EL2280C/EL2480C to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.05% and 0.05° while driving 150Ω at a gain of +2.

Applications Information — Contd.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2180C/EL2280C/EL2480C have dG and dP specifications of 0.01% and 0.01° respectively while driving 500Ω at $A_V = +1$.

Output Drive Capability

In spite of its low 3 mA of supply current, the EL2180C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2280C and the EL2480C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2180C is capable of driving 50Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2280C and EL2480C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2180C/EL2280C/EL2480C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (R_F) to reduce the peaking.

Current Limiting

The EL2180C/EL2280C/EL2480C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2180C/EL2280C/EL2480C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when R_L falls below about 25Ω, it is important to calculate the maximum junction temperature (T_{Jmax}) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2180C/EL2280C/EL2480C to remain in the safe operating area. These parameters are calculated as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} * n * PD_{MAX}) \qquad [1]$$

where:

T_{MAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
n = Number of Amplifiers in the Package
PD_{MAX} = Maximum Power Dissipation of Each Amplifier in the Package.

PD_{MAX} for each amplifier can be calculated as follows:

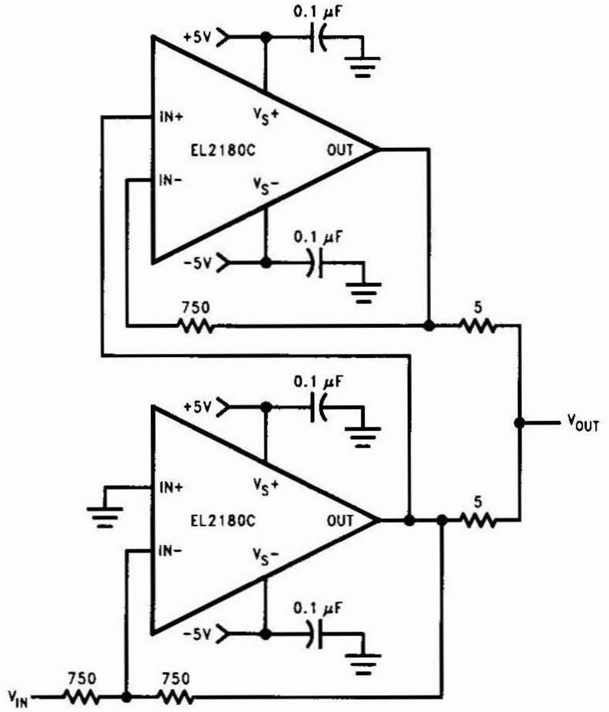
$$PD_{MAX} = (2 * V_S * I_{SMAX}) + (V_S - V_{OUTMAX}) * (V_{OUTMAX}/R_L)) \qquad [2]$$

where:

V_S = Supply Voltage
I_{SMAX} = Maximum Supply Current of 1 Amplifier
V_{OUTMAX} = Max. Output Voltage of the Application
R_L = Load Resistance

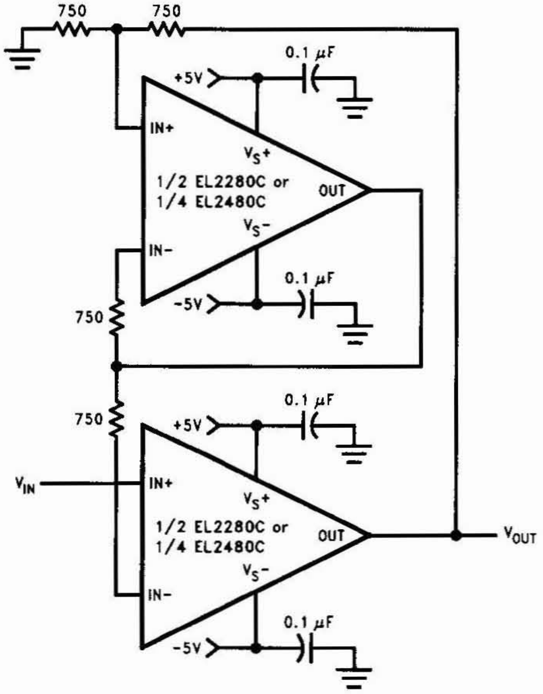
Typical Application Circuits

Inverting 200 mA Output Current Distribution Amplifier


+5V
0.1 μF
IN+
VS+
EL2180C
OUT
IN−
VS−
−5V
0.1 μF
750
5
0.1 μF
+5V
VOUT
IN+
VS+
EL2180C
OUT
IN−
VS−
5
0.1 μF
−5V
750
750
VIN

2180-42

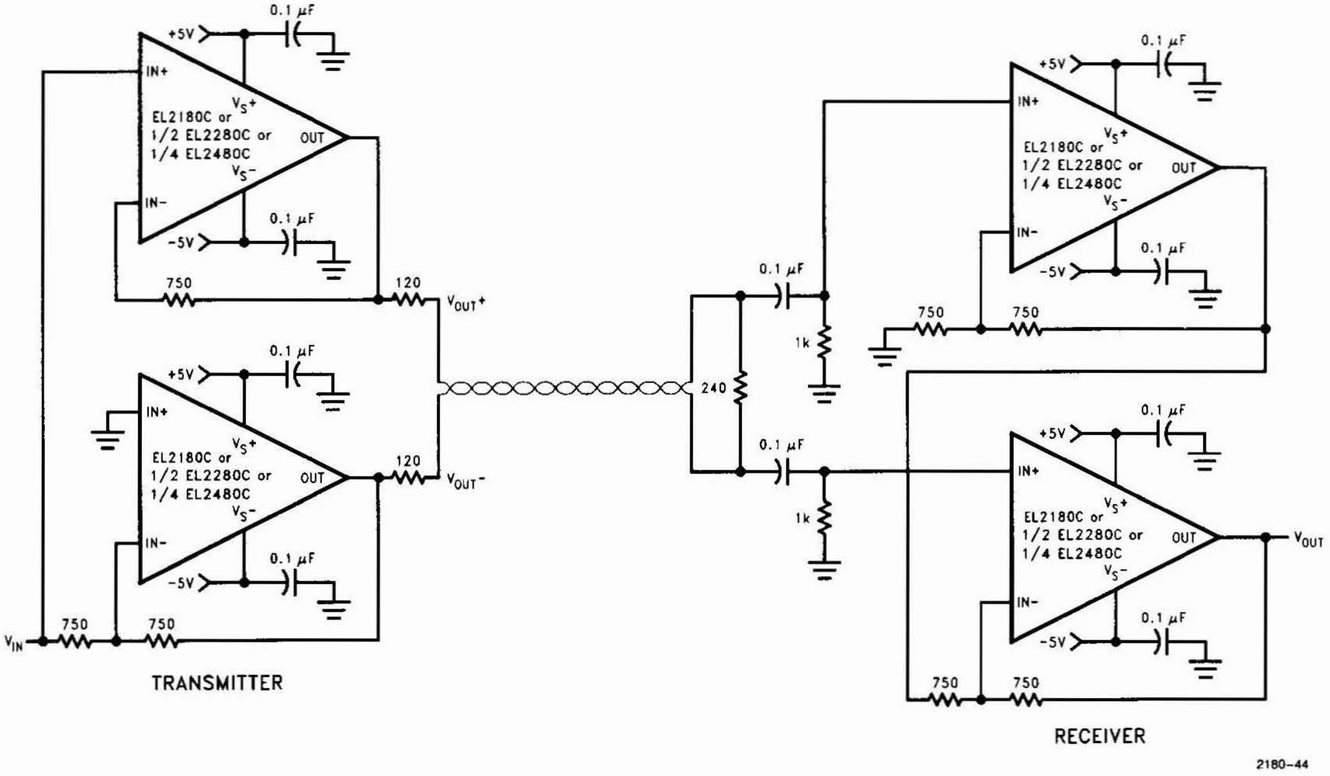
Fast-Settling Precision Amplifier


750
750
0.1 μF
+5V
IN+
VS+
1/2 EL2280C or
1/4 EL2480C
OUT
VS−
IN−
0.1 μF
750
−5V
0.1 μF
750
+5V
VIN
IN+
VS+
1/2 EL2280C or
1/4 EL2480C
OUT
VOUT
VS−
IN−
0.1 μF
−5V

2180-43

Typical Application Circuits — Contd.

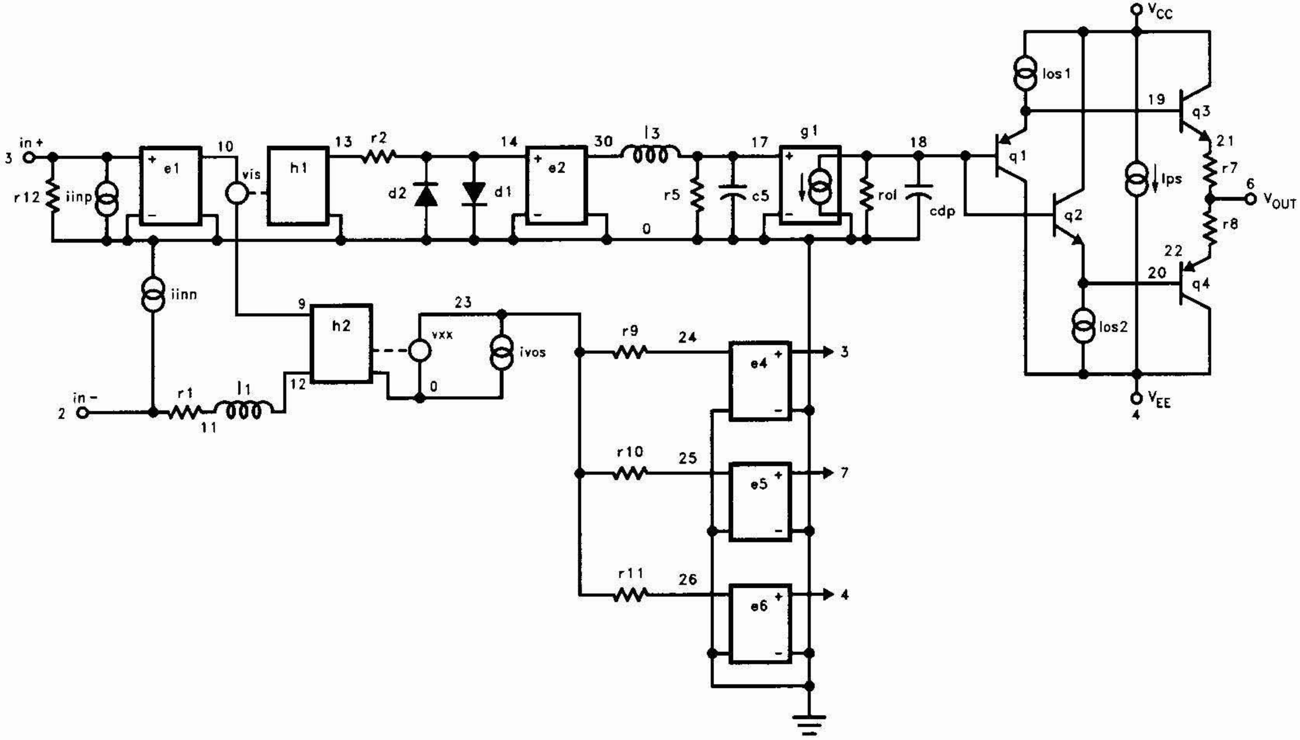
Differential Line-Driver/Receiver


+5V
0.1 µF
IN+
EL2180C or
1/2 EL2280C or
1/4 EL2480C
V_S+
V_S-
OUT
IN-
-5V
750
120
$V_{OUT}+$
$V_{OUT}-$
240
1k
V_{IN}
TRANSMITTER
RECEIVER
V_{OUT}
2180-44

EL2180C/EL2280C/EL2480C Macromodel

```
* EL2180 Macromodel
* Revision A, March 1995
* AC characteristics used: Rf = Rg = 750 ohms
* Connections:      +input
*                   |    -input
*                   |    |    +Vsupply
*                   |    |    |    -Vsupply
*                   |    |    |    |    output
*                   |    |    |    |    |
.subckt EL2180/el   3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 400
l1 11 12 25nH
iinp 3 0 1.5uA
iinm 2 0 3uA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 150nH
c5 17 0 0.8pF
r5 17 0 165
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 450K
cdp 18 0 0.675pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 1mA
ios2 20 4 1mA
*
* Supply Current
*
ips 7 4 0.2mA
*
* Error Terms
*
ivos 0 23 0.2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 -1.0
r9 24 23 316
r10 25 23 3.2K
r11 26 23 3.2K
*
* Models
*
.model qn npn(is=5e-15 bf=200 tf=0.01nS)
.model qp pnp(is=5e-15 bf=200 tf=0.01nS)
.model dclamp d(is=1e-30 ibv=0.266
+ bv=0.71v n=4)
.ends
```

EL2180C/EL2280C/EL2480C Macromodel — Contd.


in+
3
r12
iinp
e1
10
vis
h1
13
r2
d2
d1
14
e2
30
l3
r5
c5
17
g1
rol
18
cdp
0
iinn
9
h2
vxx
23
ivos
0
12
in−
2
r1
l1
11
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4
7
V_{CC}
los1
19
q3
q1
21
r7
lps
q2
6
V_{OUT}
r8
22
20
q4
los2
V_{EE}
4

2180-45

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2186C/EL2286C

250 MHz/3 mA Current Mode Feedback Amp w/Disable

Features

- Single (EL2186C) and dual (EL2286C) topologies
- 3 mA supply current (per amplifier)
- 250 MHz −3 dB bandwidth
- Low cost
- Fast disable
- Powers down to 0 mA
- Single- and dual-supply operation down to ±1.5V
- 0.05%/0.05° diff. gain/diff. phase into 150Ω
- 1200V/µs slew rate
- Large output drive current:
  100 mA (EL2186C)
  55 mA (EL2286C)
- Also available without disable in single (EL2180C), dual (EL2280C) and quad (EL2480C)
- Lower power EL2170C/EL2176C family also available (1 mA/ 70 MHz) in single, dual and quad

Applications

- Low power/battery applications
- HDSL amplifiers
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2186CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL2186CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL2286CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL2286CS	−40°C to +85°C	14-Pin SOIC	MDP0027

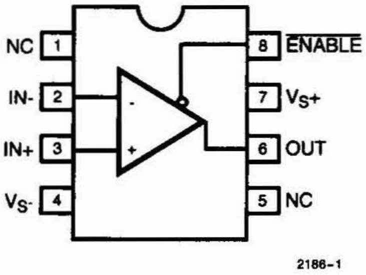
General Description

The EL2186C/EL2286C are single/dual current-feedback operational amplifiers which achieve a −3 dB bandwidth of 250 MHz at a gain of +1 while consuming only 3 mA of supply current per amplifier. They will operate with dual supplies ranging from ±1.5V to ±6V, or from single supplies ranging from +3V to +12V. The EL2186C/EL2286C also include a disable/power-down feature which reduces current consumption to 0 mA while placing the amplifier output in a high impedance state. In spite of its low supply current, the EL2286C can output 55 mA while swinging to ±4V on ±5V supplies. The EL2186C can output 100 mA with similar output swings. These attributes make the EL2186C/EL2286C excellent choices for low power and/or low voltage cable-driver, HDSL, or RGB applications.

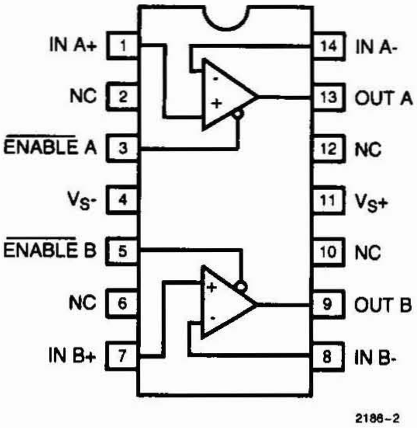
For Single, Dual and Quad applications without disable, consider the EL2180C (8-Pin Single), EL2280C (8-Pin Dual) or EL2480C (14-Pin Quad). For lower power applications where speed is still a concern, consider the EL2170C/El2176C family which also comes in similar Single, Dual and Quad configurations. The EL2170C/EL2176C family provides a −3 dB bandwidth of 70 MHz while consuming 1 mA of supply current per amplifier.

Connection Diagrams

EL2186C SO, P-DIP



EL2286C SO, P-DIP



Manufactured under U.S. Patent No. 5,418,495

May 1996 Rev. C

EL2186C/EL2286C

250 MHz/3 mA Current Mode Feedback Amp w/Disable

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+12.6V	Operating Junction Temperature	
Common-Mode Input Voltage	V_S- to V_S+	Plastic Packages	150°C
Differential Input Voltage	±6V	Output Current (EL2186C)	±120 mA
Current into +IN or −IN	±7.5 mA	Output Current (EL2286C)	±60 mA
Internal Power Dissipation	See Curves	Storage Temperature Range	−65°C to +150°C
Operating Ambient Temperature Range	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±5V, R_L = 150Ω, $\overline{\text{ENABLE}}$ = 0V, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			2.5	15	I	mV
TCV_{OS}	Average Input Offset Voltage Drift	Measured from T_{MIN} to T_{MAX}		5		V	μV/°C
dV_{OS}	V_{OS} Matching	EL2286C only		0.5		V	mV
$+I_{IN}$	+ Input Current			1.5	15	I	μA
$d+I_{IN}$	+ I_{IN} Matching	EL2286C only		20		V	nA
$-I_{IN}$	− Input Current			16	40	I	μA
$d-I_{IN}$	$-I_{IN}$ Matching	EL2286C only		2		V	μA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V	45	50		I	dB
−ICMR	− Input Current Common Mode Rejection	V_{CM} = ±3.5V		5	30	I	μA/V
PSRR	Power Supply Rejection Ratio	V_S is moved from ±4V to ±6V	60	70		I	dB
−IPSR	− Input Current Power Supply Rejection	V_S is moved from ±4V to ±6V		1	15	I	μA/V
R_{OL}	Transimpedance	V_{OUT} = ±2.5V	120	300		I	kΩ
$+R_{IN}$	+ Input Resistance	V_{CM} = ±3.5V	0.5	2		I	MΩ
$+C_{IN}$	+ Input Capacitance			1.2		V	pF
CMIR	Common Mode Input Range		±3.5	±4.0		I	V

DC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_L = 150\Omega$, $\overline{\text{ENABLE}} = 0V$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	$V_S = \pm 5$	±3.5	±4.0		I	V
		$V_S = +5$ Single-Supply, High		4.0		V	V
		$V_S = +5$ Single-Supply, Low		0.3		V	V
I_O	Output Current	EL2186C only	80	100		I	mA
		EL2286C only, per Amplifier	50	55		I	mA
I_S	Supply Current	$\overline{\text{ENABLE}} = 2.0V$, per Amplifier		3	6	I	mA
$I_{S(DIS)}$	Supply Current (Disabled)	$\overline{\text{ENABLE}} = 4.5V$		0	50	I	μA
$C_{OUT(DIS)}$	Output Capacitance (Disabled)	$\overline{\text{ENABLE}} = 4.5V$		4.4		V	pF
R_{EN}	Enable Pin Input Resistance	Measured at $\overline{\text{ENABLE}} = 2.0V, 4.5V$	45	85		I	kΩ
I_{IH}	Logic "1" Input Current	Measured at $\overline{\text{ENABLE}}$, $\overline{\text{ENABLE}} = 4.5V$		−0.04		V	μA
I_{IL}	Logic "0" Input Current	Measured at $\overline{\text{ENABLE}}$, $\overline{\text{ENABLE}} = 0V$		−53		V	μA
V_{DIS}	Minimum Voltage at $\overline{\text{ENABLE}}$ to Disable		4.5			I	V
V_{EN}	Maximum Voltage at $\overline{\text{ENABLE}}$ to Enable				2.0	I	V

AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = R_G = 750\Omega$, $R_L = 150\Omega$, $\overline{\text{ENABLE}} = 0V$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
−3 dB BW	−3 dB Bandwidth	$A_V = +1$		250		V	MHz
−3 dB BW	−3 dB Bandwidth	$A_V = +2$		180		V	MHz
0.1 dB BW	0.1 dB Bandwidth	$A_V = +2$		50		V	MHz
SR	Slew Rate	$V_{OUT} = \pm 2.5V$, $A_V = +2$	600	1200		IV	V/μs
t_r, t_f	Rise and Fall Time	$V_{OUT} = \pm 500$ mV		1.5		V	ns
t_{pd}	Propagation Delay	$V_{OUT} = \pm 500$ mV		1.5		V	ns
OS	Overshoot	$V_{OUT} = \pm 500$ mV		3.0		V	%
t_s	0.1% Settling	$V_{OUT} = \pm 2.5V$, $A_V = -1$		15		V	ns
dG	Differential Gain	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.05		V	%
dP	Differential Phase	$A_V = +2$, $R_L = 150\Omega$ (Note 1)		0.05		V	
dG	Differential Gain	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.01		V	%
dP	Differential Phase	$A_V = +1$, $R_L = 500\Omega$ (Note 1)		0.01		V	°
t_{ON}	Turn-On Time	$A_V = +2$, $V_{IN} = +1V$, $R_L = 150\Omega$ (Note 2)		40	100	I	ns
t_{OFF}	Turn-Off Time	$A_V = +2$, $V_{IN} = +1V$, $R_L = 150\Omega$ (Note 2)		1500	2000	I	ns
CS	Channel Separation	EL2286C only, f = 5 MHz		85		V	dB

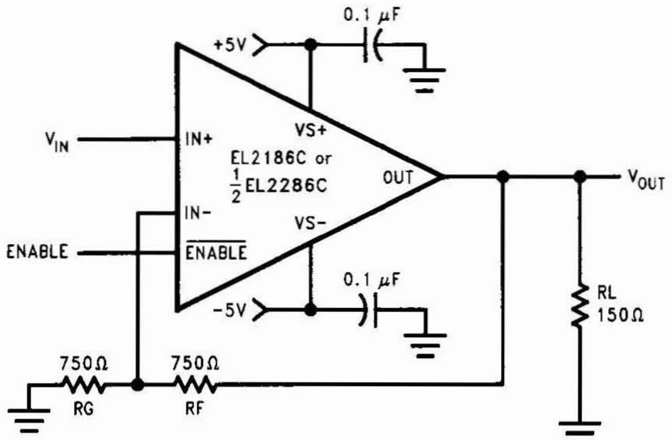
Note 1: DC offset from 0V to 0.714V, AC amplitude 286 mV_{P-P}, f = 3.58 MHz.

Note 2: Measured from the application of the logic signal until the output voltage is at the 50% point between initial and final values.

EL2186C/EL2286C

250 MHz/3 mA Current Mode Feedback Amp w/Disable

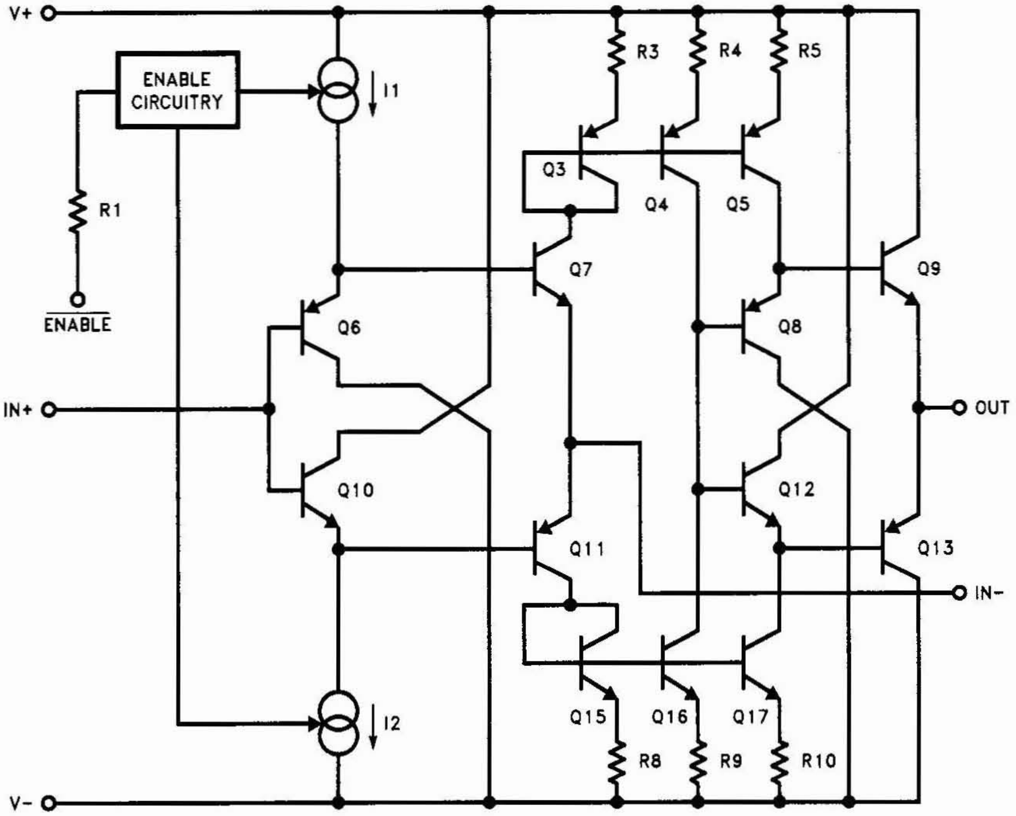
Test Circuit (per Amplifier)



0.1 μF
+5V
VS+
V_{IN}
IN+
EL2186C or
$\frac{1}{2}$EL2286C
OUT
V_{OUT}
IN−
VS−
ENABLE
$\overline{ENABLE}$
0.1 μF
−5V
RL
150Ω
750Ω
RG
750Ω
RF

2186-3

Simplified Schematic (per Amplifer)

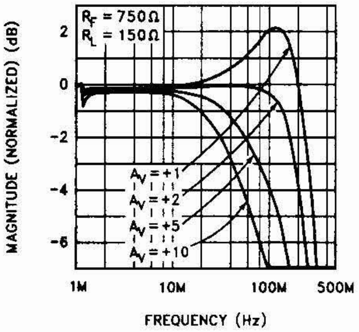


V+
R3
R4
R5
ENABLE CIRCUITRY
I1
Q3
Q4
Q5
R1
Q7
Q9
$\overline{ENABLE}$
Q6
Q8
IN+
OUT
Q10
Q12
Q11
Q13
IN−
Q15
Q16
Q17
I2
R8
R9
R10
V−

2186-4

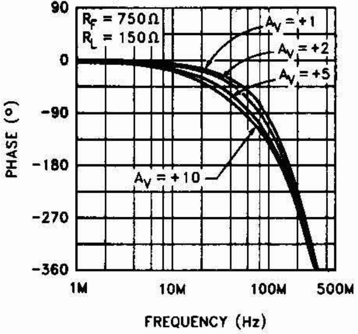
Typical Performance Curves

Non-Inverting Frequency Response (Gain)



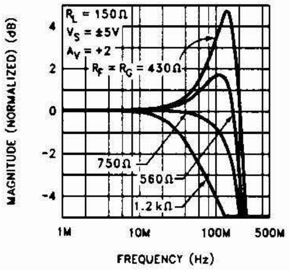
2186-5

Non-Inverting Frequency Response (Phase)



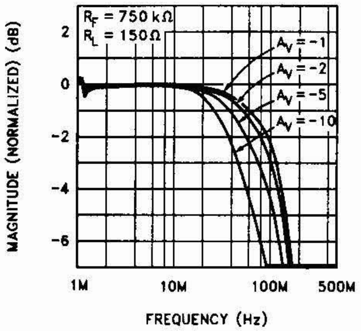
2186-6

Frequency Response for Various R_F and R_G



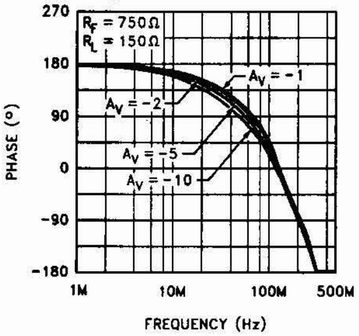
2186-7

Inverting Frequency Response (Gain)



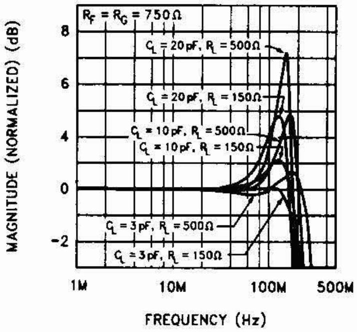
2186-8

Inverting Frequency Response (Phase)



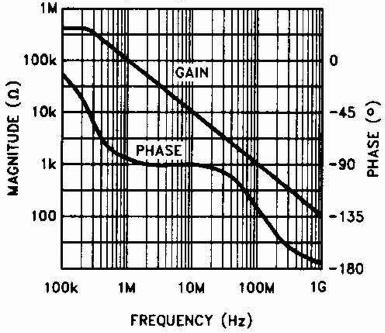
2186-9

Frequency Response for Various R_L and R_L



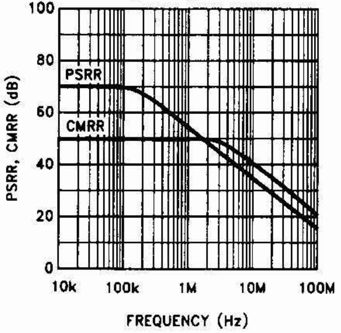
2186-10

Transimpedance (R_{OL}) vs Frequency



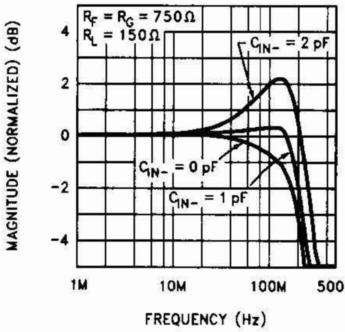
2186-11

PSRR and CMRR vs Frequency



2186-12

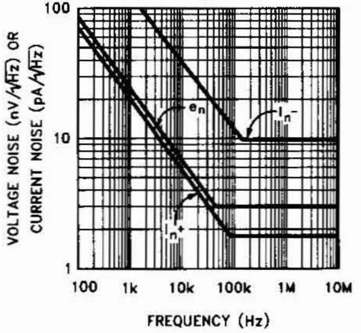
Frequency Response for Various $C_{IN}-$



2186-13

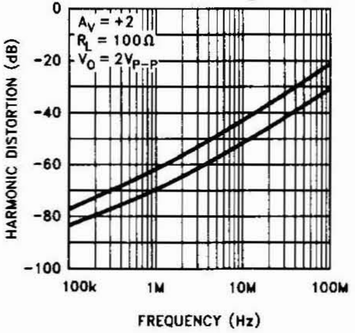
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency



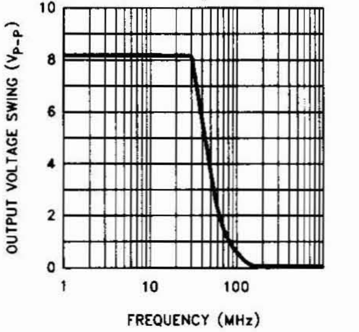
2186-14

2nd and 3rd Harmonic Distortion vs Frequency



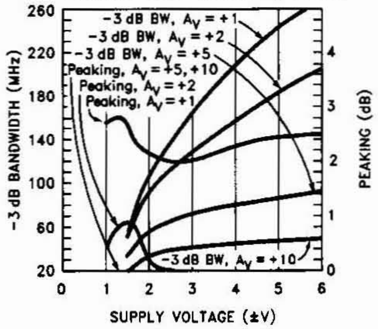
2186-15

Output Voltage Swing vs Frequency



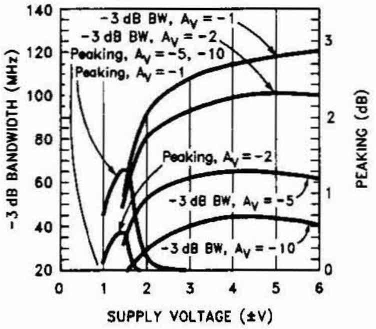
2186-16

−3 dB Bandwidth and Peaking vs Supply Voltage for Various Non-Inverting Gains



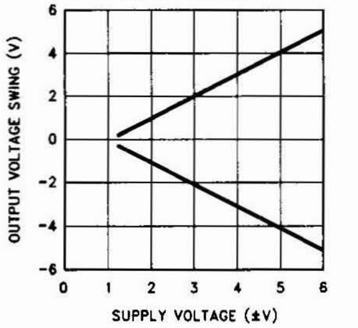
2186-17

−3 dB Bandwidth and Peaking vs Supply Voltage for Various Inverting Gains



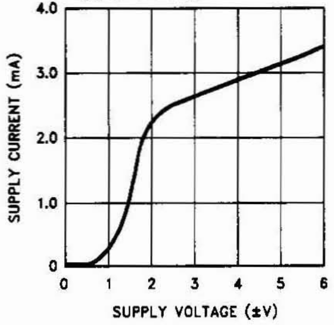
2186-18

Output Voltage Swing vs Supply Voltage



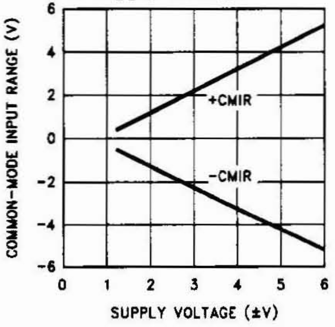
2186-19

Supply Current vs Supply Voltage



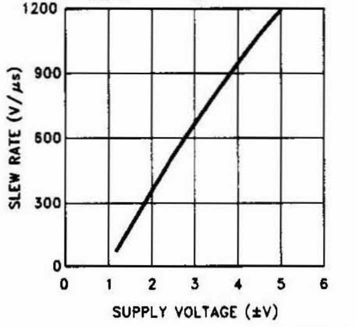
2186-20

Common-Mode Input Range vs Supply Voltage



2186-21

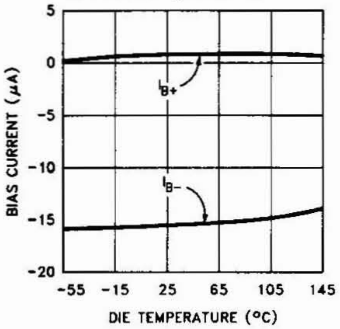
Slew Rate vs Supply Voltage



2186-22

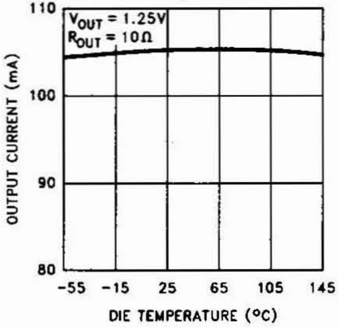
Typical Performance Curves — Contd.

Input Bias Current vs Die Temperature



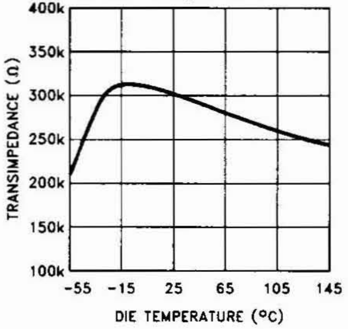
2186-23

Short-Circuit Current vs Die Temperature



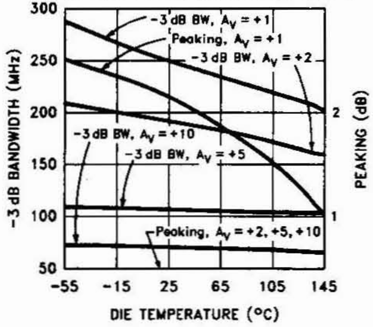
2186-24

Transimpedance (R_{OL}) vs Die Temperature



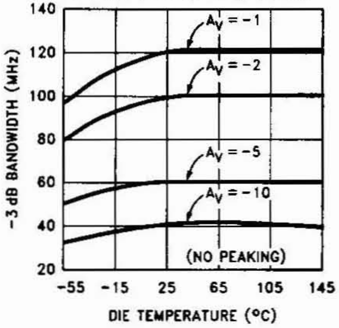
2186-25

−3 dB Bandwidth and Peaking vs Die Temperature for Various Non-Inverting Gains



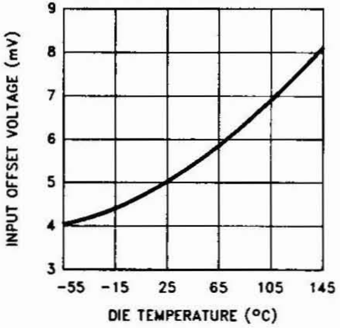
2186-26

−3 dB Bandwidth vs Die Temperature for Various Inverting Gains



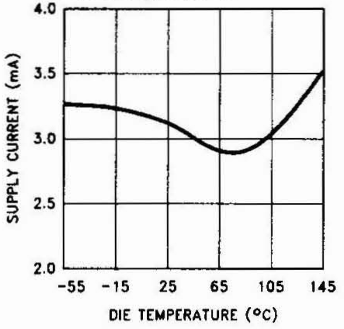
2186-27

Input Offset Voltage vs Die Temperature



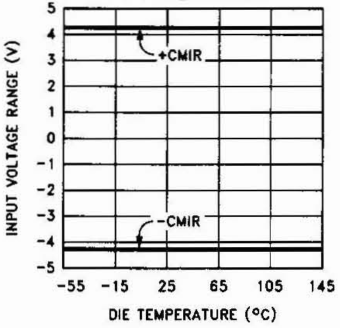
2186-28

Supply Current vs Die Temperature



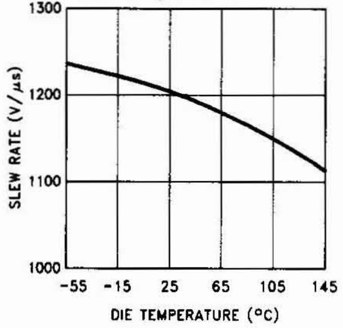
2186-29

Input Voltage Range vs Die Temperature



2186-30

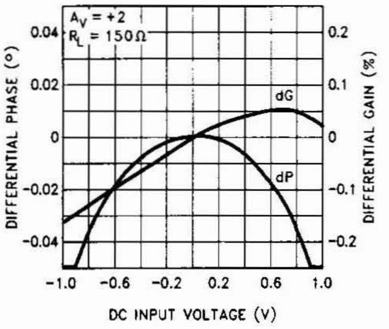
Slew Rate vs Die Temperature



2186-31

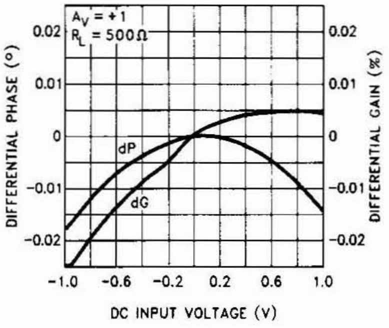
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



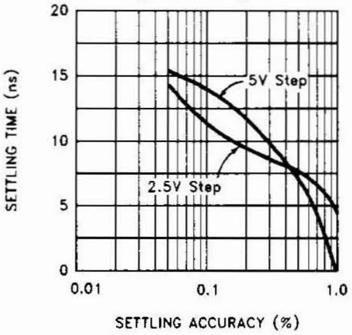
2186-32

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



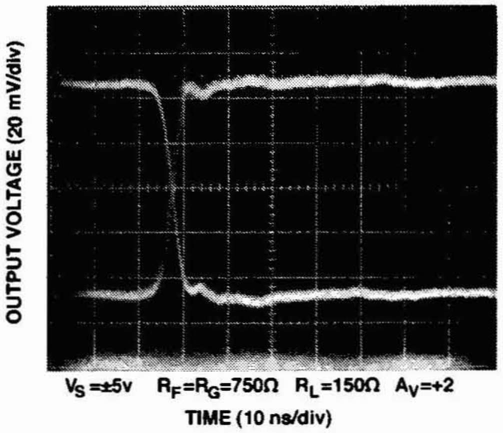
2186-33

Settling Time vs Settling Accuracy



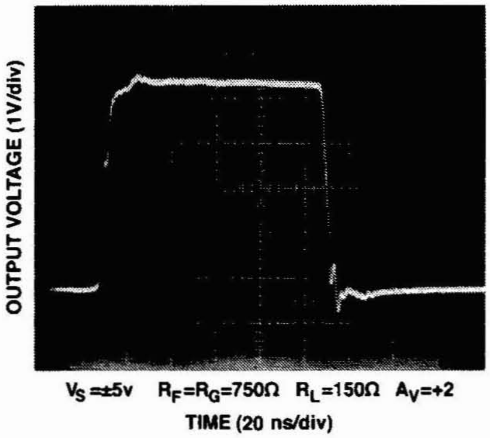
2186-34

Small-Signal Step Response



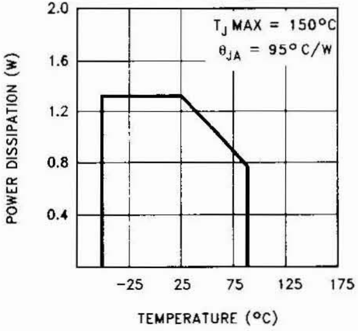
2186-35

Large-Signal Step Response



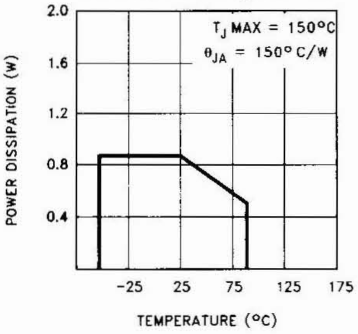
2186-36

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2186-37

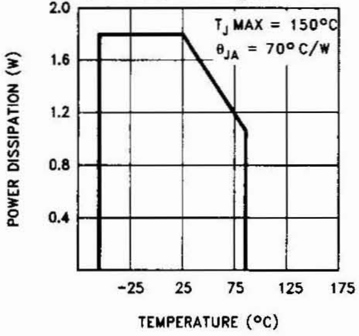
8-Lead SO Maximum Power Dissipation vs Ambient Temperature



2186-38

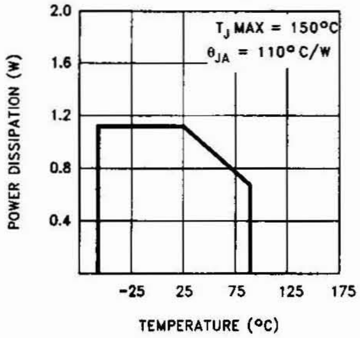
Typical Performance Curves — Contd.

14-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



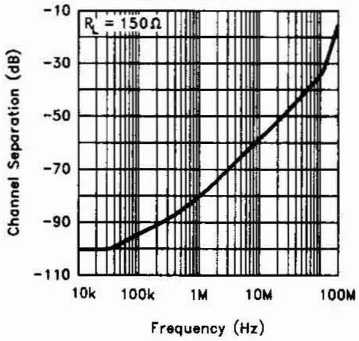
2186-39

14-Lead SO Maximum Power Dissipation vs Ambient Temperature



2186-40

Channel Separation vs Frequency (EL2286)



2186-41

Applications Information

Product Description

The EL2186C/EL2286C are current-feedback operational amplifiers that offer a wide −3 dB bandwidth of 250 MHz, a low supply current of 3 mA per amplifier and the ability to disable to 0 mA. Both products also feature high output current drive. The EL2186C can output 100 mA, while the EL2286C can output 55 mA per amplifier. The EL2186C/EL2286C work with supply voltages ranging from a single 3V to ±6V, and they are also capable of swinging to within 1V of either supply on the input and the output. Because of their current-feedback topology, the EL2186C/EL2286C do not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows their −3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2186C/EL2286C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For Single, Dual and Quad applications without disable, consider the EL2180C (8-Pin Single), EL2280C (8-Pin Dual) and EL2480C (14-Pin Quad). If lower power is required, refer to the EL2170C/EL2176C family which provides Singles, Duals, and Quads with 70 MHz of bandwidth while consuming 1 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Disable/Power-Down

The EL2186C/EL2286C amplifiers can be disabled, placing their output in a high-impedance state. When disabled, each amplifier's supply current is reduced to 0 mA. Each EL2186C/EL2286C amplifier is disabled when its $\overline{\text{ENABLE}}$ pin is floating or pulled up to within 0.5V of the positive supply. Similarly, each amplifier is enabled by pulling its $\overline{\text{ENABLE}}$ pin at least 3V below the positive supply. For ±5V supplies, this means that an EL2186C/EL2286C amplifier will be enabled when $\overline{\text{ENABLE}}$ is at 2V or less, and disabled when $\overline{\text{ENABLE}}$ is above 4.5V. Although the logic levels are not standard TTL, this choice of logic voltages allows the EL2186C/EL2286C to be enabled by tying $\overline{\text{ENABLE}}$ to ground, even in +3V single-supply applications. The $\overline{\text{ENABLE}}$ pin can be driven from CMOS outputs or open-collector TTL.

When enabled, supply current does vary somewhat with the voltage applied at $\overline{\text{ENABLE}}$. For example, with the supply voltages of the EL2186C at ±5V, if $\overline{\text{ENABLE}}$ is tied to −5V (rather than ground) the supply current will increase about 15% to 3.45 mA.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the

Applications Information — Contd.

same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.

The EL2186C/EL2286C have been specially designed to reduce power dissipation in the feedback network by using large 750Ω feedback and gain resistors. With the high bandwidths of these amplifiers, these large resistor values would normally cause stability problems when combined with parasitic capacitance, but by internally canceling the effects of a nominal amount of parasitic capacitance, the EL2186C/EL2286C remain very stable. For less experienced users, this feature makes the EL2186C/EL2286C much more forgiving, and therefore easier to use than other products not incorporating this proprietary circuitry.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2186C/EL2286C have less bandwidth than expected. In this case, the inverting input may have less parasitic capacitance than expected by the internal compensation circuitry of the EL2186C/EL2286C. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e.g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various R_F and R_G, and Frequency Response for Various C_{IN-}.

Feedback Resistor Values

The EL2186C/EL2286C have been designed and specified at gains of +1 and +2 with R_F = 750Ω. This value of feedback resistor gives 250 MHz of −3 dB bandwidth at A_V = +1 with about 2.5 dB of peaking, and 180 MHz of −3 dB bandwidth at A_V = +2 with about 0.1 dB of peaking. Since the EL2186C/EL2286C are current-feedback amplifiers, it is also possible to change the value of R_F to get more bandwidth. As seen in the curve of Frequency Response For Various R_F and R_G, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2186C/EL2286C are current-feedback amplifiers, their gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2186C/EL2286C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases.

Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of R_F below the specified 750Ω and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2186C/EL2286C have been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2186C/EL2286C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2176C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2186C/EL2286C have an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2186C/EL2286C have an input range which spans from 1V to 4V. The output range of the EL2186C/EL2286C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2186C/EL2286C, good Differ-

Applications Information — Contd.

ential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically comparable to the entire 3 mA supply current of each EL2186C/EL2286C amplifier! Special circuitry has been incorporated in the EL2186C/EL2286C to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.05% and 0.05° while driving 150Ω at a gain of +2.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2186C/EL2286C have dG and dP specifications of 0.01% and 0.01° respectively while driving 500Ω at $A_V = +1$.

Output Drive Capability

In spite of its low 3 mA of supply current, the EL2186C is capable of providing a minimum of ±80 mA of output current. Similarly, each amplifier of the EL2286C is capable of providing a minimum of ±50 mA. These output drive levels are unprecedented in amplifiers running at these supply currents. With a minimum ±80 mA of output drive, the EL2186C is capable of driving 50Ω loads to ±4V, making it an excellent choice for driving isolation transformers in telecommunications applications. Similarly, the ±50 mA minimum output drive of each EL2286C amplifier allows swings of ±2.5V into 50Ω loads.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2186C/EL2286C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (R_F) to reduce the peaking.

Current Limiting

The EL2186C/EL2286C have no internal current-limiting circuitry. If any output is shorted, it is possible to exceed the Absolute Maximum Ratings for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL2186C/EL2286C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when R_L falls below about 25Ω, it is important to calculate the maximum junction temperature (T_{Jmax}) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2186C/EL2286C to remain in the safe operating area. These parameters are calculated as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} * n * PD_{MAX}) \qquad [1]$$

where:

T_{MAX} = Maximum Ambient Temperature

θ_{JA} = Thermal Resistance of the Package

n = Number of Amplifiers in the Package

PD_{MAX} = Maximum Power Dissipation of Each Amplifier in the Package.

PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = (2 * V_S * I_{SMAX}) + (V_S - V_{OUTMAX}) * (V_{OUTMAX}/R_L) \qquad [2]$$

where:

V_S = Supply Voltage

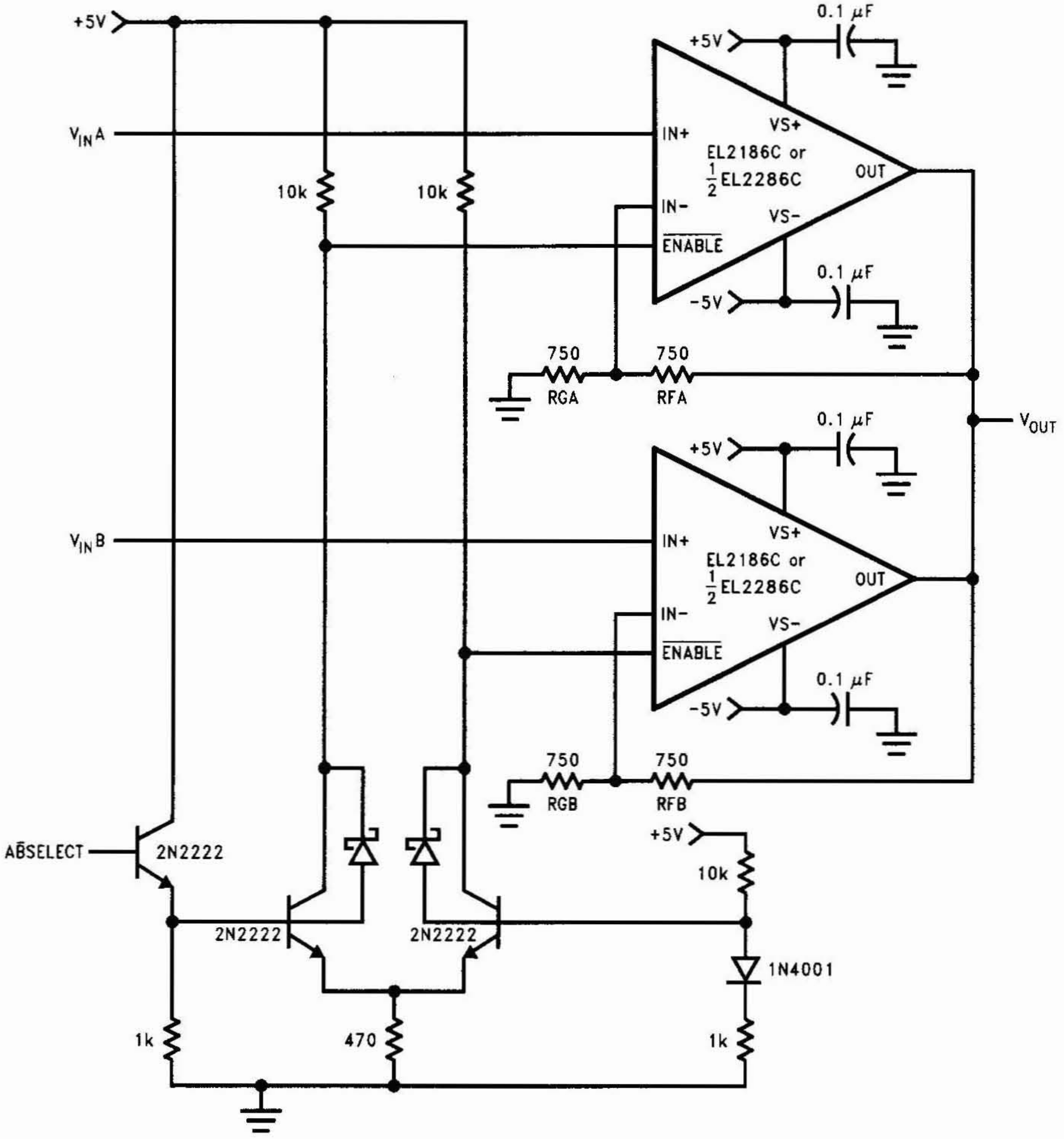
I_{SMAX} = Maximum Supply Current of 1 Amplifier

V_{OUTMAX} = Max. Output Voltage of the Application

R_L = Load Resistance

Typical Application Circuits

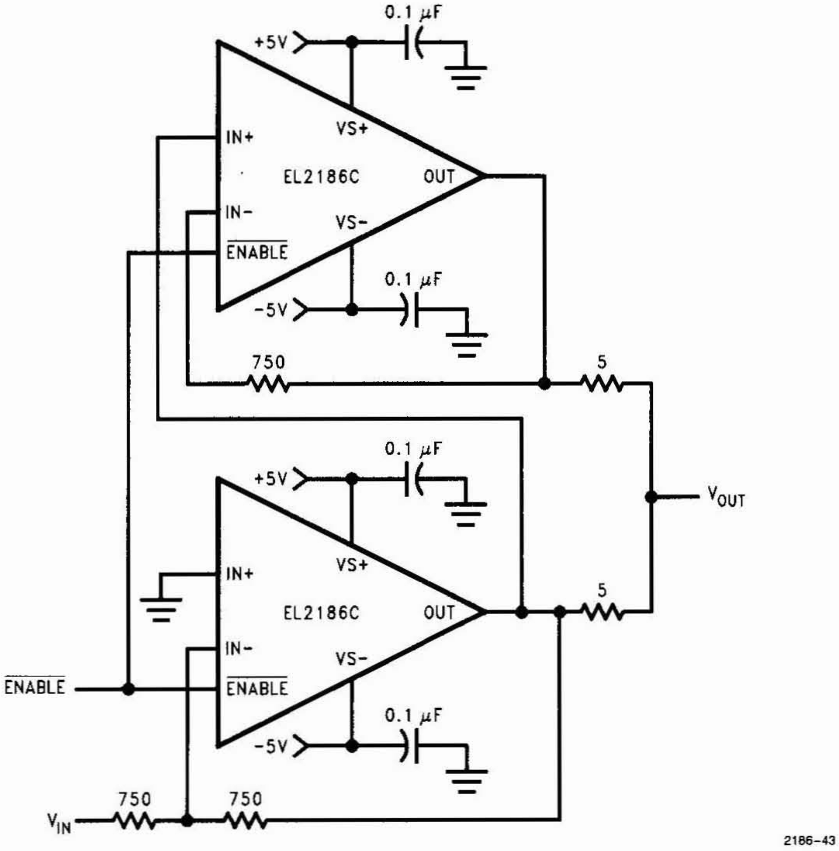
Low Power Multiplexer with Single-Ended TTL Input


+5V
$V_{IN}A$
$V_{IN}B$
10k
10k
IN+
IN−
ENABLE
VS+
VS−
OUT
EL2186C or
$\frac{1}{2}$ EL2286C
0.1 µF
+5V
−5V
750
750
RGA
RFA
RGB
RFB
V_{OUT}
A$\overline{B}$SELECT
2N2222
2N2222
2N2222
+5V
10k
1N4001
1k
470
1k

2186-42

Typical Application Circuits — Contd.

Inverting 200 mA Output Current Distribution Amplifier


0.1 μF
+5V
IN+
VS+
EL2186C
OUT
IN−
VS−
ENABLE
0.1 μF
−5V
750
5
0.1 μF
+5V
V_OUT
IN+
VS+
EL2186C
OUT
5
ENABLE
IN−
VS−
ENABLE
0.1 μF
−5V
V_IN
750
750
2186-43

DC Electrical Characteristics

V_S = ±5V, R_L = 150 Ω, $\overline{\text{ENABLE}}$ = 0V, T_A = 25°C unless otherwise specified — Contd.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
I_S	Supply Current—Enabled (per amplifier)	$\overline{\text{ENABLE}}$ = 2.0V		3	6	I	mA
$I_{S(DIS)}$	Supply Current—Disabled (per amplifier)	$\overline{\text{ENABLE}}$ = 4.5V		0	50	I	μA
$C_{OUT(DIS)}$	Output Capacitance—Disabled	$\overline{\text{ENABLE}}$ = 4.5V		4.4		V	pF
$R_{IN\text{-}EN}$	$\overline{\text{ENABLE}}$ Pin Input Resistance	$\overline{\text{ENABLE}}$ = 2.0V to 4.5V	45	85		I	kΩ
$I_{IH\text{-}EN}$	$\overline{\text{ENABLE}}$ Pin Input Current—High	$\overline{\text{ENABLE}}$ = 4.5V		−0.04		V	μA
$I_{IL\text{-}EN}$	$\overline{\text{ENABLE}}$ Pin Input Current—Low	$\overline{\text{ENABLE}}$ = 0V		−53		V	μA
V_{DIS}	Minimum Voltage at $\overline{\text{ENABLE}}$ to Disable		4.5			I	V
V_{EN}	Maximum Voltage at $\overline{\text{ENABLE}}$ to Enable				2.0	I	V

AC Electrical Characteristics

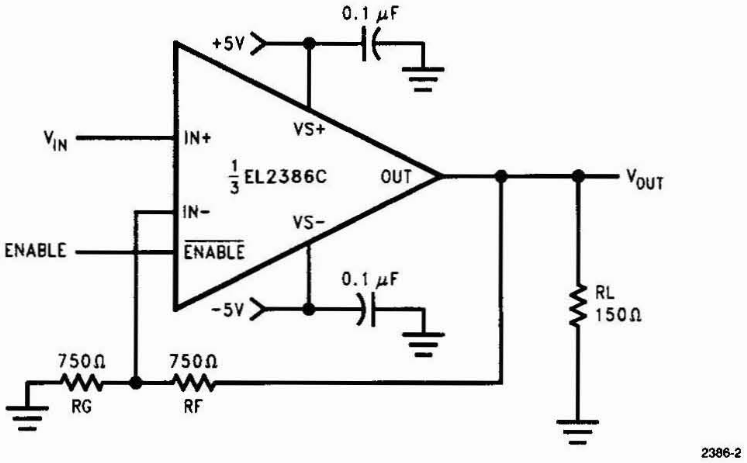
V_S = ±5V, R_F = R_G = 750 Ω, R_L = 150Ω, $\overline{\text{ENABLE}}$ = 0V, T_A = 25°C unless otherwise specified.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth	$A_V = +1$		250		V	MHz
		$A_V = +2$		180		V	MHz
BW	± 0.1 dB Bandwidth	$A_V = +2$		50		V	MHz
SR	Slew Rate	V_{OUT} = ±2.5V, Measured at ±1.25V	600	1200		IV	V/μs
t_R, t_F	Rise and Fall Time	V_{OUT} = ±500 mV		1.5		V	ns
t_{PD}	Propagation Delay	V_{OUT} = ±500 mV		1.5		V	ns
OS	Overshoot	V_{OUT} = ±500 mV		3.0		V	%
t_S	0.1% Settling	V_{OUT} = ±2.5V, $A_V = -1$		15		V	ns
dG	Differential Gain (Note 1)	$A_V = +2$, R_L = 150Ω		0.05		V	%
dP	Differential Phase (Note 1)	$A_V = +2$, R_L = 150Ω,		0.05		V	°
dG	Differential Gain (Note 1)	$A_V = +1$, R_L = 500Ω		0.01		V	%
dP	Differential Phase (Note 1)	$A_V = +1$, R_L = 500Ω		0.01		V	°
t_{ON}	Turn-On Time (Note 2)	$A_V = +2$, V_{IN} = +1V, R_L = 150Ω		40	100	I	ns
t_{OFF}	Turn-Off Time (Note 2)	$A_V = +2$, V_{IN} = +1V, R_L = 150Ω		800	2000	I	ns
CS	Channel Separation	f = 5 MHz		85		V	dB

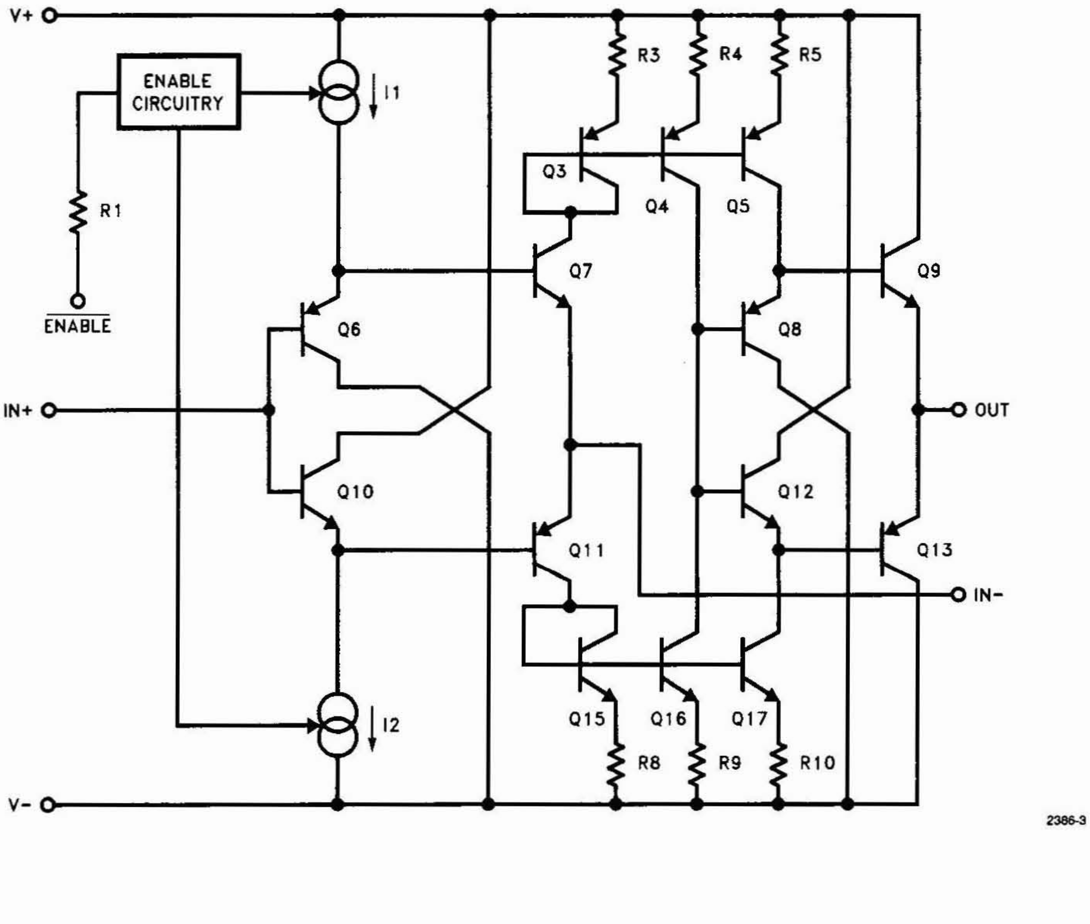
Note 1: DC offset from 0V to 0.714V, AC amplitude 286 $mV_{p\text{-}p}$, f = 3.58 MHz.

Note 2: Measured from the application of the logic signal until the output voltage is at the 50% point between initial and final values.

Test Circuit (per Amplifier)

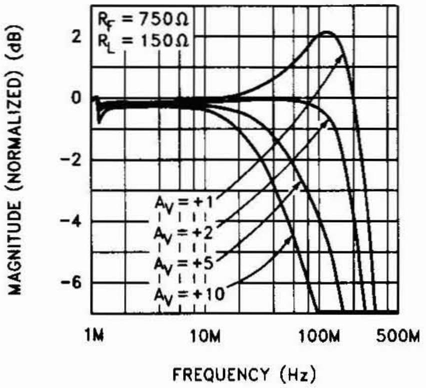

+5V
0.1 µF
VIN
IN+
VS+
1/3 EL2386C
OUT
VOUT
IN-
VS-
ENABLE
ENABLE
0.1 µF
-5V
RL
150Ω
750Ω
RG
750Ω
RF
2386-2

Simplified Schematic (per Amplifier)


V+
ENABLE CIRCUITRY
I1
R1
ENABLE
R3
R4
R5
Q3
Q4
Q5
Q7
Q9
Q6
Q8
IN+
OUT
Q10
Q12
Q11
Q13
IN-
Q15
Q16
Q17
I2
R8
R9
R10
V-
2386-3

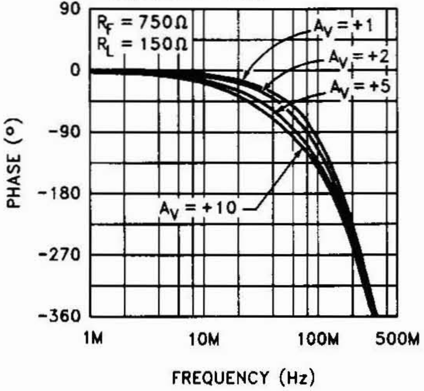
Typical Performance Curves — Contd.

Non-Inverting Frequency Response (Gain)



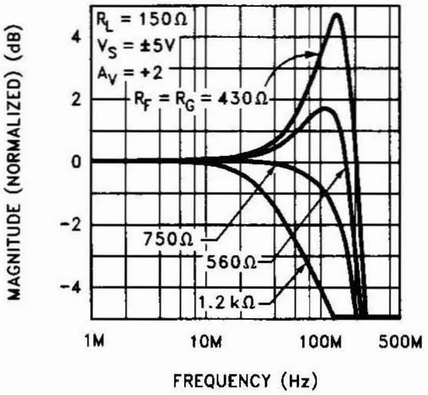
2386-4

Non-Inverting Frequency Response (Phase)



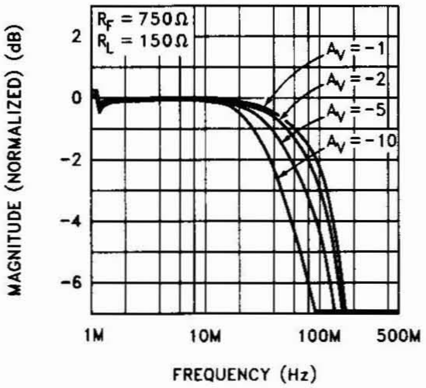
2386-5

Frequency Response for Various R_F and R_G



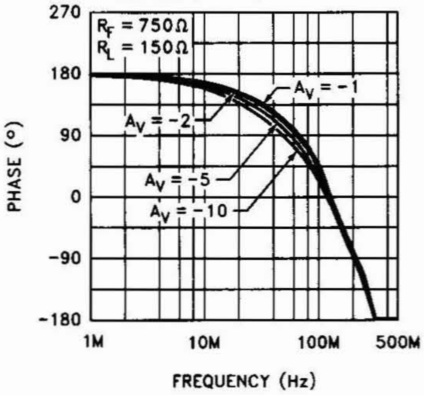
2386-6

Inverting Frequency Response (Gain)



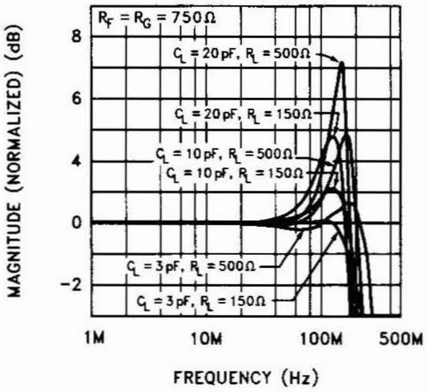
2386-7

Inverting Frequency Response (Phase)



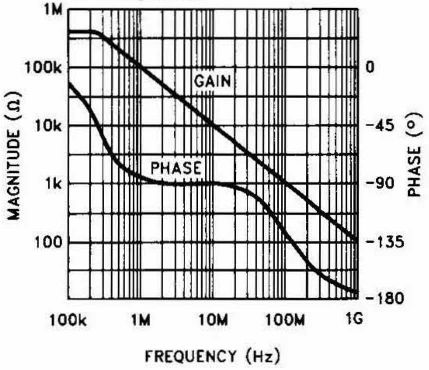
2386-8

Frequency Response for Various R_L and C_L



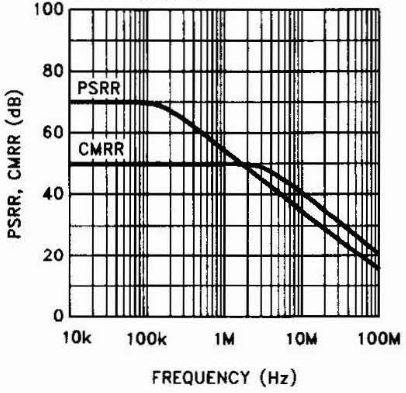
2386-9

Transimpedance (R_{OL}) vs Frequency



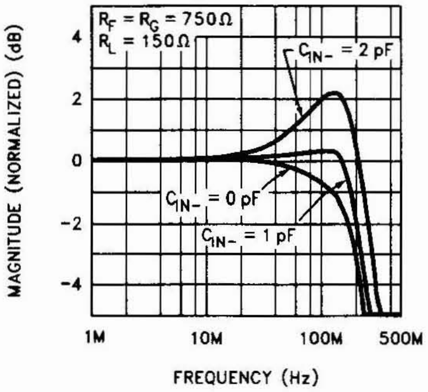
2386-10

PSRR and CMRR vs Frequency



2386-11

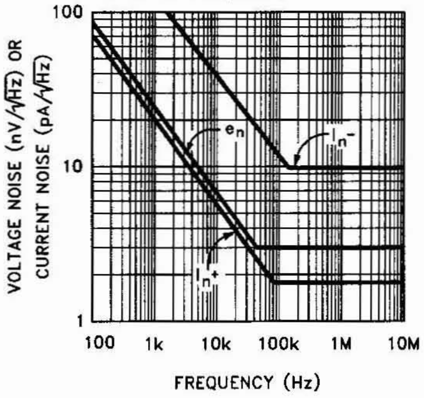
Frequency Response for Various $C_{IN}-$



2386-12

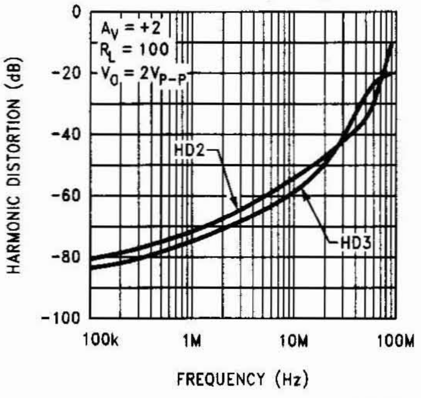
Typical Performance Curves — Contd.

Voltage and Current Noise vs Frequency



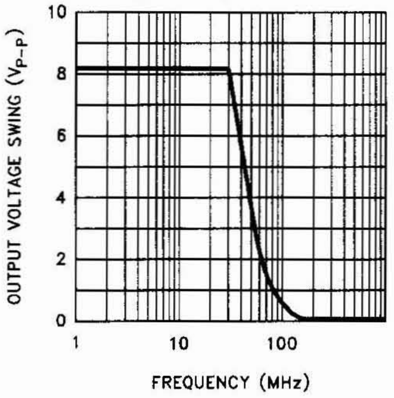
2386-13

2nd and 3rd Harmonic Distortion vs Frequency



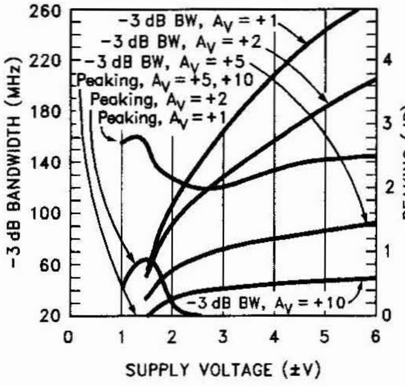
2386-14

Output Voltage Swing vs Frequency



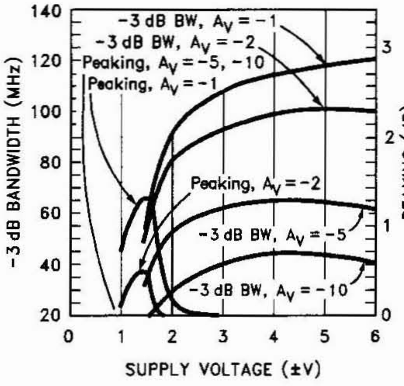
2386-15

−3 dB Bandwidth and Peaking vs Supply Voltage for Various Non-Inverting Gains



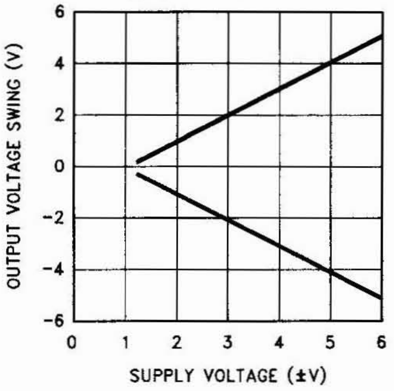
2386-16

−3 dB Bandwidth and Peaking vs Supply Voltage for Various Inverting Gains



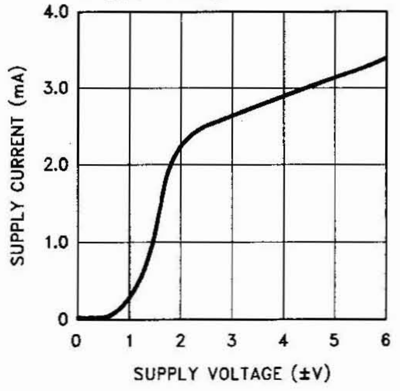
2386-17

Output Voltage Swing vs Supply Voltage



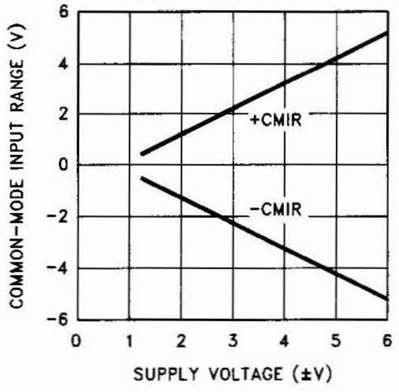
2386-18

Supply Current vs Supply Voltage



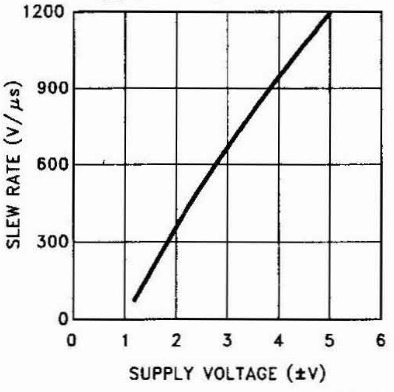
2386-19

Common-Mode Input Range vs Supply Voltage



2386-20

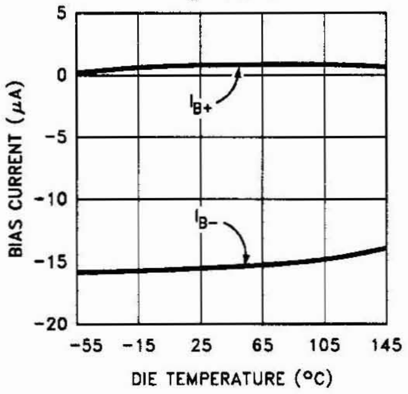
Slew Rate vs Supply Voltage



2386-21

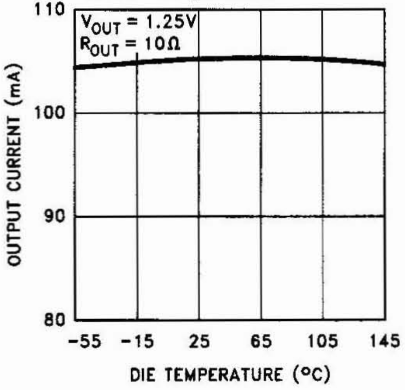
Typical Performance Curves — Contd.

Input Bias Current vs Die Temperature



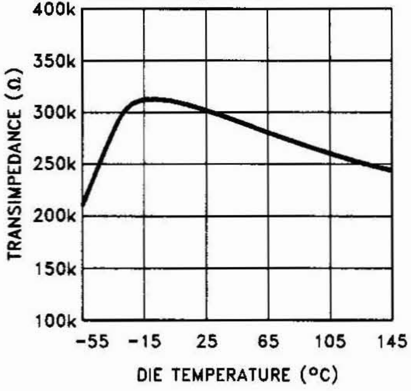
2386-22

Short-Circuit Current vs Die Temperature



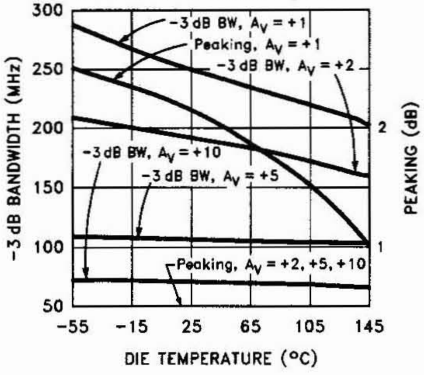
2386-23

Transimpedance (R_{OL}) vs Die Temperature



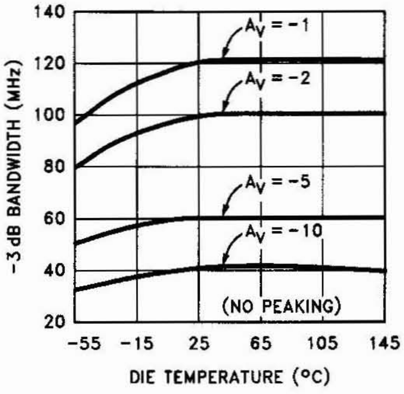
2386-24

−3 dB Bandwidth and Peaking vs Die Temperature for Various Non-Inverting Gains



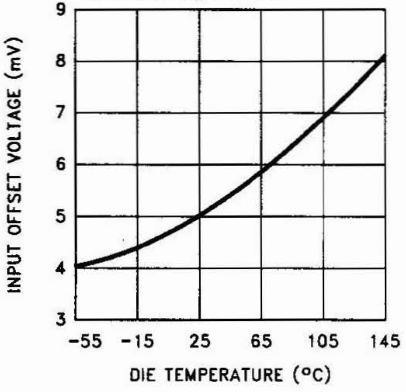
2386-25

−3 dB Bandwidth vs Die Temperature for Various Inverting Gains



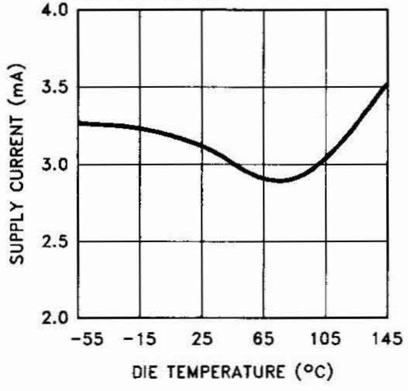
2386-26

Input Offset Voltage vs Die Temperature



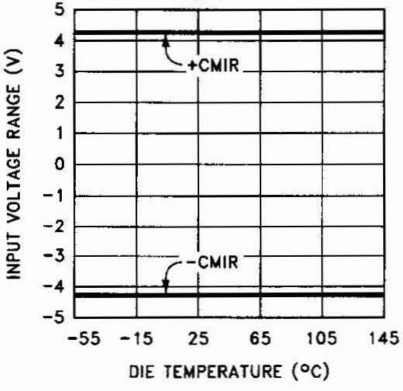
2386-27

Supply Current vs Die Temperature



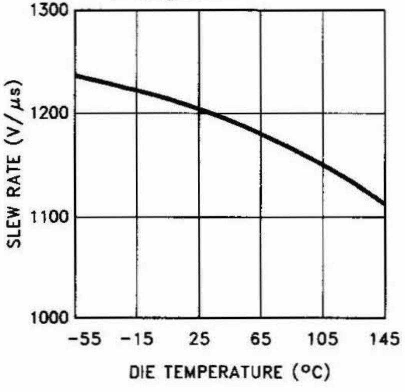
2386-28

Input Voltage Range vs Die Temperature



2386-29

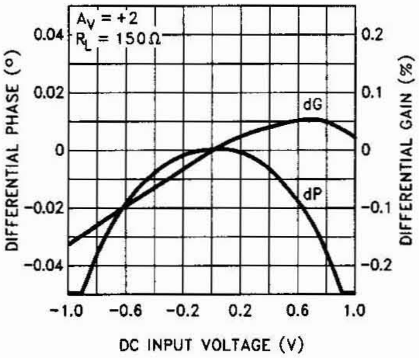
Slew Rate vs Die Temperature



2386-30

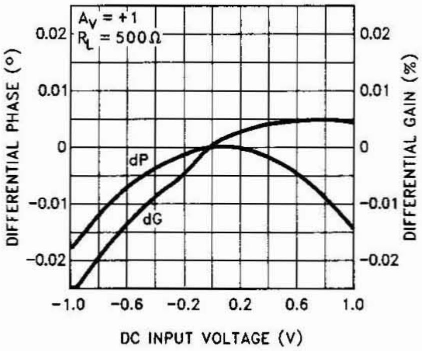
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



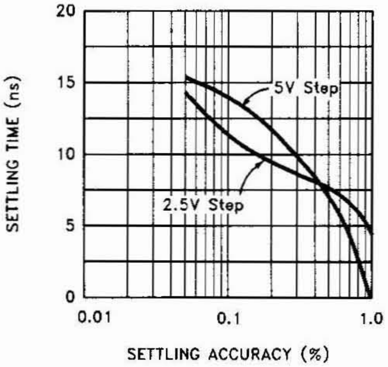
2386-31

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



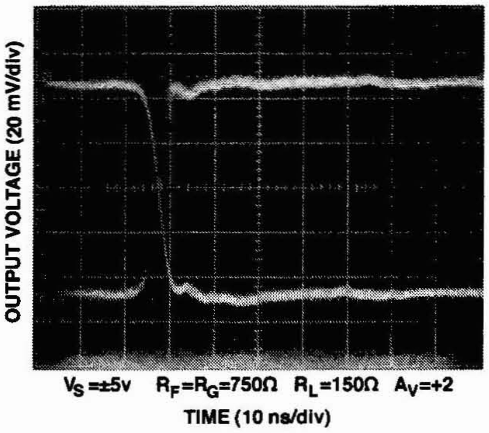
2386-32

Settling Time vs Settling Accuracy



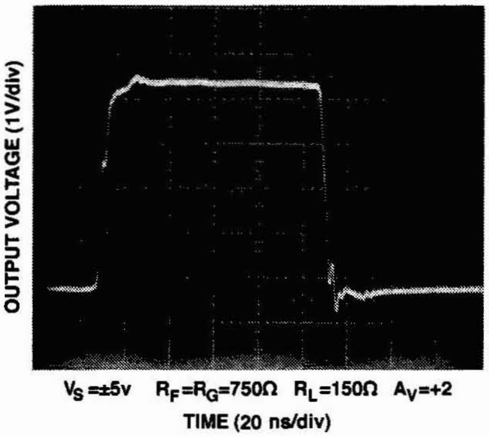
2386-33

Small-Signal Step Response



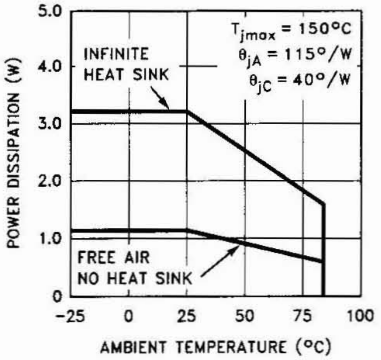
2386-34

Large-Signal Step Response



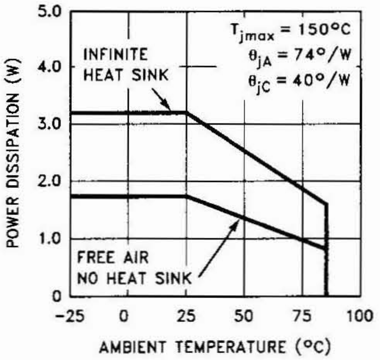
2386-35

16-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



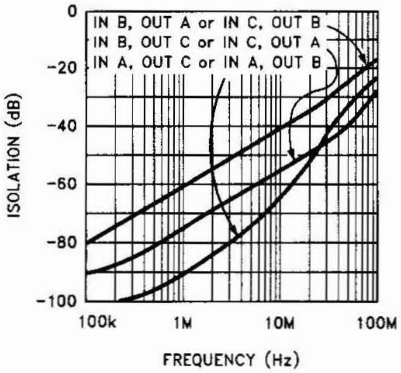
2386-36

16-Lead SO Maximum Power Dissipation vs Ambient Temperature



2386-37

Channel to Channel Isolation vs Frequency



2386-38

Applications Information

Product Description

The EL2386C is a current-feedback operational amplifier that offers a wide −3 dB bandwidth of 250 MHz, a low supply current of 3 mA per amplifier and the ability to power down to 0 mA. It also features high output current drive. The EL2386C can output 55 mA per amplifier. The EL2386C works with supply voltages ranging from a single 3V to ±6V, and it is also capable of swinging to within 1V of either supply on the input and the output. Because of its current-feedback topology, the EL2386C does not have the normal gain-bandwidth product associated with voltage-feedback operational amplifiers. This allows its −3 dB bandwidth to remain relatively constant as closed-loop gain is increased. This combination of high bandwidth and low power, together with aggressive pricing make the EL2386C the ideal choice for many low-power/high-bandwidth applications such as portable computing, HDSL, and video processing.

For Single and Dual applications, consider the EL2186C/EL2286C. For Single, Dual and Quad applications without disable, consider the EL2180C, EL2280C, or EL2480C, all in industry standard pin outs. The EL2180C also is available in the tiny SOT-23 package, which is 28% the size of an SO8 package. For lower power applications where speed is still a concern, consider the EL2170C/EL2176C family which also comes in similar Single, Dual and Quad configurations with 70 MHz of bandwidth while consuming 1 mA of supply current per amplifier.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.1 μF capacitor has been shown to work well when placed at each supply pin. For single supply operation, where pin 3 (V_{S-}) is connected to the ground plane, a single 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor across pins 14 and 3 will suffice.

For good AC performance, parasitic capacitance should be kept to a minimum especially at the inverting input (see the Capacitance at the Inverting Input section). Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Carbon or Metal-Film resistors are acceptable with the Metal-Film resistors giving slightly less peaking and bandwidth because of their additional series inductance. Use of sockets, particularly for the SO package should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

Disable/Power-Down

The EL2386C amplifier can be disabled, placing its output in a high-impedance state. When disabled, the supply current is reduced to 0 mA. The EL2386C is disabled when its $\overline{\text{ENABLE}}$ pin is floating or pulled up to within 0.5V of the positive supply. Similarly, the amplifier is enabled by pulling its $\overline{\text{ENABLE}}$ pin at least 3V below the positive supply. For ±5V supplies, this means that an EL2386C amplifier will be enabled when $\overline{\text{ENABLE}}$ is at 2V or less, and disabled when $\overline{\text{ENABLE}}$ is above 4.5V. Although the logic levels are not standard TTL, this choice of logic voltages allows the EL2386C to be enabled by tying $\overline{\text{ENABLE}}$ to ground, even in +3V single-supply applications. The $\overline{\text{ENABLE}}$ pin can be driven from CMOS outputs or open-collector TTL.

When enabled, supply current does vary somewhat with the voltage applied at $\overline{\text{ENABLE}}$. For example, with the supply voltages of the EL2186C at ±5V, if $\overline{\text{ENABLE}}$ is tied to −5V (rather than ground) the supply current will increase about 15% to 3.45 mA.

Applications Information — Contd.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage- or current-feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. The use of large value feedback and gain resistors further exacerbates the problem by further lowering the pole frequency.

The experienced user with a large amount of PC board layout experience may find in rare cases that the EL2386C has less bandwidth than expected. In this case, the inverting input may have less parasitic capacitance than expected. The reduction of feedback resistor values (or the addition of a very small amount of external capacitance at the inverting input, e. g. 0.5 pF) will increase bandwidth as desired. Please see the curves for Frequency Response for Various R_F and R_G, and Frequency Response for Various C_{IN-}.

Feedback Resistor Values

The EL2386C has been designed and specified at gains of +1 and +2 with $R_F = 750\Omega$. This value of feedback resistor gives 250 MHz of −3 dB bandwidth at $A_V = +1$ with about 2.5 dB of peaking, and 180 MHz of −3 dB bandwidth at $A_V = +2$ with about 0.1 dB of peaking. Since the EL2386C is a current-feedback amplifier, it is also possible to change the value of R_F to get more bandwidth. As seen in the curve of Frequency Response For Various R_F and R_G, bandwidth and peaking can be easily modified by varying the value of the feedback resistor.

Because the EL2386C is a current-feedback amplifier, its gain-bandwidth product is not a constant for different closed-loop gains. This feature actually allows the EL2386C to maintain about the same −3 dB bandwidth, regardless of closed-loop gain. However, as closed-loop gain is increased, bandwidth decreases slightly while stability increases. Since the loop stability is improving with higher closed-loop gains, it becomes possible to reduce the value of R_F below the specified 750Ω and still retain stability, resulting in only a slight loss of bandwidth with increased closed-loop gain.

Supply Voltage Range and Single-Supply Operation

The EL2386C has been designed to operate with supply voltages having a span of greater than 3V, and less than 12V. In practical terms, this means that the EL2386C will operate on dual supplies ranging from ±1.5V to ±6V. With a single-supply, the EL2386C will operate from +3V to +12V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL2386C has an input voltage range that extends to within 1V of either supply. So, for example, on a single +5V supply, the EL2386C has an input range which spans from 1V to 4V. The output range of the EL2386C is also quite large, extending to within 1V of the supply rail. On a ±5V supply, the output is therefore capable of swinging from −4V to +4V. Single-supply output range is even larger because of the increased negative swing due to the external pull-down resistor to ground. On a single +5V supply, output voltage range is about 0.3V to 4V.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. Until the EL2386C, good Differential Gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). These currents were typically comparable to the entire 3 mA supply current of each EL2386C amplifier! Spe-

Applications Information — Contd.

cial circuitry has been incorporated in the EL2386C to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.05% and 0.05° while driving 150Ω at a gain of +2.

Video Performance has also been measured with a 500Ω load at a gain of +1. Under these conditions, the EL2386C has dG and dP specifications of 0.01% and 0.01° respectively while driving 500Ω at $A_V = +1$.

For complete curves, see the Differential Gain and Differential Phase vs Input Voltage curves.

Output Drive Capability

In spite of its low 3 mA of supply current per amplifier, the EL2386C is capable of providing a minimum of ±50 mA of output current. This output drive level is unprecedented in amplifiers running at these supply currents. With a minimum ±50 mA of output drive, the EL2386C is capable of driving 50Ω loads to ±2.5V, making it an excellent choice for driving multiple video loads in RGB applications.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL2386C from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking. The gain resistor (R_G) can then be chosen to make up for any gain loss which may be created by this additional resistor at the output. In many cases it is also possible to simply increase the value of the feedback resistor (R_F) to reduce the peaking.

Current Limiting

The EL2386C has no internal current-limiting circuitry. If an output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±60 mA. A heat sink may be required to keep the junction temperature below absolute maximum when an output is shorted indefinitely.

Multiplexing with the EL2386C

The ENABLE pins on the EL2386C allow for multiplexing applications. Figure 1 shows an EL2386C with all 3 outputs tied together, driving a back terminated 75Ω video load. Three sine waves of varying amplitudes and frequencies are applied to the three inputs, while a 1 of 3 decoder selects one amplifier to be on at any given time. Figure 2 shows the resulting output wave form at

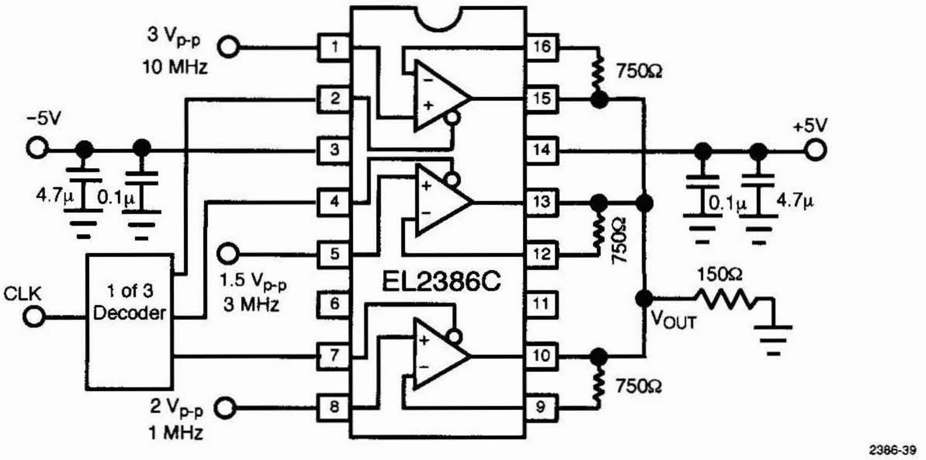
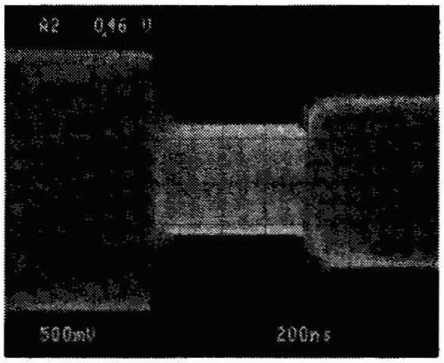


Figure 1

Applications Information — Contd.



2386-40

Figure 2

V_{OUT}. Switching is complete in about 100 ns. Notice the outputs are tied directly together. Decoupling resistors at each output are not required or advised when multiplexing.

Power Dissipation

With the high output drive capability of the EL2386C, it is possible to exceed the 150°C Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking, when R_L falls below about 25Ω, it is important to calculate the maximum junction temperature (T_{Jmax}) for the application to determine if power-supply voltages, load conditions, or package type need to be modified for the EL2386C to remain in the safe operating area.

These parameters are calculated as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} * n * PD_{MAX}) \qquad [1]$$

where:

T_{MAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
n = Number of Amplifiers in the Package
PD_{MAX} = Maximum Power Dissipation of Each Amplifier in the Package.

PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = (2 * V_S * I_{SMAX}) + (V_S - V_{OUTMAX}) * (V_{OUTMAX}/R_L) \qquad [2]$$

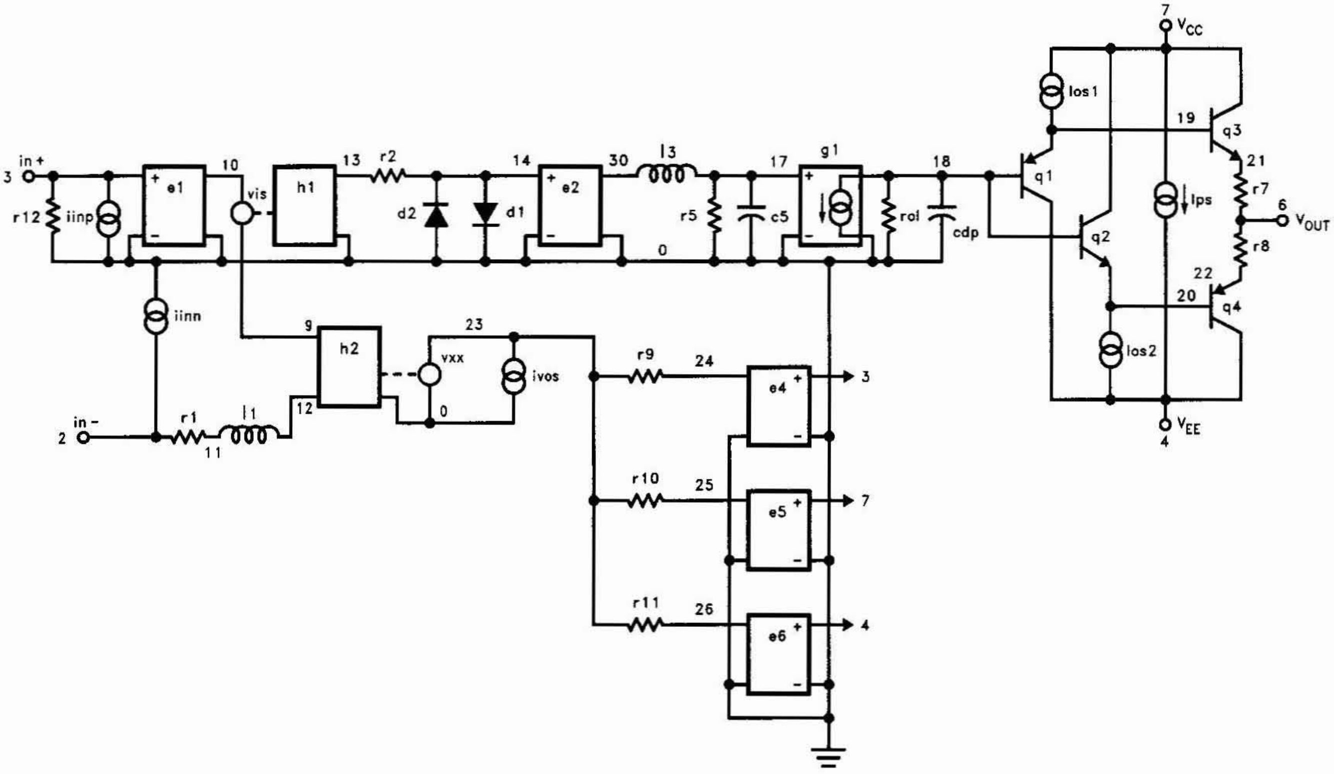
where:

V_S = Supply Voltage
I_{SMAX} = Maximum Supply Current of 1 Amplifier
V_{OUTMAX} = Max. Output Voltage of the Application
R_L = Load Resistance

EL2386C Macromodel

```
* EL2386C Macromodel
* Revision A, July 1996
* AC characteristics used: Rf = Rg = 750 ohms
* Pin numbers reflect a standard single opamp
* Connections:          +input
*                       |       -input
*                       |         |      +Vsupply
*                       |         |         |      -Vsupply
*                       |         |         |         |      output
*                       |         |         |         |         |
.subckt EL2386/EL       3         2         7         4         6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 400
l1 11 12 25nH
iinp 3 0 1.5µA
iinm 2 0 3µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 150nH
c5 17 0 0.8pF
r5 17 0 165
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 450k
cdp 18 0 0.675pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 1mA
ios2 20 4 1mA
*
* Supply Current
*
ips 7 4 0.2mA
*
* Error Terms
*
ivos 0 23 0.2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 -1.0
r9 24 23 316
r10 25 23 3.2K
r11 26 23 3.2K
*
* Models
*
.model qn npn(is=5e-15 bf=200 tf=0.1nS)
.model qp pnp(is=5e-15 bf=200 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.266
+ bv=0.71v n=4)
.ends
```

EL2386C Macromodel — Contd.



7
V_CC
Ios1
19
q3
21
r7
6
V_OUT
r8
22
20
q4
Ios2
V_EE
4
Ips
q1
q2
in+
3
r12
iinp
e1
10
vis
h1
13
r2
14
d2
d1
e2
30
l3
r5
c5
17
g1
rol
18
cdp
0
iinn
9
h2
23
vxx
ivos
0
in-
2
r1
11
l1
12
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4

2386-41

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2210C/11C/EL2310C/11C/EL2410C/11C

Low Cost, Dual, Triple and Quad Video Op Amps

Features

- Stable at gain of 2 and 100 MHz gain—bandwidth product (EL2211, EL2311, EL2411)
- Stable at gain of 1 and 50 MHz gain—bandwidth product (EL2210, EL2310, EL2410)
- 130V/μs slew rate
- Drives 150Ω load to video levels
- Inputs and outputs operate at negative supply rail
- ±5V or +10V supplies
- −60 dB isolation at 4.2 MHz

Applications

- Consumer video amplifier
- Active filters/integrators
- Cost sensitive applications
- Single supply amplifiers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2210CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL2211CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL2210CS	−40°C to +85°C	8-lead SO	MDP0027
EL2211CS	−40°C to +85°C	8-lead SO	MDP0027
EL2310CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2311CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2310CS	−40°C to +85°C	14-lead SO	MDP0027
EL2311CS	−40°C to +85°C	14-lead SO	MDP0027
EL2410CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2411CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2410CS	−40°C to +85°C	14-lead SO	MDP0027
EL2411CS	−40°C to +85°C	14-lead SO	MDP0027

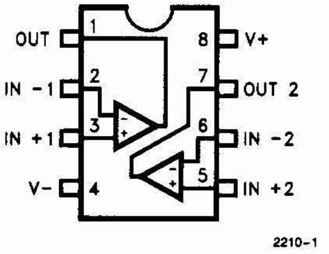
General Description

This family of dual, triple and quad operational amplifiers built using Elantec's Complementary Bipolar process offers unprecedented high frequency performance at a very low cost. They are suitable for any application such as consumer video, where traditional DC performance specifications are of secondary importance to the high frequency specifications. On ±5V supplies at a gain of +1 the EL2210C, EL2310C and the EL2410C will drive a 150Ω load to +2V, −1V with a bandwidth of 50 MHz and a channel to channel isolation of 60 dB or more. At a gain of +2 the EL2211C, EL2311C and EL2411C will drive a 150Ω load to +2V, −1V with a bandwidth of 100 MHz with the same channel to channel isolation. All four achieve 0.1 dB BW at 5 MHz.

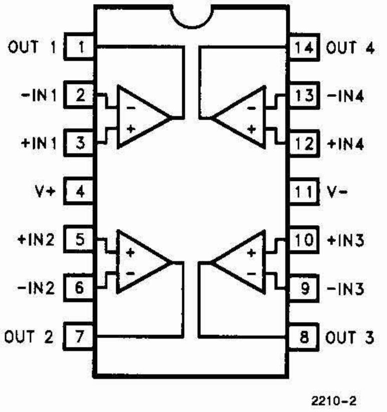
The power supply operating range is fixed at ±5V or +10/0V. In single supply operation the inputs and outputs will operate to ground. Each amplifier draws only 7 mA of supply current.

Connection Diagrams

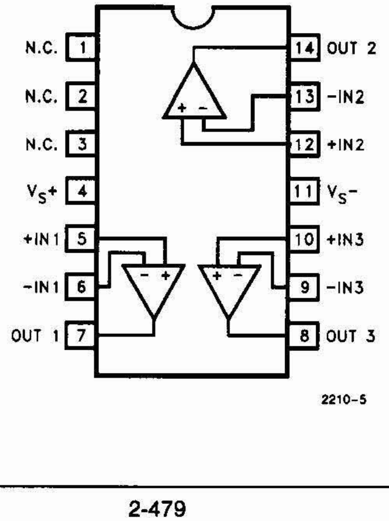
EL2210C/EL2211C



EL2410C/EL2411C



EL2310C/EL2311C



EL2210C/11C/EL2310C/11C/EL2410C/11C
Low Cost, Dual, Triple and Quad Video Op Amps

Absolute Maximum Ratings

Total Voltage Supply	18V	Power Dissapation	See Curves
Input Voltage	± Vs	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	6V	Operating Temperature Range	−40°C to +85°C
Peak Output Current	75 mA per amplifier		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

EL2210, EL2310, EL2410

DC Electrical Characteristics $V_S = \pm5V$, $R_L = 1\ K\Omega$, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			10	20	I	mV
		EL2310C only		10	25	I	mV
		EL2311C only		5	25	I	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)		−25		V	μV/°C
I_B	Input Bias Current		−15	−7	−3	I	μA
I_{OS}	Input Offset Current			0.5	1.5	I	μA
TCI_{OS}	Average Offset Current Drift	(Note 2)		−7		V	nA/°C
A_{VOL}	Open-Loop Gain	$V_{OUT} = \pm2V$, $R_L = 1\ K\Omega$	160	250		I	V/V
		$V_{OUT} = +2V/0V$, $R_L = 150\Omega$	160	250		V	
PSRR	Power Supply Rejection	$V_S = \pm4.5V$ to $\pm5.5V$	50	60		I	dB
CMRR	Common Mode Rejection	$V_{CM} = \pm2.4V$, $V_{OUT} = 0V$	60	80		I	dB
CMIR	Common Mode Input Range	$V_S = \pm5V$		−5/+3		V	V
V_{OUT}	OutputVoltage Swing	$R_L = R_F = 1\ K\Omega$ R_L to Gnd	−2.5	−3, 3	2.7	I	V
		$R_L = R_F = 1\ K\Omega + 150\Omega$ to Gnd	−0.45	−0.6, 2.9	2.5	I	
		$R_L = R_F = 1\ K\Omega$ R_L to V_{EE}	−4.95		3	V	
I_{SC}	Output Short Circuit Current	Output to Gnd (Note 1)	75	125		I	mA
I_S	Supply Current	No Load (per channel)	5.5	6.8	8.5	I	mA
R_{IN}	Input Resistance	Differential		150		V	KΩ
		Common Mode		1.5		V	MΩ
C_{IN}	Input Capacitance	$A_V = +1$ @ 10 MHz		1		V	pF
R_{OUT}	Output Resistance			0.150		V	Ω
PSOR	Power Supply Operating Range	Dual Supply	±4.5		±6.5	V	V
		Single Supply	9		13	V	

EL2211, EL2311, EL2411

DC Electrical Characteristics $V_S = \pm 5V, R_L = 1\ K\Omega, A_V = +2$, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage			5	12	I	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)		−25		V	µV/°C
I_B	Input Bias Current		−15	−7	−3	I	µA
I_{OS}	Input Offset Current			0.5	1.5	I	µA
TCI_{OS}	Average Offset Current Drift	(Note 2)		−7		V	nA/°C
A_{VOL}	Open-Loop Gain	$V_{OUT} = \pm 2V, R_L = 1\ K\Omega$	250	380		I	V/V
		$V_{OUT} = +2V/0V, R_L = 150\Omega$	250	380		V	
PSRR	Power Supply Rejection	$V_S = \pm 4.5V$ to $\pm 5.5V$	55	68		I	dB
CMRR	Common Mode Rejection	$V_{CM} = \pm 2.5V, V_{OUT} = 0V$	70	90		I	dB
CMIR	Common Mode Input Range	$V_S = \pm 5V$		−5/+3		V	V
V_{OUT}	Output Voltage Swing	$R_L = R_F = 1\ K\Omega$ R_L to Gnd	2.5	−3.5, 3.3	2.7	I	V
		$R_L = R_F = 1\ K\Omega$ $+150\Omega$ to Gnd	−0.45	−0.6, 2.9	2.5	I	
		$R_L = R_F = 1\ K\Omega$ R_L to V_{EE}	−4.95		3	V	
I_{SC}	Output Short Circuit Current	Output to Gnd (Note 1)	75	125		I	mA
I_S	Supply Current	No Load	5.5	6.8	8.5	I	mA
R_{IN}	Input Resistance	Differential		150		V	KΩ
		Common Mode		1.5		V	MΩ
C_{IN}	Input Capacitance	$A_V = +1$ @ 10 MHz		1		V	pF
R_{OUT}	Output Resistance			0.150		V	Ω
PSOR	Power Supply Operating Range	Dual Supply	±4.5		±6.5	V	V
		Single Supply	9		13	V	

EL2210, EL2310, EL2410

Closed-Loop AC Characteristics $V_S = \pm5V$, AC Test Figure 1, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min.	Typ.	Max.	Test Level	Units
BW	−3 dB Bandwidth ($V_{OUT} = 0.4\ V_{PP}$)	$A_V = +1$		110		V	MHz
BW	±0.1 dB Bandwidth ($V_{OUT} = 0.4\ V_{PP}$)	$A_V = +1$		12		V	MHz
GBWP	Gain Bandwidth Product			55		V	MHz
PM	Phase Margin			60		V	(°)
SR	Slew Rate		85	130		V	V/μs
FBWP	Full Power Bandwidth	(Note 3)	8	11		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step		2		V	ns
OS	Overshoot	0.1V Step		15		V	%
t_{PD}	Propagation Delay			3.5		V	ns
t_S	Settling to 0.1% ($A_V = 1$)	$V_S = \pm5V$, 2V Step		80		V	ns
d_G	Differential Gain (Note 4)	NTSC/PAL		0.1		V	%
d_P	Differential Phase (Note 4)	NTSC/PAL		0.2		V	(°)
e_N	Input Noise Voltage	10 KHz		15		V	nV/rt (Hz)
i_N	Input Noise Current	10 KHz		1.5		V	pA/rt (Hz)
CS	Channel Separation	P = 5 MHz		55		V	dB

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

Note 2: Measured from T_{MIN} to T_{MAX}

Note 3: For $V_S = \pm5V$, $V_{OUT} = 4\ V_{PP}$. Full power bandwidth is based on slew rate measurement using:
FPBW = SR/(2pi * V_{peak})

Note 4: Video performance measured at $V_S = \pm5V$, $A_V = +2$ with 2 times normal video level across $R_L = 150\Omega$.

EL2211, EL2311, EL2411

Closed-Loop AC Characteristics $V_S = \pm 5V$, AC Test Figure 1, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth ($V_{OUT} = 0.4\ V_{PP}$)	$A_V = +2$		100		V	MHz
BW	±0.1 dB Bandwidth ($V_{OUT} = 0.4\ V_{PP}$)	$A_V = +2$		8		V	MHz
GBWP	Gain Bandwidth Product			130		V	MHz
PM	Phase Margin			60		V	(°)
SR	Slew Rate		100	140		V	V/µs
FBWP	Full Power Bandwidth	(Note 3)	8	11		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step		2.5		V	ns
OS	Overshoot	0.1V Step		6		V	%
t_{PD}	Propagation Delay			3.5		V	ns
t_S	Settling to 0.1% ($A_V = 1$)	$V_S = \pm 5V$, 2V Step		80		V	ns
d_G	Differential Gain (Note 4)	NTSC/PAL		0.04		V	%
d_P	Differential Phase (Note 4)	NTSC/PAL		0.15		V	(°)
e_N	Input Noise Voltage	10 KHz		15		V	nV/rt (Hz)
i_N	Input Noise Current	10 KHz		1.5		V	pA/rt (Hz)
CS	Channel Separation	P = 5 MHz		55		V	dB

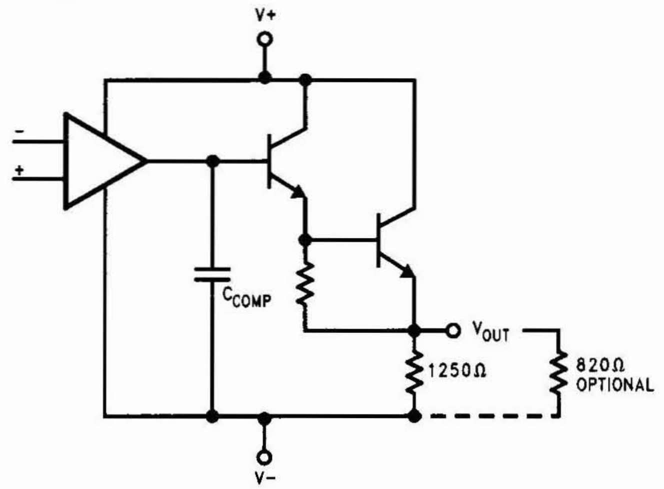
Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

Note 2: Measured from T_{MIN} to T_{MAX}

Note 3: For $V_S = \pm 5V$, $V_{OUT} = 4\ V_{PP}$. Full power bandwidth is based on slew rate measurement using:
FPBW = SR/(2pi * V_{peak})

Note 4: Video performance measured at $V_S = \pm 5V$, $A_V = +2$ with 2 times normal video level across $R_L = 150\Omega$.

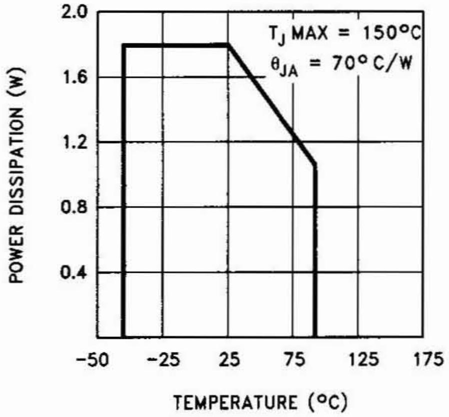
Simplified Block Diagram



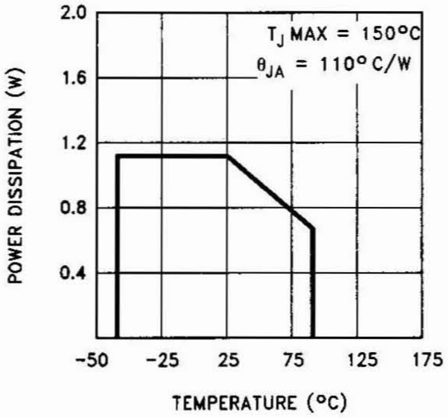
2210-3

Typical Performance Curves

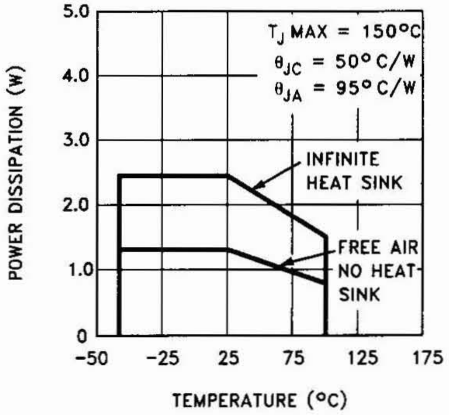
14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



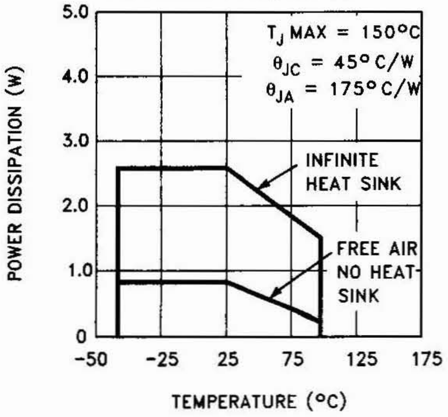
14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



8-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



8-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



2210-4

Application Information

Product Description

The EL2210, EL2310 and EL2410 are dual, triple and quad operational amplifiers stable at a gain of 1. The EL2211, EL2311 and the EL2411 are dual, triple and quad operational amplifiers stable at a gain of 2. All six are built on Elantec's proprietary complimentary process and share the same voltage mode feedback topology. This topology allows them to be used in a variety of applications where current mode feedback amplifiers are not appropriate because of restrictions placed on the feedback elements. These products are especially designed for applications where high bandwidth and good video performance characteristics are desired but the higher cost of more flexible and sophisticated products are prohibitive.

Power Supplies

These amplifiers are designed to work at a supply voltage difference of 10V to 12V. These amplifers will work on any combination of ± supplies. All Electrical characteristics are measured with ±5V supplies. Below 9V total supply voltage the amplifiers' performance will degrade dramatically. The quiescent current is a direct function of total supply voltage. With a total supply voltage of 12V the quiescent supply current will increase from a typical 6.8 mA per amplifier to 8.5 mA per amplifer.

Output Swing vs Load

Please refer to the simplified block diagram. These amplifiers provide an NPN pull-up transistor output and a passive 1250Ω pull-down resistor to the most negative supply. In an application where the load is connected to V_S- the output voltage can swing to within 200 mV of V_S-. In split supply applications where the DC load is connected to ground the negative swing is limited by the voltage divider formed by the load, the internal 1250Ω resistor and any external pull-down resistor. If R_L were 150Ω then it and the 1250Ω internal resistor limit the maximum negative swing to (V_{EE}(150/1250+150)) or −0.53V. The negative swing can be increased by adding an external resistor of appropriate value from the output to the negative supply. The simplified block diagram shows an 820Ω external pull-down resistor. This resistor is in parallel with the internal 1250Ω resistor. This will increase the negative swing to V_{EE} (150/((1250 * 820/(1250 + 820) + 150) or −1.16V.

Power Dissipation and Loading

Without any load and a 10V supply difference the power dissipation is 70 mW per amplifier. At 12V supply difference this increases to 105 mW per amplifier. At 12V this translates to a junction temperature rise above ambient of 33° for the dual and 40° for the quad amplifier. When the amplifiers provide load current the power dissipation can rapidly rise.

In ±5V operation each output can drive a grounded 150Ω load to more than 2V. This operating condition will not exceed the maximum junction temperature limit as long as the ambient temperature is below 85°C, the device is soldered in place, and the extra pull-down resistor is 820Ω or more.

If the load is connected to the most negative voltage (ground in single supply operation) you can easily exceed the absolute maximum die temperature. For example the maximum die temperature should be 150°C. At a maximum expected ambient temperature of 85°C, the total allowable power dissipation for the SO-8 package would be:

$$P_D = (150 - 75)/180°C/W = 416\ mW$$

At 12V total supply voltage each amplifier draws a maximum of 8.5 mA and dissipates 12V * 8.5 mA = 100 mW or 200 mW for the dual amplifier. Which leaves 216 mW of increased power due to the load. If the load were 150Ω connected to the most negative voltage and the maximum voltage out were V_S- +2V the load current would be 13 mA. Then an extra 266 mW ((12V − 2V) * 13.3 mA * 2) would be dissipated in the EL2210 or EL2211. The total dual amplifier power dissipation would be 266 mW + 200 mW = 466 mW, more than the maximum 416 mW allowed. If the total supply difference were reduced to 10V, the same calculations would yield 170 mW quiescent power dissipation and 213 mW due to loading. This results in a die temperature of 143°C (75°C + 69°C).

Application Information — Contd.

In the above example, if the supplies were split ±6V and the 150Ω loads were connected to ground, the load induced power dissipation would drop to 106 mW (13.3 mA * (6 − 2) * 2) and the die temperature would be below the rated maximum.

Video Performance

Following industry standard practices (see EL2044 applications section) these six devices exhibit good differential gain (dG) and good differential phase (dP) with ±5V supplies and an external 820Ω resistor to the negative supply, in a gain of 2 configuration. Driving 75Ω back terminated cables to standard video levels (1.428V at the amplifier) the EL2210, EL2310 and EL2410 have dG of 0.1% and dP of 0.2°. The EL2211, EL2311 and the EL2411 have dG of 0.04% and dP of 0.15°.

Due to the negative swing limitations described above, inverted video at a gain of 2 is just not practical. If swings below ground are required then changing the extra 820Ω resistor to 500Ω will allow reasonable dG and dP to approximately −0.75 mV. The EL2211, EL2311 and EL2411 will achieve approximately 0.1%/0.4° between 0V and −0.75V. Beyond −0.75V dG and dP get worse by orders of magnitude.

Differential gain and differential phase are fairly constant for all loads above 150Ω. Differential phase performance will improve by a factor of 3 if the supply voltage is increased to ±6V.

Output Drive Capability

None of these devices have short circuit protection. Each output is capable of more than 100 mA into a shorted output. Care must be used in the design to limit the output current with a series resistor.

Printed-Circuit Layout

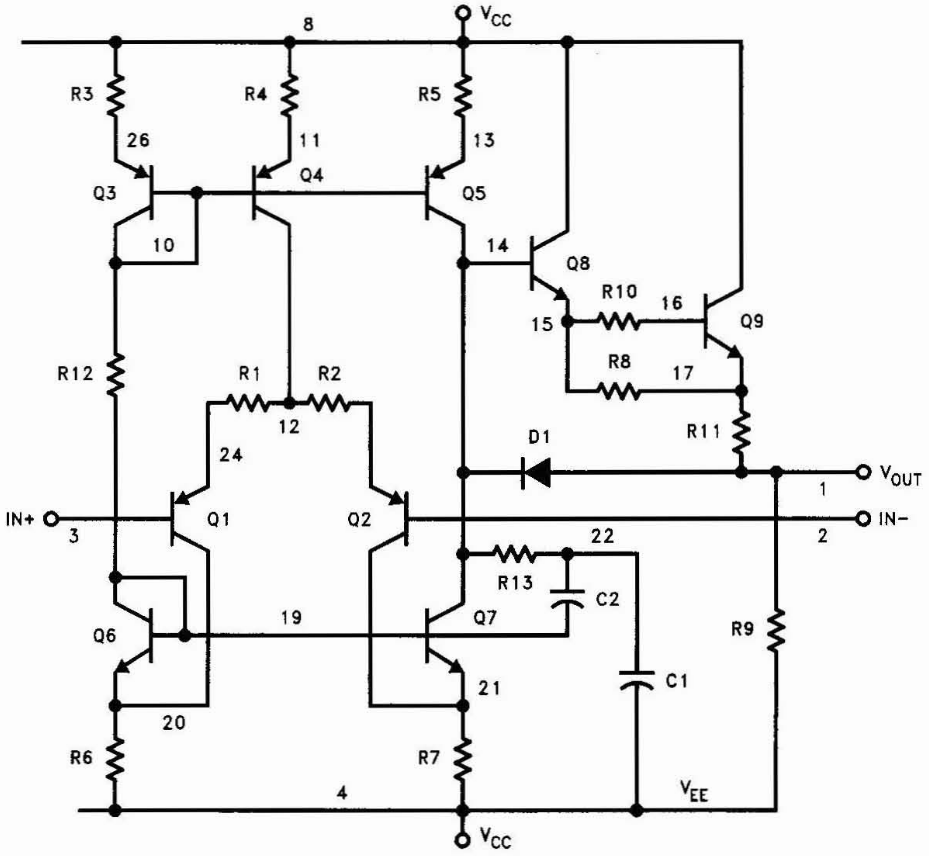
The EL2210C/EL2211C/EL2310C/EL2311C/EL2410C/EL2411C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 KΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

EL2210/EL2310/EL2410 Macromodel

```
* Revision A, June 1994
* Application Hints:
*
* A pull down resistor between the output and V- is recommended
* to allow output voltages to swing close to V-. See datasheet
* for recommended values.
*
* Connections:      +In
*                   |    -In
*                   |    |    V+
*                   |    |    |    V-
*                   |    |    |    |    Vout
*                   |    |    |         |
.subckt EL2210/EL   3    2    8    4    1
q1 20 3 24 qp
q2 21 2 25 qp
q3 10 10 26 qp
q4 12 10 11 qp
q5 14 10 13 qp
q6 19 19 20 qn
q7 14 19 21 qn
q8 8 14 15 qn
q9 8 16 17 qn 10
r1 24 12 350
r2 12 25 350
r3 8 26 250
r4 8 11 150
r5 8 13 240
r6 20 4 150
r7 21 4 150
r8 15 17 700
r9 1 4 1250
r10 15 16 40
r11 17 1 15
r12 10 19 10K
r13 14 22 20
c1 22 4 0.45pF
c2 22 19 1pF
d1 1 14 dcap
.model qn npn(bf=150 tf=0.05nS)
.model qp pnp(bf=90 tf=0.05nS)
.model dcap d(rs=200 cjo=le- 12 vj=0.8 tt=100e-9)
.ends
```

EL2211/EL2311/EL2411 Macromodel

```
* Revision A, June 1994
* Application Hints:
*
* A pull down resistor between the output and V- is recommended
* to allow output voltages to swing close to V-. See datasheet
* for recommended values.
*
* Connections:   +In
*                 |  -In
*                 |    |  V+
*                 |    |  |  V-
*                 |    |  |  |  Vout
*                 |    |  |  |   |
.subckt EL2211/EL 3    2  8  4   1
q1 20 3 24 qp
q2 21 2 25 qp
q3 10 10 26 qp
q4 12 10 11 qp
q5 14 10 13 qp
q6 19 19 20 qn
q7 14 19 21 qn
q8 8 14 15 qn
q9 8 16 17 qn 10
r1 24 12 175
r2 12 25 175
r3 8 26 250
r4 8 11 150
r5 8 13 240
r6 20 4 150
r7 21 4 150
r8 15 17 700
r9 1 4 1250
r10 15 16 40
r11 17 1 15
r12 10 19 10K
r13 14 22 20
c1 22 4 0.42pF
c2 22 19 1pF
d1 1 14 dcap
.model qn npn(bf=150 tf=0.05nS)
.model qp pnp(bf=90 tf=0.05nS)
.model dcap d(rs=200 cjo=1e-12 vj=0.8 tt=100e-9)
.ends
```


VCC
8
R3
R4
R5
26
11
13
Q3
Q4
Q5
10
14
Q8
R10
16
15
Q9
R8
17
R12
R1
R2
12
24
R11
D1
VOUT
1
IN+
3
Q1
Q2
IN−
2
22
R13
C2
Q6
19
Q7
R9
21
C1
20
R6
R7
4
VEE
VCC

2210-6

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4393C

Triple 80 MHz Video Amplifier w/Disable

Features

- 80 MHz −3 dB bandwidth for gains of 1 to 10
- 900 V/μs slew rate
- 10 MHz bandwidth flat to 0.1 dB
- Excellent differential gain and phase
- TTL/CMOS compatible
- Available in SOL-16

Applications

- RGB drivers
- RGB multiplexers
- RGB gain blocks
- Video gain blocks
- Coax cable driver
- ADC drivers/input multiplexer

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL4393CN	−40°C to +85°C	16-Lead P-DIP	MDP0031
EL4393CM	−40°C to +85°C	16-Lead SOL	MDP0027

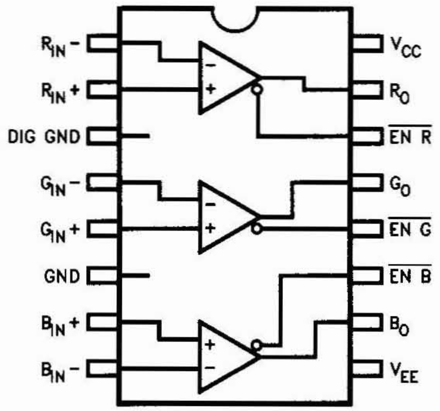
General Description

The EL4393C is three wideband current-feedback amplifiers optimized for video performance. Each amplifier can drive a load of 150Ω at video levels. Each amplifier has a disable capability, which is controlled by a TTL/CMOS compatible logic signal. The EL4393C operates on supplies as low as ±4V up to ±15V.

Being a current-feedback design, the bandwidth stays relatively constant at approximately 80 MHz over the ±1 to ±10 gain range. The EL4393C has been optimized for use with 1300Ω feedback resistors at a gain of 2.

When the outputs are disabled, the supply current consumption drops, by about 4 mA per channel that is disabled. This feature can be used to reduce power dissipation.

Connection Diagram



4393-1

EL4393C

Triple 80 MHz Video Amplifier w/Disable

Absolute Maximum Ratings ($T_A = 25°C$)

Voltage between V_S^+ and V_S^-	+33V	Internal Power Dissipation	See Curves
Voltage at V_S^+	+18V	Operating Ambient Temperature Range	−40°C to +85°C
Voltage at V_S^-	−18V	Operating Junction Temperature	150°C
Voltage between V_{IN}^+ and V_{IN}^-	±6V	Storage Temperature Range	−65°C to +150°C
Current into V_{IN}^+ or V_{IN}^-	5 mA		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 1 KΩ

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	+25°C		2	±15	I	mV
TCV_{OS}	Temperature Coefficient of V_{OS}	Full		50		V	μV/°C
I_B^+	I_{IN}^+ Input Bias Current	+25°C		0.2	5	I	μA
I_B^-	I_{IN}^- Input Bias Current	+25°C		10	65	I	μA
TCI_B^-	Temperature Coefficient of I_B^-	Full		25		V	nA/°C
CMRR	Common-Mode Rejection Ratio (Note 1)	+25°C	50	58		I	dB
−ICMR	I_{IN}^- Input Common-Mode Current (Note 1)	+25°C		3	8	I	μA/V
PSRR	Power Supply Rejection Ratio (Note 2)	+25°C	50	58		I	dB
−IPSR	I_{IN}^- Current Supply Rejection (Note 2)	+25°C		2	5	I	μA/V
R_{OL}	Transimpedance	+25°C	100	217		I	kΩ
R_{IN}	IN^+ Input Impedance	+25°C		2		I	MΩ
V_{IN}	IN^+ Input Range	+25°C	±13	±13.5		I	V
V_O	Output Voltage Swing; $R_L = 1\ k\Omega$	+25°C	±12	±13		I	V

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 1KΩ — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_{SC}	Short-Circuit Current (Note 3)	+25°C	40	70		I	mA
$I_{O,\,DIS}$	Output Current when Disabled	+25°C		5	150	I	μA
DIS V_{IL}	Disable Voltage for Logic Low	+25°C			0.8	I	V
DIS V_{IH}	Disable Voltage for Logic High	+25°C	2.2			I	V
DIS I_{IL}	Disable Logic Low Input Current	+25°C		3	25	I	μA
DIS I_{IH}	Disable Logic High Input Current	+25°C		0	5	I	μA
$I_{CC\,(en)}$	Positive Supply Current all Channels Enabled	+25°C	15	20	±29	I	mA
$I_{CC\,(dis)}$	Positive Supply Current all Channels Disabled	+25°C	6	11	16	I	mA
$I_{EE\,(en)}$	Negative Supply Current all Channels Enabled	+25°C	13	18	±28	I	mA
$I_{EE\,(dis)}$	Negative Supply Current all Channels Disabled	+25°C	4	9	14	I	mA

Note 1: $V_{CM} = \pm 10V$ for $V_S = \pm 15V$.
Note 2: V_{OS} is measured at $V_S = \pm 4.5V$ and $V_S = \pm 16V$, both supplies are changed simultaneously.
Note 3: Only one output short circuited. Pulse test or use heatsink.

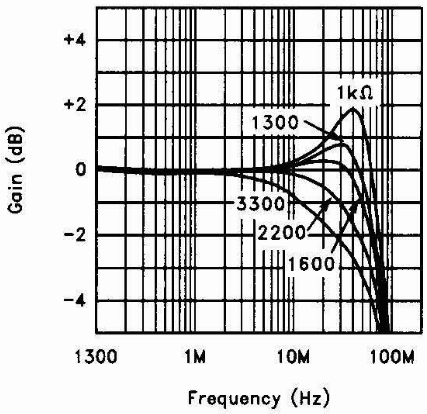
Closed Loop AC Electrical Characteristics Supplies at ±15V, Load = 150Ω and 15 pF, except where noted. Rf1 and Rf2 = 1500Ω; $A_V = 2$, $T_A = 25°C$. (See note 8 re: test fixture)

Parameter	Description	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Note 4)		960		V	V/μs
SR	Slew Rate w/ ±5V Supplies (Note 5)		470		IV	V/μs
t_s	Settling Time to 1% $5V_{p\text{-}p}$ 5V Step (Note 6)		32		V	ns
BW	Bandwidth, −3 dB ±5V Supplies, −3 dB		80 60		IV IV	MHz MHz
BW	Bandwidth, −0.1 dB ±5V Supplies, −0.1 dB		16 21		IV IV	MHz MHz
Peaking	−3 dB BW Tests		0.6		IV	dB
dG	Differential Gain at 3.58 MHz at ±5V Supplies (Note 7)		0.03 0.30		V V	% %
dθ	Differential Phase at 3.58 MHz at ±5V Supplies (Note 7)		0.088 0.096		V V	(°) (°)

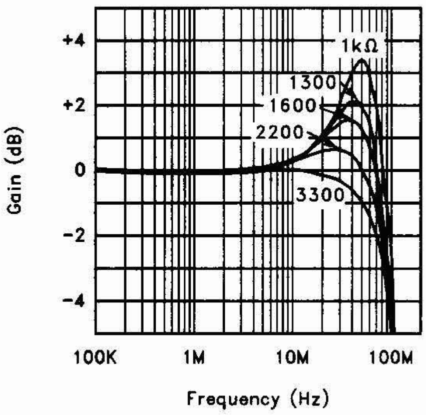
Note 4: $R_L = 300\Omega$, −5V to +5V swing, SR measured at 20% to 80%.
Note 5: −2V to +2V swing, SR measured at 20% to 80%.
Note 6: $R_L = 300\Omega$.
Note 7: DC offset from −0.7V through +0.7V AC amplitude is 286 $mV_{P\text{-}P}$, equivalent to 40 ire.
Note 8: Test fixture was designed to minimize capacitance at the $I_N{}^+$ input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.

Typical Performance Curves

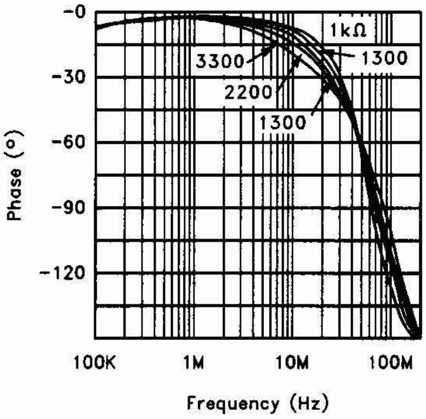
Gain Flatness vs Rf at ± 5V



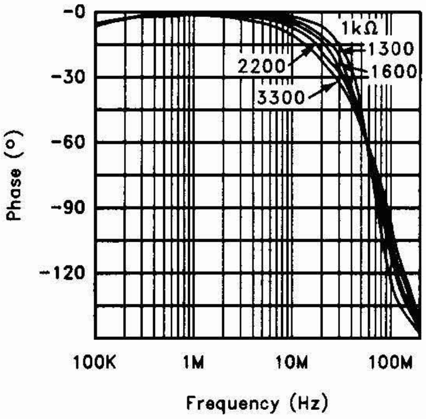
Gain Flatness vs Rf at ± 15V



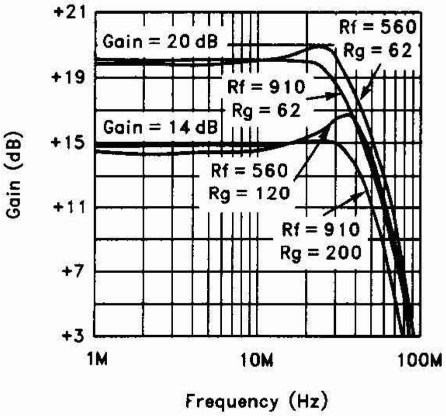
Phase vs Rf at ± 5V



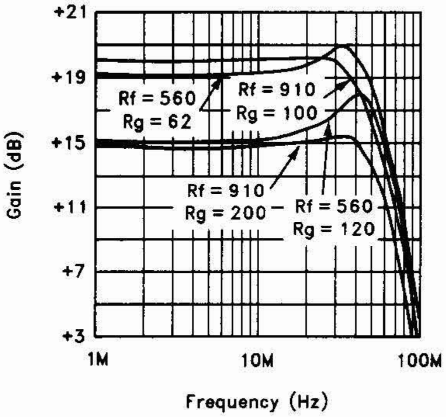
Phase vs Rf at ±15V



Gain of 5, 10 vs Various Rf, Rg at ±5V



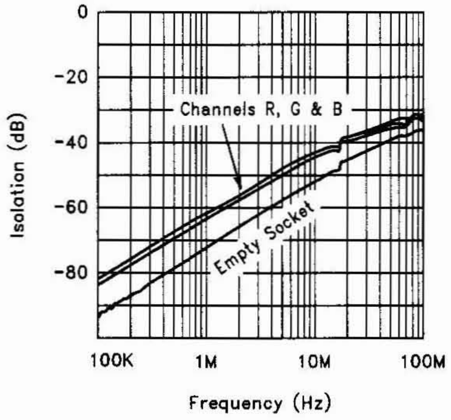
Gain of 5, 10 vs Rf, Rg at ± 15V



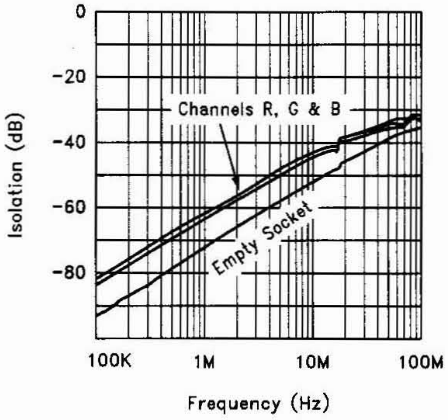
4393-3

Typical Performance Curves — Contd.

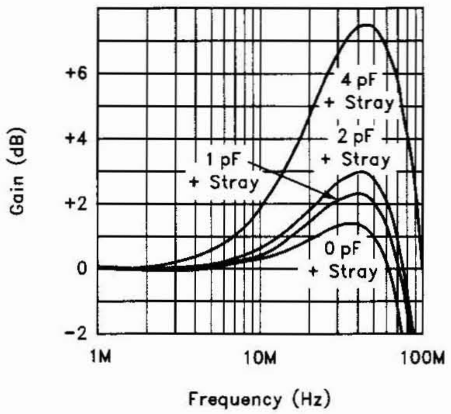
Disabled Isolation Test at ±5V



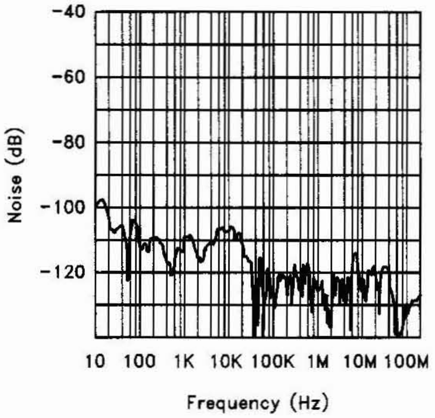
Disabled Isolation Test at ± 15V



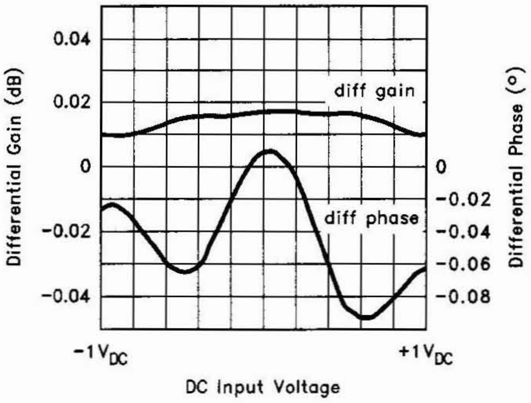
Cin—vs Peaking



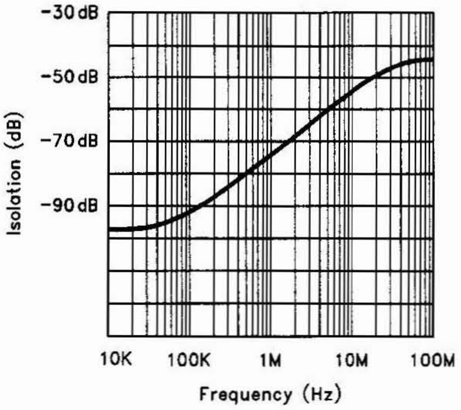
Voltage Noise



Differential Gain & Phase at 3.58 MHz



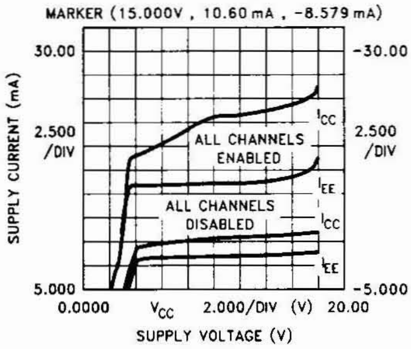
EL4393 MUX Channel Channel Isolation



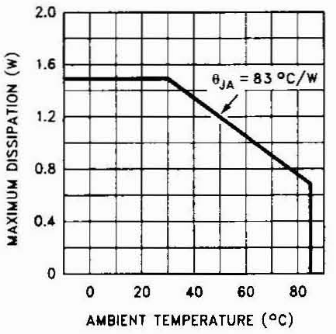
4393-11

Typical Performance Curves — Contd.

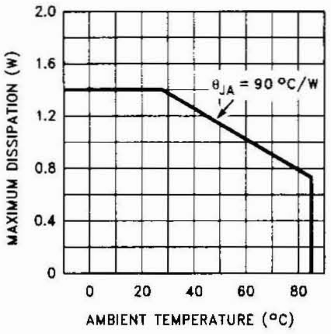
Supply Current vs Supply Voltage



Maximum Power Dissipation vs Ambient Temperature— 16-Pin PDIP

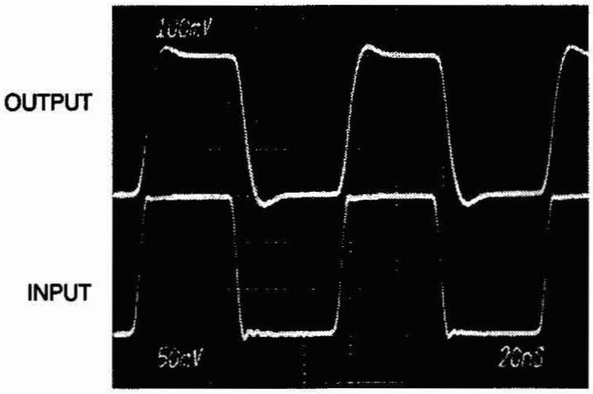


Maximum Power Dissipation vs Ambient Temperature— 16-Pin SOL



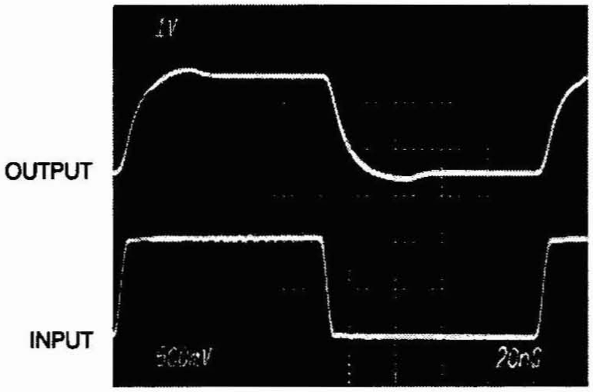
4393-4

Small Signal Pulse Response



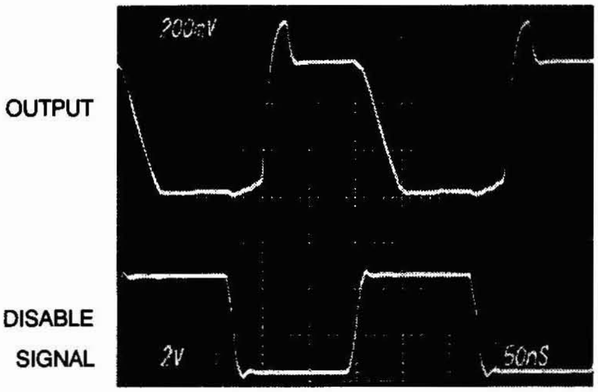
4393-5

Large Signal Pulse Response



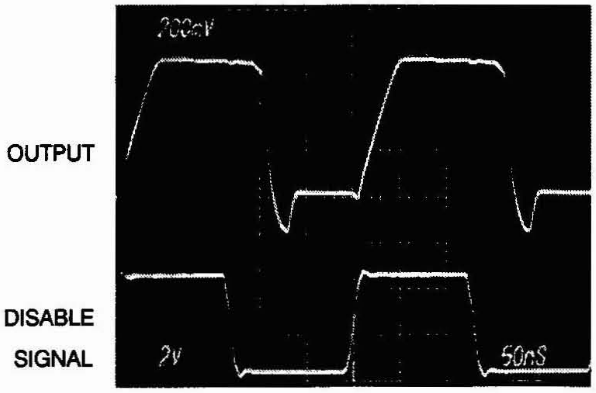
4393-6

Enable/Disable with + VE Voltage Output



4393-7

Enable/Disable with − VE Voltage Output



4393-8

Typical Application for EL4393, and General Rules for PCB Layout

The figure shows two EL4393's configured as a 2:1 RGB multiplexer, and cable driver, driving 75Ω, back terminated cables. Each channel of the EL4393 is configured to give a gain of two, to make up for the losses of the back terminating resistor.

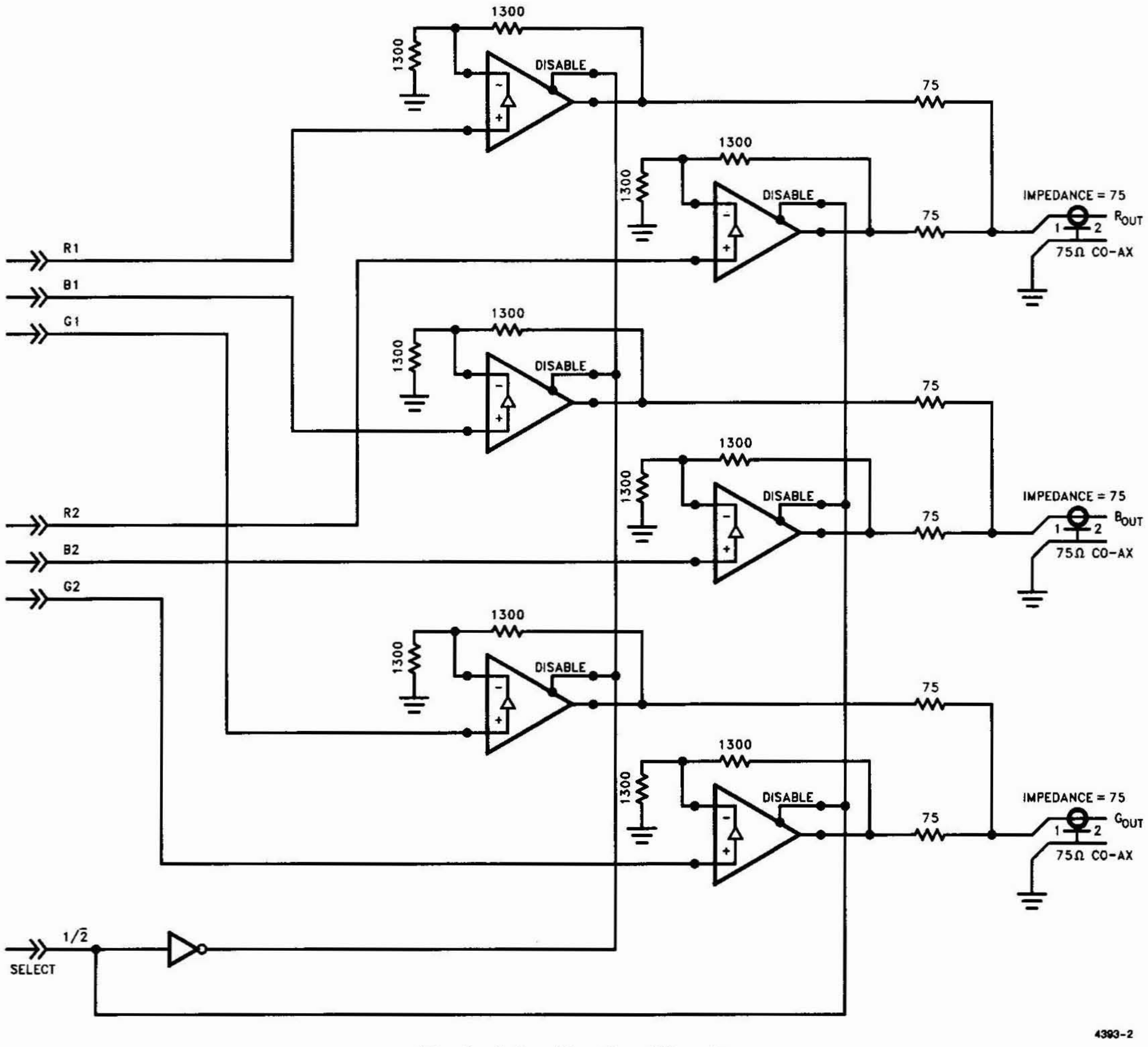
In this example, the Disable pins of each RGB section are driven by a complementary TTL "select" signal. Larger multiplexers can be assembled, with a 1-of-n TTL decoder selecting each RGB triplet.

The circuit gives channel isolations of typically better than −50 dB at 10 MHz, and with a 20 dB/decade slope, extending down to better than −90 dB at frequencies below 100 kHz.

The schematic does not show things like power supply decoupling, or pcb layout, grounding and signal returns, but these will all affect the overall performance of the circuit, and care should be taken with these aspects.

It is recommended that the V_{CC} and V_{EE} pins each be decoupled by a 0.1 µF NPO or X7R dielectric ceramic capacitors to ground within 0.1 inch of the part, and in parallel with the 0.1 µF, A 47 µF tantalum capacitor, also to ground. The 47 µF capacitors should be within 0.25 inch of their power pins. The ground plane should be underneath the package, but cut away from the In− inputs. Care should be taken with the center channel feedback—it must be kept away from any of the in+ or in− pins, if it has to go under the package. Route the G-out line between the pin 3 ground and the pin 4 In− if going under the package is essential. Otherwise, loop the G-out trace around all the other circuitry, to its Rf resistor. The Rf and if used, Rg resistors should be on the input side of the package, to minimize trace length on the In− pins.

The digital input disables are on the output side of the package, so that a good ground plane down the center of the board underneath the package will isolate any fast edges from the sensitive inputs.

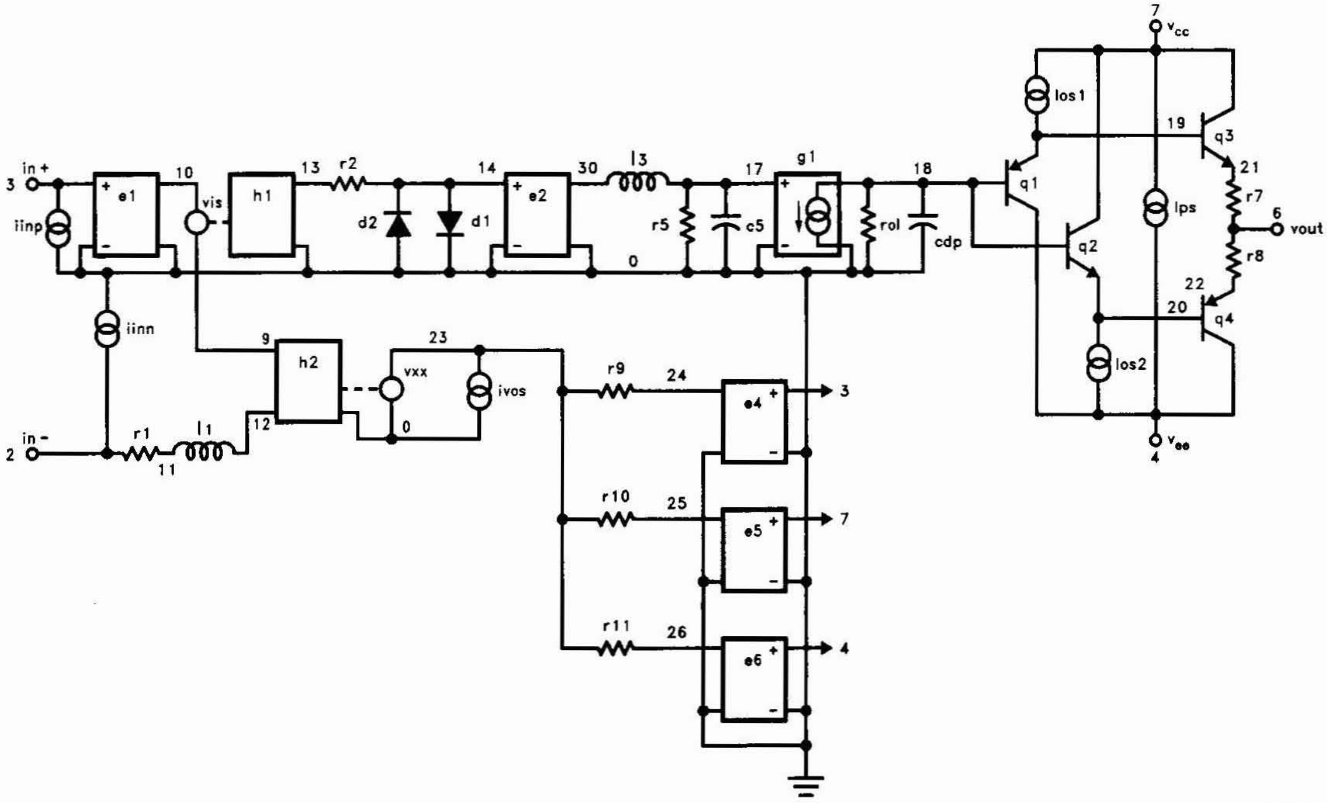

1300
1300
DISABLE
75
IMPEDANCE = 75
R_{OUT}
B_{OUT}
G_{OUT}
75Ω CO-AX
1
2
R1
B1
G1
R2
B2
G2
1/$\overline{2}$
SELECT
4393-2

Typical Application Circuit

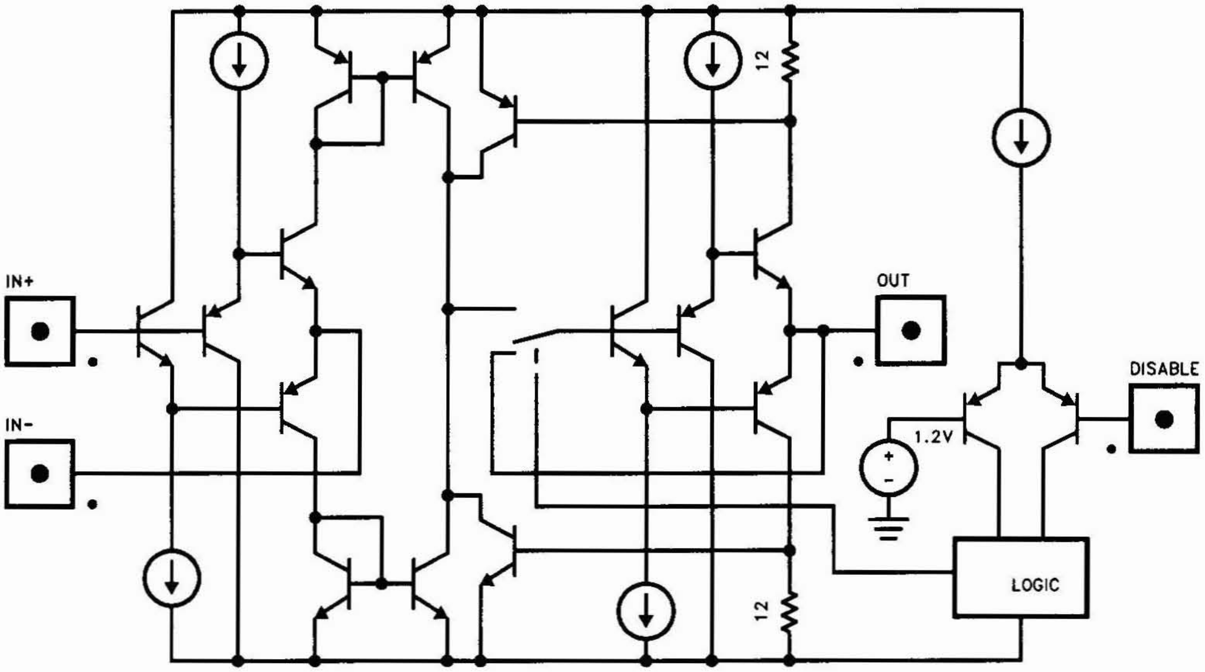
EL4393C Macromodel

```
* Revision A, July 1993
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:        +input
*                     |      -Input
*                     |      |      +Vsupply
*                     |      |      |      -Vsupply
*                     |      |      |      |      Putput
*                     |      |      |      |      |
* subckt EL4393/EL    3      2      7      4      6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 29 nH
iinp 3 0 0.2 µA
iinm 2 0 10 µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l5 30 17 1.2 µH
c5 17 0 1 pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 250k
cdp 18 0 2.2 pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2.5 mA
ios2 20 4 2.5 mA
*
* Error Terms
*
ivos 0 23 2 mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 1K
r10 25 23 1K
r11 26 33 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.2nS)
.model qp pnp (is=5e-15 bf=100 tf=0.2nS)
.model dclamp d (is=1e-30 ibv=0.266 bv=1.5 n=4)
.ends
```

EL4393C Macromodel — Contd.


in +
3
iinp
e1
10
vis
h1
13
r2
14
d2
d1
e2
30
l3
17
r5
c5
g1
18
rol
cdp
0
iinn
9
h2
23
vxx
ivos
0
in -
2
r1
11
l1
12
r9
24
e4
3
r10
25
e5
7
r11
26
e6
4
7
vcc
ios1
19
q3
q1
21
r7
Ips
6
vout
q2
r8
22
20
q4
ios2
4
vee

4393-9


IN+
IN-
12
12
OUT
DISABLE
1.2V
+
-
LOGIC

4393-10

Simplified Schematic of One Channel of EL4393

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4430C/EL4431C
Video Instrumentation Amplifiers

Features

- Fully differential inputs and feedback
  - — Differential input range of ±2V
  - — Common-mode range of ±12V
  - — High CMRR at 4 MHz of 70 dB
  - — Stable at gains of 1, 2
- Calibrated and clean input clipping
- 4430—80 MHz @ G = 1
- 4431—160 MHz GBWP
- 380V/μs slew rate
- 0.02% or ° differential gain or phase
- Operates on ±5 to ±15V supplies with no AC degradation

Applications

- Line receivers
- "Loop-through" interface
- Level translation
- Magnetic head pre-amplification
- Differential-to-single-ended conversion

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL4430CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL4430CS	−40°C to +85°C	8-lead SO	MDP0027
EL4431CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL4431CS	−40°C to +85°C	8-lead SO	MDP0027

General Description

The EL4430 and 4431 are video instrumentation amplifiers which are ideal for line receivers, differential-to-single-ended converters, transducer interfacing, and any situation where a differential signal must be extracted from a background of common-mode noise or DC offset.

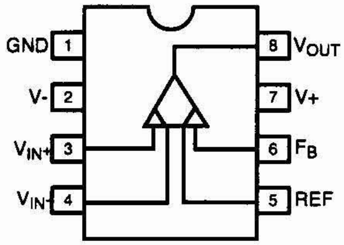
These devices have two differential signal inputs and two differential feedback terminals. The FB terminal connects to the amplifier output, or a divided version of it to increase circuit gain, and the REF terminal is connected to the output ground or offset reference.

The EL4430 is compensated to be stable at a gain of 1 or more, and the EL4431 for a gain of 2 or more.

The amplifiers have an operational temperature of −40°C to +85°C and are packaged in plastic 8-pin DIP and SO-8.

The EL4430 and EL4431 are fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is free from latchup.

Connection Diagram



EL4430C/EL4431C
Video Instrumentation Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

V+	Positive Supply Voltage	16.5V	I_{OUT}	Continuous Output Current	30 mA
V_S	V+ to V− Supply Voltage	33V	P_D	Maximum Power Dissipation	See Curves
V_{IN}	Voltage at any Input or Feedback	V+ to V−	T_A	Operating Temperature Range	−40°C to +85°C
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V	T_S	Storage Temperature Range	−60°C to +150°C
I_{IN}	Current into any Input, or Feedback Pin	4 mA			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics

Power supplies at ±5V, T_A = 25°. For the EL4431, $R_F = R_G = 500\Omega$.

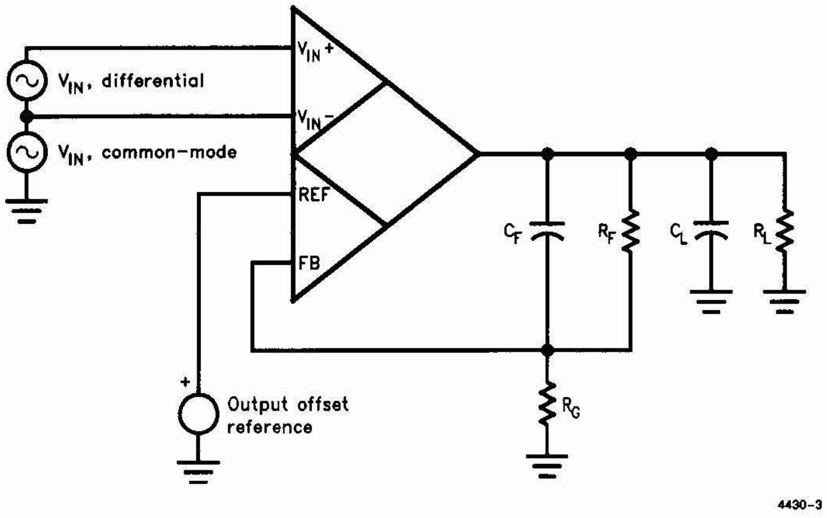
Parameter	Description		Min	Typ	Max	Test Level	Units
V_{DIFF}	Differential input voltage - Clipping (V_{CM} = 0)	EL4430/31	2.0	2.3		I	V
	0.1% nonlinearity	EL4430/31		1.8		V	V
V_{CM}	Common-mode range (V_{DIFF} = 0)	V_S = ±5V	±2	±3.0		I	V
		V_S = ±15V	±12	±13.0		I	V
V_{OS}	Input offset voltage	EL4430/31		2	8	I	mV
I_B	Input bias current (IN+, IN−, REF, and FB terminals)			12	20	I	µA
I_{OS}	Input offset current between IN+ and IN− and between REF and FB			0.2	2	I	µA
R_{IN}	Input resistance	EL4430/31	100	230		I	kΩ
CMRR	Common-mode rejection ratio		70	90		I	dB
PSRR	Power supply rejection ratio	EL4430/31		60		V	dB
E_G	Gain error, excluding feedback resistors	EL4430/31	−1.5	−0.2	+0.5	I	%
V_O	Output voltage swing	EL4430, V_S = ±5V	±2	±2.8		I	V
		V_S = ±15V	±12	±12.8		I	V
		EL4431, V_S = ±5V	±2.5	±3.0		I	V
		V_S = ±15V	±12.5	±13.0		I	V
I_{SC}	Output short-circuit current		40	90		I	mA
I_S	Supply current, V_S = ±15V			13.5	16	I	mA

Closed-Loop AC Electrical Characteristics

Power supplies at ±12V, $T_A = 25°C$, $R_L = 500\Omega$ for the EL4430, $R_L = 150\Omega$ for the EL4431, $C_L = 15$ pF. For the EL4431, $R_F = R_G = 500\Omega$.

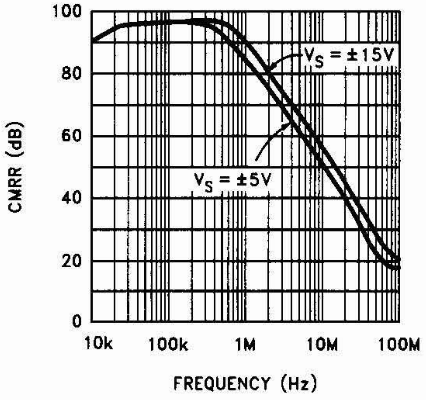
Parameter	Description		Min	Typ	Max	Test Level	Units
BW, −3 dB	−3 dB small-signal bandwidth	EL4430		82		V	MHz
		EL4431		80		V	MHz
BW, ±0.1 dB	0.1 dB flatness bandwidth	EL4430		20		V	MHz
		EL4431		14		V	MHz
Peaking	Frequency response peaking	EL4430		0.6		V	dB
		EL4431		1.0		V	dB
SR	Slew rate, V_{OUT} between −2V and +2V	All		380		V	V/µs
V_N	Input-referred noise voltage density	EL4430/31		26		V	nV/rt-Hz
dG	Differential gain error, Voffset between −0.7V and +0.7V	EL4430		0.02		V	%
		EL4431, $R_L = 150\Omega$		0.04		V	%
dθ	Differential gain error, Voffset between −0.7V and +0.7V	EL4430		0.02		V	(°)
		EL4431, $R_L = 150\Omega$		0.08		V	(°)
T_S	Settling time, to 0.1% from a 4V step	EL4430		48		V	ns

Test Circuit



Typical Performance Curves

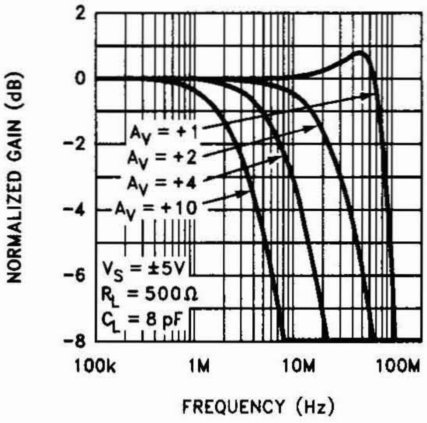
EL4430 and EL4431 Common-Mode Rejection Ratio vs Frequency



4430-4

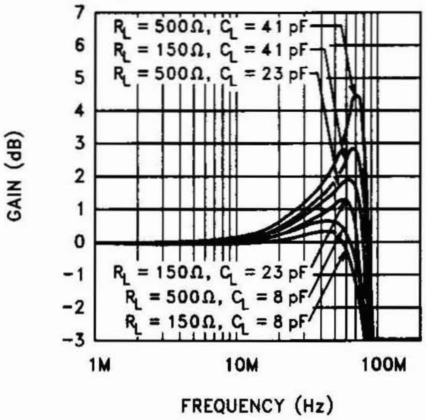
Typical Performance Curves — Contd.

EL4430 Frequency Response vs Gain



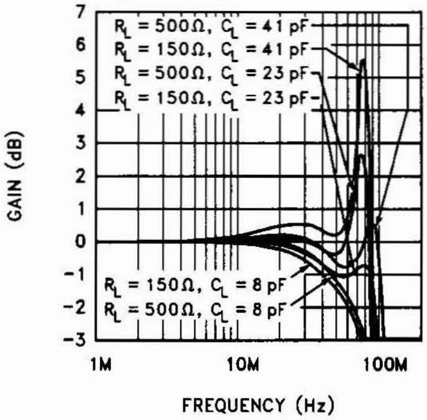
4430-5

EL4430 Frequency Response for Various R_L, C_L
$V_S = \pm5V$



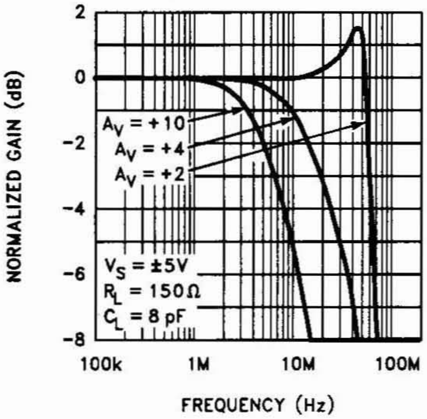
4430-6

EL4430 Frequency Response for Various R_L, C_L
$V_S = \pm15V$



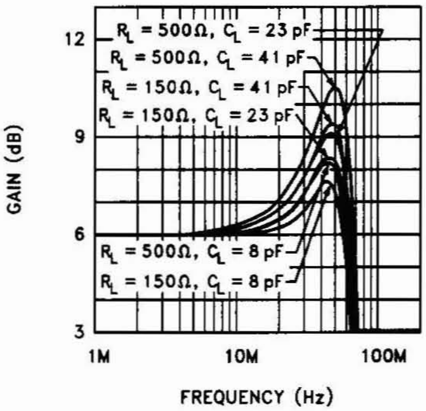
4430-7

EL4431 Frequency Response vs Gain



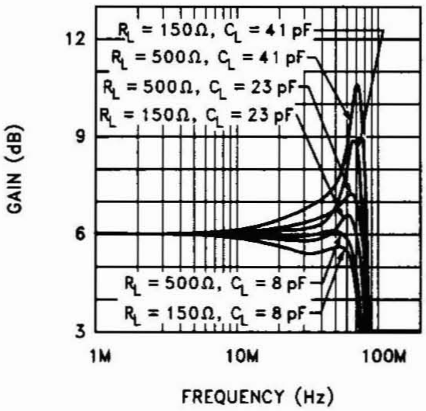
4430-8

EL4431 Frequency Response for Various R_L, C_L
$V_S = \pm5V$



4430-9

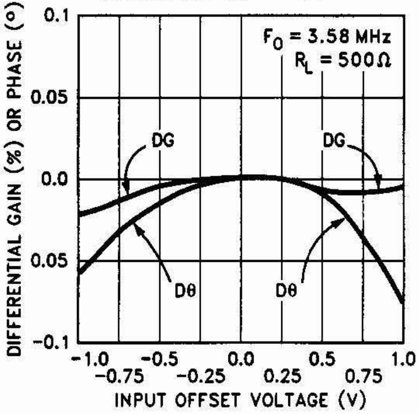
EL4431 Frequency Response for Various R_L, C_L
$V_S = \pm15V$



4430-10

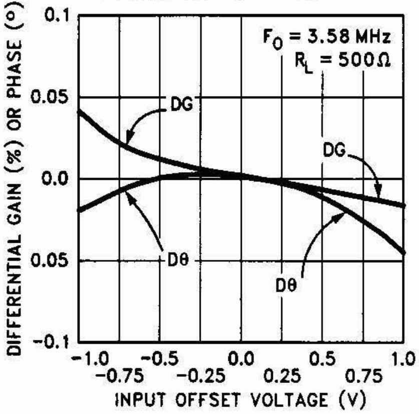
Typical Performance Curves — Contd.

EL4430 Differential Gain and Phase vs Input Offset Voltage for V_S = ±5V



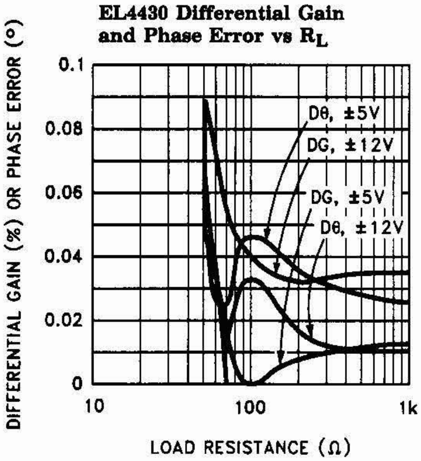
4430-14

EL4430 Differential Gain and Phase vs Input Offset Voltage for V_S = ±12V



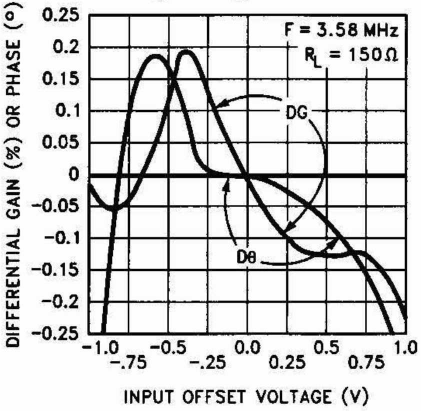
4430-15

EL4430 Differential Gain and Phase Error vs R_L



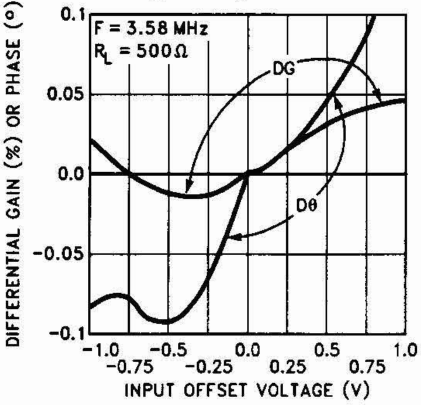
4430-16

EL4431 Differential Gain and Phase vs Input Offset Voltage for V_S = ±5V



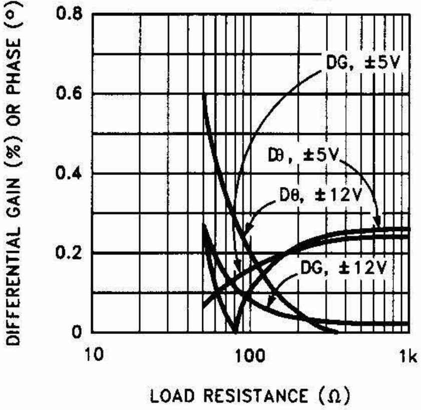
4430-17

EL4431 Differential Gain and Phase vs Input Offset Voltage for V_S = ±12V



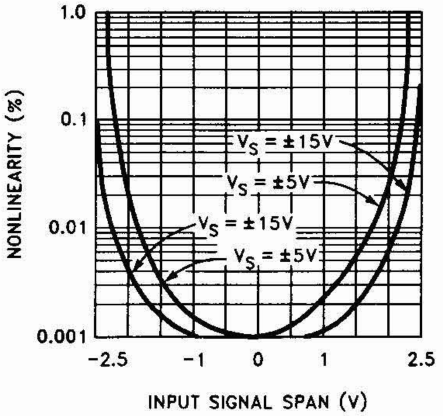
4430-18

EL4431 Differential Gain and Phase Error vs R_L



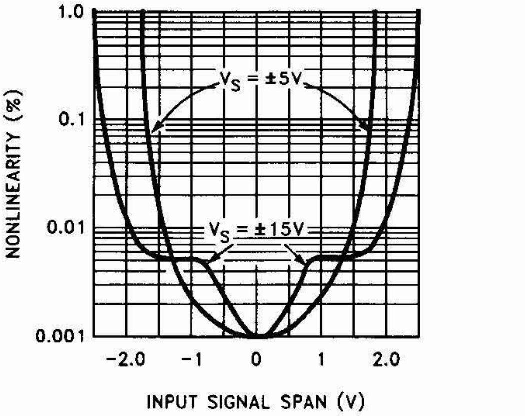
4430-19

EL4430 Nonlinearity vs Input Signal Span



4430-20

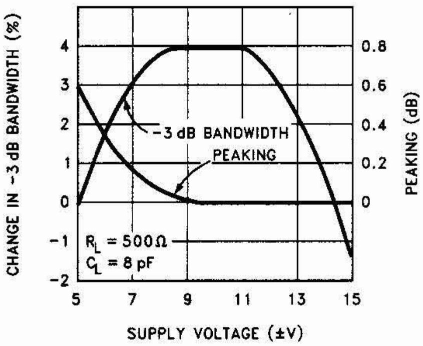
EL4431 Nonlinearity vs Input Signal Span



4430-21

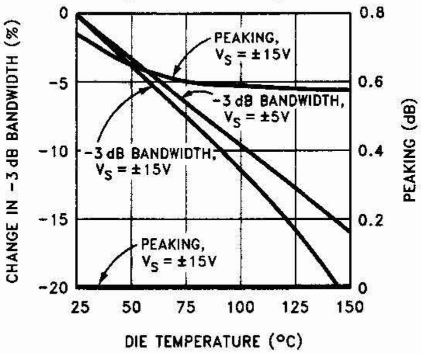
Typical Performance Curves — Contd.

EL4430 −3 dB Bandwidth and Peaking vs Supply Voltage for $A_V = +1$



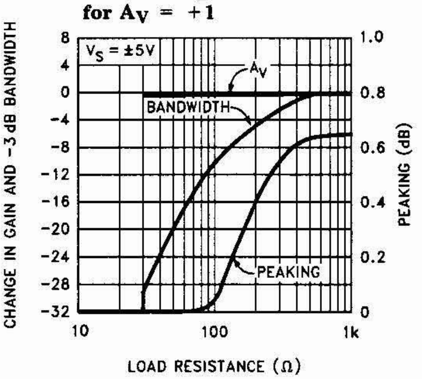
4430-23

EL4430 −3 dB Bandwidth and Peaking vs Die Temperature for $A_V = +1$



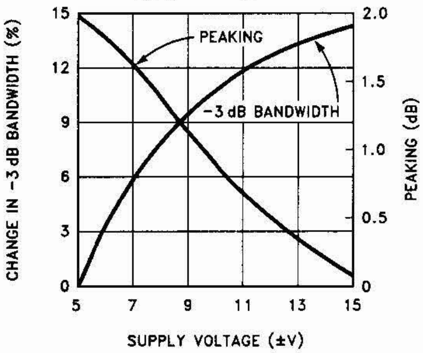
4430-24

EL4430 Gain, −3 dB Bandwidth and Peaking vs Load Resistance for $A_V = +1$



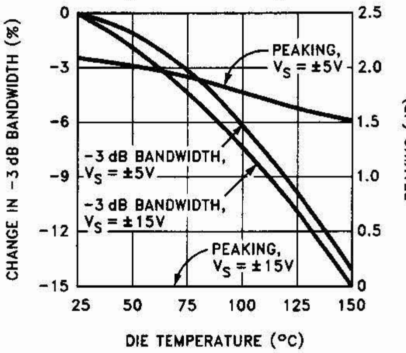
4430-25

EL4431 −3 dB Bandwidth and Peaking vs Supply Voltage



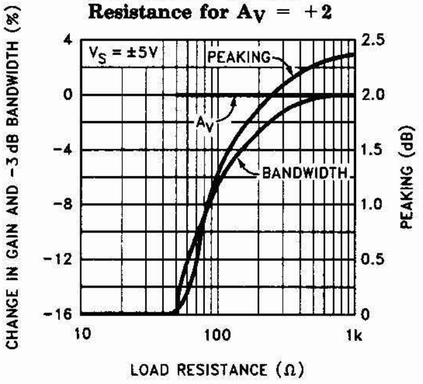
4430-26

EL4431 −3 dB Bandwidth and Peaking vs Die Temperature for $A_V = +2$



4430-27

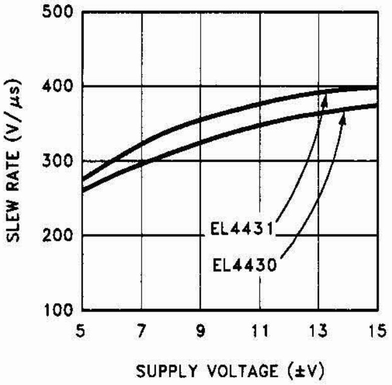
EL4431 Gain, −3 dB Bandwidth and Peaking vs Load Resistance for $A_V = +2$



4430-28

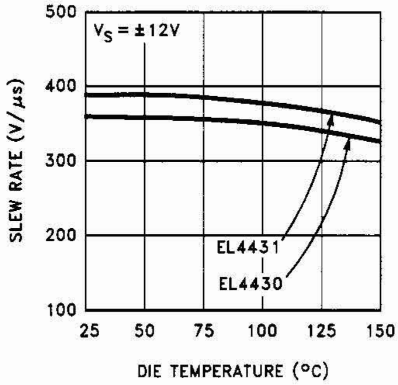
Typical Performance Curves — Contd.

Slew Rate vs Supply Voltage



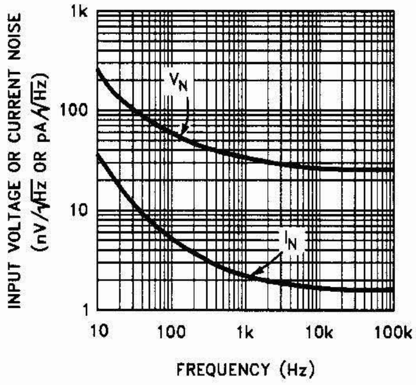
4430-32

Slew Rate vs Die Temperature



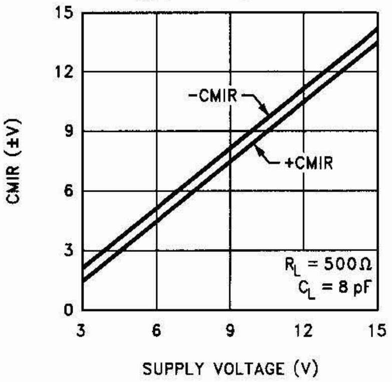
4430-33

Input Voltage and Current Noise vs Frequency



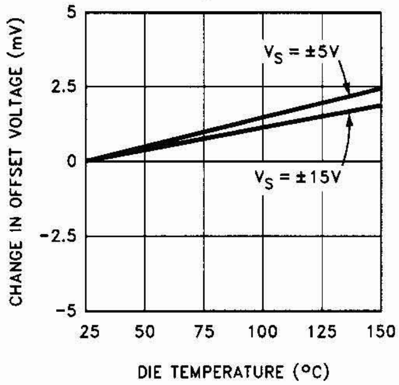
4430-34

Common Mode Input Range vs Supply Voltage



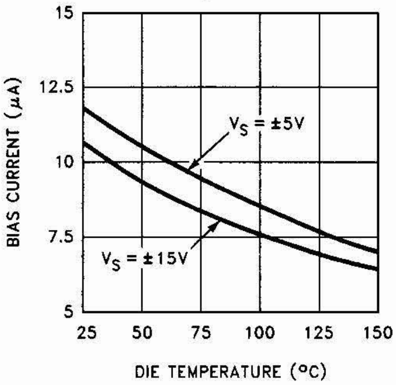
4430-35

Offset Voltage vs Die Temperature



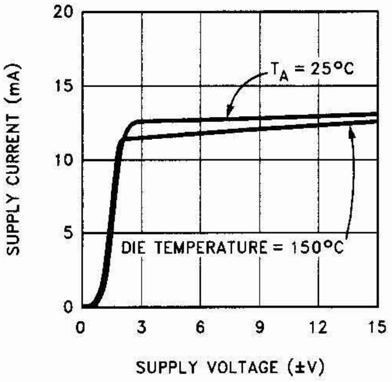
4430-36

Bias Current vs Die Temperature



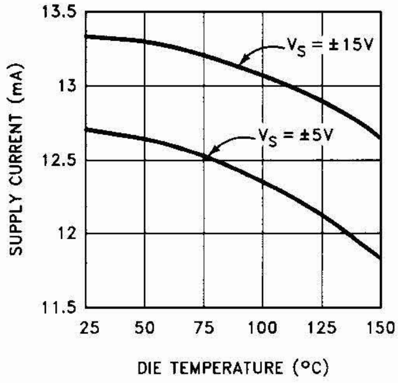
4430-37

Supply Current vs Supply Voltage



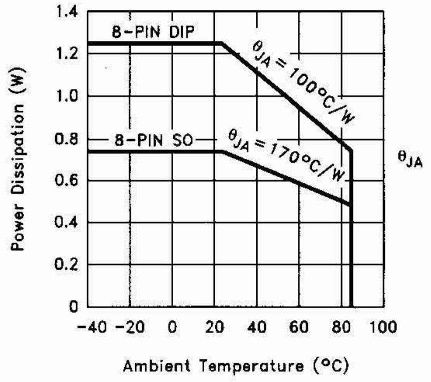
4430-38

Supply Current vs Die Temperature



4430-39

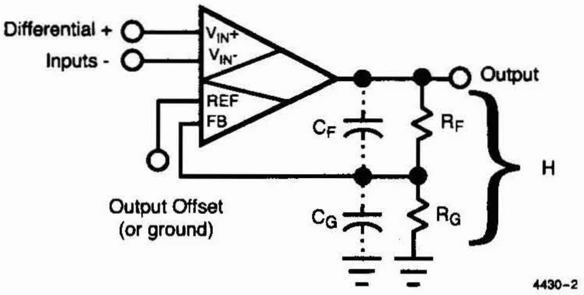
Power Dissipation vs Ambient Temperature



4430-40

Applications Information

The EL4430 and EL4431 are designed to convert a fully differential input to a single-ended output. It has two sets of inputs; one which is connected to the signal and does not respond to its common-mode level, and another which is used to complete a feedback loop with the output. Here is a typical connection:



The gain of the feedback divider is H. The transfer function of the part is

$$V_{OUT} = A_O \times ((V_{IN}+) - (V_{IN}-) + (V_{REF} - V_{FB})).$$

V_{FB} is connected to V_{OUT} through a feedback network, so $V_{FB} = H \times V_{OUT}$. A_O is the open-loop gain of the amplifier, and is about 600 for the EL4430 and EL4431. The large value of A_O drives

$$(V_{IN}+) - (V_{IN}-) + (V_{REF} - V_{FB}) \rightarrow 0.$$

Rearranging and substituting for V_{FB}

$$V_{OUT} = ((V_{IN}+) - (V_{IN}-) + V_{REF})/H.$$

Thus, the output is equal to the difference of the V_{IN}'s and offset by V_{REF}, all gained up by the feedback divider ratio. The input impedance of the FB terminal (equal to R_{IN} of the input terminals) is in parallel with an R_G, and raises circuit gain slightly.

The EL4430 is stable for a gain of 1 (a direct connection between V_{OUT} and FB) or more and the EL4431 for gains of 2 or more. It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel of resistors R_F and R_G and stray capacitance should be at least 200 MHz; typical strays of 3 pF thus require a feedback impedance of 270Ω or less. Two 510Ω resistors are acceptable for a gain of 2; 300Ω and 2700Ω make a good gain-of-10 divider. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB terminal input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors (for a gain of 2) across equal divider resistors will dominate parasitic effects and allow a higher divider resistance.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to 4″ of unshielded wiring or about 6″ of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often, placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of approximately 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between $(V-)+3V$ and $(V+)-3V$ to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±2V in the EL4430 and EL4431. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6µA maximum DC current, and may be biased anywhere between $(V-)+2.5V$ and $(V+)-3.5V$. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances CMRR over frequency, and if connected to a potential other than ground, it must be bypassed.

Applications Information — Contd.

Power Supplies

The instrumentation amplifiers work well on any supplies from ±3V to ±15. The supplies may be of different voltages as long as the requirements of the Gnd pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as low as 0.01μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V- to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the amplifiers increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \times V_S \times I_S, \max + (V_S - V_O) \times V_O/R_{PAR}$$

where I_S, max is the maximum supply current

V_S is the ± supply voltage (assumed equal)

V_O is the output voltage

R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4431 draws a maximum of 16 mA and we might require a 2V peak output into 150Ω and a 270Ω + 270Ω feedback divider. The R_{PAR} is 117Ω. The dissipation with ±5V supplies is 201 mW. The maximum supply voltage that the device can run on for a given P_D and the other parameter is

$$V_S, \max = (P_D + V_O2/R_{PAR})/(2I_S + V_O/R_{PAR})$$

The maximum dissipation a package can offer is

$$P_D, \max = (T_J, \max - T_A \max)/\theta_{JA}$$

where T_J, max is the maximum die junction temperature, 150°C for reliability, less to retain optimum electrical performance.

T_A, max is the ambient temperature, 70°C for commercial and 85°C for industrial range.

θ_{JA} is the thermal resistance of the mounted package, obtained from datasheet dissipation curves.

The more difficult case is the SO-8 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 170°C/W gives a dissipation of 382 mW at 85°C. This allows a maximum supply voltage of ±8.5V for the EL4431 operated in our example. If an EL4430 were driving a light load ($R_{PAR} \rightarrow \infty$), it could operate on ±15V supplies at a 70°C maximum ambient.

Output Loading

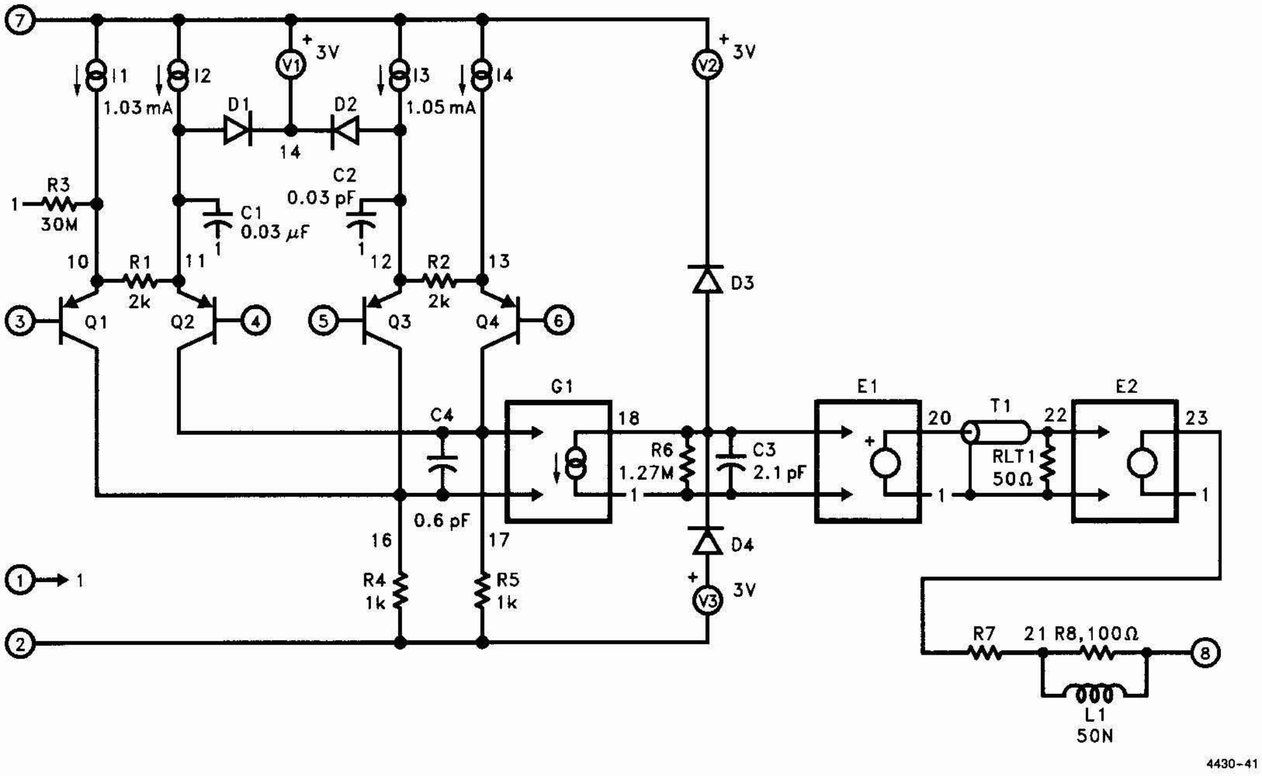
The output stage of the instrumentation amplifiers is very powerful. It typically can source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this datasheet, or higher purely transient currents.

Gain or gain accuracy degrades only 10% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads <100Ω

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it (12Ω to 51Ω should suffice). A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.

```
*  Macromodel
*  This is a Pspice-compatible macromodel of the EL4430 video instrumentation
*  amplifier assembled as a subcircuit. The pins are numbered sequentially
*  as the subcircuit interface nodes. T1 is a transmission line which provides
*  a good emulation of the more complicated real device. This model correctly
*  displays the characteristics of input clipping, frequency response, CMRR
*  both AC and DC, output clipping, output sensitivity to capacitive loads,
*  gain accuracy, slewrate limiting, input bias current and impedance. The
*  macromodel does not exhibit proper results with respect to supply current,
*  supply sensitivities, offsets, output current limit, differential gain or
*  phase, nor temperature.
*  Connections:      IN+
*                     |   VIN-
*                     |    |    V-
*                     |    |    |    V+
*                     |    |    |    |    VFB
*                     |    |    |    |    |    VREF
*                     |    |    |    |    |    |    VOUT
*                     |    |    |    |    |    |    |    GND
*                     |    |    |    |    |    |    |    |
.SUBCKT EL4430/EL     3    4    2    7    6    5    8    1
***
*** EL4430 macromodel ***
***
******
i1 7 10 .00103
i2 7 11 .00103
i3 7 12 .00105
i4 7 13 .00105
v1 7 14 3
v2 7 15 3
v3 19 2 3
******
c1 11 1 .03p
c2 12 1 .03p
c3 18 1 2.1p
c4 16 17 0.6p
******
r1 10 11 2000
r2 12 13 2000
r3 10 1 30e6
r4 16 2 1000
r5 17 2 1000
r6 18 1 1.27e6
r7 23 21 20
r8 21 8 100
******
l1 21 8 50n
******
d1 11 14 diode
d2 12 14 diode
d3 18 15 diode
d4 19 18 diode
.model diode d(tt=120n)
******
q1 16 3 10 1 pnp
q2 17 4 11 1 pnp
q3 16 5 12 1 pnp
q4 17 6 13 1 pnp
.model pnp pnp (bf=90 va=44 tr=50n)
******
g1 18 1 17 16 .0005
e1 20 1 1 18 1.0
t1 22 1 20 1 z0=50 td=1.5n
rlt1 22 1 50
e2 23 1 22 1 1.0
******
.ENDS
```

EL4430C/EL4431C Macromodel — Contd.


7
I1
1.03 mA
I2
V1
+ 3V
I3
1.05 mA
I4
V2
+ 3V
D1
D2
14
C2
0.03 pF
R3
1
30M
C1
0.03 μF
1
1
10
R1
2k
11
12
R2
2k
13
3
Q1
Q2
4
5
Q3
Q4
6
D3
G1
18
C4
R6
1.27M
C3
2.1 pF
1
0.6 pF
E1
+
20
T1
RLT1
50Ω
22
1
E2
23
1
16
17
D4
1
1
R4
1k
R5
1k
V3
+ 3V
2
R7
21
R8, 100Ω
8
L1
50N
4430-41

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4451C

Wideband Variable-Gain Amplifier, Gain of 2

Features

- Complete variable-gain amplifier with output amplifier, requires no extra components
- Excellent linearity of 0.2%
- 70 MHz signal bandwidth
- Operates on ±5V to ±15V supplies
- All inputs are differential
- 400V/µs slew rate
- >70dB attenuation @ 4 MHz

Applications

- Leveling of varying inputs
- Variable filters
- Fading
- Text insertion into video

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4451CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL4451CS	−40°C to +85°C	14-Lead SO	MDP0027

General Description

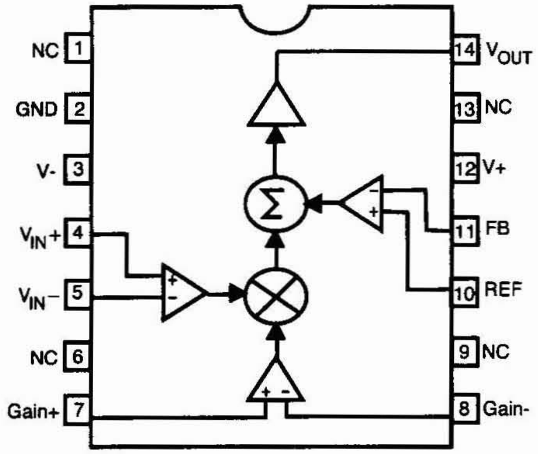
The EL4451C is a complete variable gain circuit. It offers wide bandwidth and excellent linearity while including a powerful output voltage amplifier, drawing modest supply current.

The EL4451C operates on ±5V to ±15V supplies and has an analog input range of ±2V, making it ideal for video signal processing. AC characteristics do not change appreciably over the ±5V to ±15V supply range.

The circuit has an operational temperature range of −40°C to +85°C and is packaged in plastic 14-pin DIP and 14-lead SO.

The EL4451C is fabricated with Elantec's proprietary complementary bipolar process which provides excellent signal symmetry and is free from latch up.

Connection Diagram



4451-1

October 1994 Rev A

Absolute Maximum Ratings (T_A = 25°C)

V+	Positive Supply Voltage	16.5V
V_S	V+ to V− Supply Voltage	33V
V_{IN}	Voltage at any Input or Feedback	V+ to V−
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V
I_{IN}	Current into any Input, or Feedback Pin	4mA

I_{OUT}	Continuous Output Current	30mA
P_D	Maximum Power Dissipation	See Curves
T_A	Operating Temperature Range	−40°C to +85°C
T_S	Storage Temperature Range	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics Power Supplies at ±5V, T_A = 25°C, R_L = 500Ω.

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{DIFF}	Signal input differential input voltage - Clipping	1.8	2.0		I	V
	0.2% nonlinearity		1.3		V	V
V_{CM}	Common-mode range of V_{IN}; V_{DIFF} = 0, V_s = ±5V	±2.0	±2.8		I	V
	V_s = ±15V		±12.8		V	V
V_{OS}	Input offset voltage		7	25	I	mV
V_{OS}, FB	Output offset voltage		8	25	I	mV
$V_{G, 100\%}$	Extrapolated voltage for 100% gain	1.9	2.1	2.2	I	V
$V_{G, 0\%}$	Extrapolated voltage for 0% gain	−0.16	−0.06	0.06	I	V
$V_{G, 1V}$	Gain at V_{GAIN} = 1V	0.95	1.05	1.15	I	V/V
I_B	Input bias current (all inputs)	−20	−9	0	I	μA
I_{OS}	Input offset current between V_{IN}+ and V_{IN}−, Gain+ and Gain−, FB and Ref		0.2	4	I	μA
NL	Nonlinearity, V_{IN} between −1V and +1V, V_G = 1V		0.2	0.5	I	%
Ft	Signal feedthrough, V_G = −1V		−100	−70	I	dB
R_{IN}, V_{IN}	Input resistance, V_{IN}	100	230		I	KΩ
R_{IN}, FB	Input resistance, FB	200	460		V	KΩ
R_{IN}, R_{GAIN}	Input resistance, gain input	50	100		I	KΩ

Open-Loop DC Electrical Characteristics — Contd.

Power Supplies at ±5V, T_A = 25°C, R_L = 500Ω.

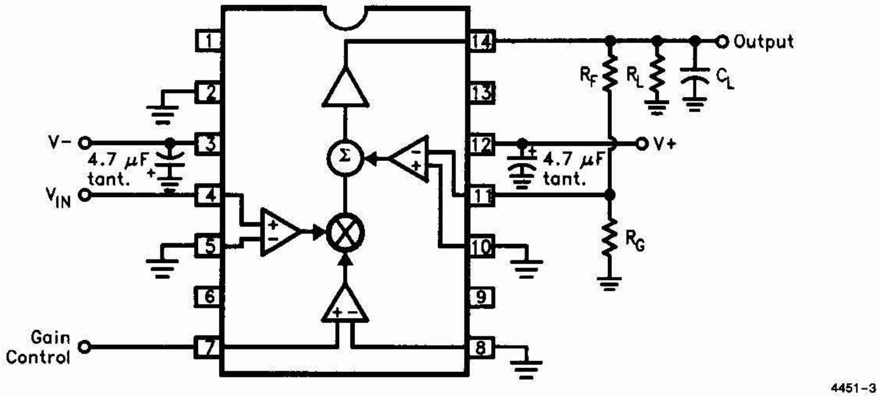
Parameter	Description	Min	Typ	Max	Test Level	Units
CMRR	Common-mode rejection ratio of V_{IN}	70	90		I	dB
PSRR	Power supply rejection ratio of $V_{OS, FB}$, V_S = ±5V to ±15V	50	60		I	dB
V_O	Output voltage swing V_S = ±5V (V_{IN} = 0, V_{REF} varied) V_S = ±15V	±2.5 ±12.5	±2.8 ±12.8		I	V
I_{SC}	Output short-circuit current	40	85		I	mA
I_S	Supply current, V_S = ±15V		15.5	18	I	mA

Closed-Loop AC Electrical Characteristics

Power supplies at ±12V, T_A = 25°C. R_L = 500Ω, C_L = 15pF, V_G = 1V

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, −3dB	−3dB small-signal bandwidth, signal input		70		V	MHz
BW, ±0.1dB	0.1dB flatness bandwidth, signal input		10		V	MHz
Peaking	Frequency response peaking		0.6		V	dB
BW, gain	−3dB small-signal bandwidth, gain input		70		V	MHz
SR	Slew rate, V_{OUT} between −2V and +2V, R_F = R_G = 500Ω		400		V	V/µs
V_N	Input referred noise voltage density		110		V	nV/√Hz
dG	Differential gain error, Voffset between −0.7V and +0.7V		0.9		V	%
dθ	Differential phase error, Voffset between −0.7V and +0.7V		0. 2		V	°

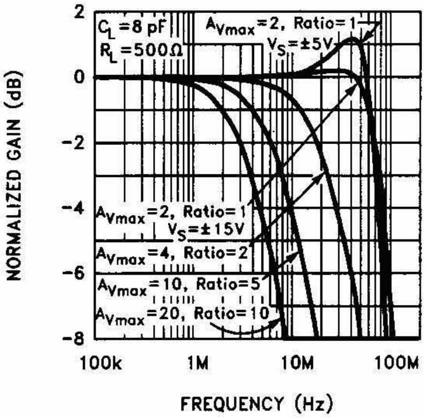
Test Circuit



Note: For typical performance curves, R_F = 0, R_G = ∞, V_{GAIN} = 1V, R_L = 500Ω, and C_L = 15 pF unless otherwise noted.

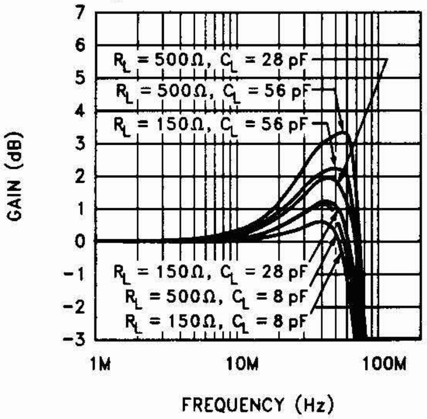
Typical Performance Curves

Frequency Response for Various Feedback Divider Ratios



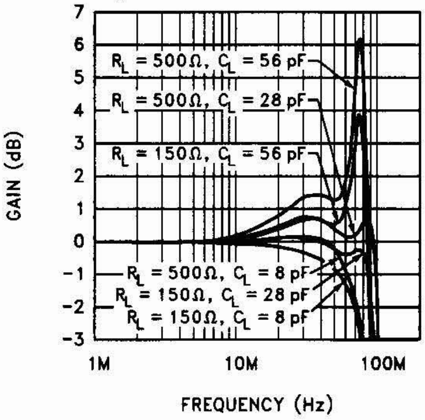
4451-4

Frequency Response for Various R_L, C_L V_S = ±5V



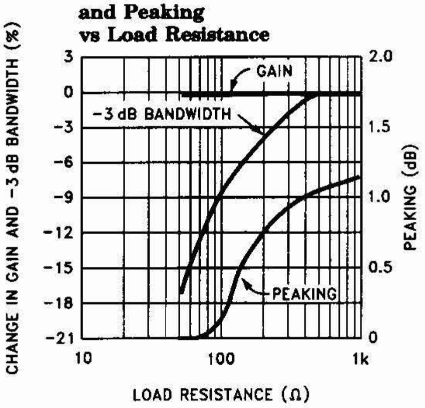
4451-5

Frequency Response for Various R_L, C_L V_S = ±15V



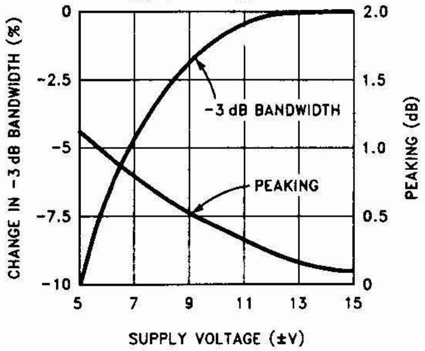
4451-6

Gain, −3 dB Bandwidth, and Peaking vs Load Resistance



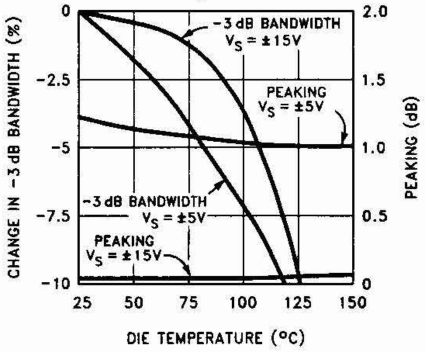
4451-7

−3 dB Bandwidth and Peaking vs Supply Voltage



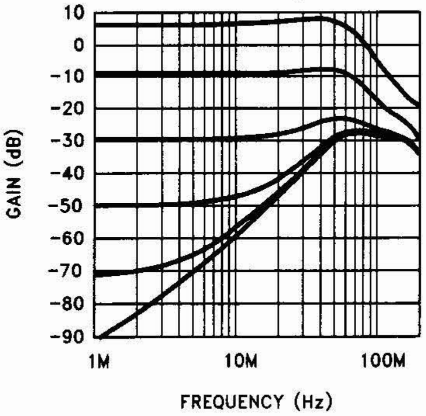
4451-8

−3 dB Bandwidth and Peaking vs Die Temperature



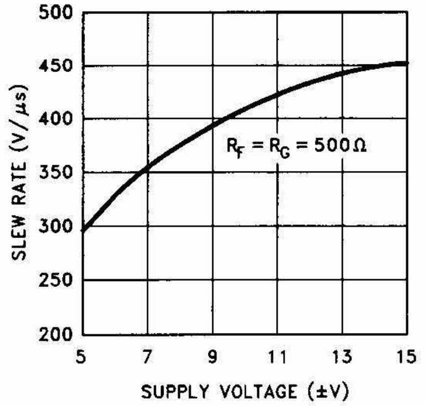
4451-9

Frequency Response for Various Gain Settings



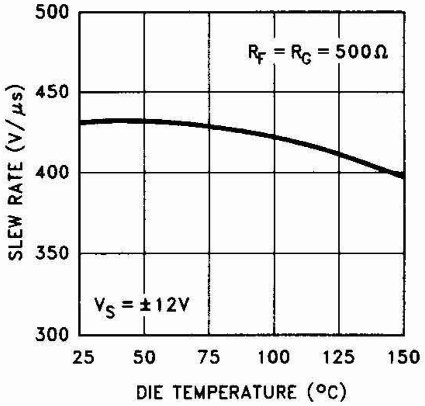
4451-10

Slew Rate vs Supply Voltage



4451-11

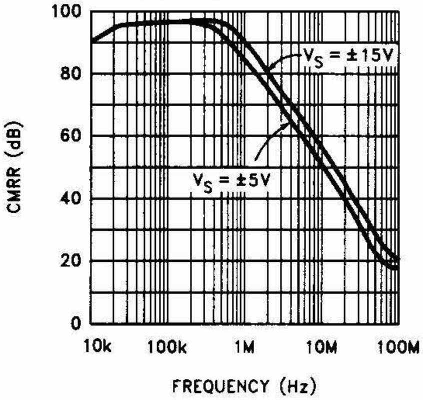
Slew Rate vs Die Temperature



4451-12

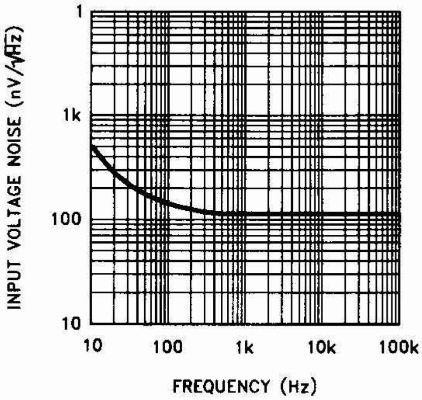
Typical Performance Curves — Contd.

Common-Mode Rejection Ratio vs Frequency



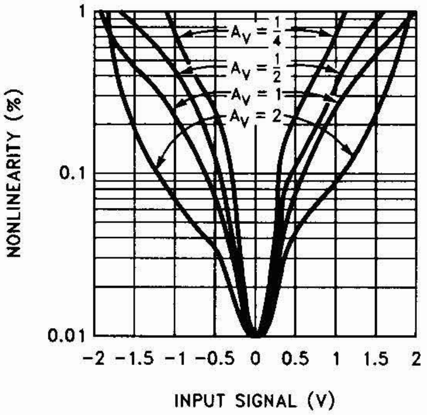
4451-13

Input Voltage Noise vs Frequency



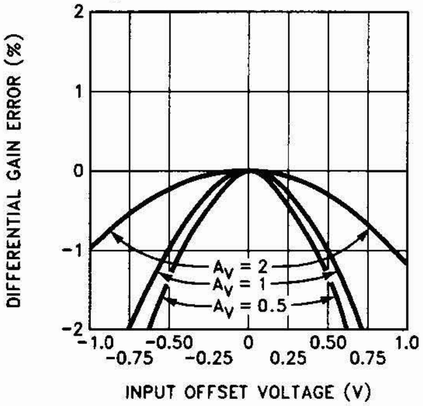
4451-14

Nonlinearity vs Input Signal



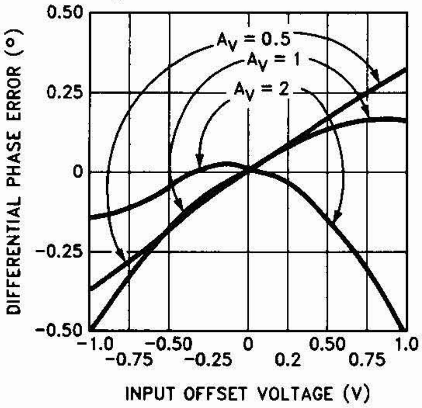
4451-15

Differential Gain Error vs Input Offset Voltage V_S = ±5V or ±12V



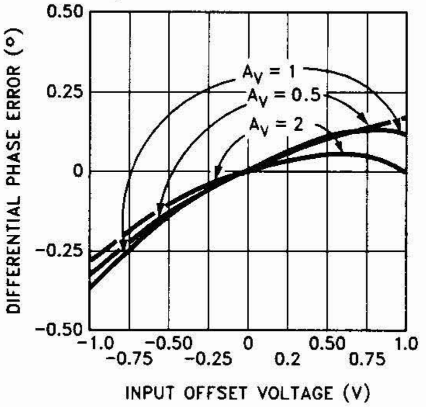
4451-16

Differential Phase Error vs Input Offset Voltage V_S = ±5V



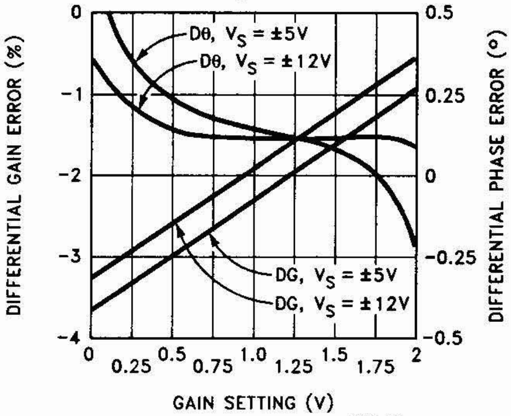
4451-17

Differential Phase Error vs Input Offset Voltage V_S = ±12V



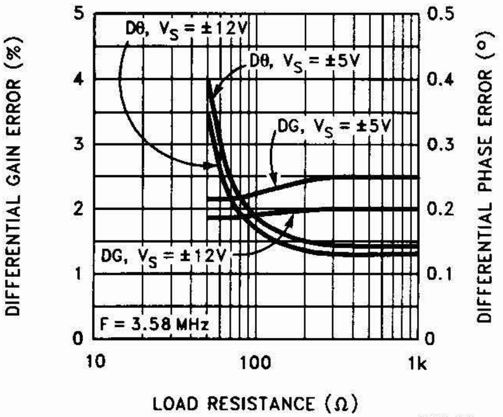
4451-18

Differential Gain and Phase Errors vs Gain Setting



4451-19

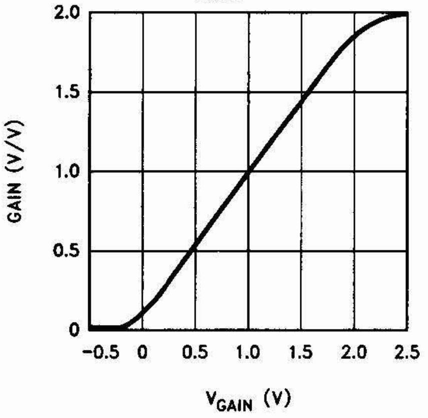
Differential Gain and Phase Errors vs Load Resistance



4451-20

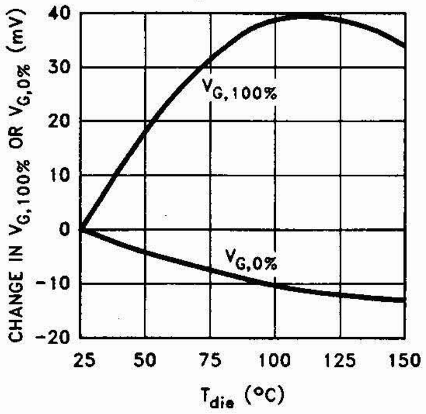
Typical Performance Curves — Contd.

Gain vs V_{GAIN}



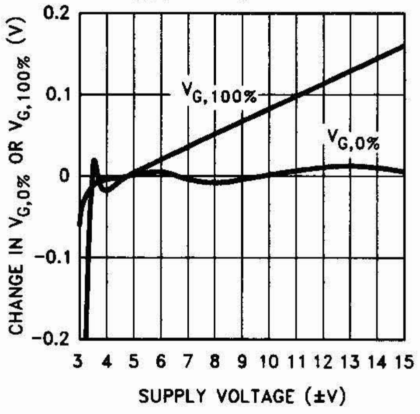
4451-21

Change in $V_{G,100\%}$ and $V_{G,0\%}$ vs Die Temperature



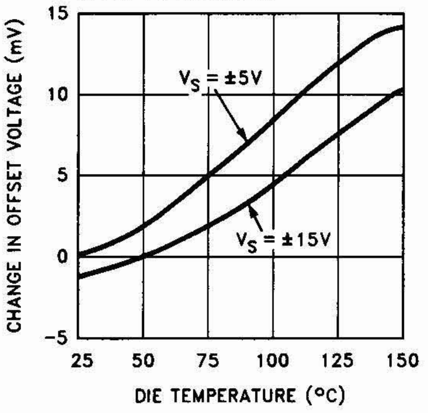
4451-22

$V_{G,0\%}$ and $V_{G,100\%}$ vs Supply Voltage



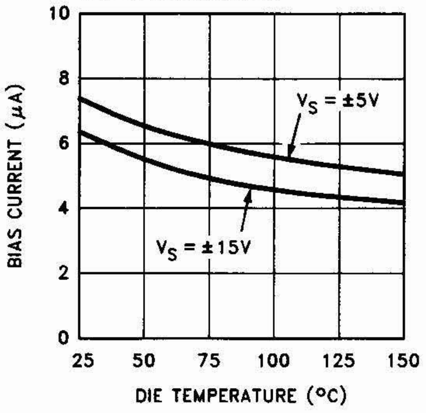
4451-23

Offset Voltage vs Die Temperature



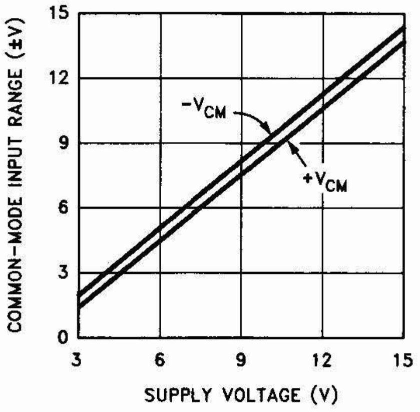
4451-24

Bias Current vs Die Temperature



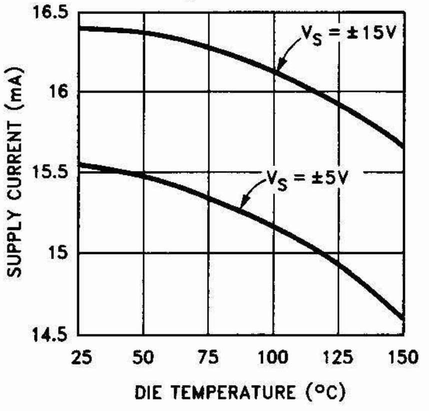
4451-25

Common Mode Input Range vs Supply Voltage



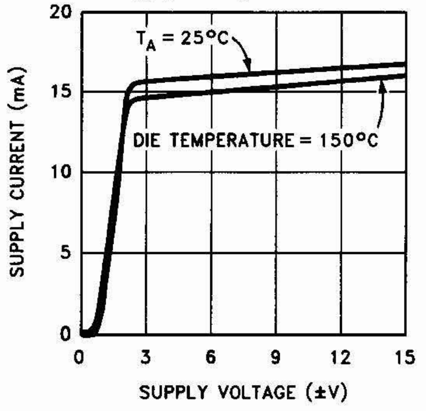
4451-26

Supply Current vs Die Temperature



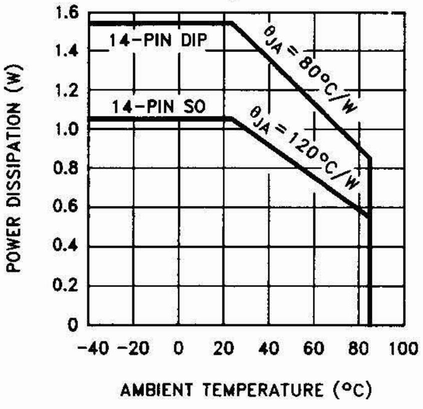
4451-27

Supply Current vs Supply Voltage



4451-28

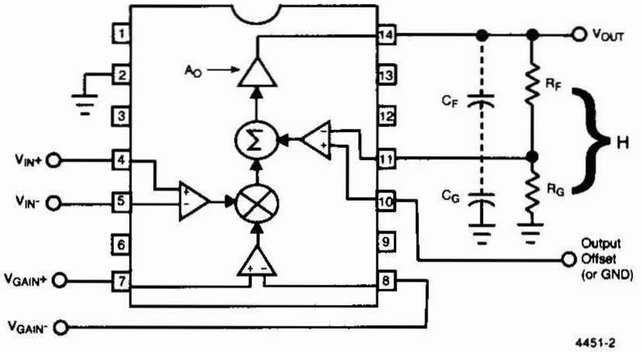
14-Pin Package Power Dissipation vs Ambient Temperature



4451-29

Applications Information

The EL4451 is a complete two-quadrant multiplier/gain control with 70 MHz bandwidth. It has three sets of inputs; a differential signal input V_{IN}, a differential gain-controlling input V_{GAIN}, and another differential input which is used to complete a feedback loop with the output. Here is a typical connection:



The gain of the feedback divider is

$$H = \frac{R_G}{R_G + R_F}.$$

The transfer function of the part is

$$V_{OUT} = A_O \times (((V_{IN}+) - (V_{IN}-)) \times ((V_{GAIN}+) - (V_{GAIN}-)) + (V_{REF} - V_{FB})).$$

V_{FB} is connected to V_{OUT} through a feedback network, so $V_{FB} = H \times V_{OUT}$. A_O is the open-loop gain of the amplifier, and is approximately 600. The large value of A_O drives

$$((V_{IN}+) - (V_{IN}-)) \times ((V_{GAIN}+) - (V_{GAIN}-)) + (V_{REF} - V_{FB}) \rightarrow 0.$$

Rearranging and substituting for V_{FB}

$$V_{OUT} = (((V_{IN}+) - (V_{IN}-)) \times ((V_{GAIN}+) - (V_{GAIN})) + V_{REF})/H,$$

or

$$V_{OUT} = (V_{IN} \times V_{GAIN} + V_{REF})/H$$

Thus the output is equal to the difference of the V_{IN}'s times the difference of $V_{GAIN'S}$ and offset by V_{REF}, all gained up by the feedback divider ratio. The EL4451 is stable for a direct connection between V_{OUT} and FB, and the divider may be used for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 150 MHz; typical strays of 3 pF thus require a feedback impedance of 360Ω or less. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback and the gain resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10pF capacitors across equal divider resistors for a maximum gain of 4 will dominate parasitic effects and allow a higher divider resistance.

The REF pin can be used as the output's ground reference, for DC offsetting of the output, or it can be used to sum in another signal.

Gain-Control Characteristics

The quantity V_{GAIN} in the above equations is bounded as $0 \leq V_{GAIN} \leq 2$, even though the externally applied voltages exceed this range. Actually, the gain transfer function around 0 and 2V is "soft"; that is, the gain does not clip abruptly below the 0%-V_{GAIN} voltage nor above the 100%-V_{GAIN} level. An overdrive of 0.3V must be applied to V_{GAIN} to obtain truly 0% or 100%. Because the 0%- or 100%- V_{GAIN} levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied V_{GAIN} range of −0.5V to +2.5V will assure the full numerical span of $0 \leq V_{GAIN} \leq 2$.

The gain control has a small-signal bandwidth equal to the V_{IN} channel bandwidth, and overload recovery resolves in about 20 nsec.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or 6″ of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Applications Information — Contd.

Signal Amplitudes

Signal input common-mode voltage must be between (V−)+3V and (V+)−3V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±2V in the EL4451. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6μA maximum DC current, and may be biased anywhere between (V−)+2.5V and (V+)−3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and feedthrough over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4451 works with any supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the ground pin are observed (see the Ground Pin section). The supplies should be bypassed close to the device with short leads. 4.7μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4451 increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \times V_S \times I_{S,\,max} + (V_S - V_O) \times V_O/R_{PAR}$$

where I_S, max is the maximum supply current

V_S is the ± supply voltage (assumed equal)

V_O is the output voltage

R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4451 draws a maximum of 18mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with ±5V supplies is 180 mW. The maximum supply voltage that the device can run on for a given P_D and other parameters is

$$V_{S,\,max} = (P_D + V_O^2/R_{PAR}) / (2I_S + V_O/R_{PAR})$$

The maximum dissipation a package can offer is

$$P_{D,\,max} = (T_{J,\,max} - T_{A,\,max}) / \theta_{JA}$$

Where T_J, max is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance

T_A, max is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°C/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded.

Output Loading

The output stage of the EL4451 is very powerful. It typically can source 80mA and sink 120mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads <100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220pF load.

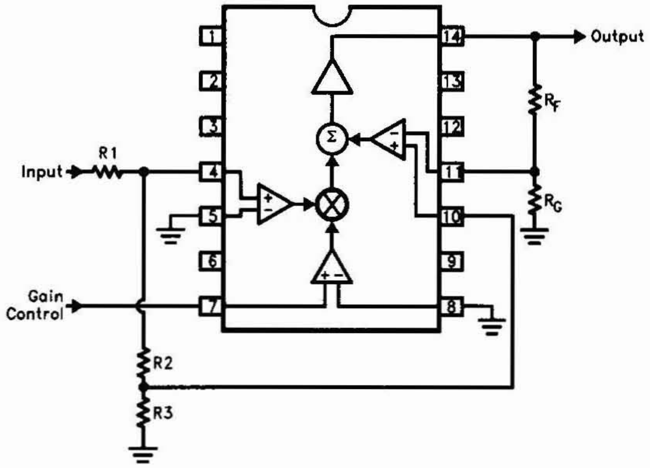
Applications Information — Contd.

Leveling Circuits

Often a variable-gain control is used to normalize an input signal to a standard amplitude from a modest range of possible input amplitude. A good example is in video systems, where an unterminated cable will yield a twice-sized standard video amplitude, and an erroneously twice-terminated cable gives a 2/3-sized input.

Here is a ±6 dB range preamplifier:

Linearized Leveling Amplifier

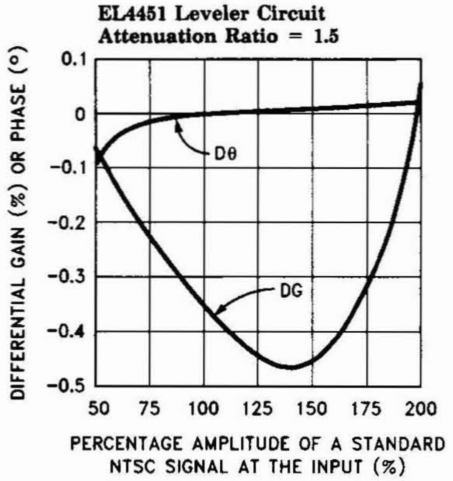


4451-30

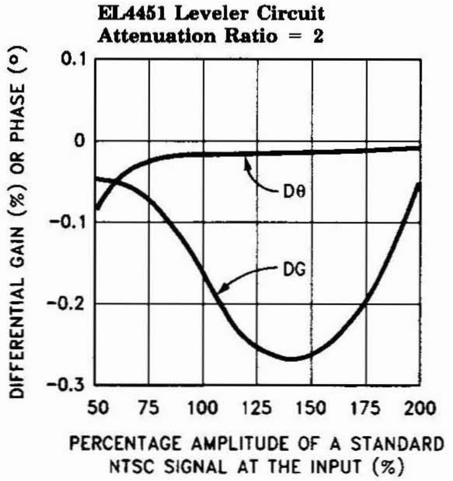
In this arrangement, the EL4451 outputs a mixture of the signal routed through the multiplier and the REF terminal. The multiplier port produces the most distortion and needs to handle a fraction of an oversized video input, whereas the REF port is just like an op-amp input summing into the output. Thus, for oversized inputs the gain will be decreased and the majority of the signal is routed through the linear REF terminal. For undersized inputs, the gain is increased and the multiplier's contribution added to the output.

Here are some component values for two designs:

Attenuation Ratio	R_F	R_G	R_1	R_2	R_3	−3 dB Bandwidth
1.5	200Ω	400Ω	300Ω	100Ω	200Ω	47 MHz
2	400Ω	400Ω	500Ω	100Ω	200Ω	28 MHz


EL4451 Leveler Circuit
Attenuation Ratio = 1.5

4451-31


EL4451 Leveler Circuit
Attenuation Ratio = 2

4451-32

With the higher attenuation ratio, the multiplier sees a smaller input amplitude and distorts less, however the higher output gain reduces circuit bandwidth. As seen in the next curves, the peak differential gain error is 0.47% for the attenuation ratio of 1.5, but only 0.27% with the gain of 2 constants. To maintain bandwidth, an external op amp can be used instead of the R_F - R_G divider to boost the EL4451's output by the attenuation ratio.

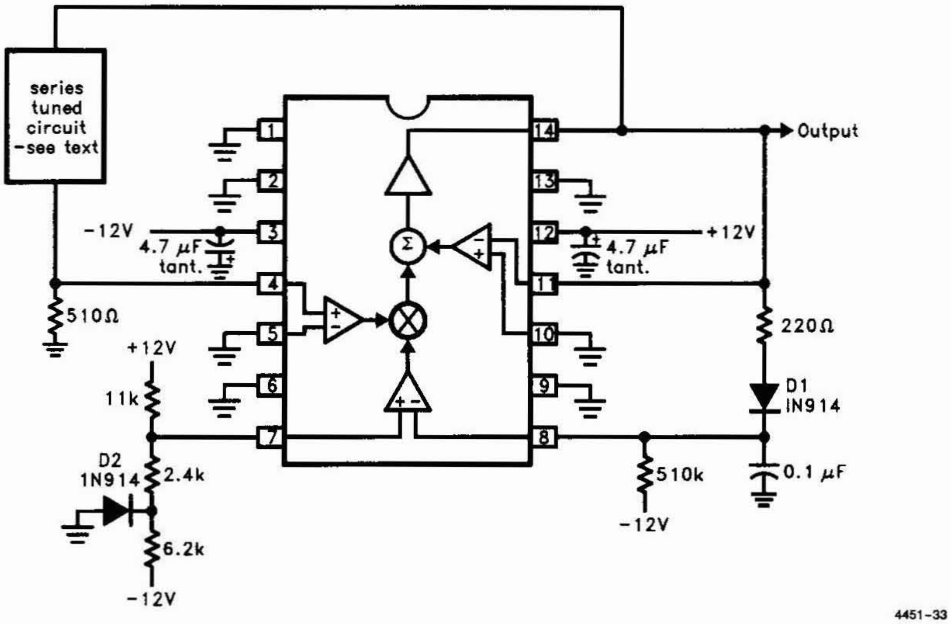
Sinewave Oscillators

Generating a stable, low distortion sinewave has long been a difficult task. Because a linear oscillator's output tends to grow or diminish continuously, either a clipping circuit or automatic gain control (AGC) is needed. Clipping circuits generate severe distortion which needs subsequent filtering, and AGC's can be complicated.

Applications Information — Contd.

Here is the EL4451 used as an oscillator with simple AGC:

Low-Distortion Sinewave Oscillator


series tuned circuit -see text
Output
-12V
4.7 μF tant.
+12V
4.7 μF tant.
510Ω
+12V
11k
D2 1N914
2.4k
6.2k
-12V
220Ω
D1 1N914
510k
-12V
0.1 μF
1
2
3
4
5
6
7
8
9
10
11
12
13
14
Σ
+
−
4451-33

The oscillation frequency is set by the resonance of a series-tuned circuit, which may be an L-C combination or a crystal. At resonance, the series impedance of the tuned circuit drops and its phase lag is 0°, so the EL4451 needs a gain just over unity to sustain oscillation. The $V_{GAIN}-$ terminal is initially at $-0.7V$ and the $V_{GAIN}+$ terminal at about $+2.1V$, setting the maximum gain in the EL4451. At such high gain, the loop oscillates and output amplitude grows until D_1 rectifies more positive voltage at $V_{GAIN}-$, ultimately reducing gain until a stable 0.5Vrms output is produced.

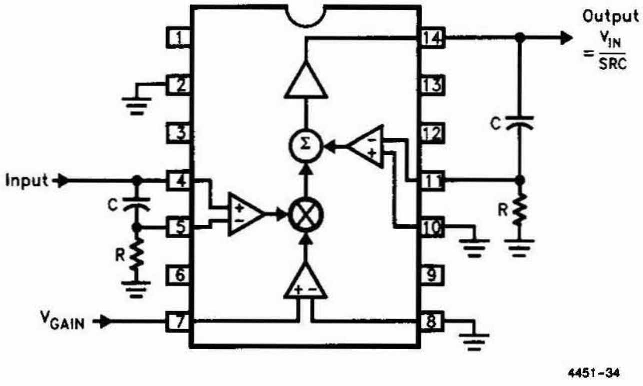
Using a 2 MHz crystal, output distortion was -53 dBc, or 0.22%. Sideband modulation was only 14 Hz wide at -90 dBc, limited by the filter of the spectrum analyzer used.

The circuit works up to 30 MHz. A parallel-tuned circuit can replace the 510Ω resistor and the 510Ω resistor moved in place of the series-tuned element to allow grounding of the tuned components.

Filters

The EL4451 can be connected to act as a voltage-variable integrator as shown:

EL4451 Connected As Variable Integrator

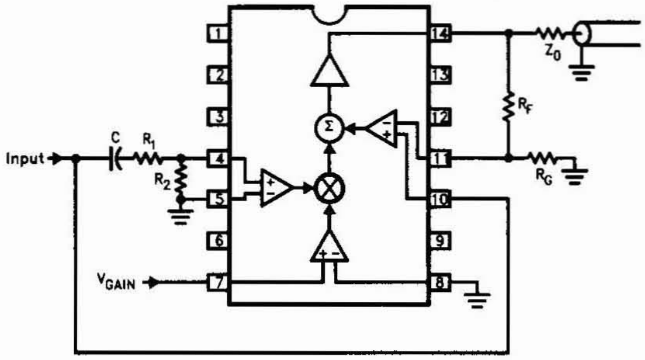

Output
$= \frac{V_{IN}}{SRC}$
Input
C
R
V_{GAIN}
C
R
1
2
3
4
5
6
7
8
9
10
11
12
13
14
Σ
4451-34

The input RC cancels a zero produced by the output op-amp feedback connection at $\omega = 1/RC$. With the input RC connected $V_{OUT}/V_{IN} = 1/sRC$; without it $V_{OUT}/V_{IN} = (1 + sRC)/sRC$. This variable integrator may be used in networks such as the Bi-quad. In some applications the input RC may be omitted. If a negative gain is required, the $V_{IN}+$ and $V_{IN}-$ terminals can be exchanged.

Applications Information — Contd.

A voltage-controlled equalizer and cable driver can be constructed so:

Equalization and Line Driver Amplifier



4451-35

The main signal path is via the REF pin. This ensures maximum signal linearity, while the multiplier input is used to allow a variable amount of frequency-shaped input from R_1, R_2, and C. For optimum linearity, the multiplier input is attenuated by R_1 and R_2. This may not be necessary, depending on input signal amplitude, and R_1 might be set to 0. $R_1$and R_2 should be set to provide sufficient peaking, depending on cable high-frequency losses, at maximum gain. R_F and R_G are chosen to provide the desired circuit gain, including backmatch resistor loss.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4452C

Wideband Variable-Gain Amplifier with Gain of 10

Features

- Complete variable-gain amplifier complete with output amplifier
- Compensated for Gain ≥ 10
- 50 MHz signal bandwidth
- 50 MHz gain-control bandwidth
- Low 29 nV/√Hz input noise
- Operates on ±5V to ±15V supplies
- All inputs are differential
- >70 dB attenuation @ 5 MHz

Applications

- AGC variable-gain amplifier
- IF amplifier
- Transducer amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4452CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL4452CS	−40°C to +85°C	14-lead SO	MDP0027

General Description

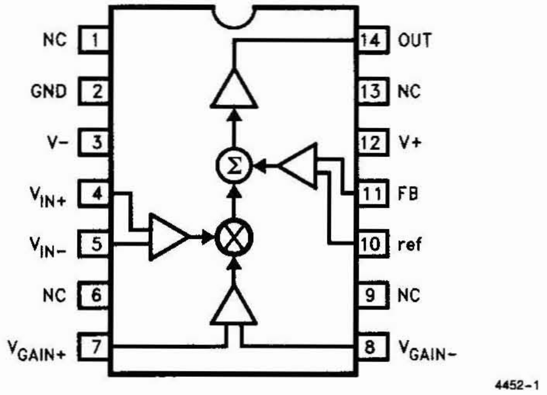
The EL4452 is a complete variable-gain circuit. It offers wide bandwidth and excellent linearity, while including a powerful output voltage amplifier, drawing modest current. The higher gain and lower input noise makes the EL4452 ideal for use in AGC systems.

The EL4452 operates on ±5V to ±15V and has an analog input range of ±0.5V. AC characteristics do not change appreciably over the supply range.

The circuit has an operational temperature of −40°C to +85°C and is packaged in 14-pin P-DIP and SO-14.

The EL4452 is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is very rugged.

Connection Diagram



December 1994 Rev A

Absolute Maximum Ratings (T_A = 25°C)

V+	Positive Supply Voltage	16.5V	I_{IN}	Current into any Input or Feedback Pin	4 mA
V_S	V+ to V− Supply Voltage	33V	I_{OUT}	Output Current	30 mA
V_{IN}	Voltage at any Input or Feedback	V+ to V−	P_D	Maximum Power Dissipation	See Curves
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V	T_A	Operating Temperature Range	−40°C to +85°C
			T_S	Storage Temperature Range	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics

Power supplies at ±5V, T_A = 25°C, R_F = 910Ω, R_G = 100Ω, R_L = 500Ω

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{DIFF}	Signal Input Differential Input Voltage - Clipping	0.4	0.5		I	V
	0.6% Nonlinearity		0.4		V	V
V_{CM}	Common-Mode Range (All Inputs; V_{DIFF} = 0) V_S = ±5V	±2.0	±2.8		I	V
	V_S = ±15V	±12.0	±12.8		V	V
V_{OS}	Input Offset Voltage			10	I	mV
V_{OS}, FB	Output Offset Voltage			10	I	mV
V_G, 100%	Extrapolated Voltage for 100% Gain	1.8	2.1	2.2	I	V
V_G, 0%	Extrapolated Voltage for 0% Gain	−0.16	−0.06	0.04	I	V
V_G, 1V	Gain at V_{GAIN} = 1 (Rf = 910Ω, Rg = 100Ω)	4.9	5.35	5.9	I	V/V
I_B	Input Bias Current (All Inputs)	−20	−9	0	I	μA
I_{OS}	Input Offset Current Between V_{IN}+ and V_{IN}−, V_{GAIN}+ and V_{GAIN}−		0.5	4	I	μA
F_T	Signal Feedthrough, V_G = −1V		−100	−70	I	dB
R_{IN}, Signal	Input Resistance, Signal Input	25	60		I	kΩ
R_{IN}, Gain	Input Resistance, Gain Input	50	120		I	kΩ
R_{IN}, FB	Input Resistance, Feedback	25	60		V	kΩ
CMRR	Common-Mode Rejection Ratio, V_{IN}	70	90		I	dB

Open-Loop DC Electrical Characteristics — Contd.

Power supplies at ±5V, T_A = 25°C, R_F = 910Ω, R_G = 100Ω, R_L = 500Ω

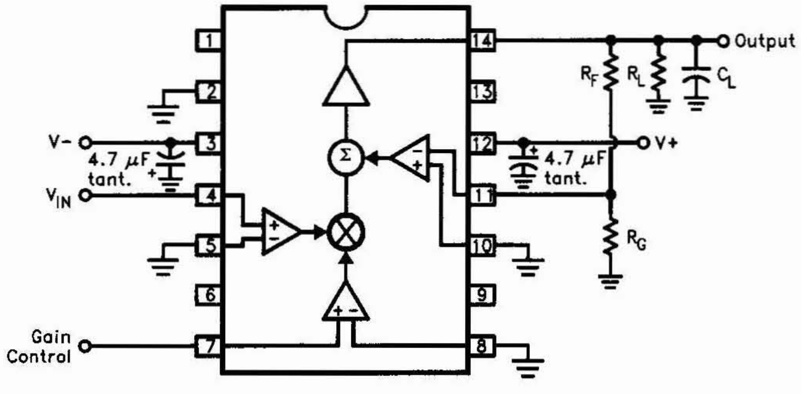
Parameter	Description	Min	Typ	Max	Test Level	Units
PSRR	Power-Supply Rejection Ratio, V_{OS}, FB; Supplies from ±5V to ±15V	65	83		I	dB
E_G	Gain Error, Excluding Feedback Resistors, V_{GAIN} = 2.5V	−7		+7	I	%
NL	Nonlinearity, V_{IN} from −0.25V to +0.25, V_{GAIN} = 1V		0.3	0.6	I	%
V_O	Output Voltage Swing V_S = ±5V (V_{IN} = 0, V_{REF} Varied) V_S = ±15V	±2.5 ±12.5	±2.8 ±12.8		I I	V V
I_{SC}	Output Short-Circuit Current	40	85		I	mA
I_S	Supply Current, V_S = ±15V		15.5	18	I	mA

Closed-Loop AC Electrical Characteristics

Power supplies at ±12V, T_A = 25°C, R_L = 500Ω, C_L = 15pF

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, −3dB	−3dB Small-Signal Bandwidth, Signal Input		50		V	MHz
BW, ±0.1dB	0.1dB Flatness Bandwidth, Signal Input		10		V	MHz
Peaking	Frequency Response Peaking		0.1		V	dB
BW, Gain	−3dB Small-Signal Bandwidth, Gain Input		50		V	MHz
SR	Slew Rate, V_{OUT} between −2V and +2V	350	400	550	I	V/μs
V_N	Input-Referred Noise Voltage Density		29		V	nV/rt-Hz

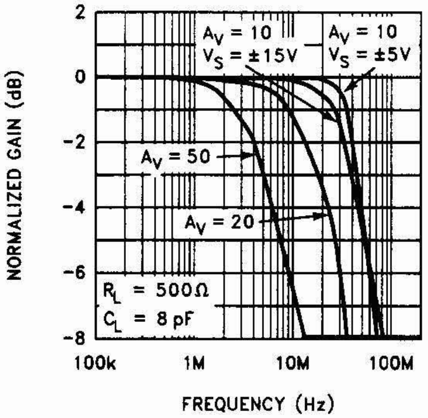
Test Circuit



Note: For typical performance curves, R_F = 910Ω, R_G = 100Ω, V_{GAIN} = 1V, R_L = 500Ω, and C_L = 15 pF unless otherwise noted.

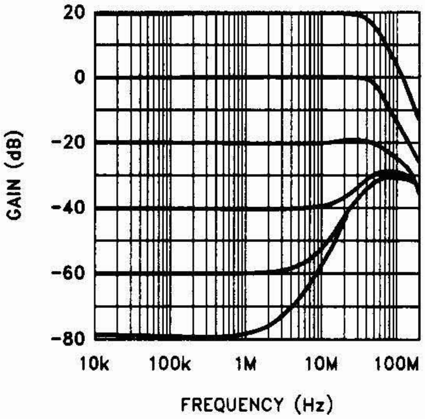
Typical Performance Curves

Frequency Response for Various Feedback Divider Ratios



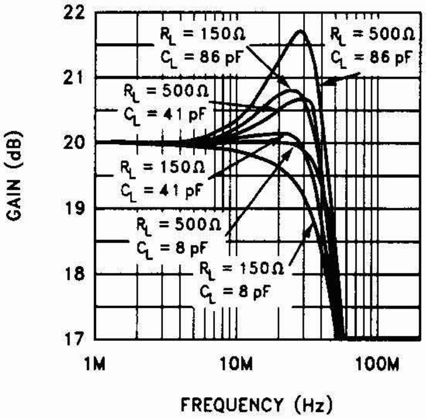
4452-3

Frequency Response for Various Gains



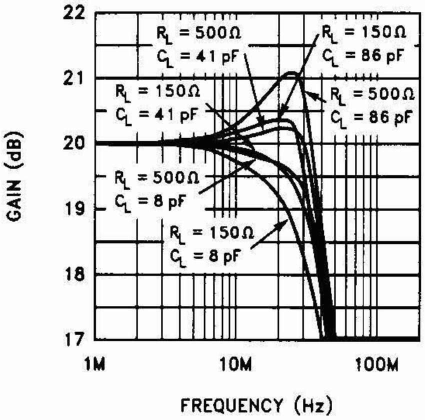
4452-4

Frequency Response for Various R_L, C_L, V_S = ±5V



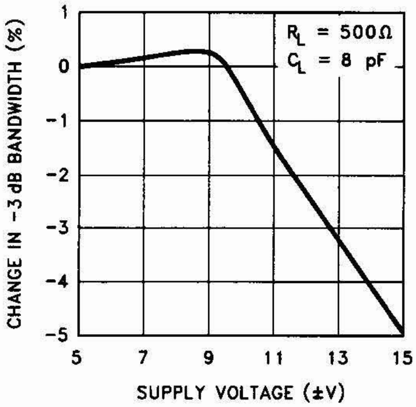
4452-5

Frequency Response for Various R_L, C_L, V_S = ±15V



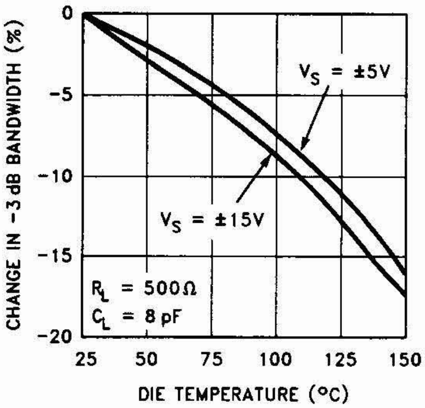
4452-6

−3 dB Bandwidth vs Supply Voltage



4452-7

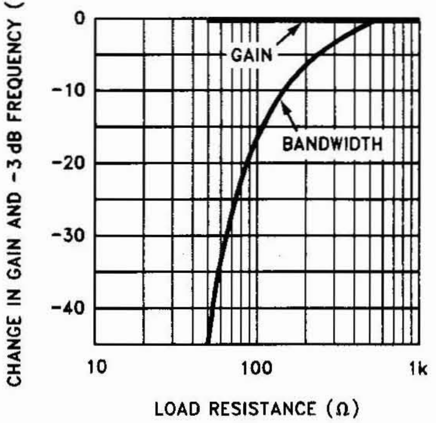
−3 dB Bandwidth vs Die Temperature



4452-8

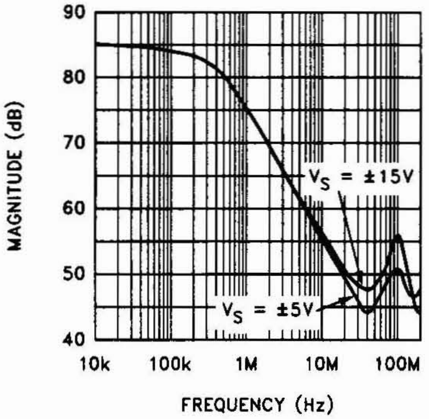
Typical Performance Curves — Contd.

Gain and −3 dB Bandwidth vs Load Resistance



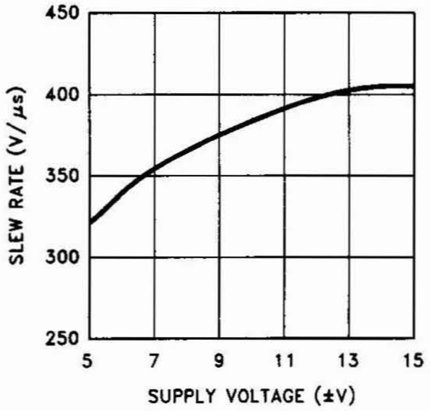
4452-9

Input Common-Mode Rejection Ratio vs Frequency



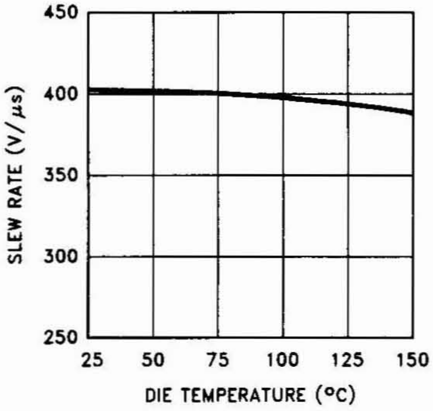
4452-10

Slew Rate vs Supply Voltage



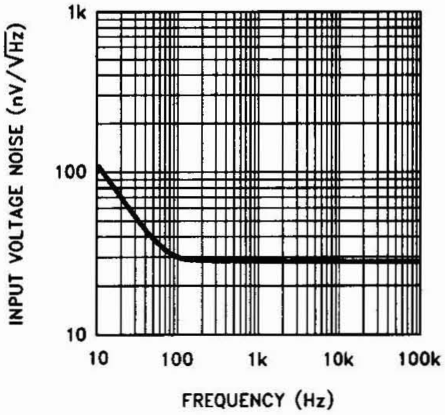
4452-11

Slew Rate vs Die Temperature



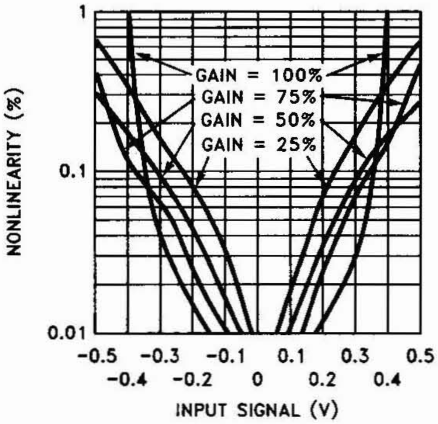
4452-12

Input Voltage Noise vs Frequency



4452-13

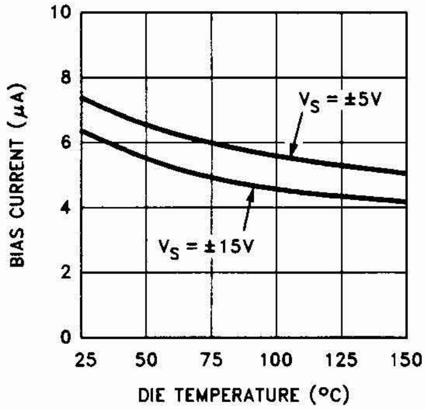
Nonlinearity vs Input Signal



4452-14

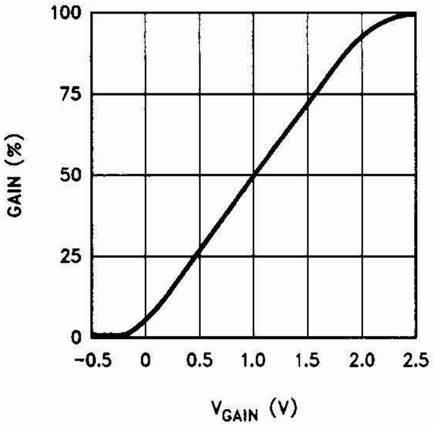
Typical Performance Curves — Contd.

Bias Current vs Die Temperature



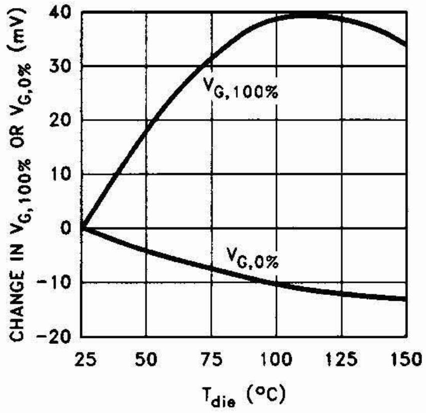
4452-15

Gain vs V_{GAIN}



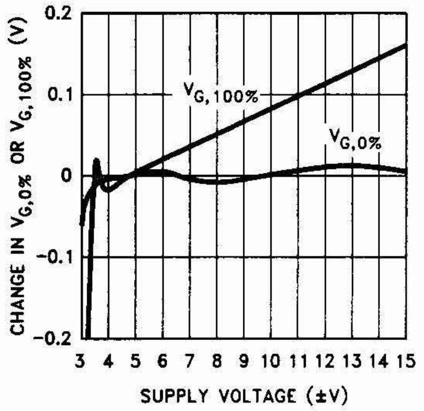
4452-16

Change in $V_{G,100\%}$ and $V_{G,0\%}$ vs Die Temperature



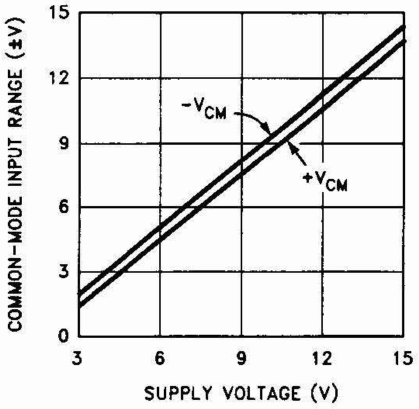
4452-17

$V_{G,0\%}$ and $V_{G,100\%}$ vs Supply Voltage



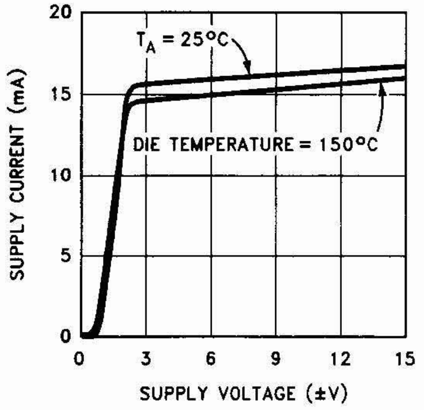
4452-18

Common Mode Input Range vs Supply Voltage



4452-19

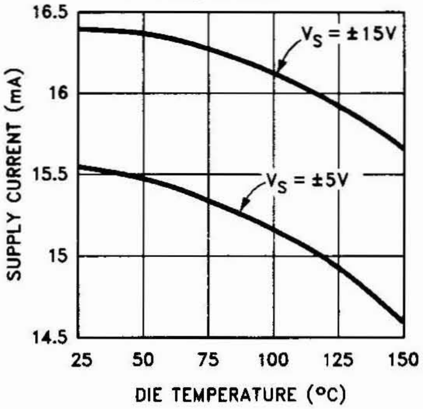
Supply Current vs Supply Voltage



4452-20

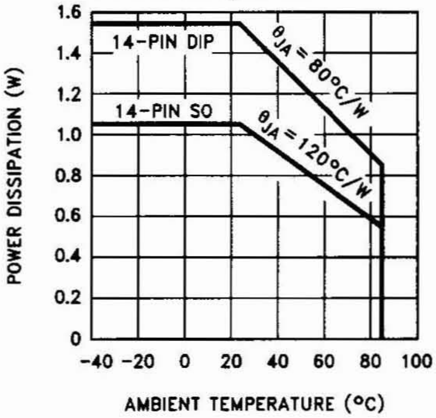
Typical Performance Curves — Contd.

Supply Current vs Die Temperature



4452-21

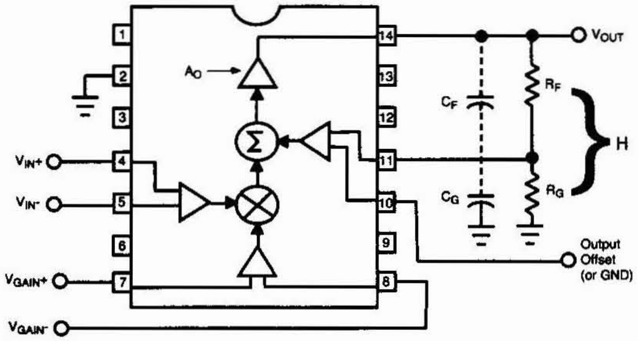
14-Pin Package Power Dissipation vs Ambient Temperature



4452-22

Applications Information

The EL4452 is a complete two-quadrant multiplier/gain control with 50 MHz bandwidth. It has three sets of inputs; a differential signal input V_{IN}, a differential gain-controlling input V_{GAIN}, and another differential input which is used to complete a feedback loop with the output. Here is a typical connection:



4451-23

The gain of the feedback divider is H. The transfer function of the part is

$V_{OUT} = A_O \times (((V_{IN}+) - (V_{IN}-)) \times ((V_{GAIN}+) - (V_{GAIN}-)) + (V_{REF} - V_{FB}))$.

V_{FB} is connected to V_{OUT} through a feedback network, so $V_{FB} = H \times V_{OUT}$. A_O is the open-loop gain of the amplifier, and is approximately 3300. The large value of A_O drives

$((V_{IN}+) - (V_{IN}-)) \times \frac{1}{2}((V_{GAIN}+) - (V_{GAIN}-)) + (V_{REF} - V_{FB}) \rightarrow 0$.

Rearranging and substituting for V_{FB}

$V_{OUT} = (((V_{IN}+) - (V_{IN}-)) \times \frac{1}{2}((V_{GAIN}+) - (V_{GAIN})) + V_{REF})/H$,

or

$V_{OUT} = (V_{IN} \times \frac{1}{2} V_{GAIN} + V_{REF})/H$

Applications Information — Contd.

Thus the output is equal to the difference of the V_{IN}'s times the difference of V_{GAIN}'S and offset by V_{REF}, all gained up by the feedback divider ratio. The EL4452 is stable for a divider ratio of $1/10$, and the divider may be set for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 130 MHz; typical strays of 3 pF thus require a feedback impedance of 400Ω or less. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback and the gain resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, a 3 pF capacitor across R_F and 27 pF to ground will dominate parasitic effects in a $1/10$ divider and allow a higher divider resistance.

The REF pin can be used as the output's ground reference, for DC offsetting of the output, or it can be used to sum in another signal.

Gain-Control Characteristics

The quantity V_{GAIN} in the above equations is bounded as $0 \leq V_{GAIN} \leq 2$, even though the externally applied voltages exceed this range. Actually, the gain transfer function around 0 and 2V is "soft"; that is, the gain does not clip abruptly below the 0%-V_{GAIN} voltage nor above the 100%-V_{GAIN} level. An overdrive of 0.3V must be applied to V_{GAIN} to obtain truly 0% or 100%. Because the 0%- or 100%- V_{GAIN} levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied V_{GAIN} range of −0.5V to +2.5V will assure the full numerical span of $0 \leq V_{GAIN} \leq 2$.

The gain control has a small-signal bandwidth equal to the V_{IN} channel bandwidth, and overload recovery resolves in about 20 nsec.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or 6″ of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between (V−) + 2.5V and (V+) − 2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±0.5V in the EL4452. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 μA maximum DC current, and may be biased anywhere between (V−)+2.5V and (V+)−3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and feedthrough over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4452 operates with power supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the ground pin are observed (see the Ground Pin section). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs

Applications Information — Contd.

and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4452 increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \times V_S \times I_S, \max + (V_S - V_O) \times V_O / R_{PAR}$$

where I_S, max is the maximum supply current

V_S is the ± supply voltage (assumed equal)

V_O is the output voltage

R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4452 draws a maximum of 18mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with ±5V supplies is 180 mW. The maximum supply voltage that the device can run on for a given P_D and other parameters is

$$V_S, \max = (P_D + V_O^2 / R_{PAR}) / (2I_S + V_O / R_{PAR})$$

The maximum dissipation a package can offer is

$$P_D, \max = (T_J, \max - T_A, \max) \, / \, \theta_{JA}$$

Where T_J, max is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance

T_A, max is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°C/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded.

Output Loading

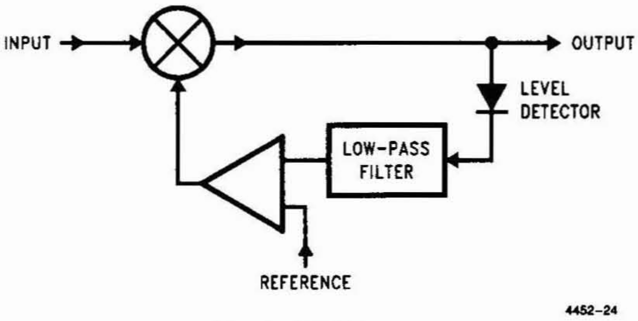
The output stage of the EL4452 is very powerful. It can typically source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to a 100Ω load. Heavy resistive loading will degrade frequency response and distortion for loads <100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 1 dB with even a 220 pF load.

AGC Circuits

The basic AGC (automatic gain control) loop is this:



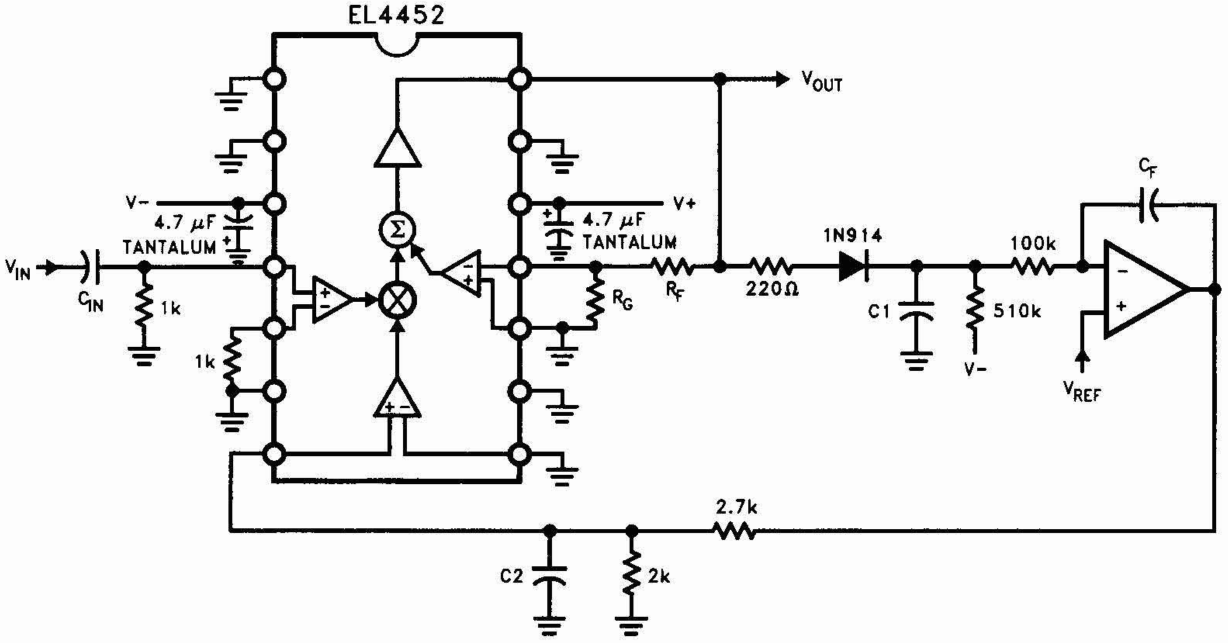
Basic AGC Loop

A multiplier scales the input signal and provides necessary gain and buffers the signal presented to the output load, a level detector (shown schematically here as a diode) converts some measure of the output signal amplitude to a DC level, a low-pass filter attenuates any signal ripple present on that DC level, and an amplifier compares that level to a reference and amplifies the error to create a gain-control voltage for the multiplier. The circuitry is a servo that attempts to keep the output amplitude constant by continuously adjusting the multiplier's gain control input.

Applications Information — Contd.

Most AGC's deal with repetitive input signals that are capacitively coupled. It is generally desirable to keep DC offsets from mixing with AC signals and fooling the level detector into maintaining the DC output offset level constant, rather than a smaller AC component. To that end, either the level detector is AC-coupled, or the reference voltage must be made greater than the maximum multiplier gain times the input offset. For instance, if the level detector output equaled the reference voltage at 1V of EL4452 output, the 8 mV of input offset would require a maximum gain of 125 through the EL4452. Bias current-induced offsets could increase this further.

Depending on the nature of the signal, different level detector strategies will be employed. If the system goal is to prevent overload of subsequent stages, peak detectors are preferred. Other strategies use an RMS detector to maintain constant output power. Here is a simple AGC using peak detection:



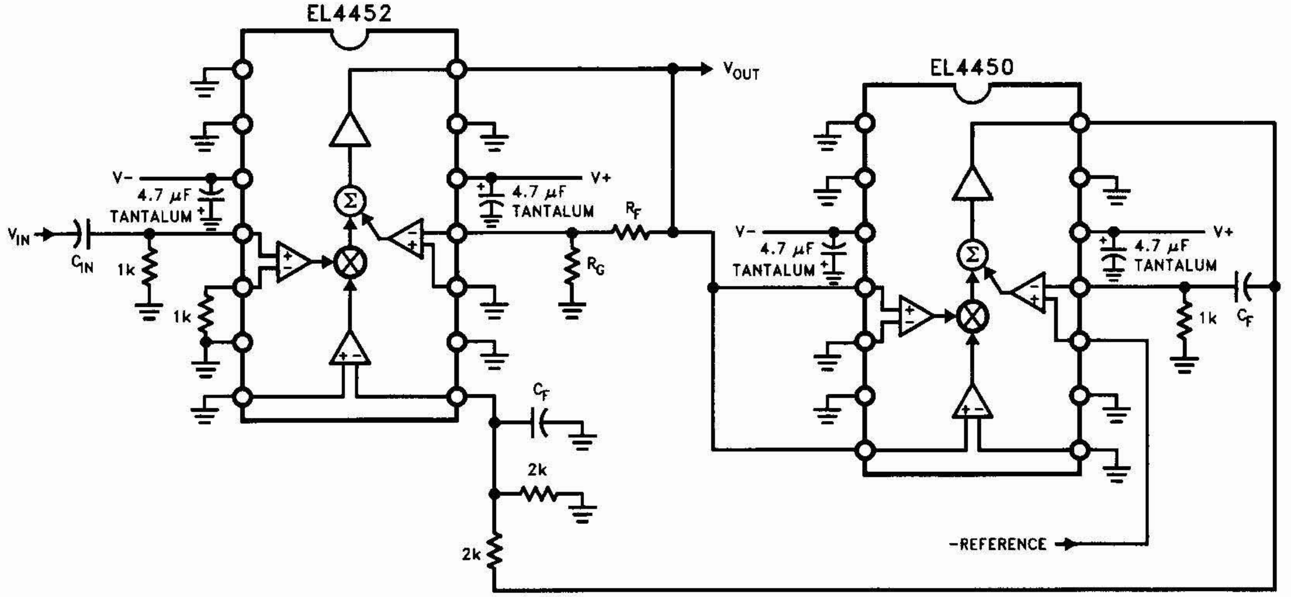
4452-25

Applications Information — Contd.

The output of the EL4452 drives a diode detector which is compared to V_{REF} by an offset integrator. Its output feeds the gain-control input of the EL4452. The integrator's output is attenuated by the 2 kΩ and 2.7 kΩ resistors to prevent the op-amp from overloading the gain-control pin during zero input conditions. The 510 kΩ resistor provides a pull-down current to the peak level storage capacitor C1 to allow it to drift negative when output amplitude reduces. Thus the detector is of fast attack and slow decay design, able to reduce AGC gain rapidly when signal amplitude suddenly increases, and increases gain slowly when the input drops out momentarily. The value of C1 determines drop-out reaction rates, and the value of C_F affects overall loop time constant as well as the amount of ripple on the gain-control line. C2 can be used to reduce this ripple further, although it contributes to loop overshoot when input amplitude changes suddenly. The op-amp can be any inexpensive low-frequency type.

The major problem with diode detectors is their large and variable forward voltage. They require at least a 2 V_{P-P} peak output signal to function reliably, and the forward voltage should be compensated by including a negative V_D added to V_{REF}. Even this is only moderately successful. At the expense of bandwidth, op-amp circuits can greatly improve diode rectifiers (see "An Improved Peak Detector", an Elantec application note). Fortunately, the detector will see a constant amplitude of signal if the AGC is operating correctly.

A better-calibrated method is to use a four-quadrant multiplier as a square-law detector. Here is a circuit employing the EL4450:



4452-26

Applications Information — Contd.

In this circuit, the EL4450 not only calculates the square of the input, but also provides the offset integrator function. The product of the two multiplier inputs adds to the −Reference input and are passed to the output amplifier, which through C_F behaves as a pseudo-integrator. The "integrator" gain does not pass through zero at high frequencies but has a zero at $1/(2\pi C_F \times 1\ k\Omega)$. This zero is cancelled by the pole caused by the second capacitor of value C_F connected at the EL4452 $-V_{GAIN}$ input. The −Reference can be exchanged for a positive reference by connecting it to the ground return of the 1 kΩ resistor at the FB terminal and grounding REF.

As a general consideration, the input signal applied to an EL4452 should be kept below about 250 mV peak for good linearity. If the AGC were designed to produce a 1V peak output, the input range would be 100 mV−250 mV peak when the EL4452 has a feedback network that establishes a maximum gain of 10. This is an input range of only 2.5:1 for precise output regulation. Raising the maximum gain to 25 allows a 40 mV−250 mV input range with the output still regulated, better than 6:1. Unfortunately, the bandwidth will be reduced. Bandwidth can be maintained by adding a high frequency op-amp cascaded with the output to make up gain beyond the 10 of the EL4452, current feedback devices being the most flexible. The op-amp's input should be capacitor coupled to prevent gained-up offsets from confusing the level detector during AGC control line variations.

Application
Specific
Video

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Video Fader/Variable Gain Amplifiers

Listed by decreasing bandwidth. All use supplies up to ±16V.

Part #	Features	Bandwidth −3 dB	Diff Gain	Diff Phase	Is at 15V	Input Volts Full Scale	Slew Rate	Input Bias I_B	V_{OS}	Supply Volts Range		Package P = Pins N = PDIP S = SOIC
		Typ	Typ	Typ	Max	Typ	Typ	Max	Max	Min	Max	
EL4453C	Diff Inputs	80 MHz	0.05%	0.05°	21 mA	±2V	380V/μs	20 μA	25 mV	±4.5V	±16V	14P-N-S
EL4094C	Only ±In's	60 MHz	0.02%	0.04°	19 mA	±2V	500V/μs	10 μA	20 mV	±4.5V	±16V	8P-N-S
EL4095C	Logic/Diff In	60 MHz	0.02%	0.02°	21 mA	±2V	330V/μs	10 μA/30 μA	5 mV	±4.5V	±16V	14P-N-S

Video/RGB DC-Restored Sample and Hold Amplifiers

Current Mode Feedback Amplifiers

Listed by decreasing bandwidth. Specs at 25°C and at bold V_S.

Part #	Features	Includes	Bandwidth −3 dB	Diff Gain	Diff Phase	Is at V_S	A_{VOL}*	Slew Rate	Sample to Hold Delay	I_{OUT} 10Ω Load	V_{OS}	Supply Volts Range		Package P = Pins N = PDIP S = SOIC M = SOL
			Typ	Typ	Typ	Max	Typ	Typ	Typ	Min	Max	Min	Max	
EL4093C	Wide BW	Video S and H	300 MHz	0.04%	0.02°	11.5 mA	533V/V	1500V/μs	15 ns	60 mA	1.5 mV	±4V	±6V	16P-N-S
EL2090C	High Performance	Video S and H	100 MHz	0.01%	0.02°	17 mA	1000V/V	600V/μs	20 ns	50 mA	10 mV	±4V	±15V	14P-N-S 16P-M
EL4089C	Low Cost + In Clamp	Video Clamp	60 MHz	0.02%	0.05°	11 mA	2667V/V	500V/μs	25 ns	54 mA	7 mV	±4V	±15V	8P-N-S
EL4390C	3 Amps + In Clamp	RGB Clamp	95 MHz	0.02%	0.03°	32 mA	169V/V	800V/μs	35 ns	45 mA	35 mV	±4V	±15V	16P-N-M

*Derived from: $A_{VOL} \approx R_{OL}/(R_F + (-R_{IN} * A_V)$

Video Horizontal Genlock

Part #	Pal Frequency Divisors Clocks per Horizontal Line				NTSC Frequency Clocks per Horizontal Line				Logic Levels	Vco Control		I_{DD}	Package P = Pins N = PDIP S = SOIC
	3 Fsc	**CCIR 601**	**Square Pixels**	**4 Fsc**	**3 Fsc**	**CCIR 601**	**Square Pixels**	**4 Fsc**		**Range**	**Leak**	**Max**	
EL4584C	851	864	944	1135	682	858	780	910	TTL/CMOS	0V–5V	100 nA	4 mA	16P-N-S
	6 Fsc			**8 Fsc**	**6 Fsc**			**8 Fsc**					
EL4585C	1702	1728	1888	2270	1364	1716	1560	1820	TTL/CMOS	0V–5V	100 nA	4 mA	16P-N-S

Video Sync Separators

- **NTSC, PAL, SECAM and Non Standard Video Sync Separation.**
- **External Resistor Sets Internal Timing for Scan Rate.**
- **Composite Video Input with Video Sync Tip Reference Clamp.**
- **Input Levels from 0.5 $V_{P\text{-}P}$ to 2 $V_{P\text{-}P}$.**
- **Single 5V Supply Low Power.**
- **Default Vertical Sync.**
- **Composite Sync Output.**
- **Vertical Sync Output.**
- **Odd/Even Field Output.**
- **Burst/Back Porch Output.**
- **Outputs TTL/CMOS Levels.**
- **EL4583—Horizontal Sync Out.**

Part #	Features	Sync Slicing Point from Sync Ref Tip	Color Burst Filter	Prop Delay In to CSync	I_{DD} at 5Vs	Package P = Pins N = PDIP S = SOIC
				Typ	**Max**	
EL1881C	Low Cost	70 mV	External	45 ns	3 mA	8P-N-S
EL1882C	50% Slicing	50% w/AGC	External	25 ns	3 mA	8P-N-S
EL4581C	50% + Video Filter	50% w/S and H	3 Pole Internal	260 ns	3 mA	8P-N-S
EL4583C	Multi Featured *	50% w/S and H	3 Pole Internal	250 ns	4 mA	16P-N-S

*Filter input, filter output, resistor set color burst filter frequency, horizontal sync output, no sync pulse detected output, sync pulse level output, resistor sets no sync pulse detect level.

Multipliers/Variable Gain Amps, Voltage Mode Input

Wide Bandwidth/Video with Voltage Mode Feedback

Listed by decreasing bandwidth. Up to ±15V supplies.

Part #	Features	Bandwidth −3 dB	Input Volts Full Scale	Linearity Signal Port	Linearity, Gain Port	Diff Gain	Diff Phase	Slew Rate	Input V_{OS}	Input Bias I_B	I_S	Supply Volts Range		Package P = Pins N = PDIP S = SOIC
		Typ	Typ	Typ	Typ	Typ	Typ	Typ	Max	Max	Max	Min	Max	
EL4450C	4 Quadrant	90 MHz	±2V	0.3%	0.2%	—	—	400V/μs	35 mV	20 μA	18 mA	±4.5V	±16V	14P-N-S
EL4451C	2 Quad Leveler	70 MHz	±2V	0.2%	2%	0.9%	0.2°	400V/μs	25 mV	20 μA	18 mA	±4.5V	±16V	14P-N-S
EL4452C	2 Quad High Gain	50 MHz	±0.5V	0.3%	2%	—	—	400V/μs	10 mV	20 μA	18 mA	±4.5V	±16V	14P-N-S

Multipliers/Variable Gain Amps, Current Mode Input

Wide Bandwidth/Video

Listed by decreasing bandwidth. Up to ±15V supplies.

Part #	Features	Bandwidth −3 dB	Linearity, Signal Port	Linearity, Gain Port	Diff. Gain	Diff. Phase	I_S	Supply Volts Range		Package P = Pins N = PDIP S = SOIC
		Typ	Typ	Typ	Typ	Typ	Max	Min	Max	
EL4083C	4 Quadrant	225 MHz	0.1%	0.1%	0.1%	0.05°	48 mA	±4.5V	±16V	8P-N-S
EL2082C	2 Quadrant	150 MHz	0.1%	2%	0.25%	0.05°	16 mA	±4.5V	±16V	8P-N-S

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1881C

Sync Separator, Low Power

Features

- NTSC, PAL, SECAM, non-standard video sync separation
- Fixed 70 mV slicing of video input levels from 0.5 $V_{P\text{-}P}$ to 2 $V_{P\text{-}P}$
- Low supply current - 1.5 mA typ.
- Single +5V supply
- Composite, vertical sync output
- Odd/Even field output
- Burst/Back porch output
- Plug-in compatible with industry standard LM1881 in 5V applications
- Available in 8-pin DIP and SO package

Applications

- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1881CN	−40°C to +85°C	8-pin DIP	MDP0031
EL1881CS	−40°C to +85°C	8-lead SO	MDP0027

Demo Board

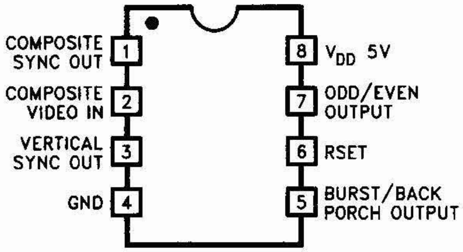
A dedicated demo board is not available. However, this device can be placed on the EL4584/5 demo board.

General Description

The EL1881C video sync separator is manufactured using Elantec's high performance analog CMOS process. This device extracts sync timing information from both standard and non-standard video input. It provides composite sync, vertical sync, burst/back porch timing and odd/even field detection. Fixed 70 mV sync tip slicing provides sync edge detection when the video input level is between 0.5 Vp-p and 2 Vp-p (sync tip amplitude 143 mV to 572 mV). A single external resistor sets all internal timing to adjust for various video standards. The **composite sync** output follows **video in** sync pulses, and a **vertical sync** pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The **odd/even** output indicates field polarity detected during the vertical blanking interval. The EL1881C is plug-in compatible with the industry standard LM1881 and can be substituted for that part in 5V applications with lower required supply current.

Connection Diagram

EL1881C SO, P-DIP Packages



1881-1

EL1881C

Sync Separator, Low Power

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Operating Ambient Temperature Range	−40°C to +85°C
Storage Temperature	−65°C to +150°C	Operating Junction Temperature	125°C
Lead Temperature (5 sec)	260°C	Power Dissipation	400 mW
Pin Voltages	−0.5V to V_{CC} + 0.5V		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics Unless otherwise stated, V_{DD} = 5V, T_A = 25°C, R_{SET} = 681 kΩ

Parameter	Description	Min	Typ	Max	Test Level	Units
I_{DD}, Quiescent	V_{DD} = 5V	0.75	1.5	3.0	I	mA
Clamp Voltage	Pin 2, Unloaded	1.35	1.5	1.65	I	V
Clamp Discharge Current	Pin 2 = 2V	3.2	12	16	I	μA
Clamp Charge Current	Pin 2 = 1V	−2.0	−1.5	−0.8	I	mA
R_{SET} Pin Reference Voltage	Pin 6	1.20	1.31	1.44	I	V
V_{OL} Output Low Voltage	I_{OL} = 1.6 mA		0.4	0.8	I	V
V_{OH} Output High Voltage	I_{OH} = −40 μA I_{OH} = −1.6 mA	4 2.4	4.8 3.5		IV I	V

Dynamic Characteristics

Parameter	Description	Min	Typ	Max	Test Level	Units
Comp Sync Prop Delay, t_{CS}	See Figure 2	20	45	90	I	ns
Vertical Sync Width, t_{VS}	Normal or Default trigger, 50%–50%	190	270	350	I	μs
Vertical Sync Default Delay, t_{VSD}	See Figure 3	35	65	85	I	μs
Burst/Back Porch Delay, t_{BD}	See Figure 2	250	450	650	I	ns
Burst/Back Porch Width, t_B	See Figure 2	2.5	3.6	4.5	I	μs
Input Dynamic Range	Video input amplitude to maintain 50% slice spec	0.5		2	I	V_{P-P}
Slice Level	V_{SLICE}/V_{CLAMP}	55	70	85	I	mV

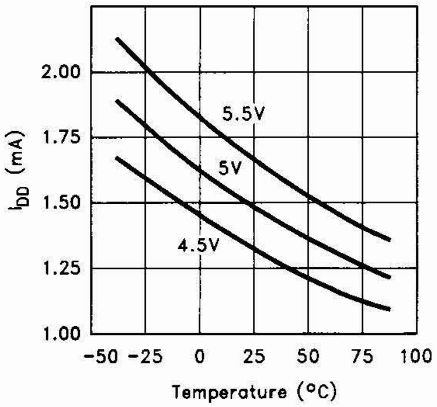
Pin Descriptions

Pin No.	Pin Name	Function
1	Composite Sync Out	Composite sync pulse output. Sync pulses start on a falling edge and end on a rising edge.
2	Composite Video In	AC coupled composite video input. Sync tip must be at the lowest potential (Positive picture phase).
3	Vertical Sync Out	Vertical sync pulse output. The falling edge of Vert Sync is the start of the vertical period.
4	Gnd	Supply ground.
5	Burst/Back Porch Output	Burst/Back porch output. Low during burst portion of composite video.
6	R_{SET}	An external resistor to ground sets all internal timing. A 681k 1% resistor will provide correct timing for NTSC signals.
7	Odd/Even Output	Odd/Even field output. High during odd fields, low during even fields. Transitions occur at start of Vert Sync pulse.
8	V_{DD} 5V	Positive supply. (5V)

Note: R_{SET} must be a 1% resistor.

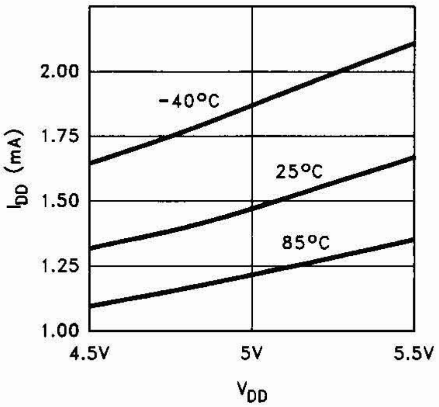
Typical Performance Curves

Supply Current, Quiescent
R_{SET} = 681k



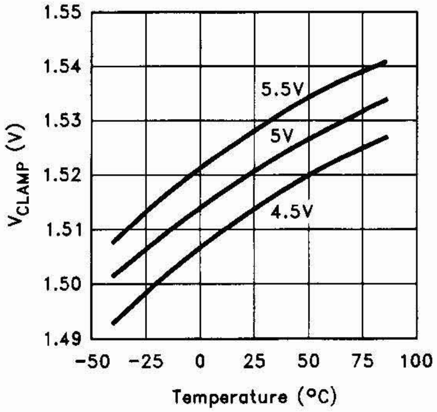
1881-2

I_{DD} vs V_{DD}
R_{SET} = 681k



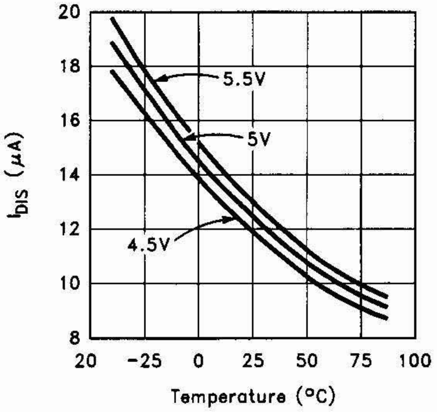
1881-3

V_{CLAMP} Voltage
R_{SET} = 681k



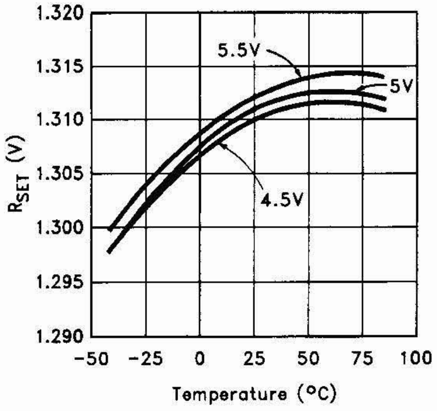
1881-4

Clamp Discharge Current
R_{SET} = 681k



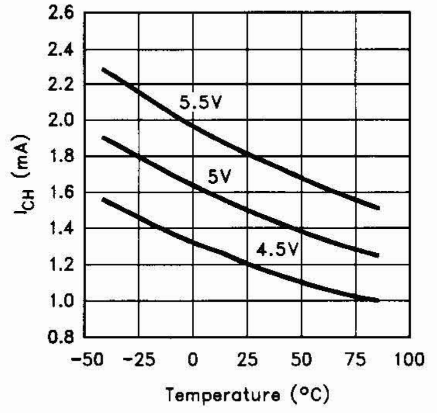
1881-5

V_{RSET}
R_{SET} = 681k



1881-6

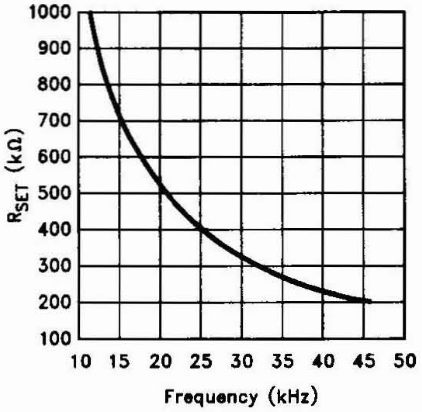
Clamp Charge Current
R_{SET} = 681k



1881-7

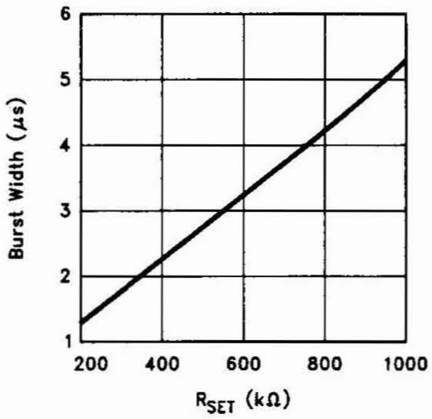
Typical Performance Curves — Contd.

R_{SET} vs Horizontal Frequency



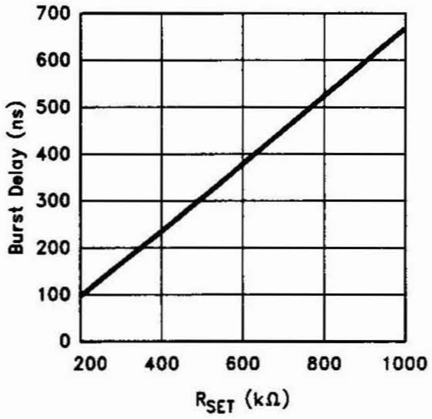
1881-8

Burst/Back Porch Width vs R_{SET}
V_{DD} = 5V, T = 25°C



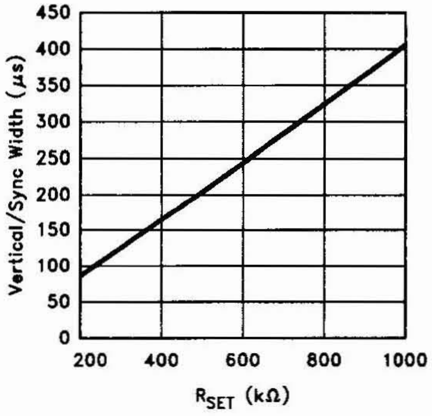
1881-9

Burst/Back Porch Delay vs R_{SET}
V_{DD} = 5V, T = 25°C



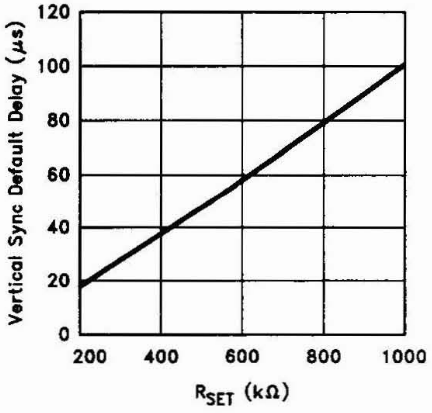
1881-10

Vertical Sync Width vs R_{SET}
V_{DD} = 5V, T = 25°C



1881-11

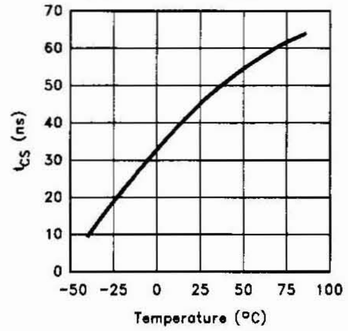
Vertical Default Delay vs R_{SET}
V_{DD} = 5V, T = 25°C



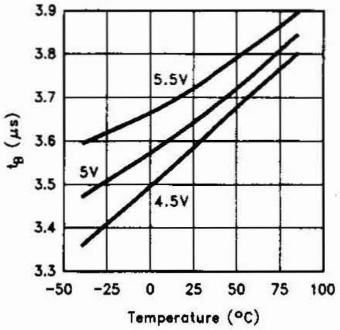
1881-12

Typical Performance Curves — Contd.

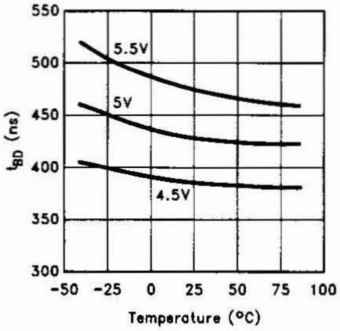
Composite Sync Prop Delay
R_{SET} = 681k, V_{DD} = 5V



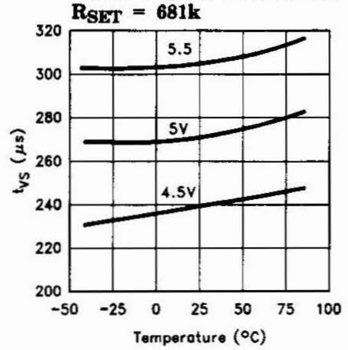
Burst/Back Porch Width,
R_{SET} = 681k



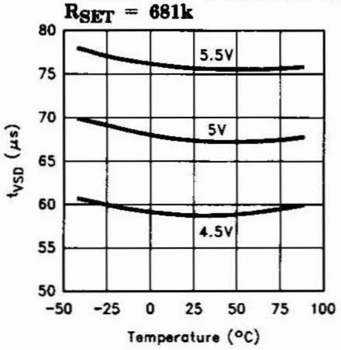
Burst/Back Porch Delay Time,
R_{SET} = 681k



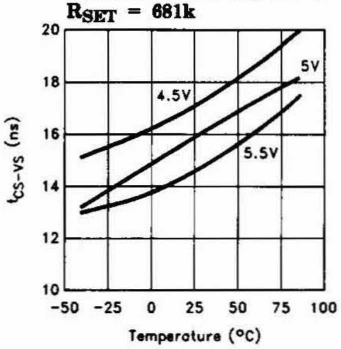
Vertical Sync Pulse Width
R_{SET} = 681k



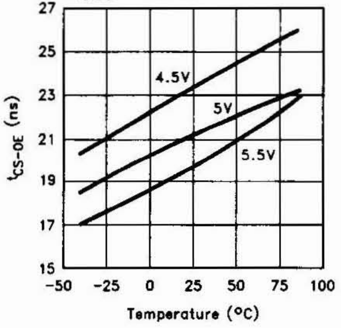
Vertical Sync Default Delay Time,
R_{SET} = 681k



Composite Sync to
Vertical Sync Delay Time
R_{SET} = 681k



Composite Sync to
Odd/Even Delay Time
R_{SET} = 681k



1881-13

Timing Diagrams

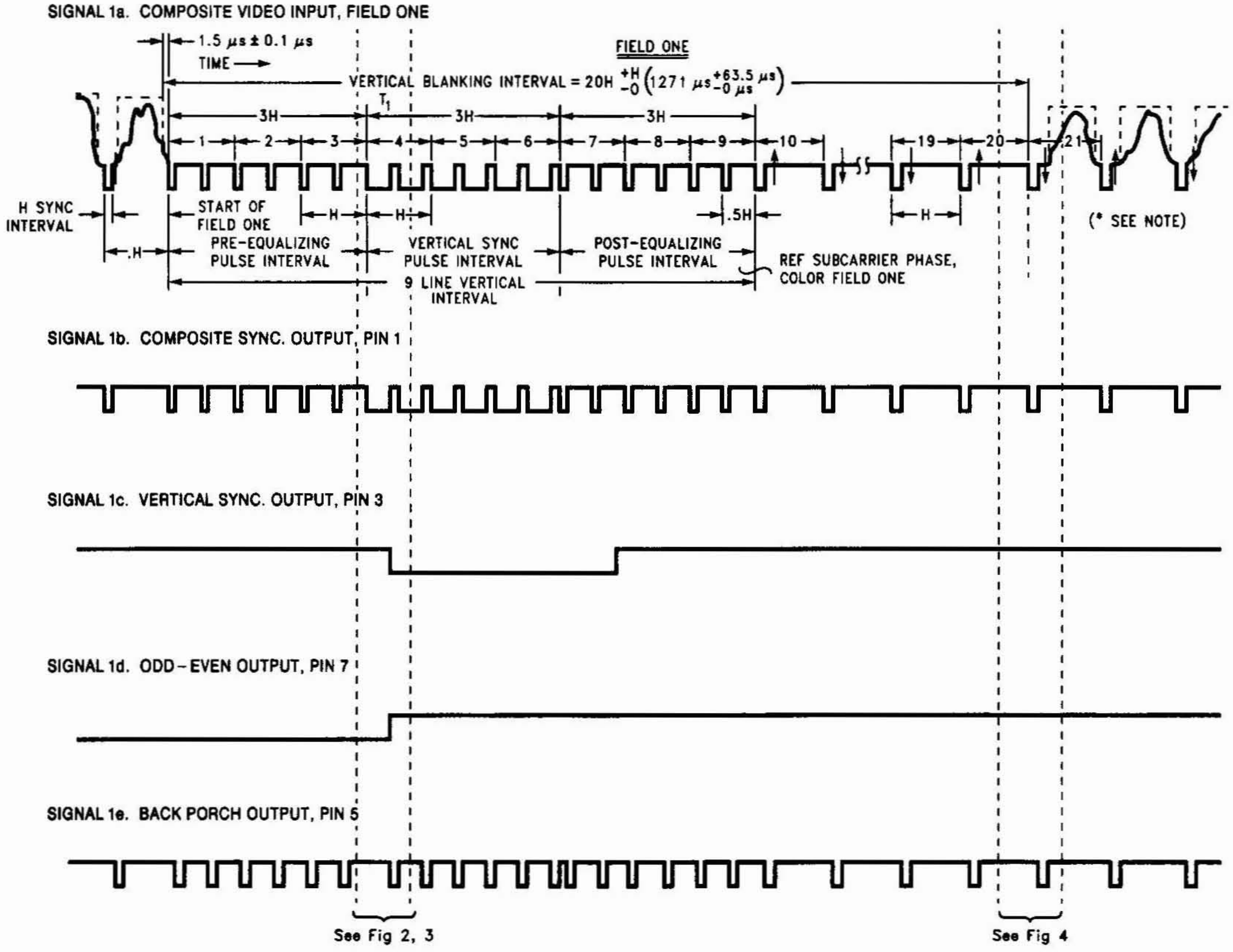

SIGNAL 1a. COMPOSITE VIDEO INPUT, FIELD ONE
1.5 µs ± 0.1 µs
TIME
FIELD ONE
VERTICAL BLANKING INTERVAL = 20H +H -0 (1271 µs +63.5 µs -0 µs)
T1
3H
3H
3H
1
2
3
4
5
6
7
8
9
10
19
20
21
H SYNC INTERVAL
H
START OF FIELD ONE
H
H
.5H
H
(* SEE NOTE)
PRE-EQUALIZING PULSE INTERVAL
VERTICAL SYNC PULSE INTERVAL
POST-EQUALIZING PULSE INTERVAL
REF SUBCARRIER PHASE, COLOR FIELD ONE
9 LINE VERTICAL INTERVAL
SIGNAL 1b. COMPOSITE SYNC. OUTPUT, PIN 1
SIGNAL 1c. VERTICAL SYNC. OUTPUT, PIN 3
SIGNAL 1d. ODD-EVEN OUTPUT, PIN 7
SIGNAL 1e. BACK PORCH OUTPUT, PIN 5
See Fig 2, 3
See Fig 4
1881-14

Figure 1. Standard (NTSC Input) Timing

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

* Signal 1a drawing reproduced with permission from EIA.

Expanded Timing Diagrams

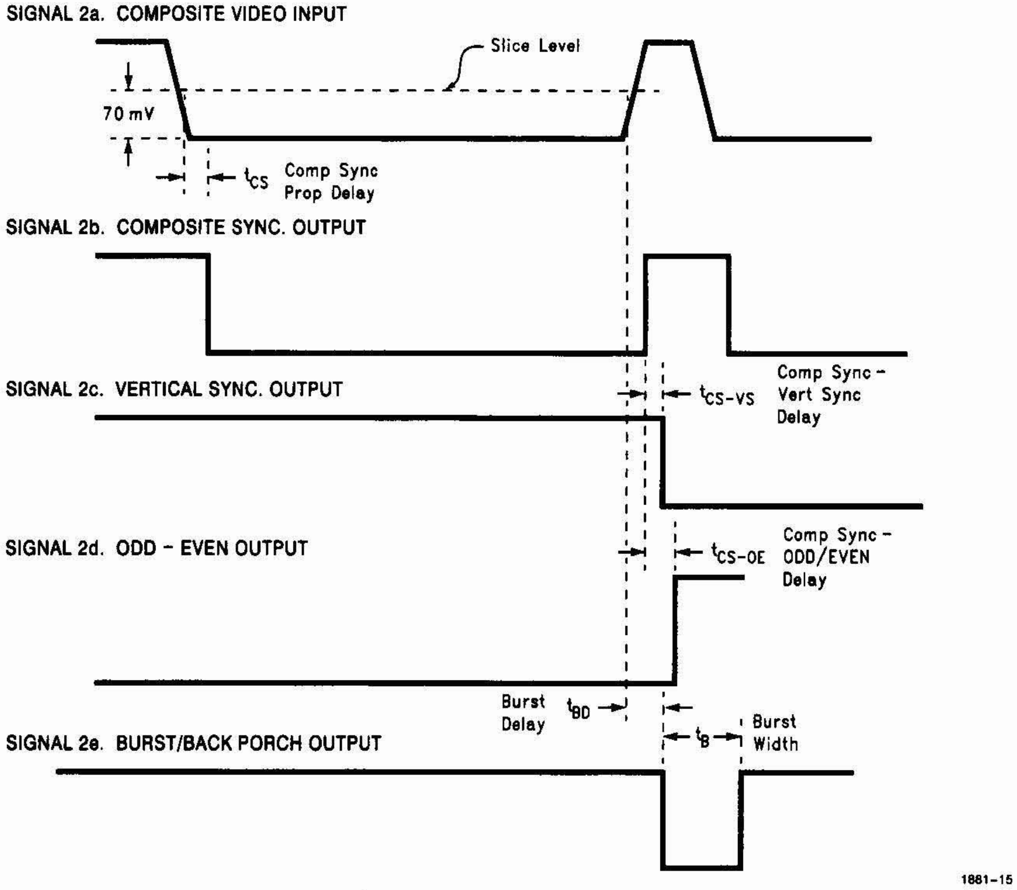

SIGNAL 2a. COMPOSITE VIDEO INPUT
Slice Level
70 mV
t_{CS} Comp Sync Prop Delay
SIGNAL 2b. COMPOSITE SYNC. OUTPUT
SIGNAL 2c. VERTICAL SYNC. OUTPUT
t_{CS-VS} Comp Sync - Vert Sync Delay
SIGNAL 2d. ODD - EVEN OUTPUT
t_{CS-OE} Comp Sync - ODD/EVEN Delay
Burst Delay t_{BD}
t_B Burst Width
SIGNAL 2e. BURST/BACK PORCH OUTPUT
1881-15

Figure 2. Standard Vertical Timing

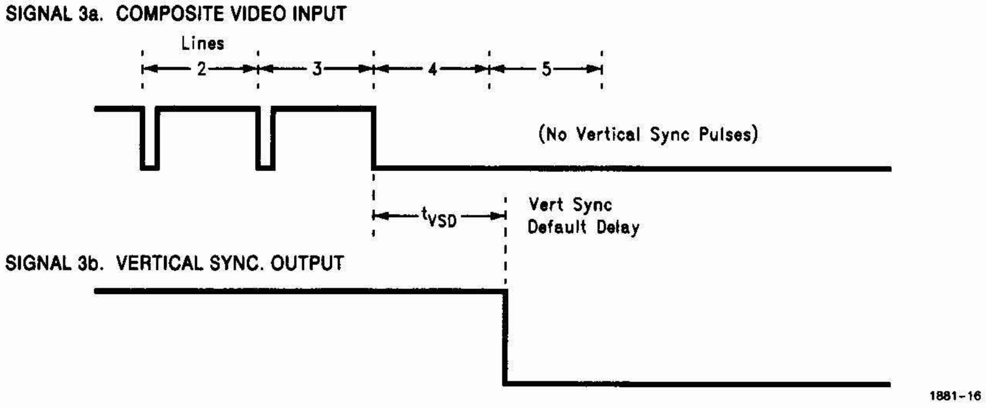

SIGNAL 3a. COMPOSITE VIDEO INPUT
Lines
2
3
4
5
(No Vertical Sync Pulses)
t_{VSD} Vert Sync Default Delay
SIGNAL 3b. VERTICAL SYNC. OUTPUT
1881-16

Figure 3. Non-Standard Vertical Timing

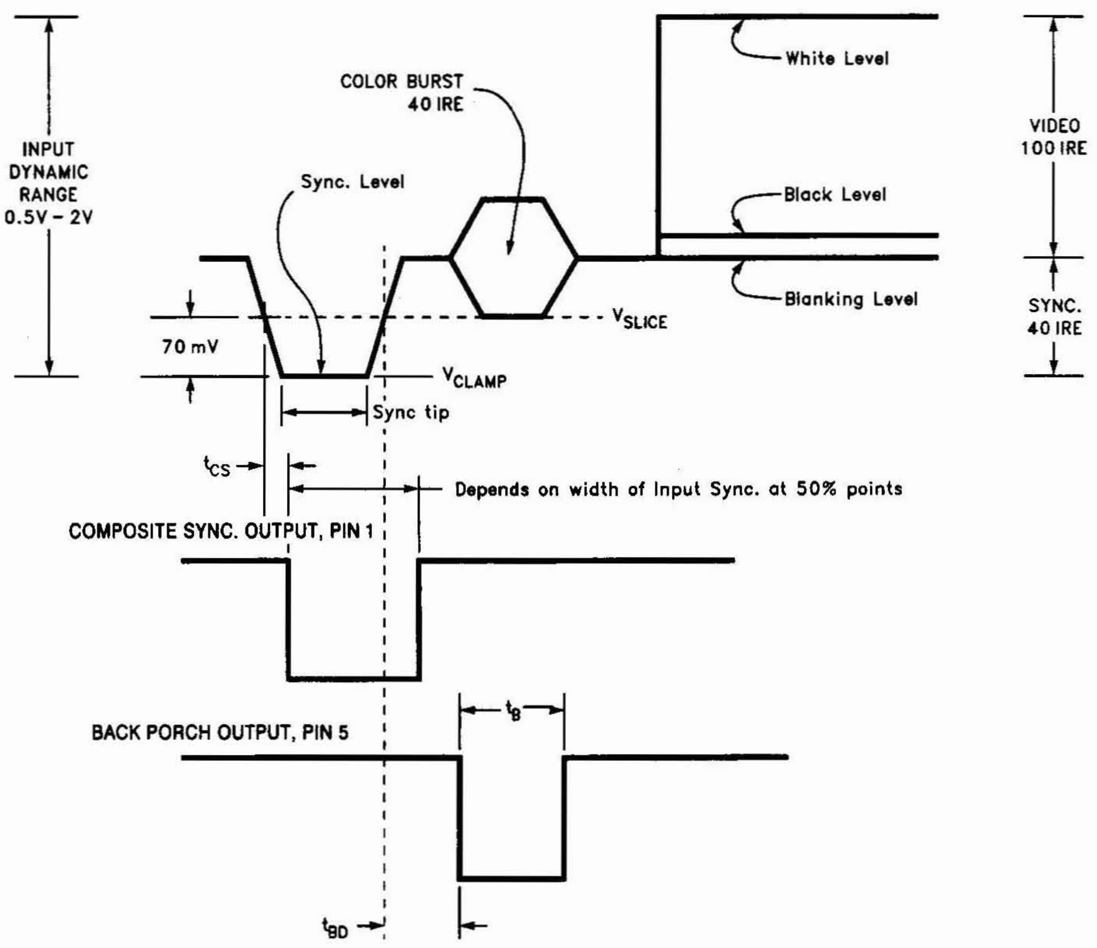

INPUT DYNAMIC RANGE 0.5V – 2V
COLOR BURST 40 IRE
Sync. Level
White Level
VIDEO 100 IRE
Black Level
Blanking Level
SYNC. 40 IRE
70 mV
V_SLICE
V_CLAMP
Sync tip
t_CS
Depends on width of Input Sync. at 50% points
COMPOSITE SYNC. OUTPUT, PIN 1
BACK PORCH OUTPUT, PIN 5
t_B
t_BD
1881-19

Figure 4. Standard (NTSC Input) H. Sync Detail

Applications Information

Video In

A simplified block diagram is shown following page.

An AC coupled video signal is input to **Video In** pin 2 via C1, nominally 0.1 μF. Clamp charge current will prevent the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 1 mA. A clamp discharge current of about 10 μA is always attempting to discharge C1 to Sync Tip Ref, thus charge is lost between sync pulses that must be replaced during sync pulses. The droop voltage that will occur can be calculated from IT = CV, where V is the droop voltage, I is the discharge current, T is the time between sync pulses (sync period − sync tip width), and C is C1.

An NTSC video signal has a horizontal frequency of 15.73 kHz, and a sync tip width of 4.7 μs. This gives a period of 63.6 μs and a time T = 58.9 μs. The droop voltage will then be V = 5.9 mV. This is less than 2% of a nominal sync tip amplitude of 286 mV. The charge represented by this droop is replaced in a time given by T=CV/I, where I = clamp charge current = 1 mA. Here T = 590 ns, about 12% of the sync pulse width of 4.7 μs. It is important to choose C1 large enough so that the droop voltage does not approach the switching threshold of the internal comparator.

Fixed Gain Buffer

The clamped video signal then passes to the fixed gain buffer which places the sync slice level at the equivalent level of 70 mV above sync tip. The output of this buffer is presented to the comparator, along with the slice reference. The comparator output is level shifted and buffered to TTL levels, and sent out as **Composite Sync** to pin 1.

Burst

A low-going Burst pulse follows each rising edge of sync, and lasts approximately 3.5 μs for an R_{SET} of 681 kΩ.

Vertical Sync

A low-going **Vertical Sync** pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the EL1881C on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 60 μs after the last falling edge of the vertical equalizing phase for R_{SET} = 681 kΩ.

Odd/Even

Because a typical television picture is composed of two interlaced fields, there is an odd field that includes all the odd lines, and an even field that consists of the even lines. This odd/even field information is decoded by the EL1881C during the end of picture information and the beginning of vertical information. The odd/even circuit includes a T-flip-flop that is reset during full horizontal lines, but not during half lines or vertical equalization pulses. The T-flip-flop is clocked during each falling edge of these half h-period pulses. Even fields will toggle until a low state is clocked to the odd/even pin 7 at the beginning of vertical sync, and odd fields will cause a high state to be clocked to the odd/even pin at the start of the next vertical sync pulse. Odd/even can be ignored if using non-interlaced video, as there is no change in timing from one field to the next.

R_{SET}

An external R_{SET} resistor, connected from R_{SET} pin 6 to ground, produces a reference current that is used internally as the timing reference for vertical sync width, vertical sync default delay, burst gate delay and burst width. Decreasing the value of R_{SET} increases the reference current, which in turn decreases reference times and pulse widths. A higher frequency video input necessitates a lower R_{SET} value.

Applications Information — Contd.

Chroma Filter

A chroma filter is suggested to increase the S/N ratio of the incoming video signal. Use of the optional chroma filter is shown in Figure 5. It can be implemented very simply and inexpensively with a series resistor of 620Ω and a parallel capacitor of 500 pF, which gives a single pole roll-off frequency of about 500 kHz. This sufficiently attenuates the 3.58 MHz (NTSC) or 4.43 MHz (PAL) color burst signal, yet passes the approximately 15 kHz sync signals without appreciable attenuation. A chroma filter will increase the propagation delay from the composite input to the outputs.

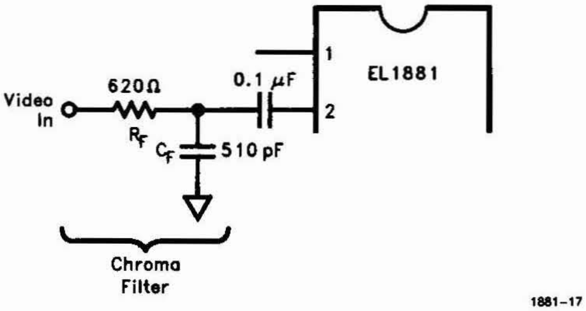

Video In
620Ω
R_F
C_F
510 pF
0.1 μF
1
2
EL1881
Chroma Filter
1881-17

Figure 5

Simplified Block Diagram

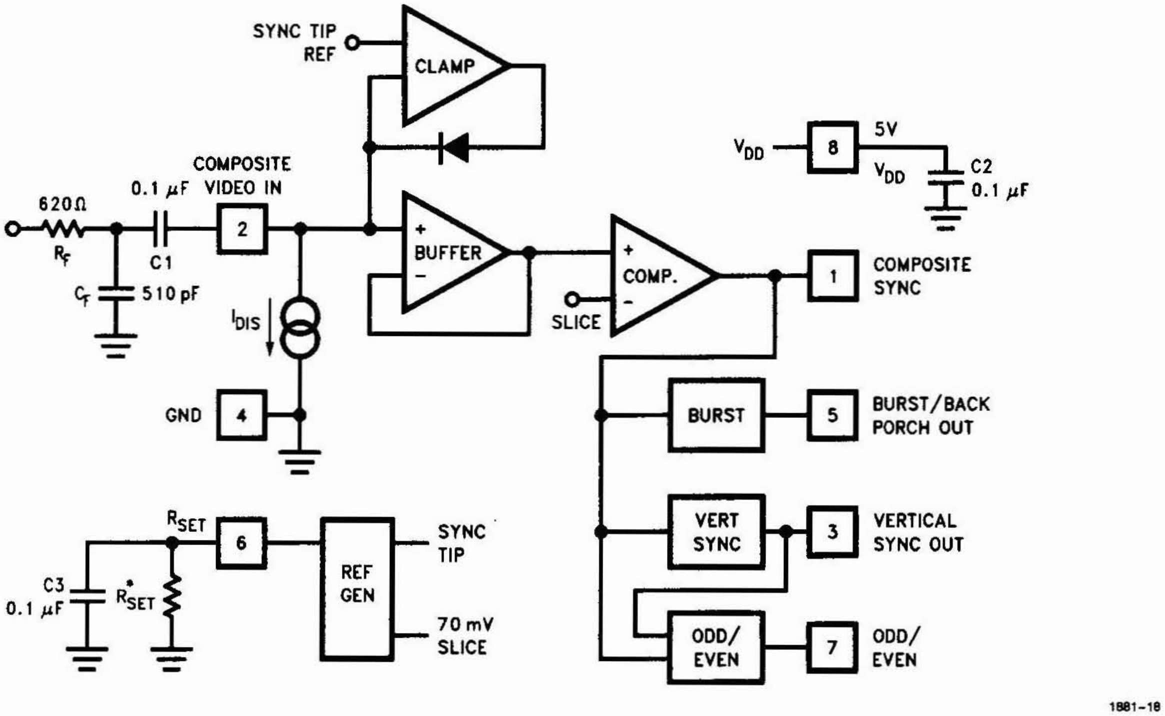

SYNC TIP REF
CLAMP
COMPOSITE VIDEO IN
620Ω
R_F
0.1 μF
C1
C_F
510 pF
2
I_{DIS}
GND
4
+
BUFFER
−
+
COMP.
−
SLICE
V_{DD}
8
5V
V_{DD}
C2
0.1 μF
1
COMPOSITE SYNC
BURST
5
BURST/BACK PORCH OUT
VERT SYNC
3
VERTICAL SYNC OUT
ODD/ EVEN
7
ODD/ EVEN
R_{SET}
6
C3
0.1 μF
R_{SET}*
REF GEN
SYNC TIP
70 mV SLICE
1881-18

Figure 6

* Note: R_{SET} must be a 1% resistor.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1882C

Sync Separator w/50% Slice, AGC

Features

- NTSC, PAL, SECAM, non-standard video sync separation
- Precision 50% slicing of video input levels from 0.5 V_{P-P} to 2 V_{P-P}
- Low supply current - 1.5 mA typ.
- Single +5V supply
- Composite, vertical sync output
- Odd/Even field output
- Burst/Back porch output
- Plug-in compatible with industry standard LM1881 in 5V applications
- Available in 8-pin DIP and SO package

Applications

- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1882CN	−40°C to +85°C	8-pin DIP	MDP0031
EL1882CS	−40°C to +85°C	8-lead SO	MDP0027

Demo Board

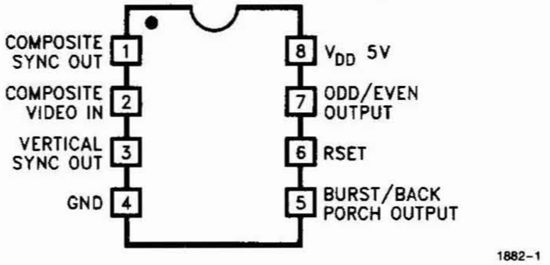
A dedicated demo board is not available. However, this device can be placed on the EL4584/5 demo board.

General Description

The EL1882C video sync separator is manufactured using Elantec's high performance analog CMOS process. This device extracts sync timing information from both standard and non-standard video input. It provides composite sync, vertical sync, burst/back porch timing and odd/even field detection. 50% sync tip slicing provides precise sync edge detection when the video input level is between 0.5 Vp-p and 2 Vp-p (sync tip amplitude 143 mV to 572 mV). A single external resistor sets all internal timing to adjust for various video standards. The **composite sync** output follows **video in** sync pulses, and a **vertical sync** pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The **odd/even** output indicates field polarity detected during the vertical blanking interval. The EL1882C is plug-in compatible with the industry standard LM1881 and can be substituted for that part in 5V applications with improved 50% slicing and lower required supply current.

Connection Diagram

EL1882C SO, P-DIP Packages



January 1996 Rev A

EL1882C

Sync Separator w/50% Slice, AGC

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Operating Ambient Temperature Range	−40°C to +85°C
Storage Temperature	−65°C to +150°C	Operating Junction Temperature	125°C
Lead Temperature (5 sec)	260°C	Power Dissipation	400 mW
Pin Voltages	−0.5V to V_{CC} + 0.5V		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics Unless otherwise stated, V_{DD} = 5V, T_A = 25°C, R_{SET} = 680 kΩ

Parameter	Description	Min	Typ	Max	Test Level	Units
I_{DD}, Quiescent	V_{DD} = 5V	0.75	1.5	3.0	I	mA
Clamp Voltage	Pin 2, Unloaded	1.35	1.5	1.65	I	V
Clamp Discharge Current	Pin 2 = 2V	3.2	12	16	I	μA
Clamp Charge Current	Pin 2 = 1V	−2.0	−1.5	−0.8	I	mA
R_{SET} Pin Reference Voltage	Pin 6	1.20	1.31	1.40	I	V
V_{OL} Output Low Voltage	I_{OL} = 1.6 mA		0.4	0.8	I	V
V_{OH} Output High Voltage	I_{OH} = −40 μA I_{OH} = −1.6 mA	4 2.4	4.8 3.5		IV I	V

Dynamic Characteristics

Parameter	Description	Min	Typ	Max	Test Level	Units
Comp Sync Prop Delay, t_{CS}	See Figure 2	10	25	40	I	ns
Vertical Sync Width, t_{VS}	Normal or Default trigger, 50%–50%	190	270	350	I	μs
Vertical Sync Default Delay, t_{VSD}	See Figure 3	35	65	85	I	μs
Burst/Back Porch Delay, t_{BD}	See Figure 2	250	450	650	I	ns
Burst/Back Porch Width, t_B	See Figure 2	2.5	3.6	4.5	I	μs
Input Dynamic Range	Video input amplitude to maintain 50% slice spec	0.5		2	I	V_{P-P}
Slice Level	V_{SLICE}/V_{CLAMP}	40	50	60	I	%

EL1882C
Sync Separator w/50% Slice, AGC

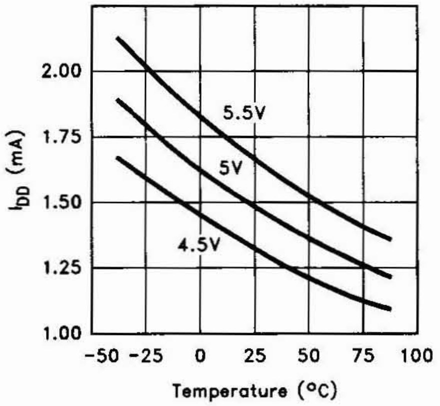
Pin Descriptions

Pin No.	Pin Name	Function
1	Composite Sync Out	Composite sync pulse output. Sync pulses start on a falling edge and end on a rising edge.
2	Composite Video In	AC coupled composite video input. Sync tip must be at the lowest potential (Positive picture phase).
3	Vertical Sync Out	Vertical sync pulse output. The falling edge of Vert Sync is the start of the vertical period.
4	Gnd	Supply ground.
5	Burst/Back Porch Output	Burst/Back porch output. Low during burst portion of composite video.
6	R_{SET}	An external resistor to ground sets all internal timing. A 681k 1% resistor will provide correct timing for NTSC signals.
7	Odd/Even Output	Odd/Even field output. High during odd fields, low during even fields. Transitions occur at start of Vert Sync pulse.
8	V_{DD} 5V	Positive supply. (5V)

Note: R_{SET} must be a 1% resistor.

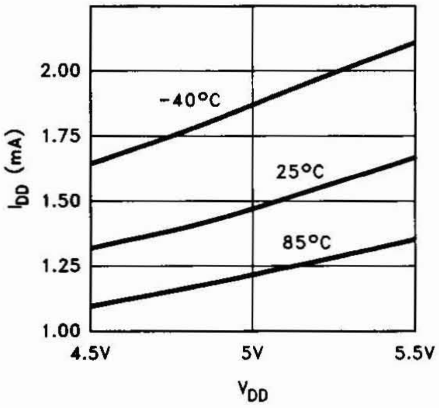
Typical Performance Curves

Supply Current, Quiescent
R_{SET} = 681k



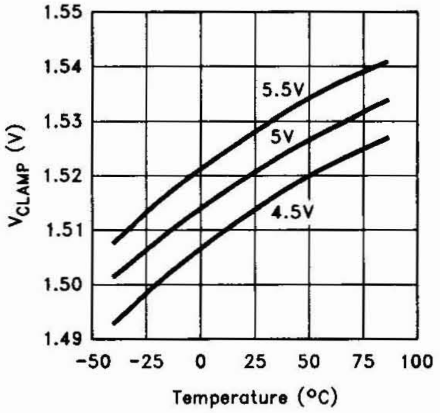
1882-2

I_{DD} vs V_{DD}
R_{SET} = 681k



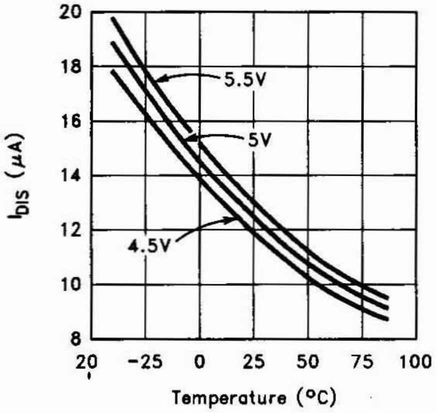
1882-3

V_{CLAMP} Voltage
R_{SET} = 681k



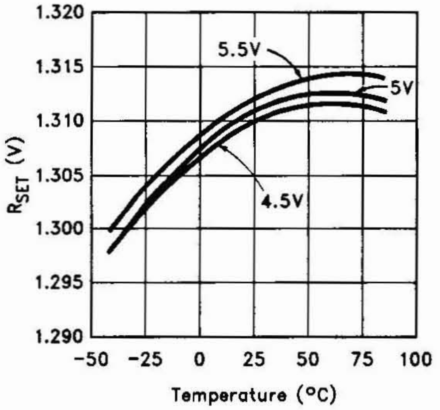
1882-4

Clamp Discharge Current
R_{SET} = 681k



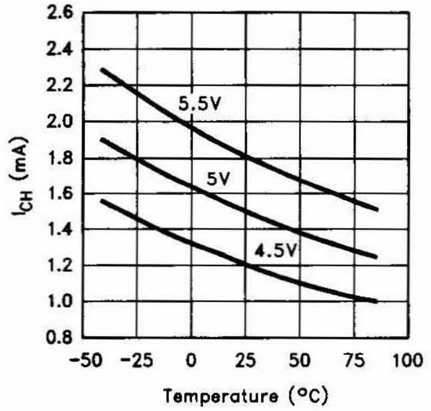
1882-5

V_{RSET}
R_{SET} = 681k



1882-6

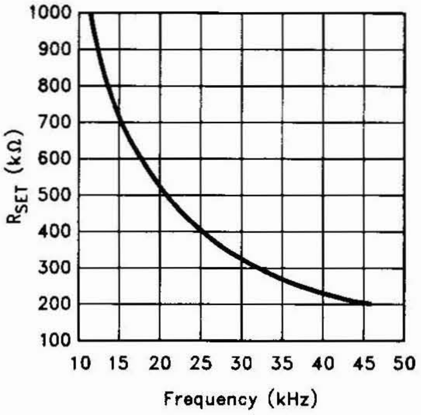
Clamp Charge Current
R_{SET} = 681k



1882-7

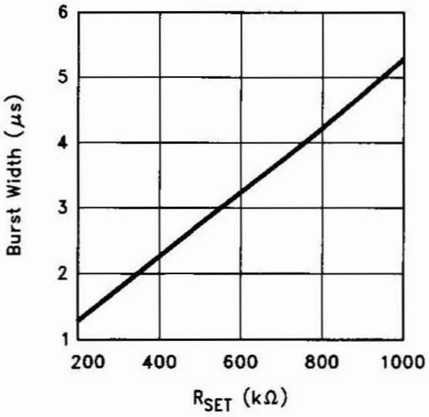
Typical Performance Curves — Contd.

R_{SET} vs Horizontal Frequency



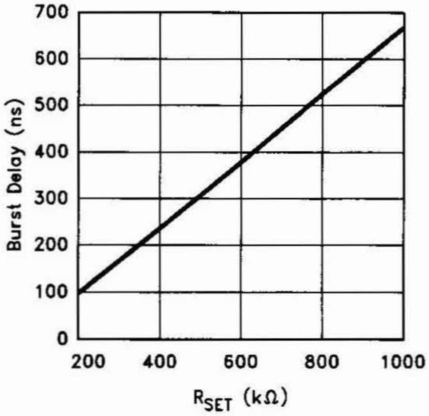
1882-8

Burst/Back Porch Width vs R_{SET}
V_{DD} = 5V, T = 25°C



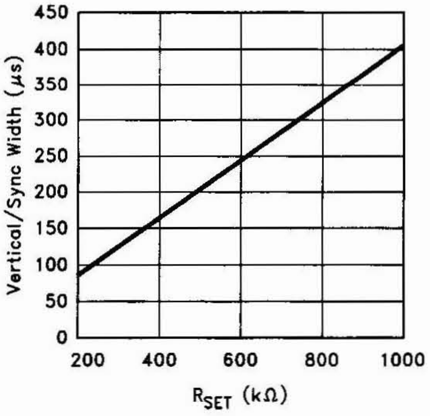
1882-9

Burst/Back Porch Delay vs R_{SET}
V_{DD} = 5V, T = 25°C



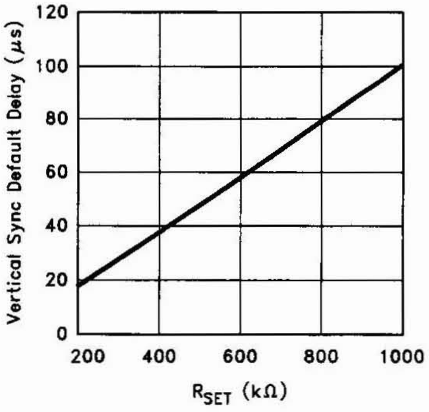
1882-10

Vertical Sync Width vs R_{SET}
V_{DD} = 5V, T = 25°C



1882-11

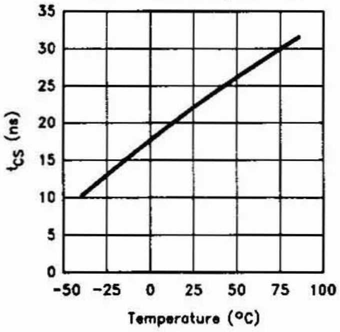
Vertical Default Delay vs R_{SET}
V_{DD} = 5V, T = 25°C



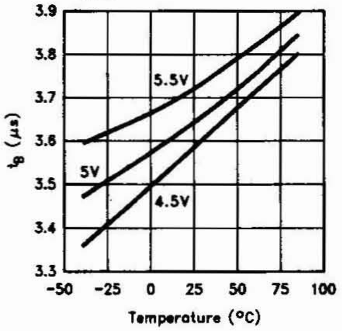
1882-12

Typical Performance Curves — Contd.

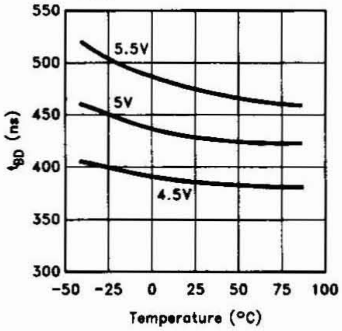
Composite Sync Prop Delay
R_{SET} = 681k, V_{DD} = 5V



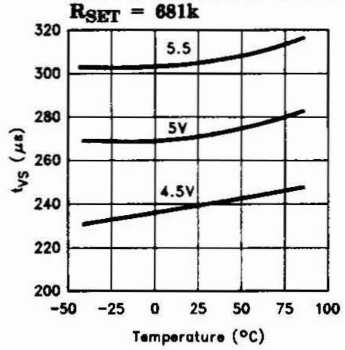
Burst/Back Porch Width,
R_{SET} = 681k



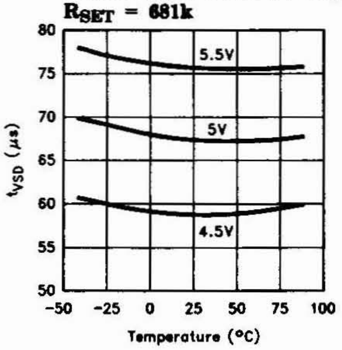
Burst/Back Porch Delay Time,
R_{SET} = 681k



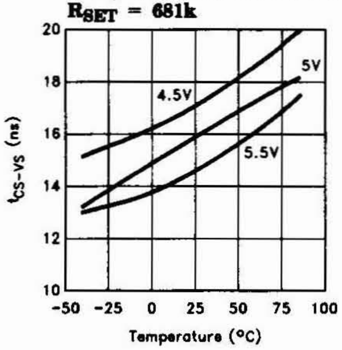
Vertical Sync Pulse Width
R_{SET} = 681k



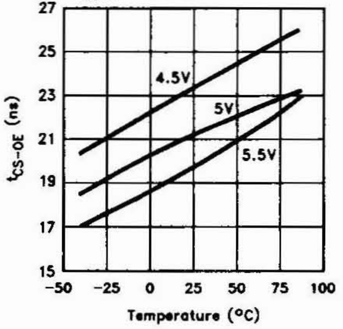
Vertical Sync Default Delay Time,
R_{SET} = 681k



Composite Sync vs Delay Time
R_{SET} = 681k



Composite Sync to
Odd/Even Delay Time
R_{SET} = 681k



1882-13

Timing Diagrams

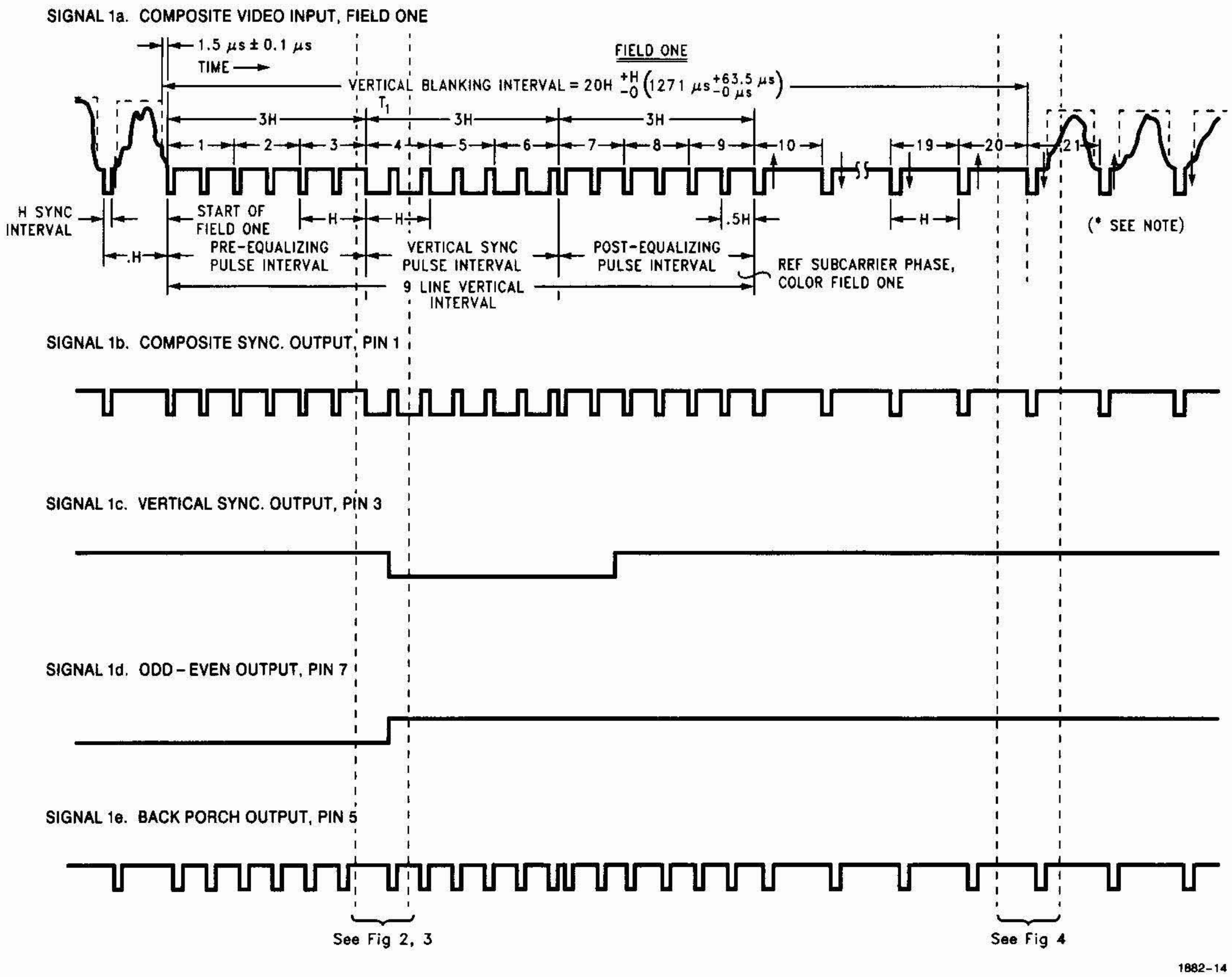

SIGNAL 1a. COMPOSITE VIDEO INPUT, FIELD ONE
1.5 μs ± 0.1 μs
TIME →
FIELD ONE
VERTICAL BLANKING INTERVAL = 20H +H -0 (1271 μs +63.5 μs -0 μs)
T1
3H
3H
3H
1
2
3
4
5
6
7
8
9
10
19
20
21
H SYNC INTERVAL
.H
START OF FIELD ONE
H
H
.5H
H
PRE-EQUALIZING PULSE INTERVAL
VERTICAL SYNC PULSE INTERVAL
POST-EQUALIZING PULSE INTERVAL
9 LINE VERTICAL INTERVAL
REF SUBCARRIER PHASE, COLOR FIELD ONE
(* SEE NOTE)
SIGNAL 1b. COMPOSITE SYNC. OUTPUT, PIN 1
SIGNAL 1c. VERTICAL SYNC. OUTPUT, PIN 3
SIGNAL 1d. ODD-EVEN OUTPUT, PIN 7
SIGNAL 1e. BACK PORCH OUTPUT, PIN 5
See Fig 2, 3
See Fig 4
1882-14

Figure 1. Standard (NTSC Input) Timing

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

* Signal 1a drawing reproduced with permission from EIA.

Expanded Timing Diagrams

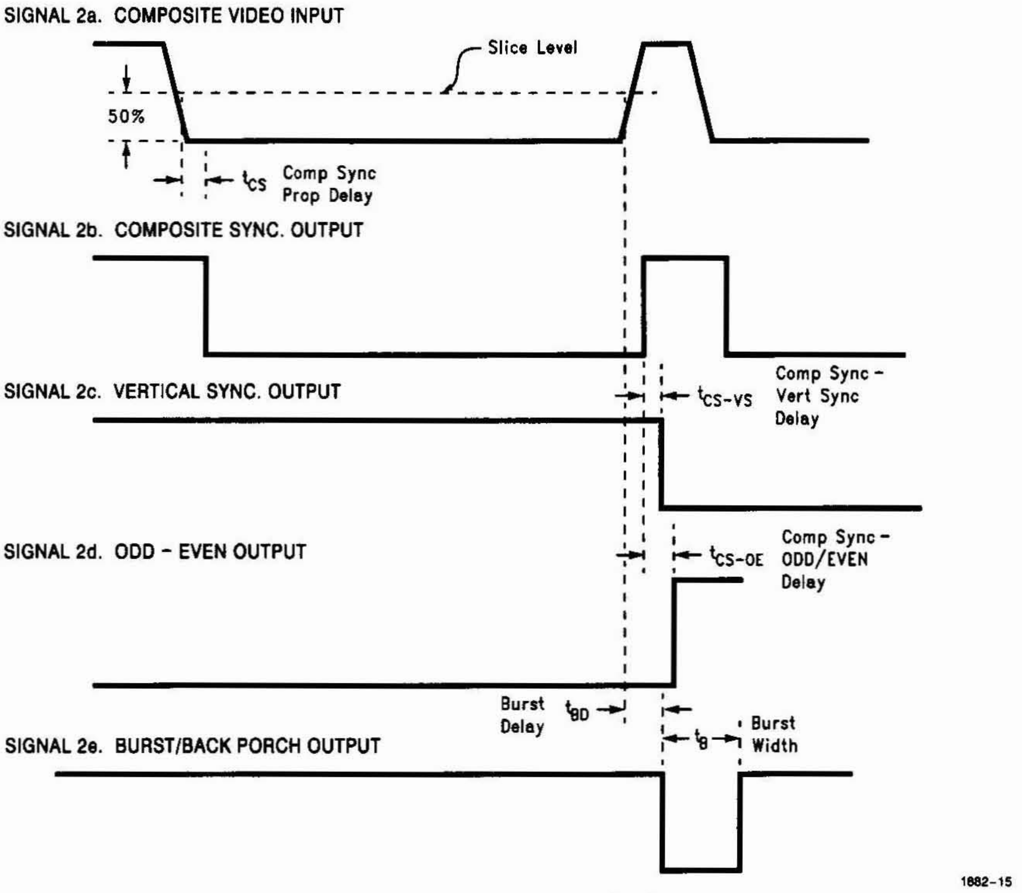

SIGNAL 2a. COMPOSITE VIDEO INPUT
Slice Level
50%
t_{CS} Comp Sync Prop Delay
SIGNAL 2b. COMPOSITE SYNC. OUTPUT
SIGNAL 2c. VERTICAL SYNC. OUTPUT
t_{CS-VS} Comp Sync - Vert Sync Delay
SIGNAL 2d. ODD - EVEN OUTPUT
t_{CS-OE} Comp Sync - ODD/EVEN Delay
Burst Delay t_{BD}
t_B Burst Width
SIGNAL 2e. BURST/BACK PORCH OUTPUT
1882-15

Figure 2. Standard Vertical Timing

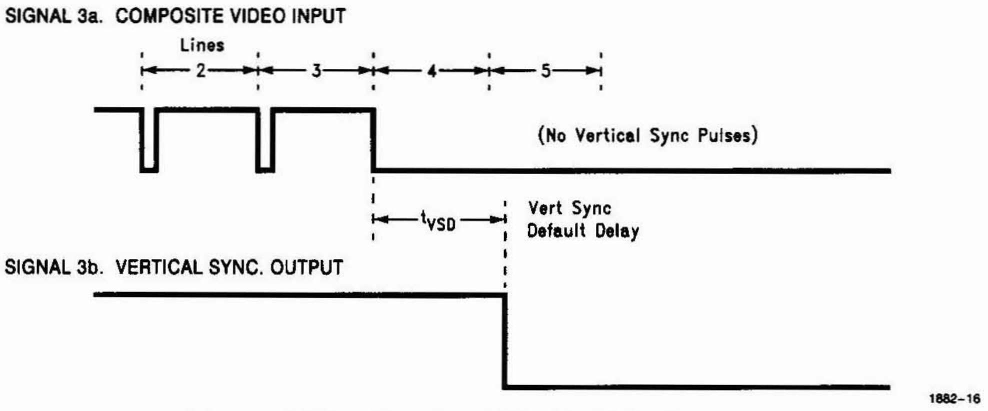
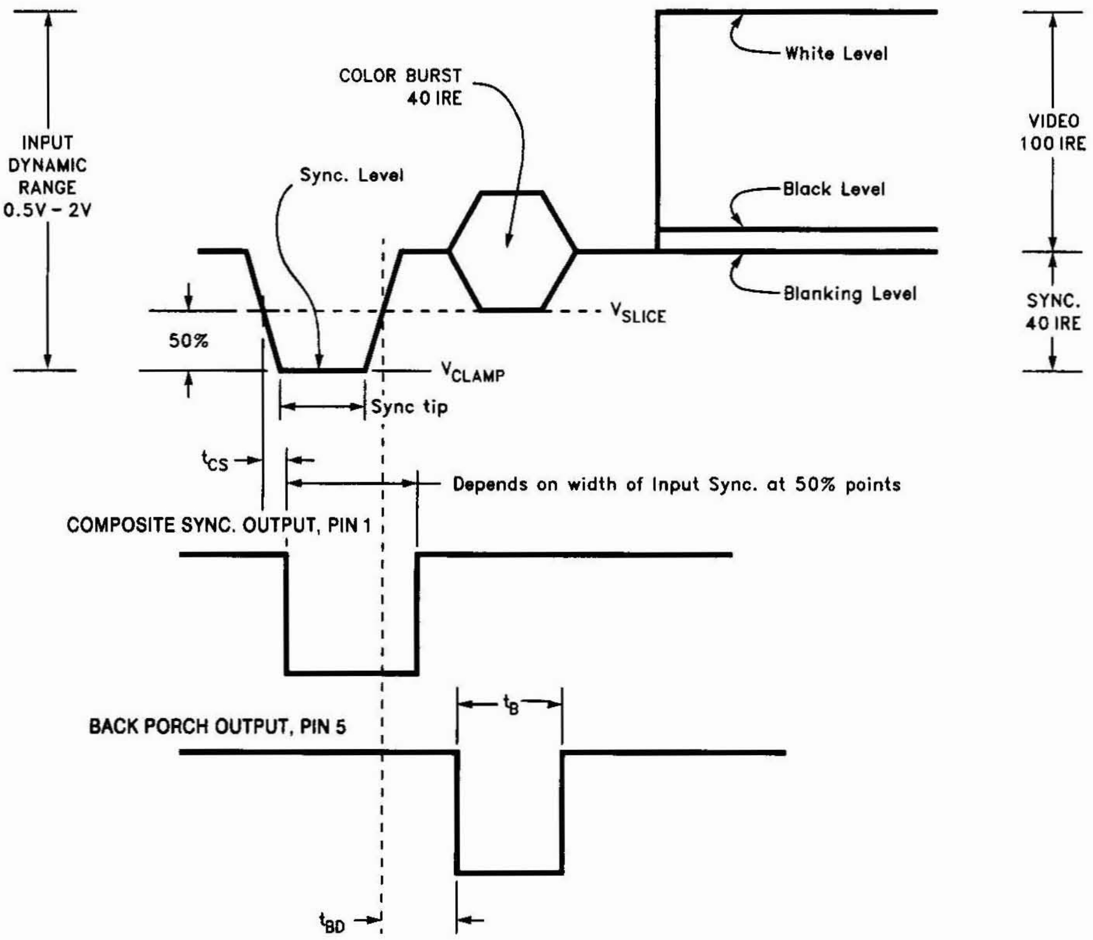

SIGNAL 3a. COMPOSITE VIDEO INPUT
Lines
2
3
4
5
(No Vertical Sync Pulses)
t_{VSD} Vert Sync Default Delay
SIGNAL 3b. VERTICAL SYNC. OUTPUT
1882-16

Figure 3. Non-Standard Vertical Timing


INPUT DYNAMIC RANGE 0.5V - 2V
COLOR BURST 40 IRE
Sync. Level
White Level
Black Level
Blanking Level
VIDEO 100 IRE
SYNC. 40 IRE
50%
V_{SLICE}
V_{CLAMP}
Sync tip
t_{CS}
Depends on width of Input Sync. at 50% points
COMPOSITE SYNC. OUTPUT, PIN 1
BACK PORCH OUTPUT, PIN 5
t_B
t_{BD}

1882-19

Figure 4. Standard (NTSC Input) H. Sync Detail

Applications Information

Video In

A simplified block diagram is shown following page.

An AC coupled video signal is input to **Video In** pin 2 via C1, nominally 0.1 μF. Clamp charge current will prevent the signal on pin 2 from going any more negative than Sync Tip Ref, about 1.5V. This charge current is nominally about 1 mA. A clamp discharge current of about 10 μA is always attempting to discharge C1 to Sync Tip Ref, thus charge is lost between sync pulses that must be replaced during sync pulses. The droop voltage that will occur can be calculated from IT = CV, where V is the droop voltage, I is the discharge current, T is the time between sync pulses (sync period − sync tip width), and C is C1.

An NTSC video signal has a horizontal frequency of 15.73 kHz, and a sync tip width of 4.7 μs. This gives a period of 63.6 μs and a time T = 58.9 μs. The droop voltage will then be V = 5.9 mV. This is less than 2% of a nominal sync tip amplitude of 286 mV. The charge represented by this droop is replaced in a time given by T = CV/I, where I = clamp charge current = 1 mA. Here T = 590 ns, about 12% of the sync pulse width of 4.7 μs. It is important to choose C1 large enough so that the droop voltage does not approach the 50% switching threshold of the internal comparator.

AGC and Composite Sync

The clamped video signal then passes to the AGC, which will maintain the blanking level of its output (sensed during burst) at the blanking reference level. The AGC should therefore present a constant amplitude signal to the comparator, if the input is within the AGC's dynamic range. A 50% slicing reference is compared with the AGC's output at the comp circuit. Comp's output is level shifted and buffered to TTL levels, and sent out as **Comp Sync** on pin 1.

Burst

A low-going Burst pulse follows each rising edge of sync, and lasts approximately 3.5 μs for an R_{SET} of 681 kΩ. This signal is used internally to gate the AGC feedback for determining blanking level.

Vertical Sync

A low-going **Vertical Sync** pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the EL1882C on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 60 μs after the last falling edge of the vertical equalizing phase for R_{SET} = 681 kΩ.

Odd/Even

Because a typical television picture is composed of two interlaced fields, there is an odd field that includes all the odd lines, and an even field that consists of the even lines. This odd/even field information is decoded by the EL1882C during the end of picture information and the beginning of vertical information. The odd/even circuit includes a T-flip-flop that is reset during full horizontal lines, but not during half lines or vertical equalization pulses. The T-flip-flop is clocked during each falling edge of these half h-period pulses. Even fields will toggle until a low state is clocked to the odd/even pin 7 at the beginning of vertical sync, and odd fields will cause a high state to be clocked to the odd/even pin at the start of the next vertical sync pulse. Odd/even can be ignored if using non-interlaced video, as there is no change in timing from one field to the next.

R_{SET}

An external R_{SET} resistor, connected from R_{SET} pin 6 to ground, produces a reference current that is used internally as the timing reference for vertical sync width, vertical sync default delay, burst gate delay and burst width. Decreasing the value of R_{SET} increases the reference current, which in turn decreases reference times and pulse widths. A higher frequency video input necessitates a lower R_{SET} value.

Applications Information — Contd.

Chroma Filter

When the EL1882 is used in composite color systems, a chroma filter is required at the video input. This is so because the color burst signal extends to the 50% point of the sync pulse (−20 IRE). Since the EL1882 slices at the 50% level, a chroma filter is required to attenuate the color burst signal to a point above the 50% level. Without this filter false sync triggering may occur during color burst. An example chroma filter is shown in Figure 5. It can be implemented very simply and inexpensively with a series resistor of 620Ω and a parallel capacitor of 500 pF, which gives a single pole roll-off frequency of about 500 kHz. This sufficiently attenuates the 3.58 MHz (NTSC) or 4.43 MHz (PAL) color burst signal, yet passes the approximately 15 kHz sync signals without appreciable attenuation. A chroma filter will increase the propagation delay from composite sync to outputs.

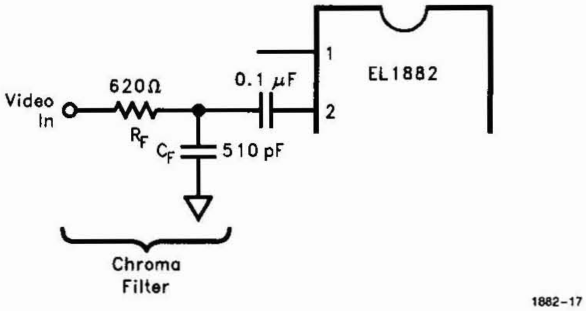

Video In
620Ω
R_F
C_F
510 pF
0.1 μF
1
2
EL1882
Chroma Filter
1882-17

Figure 5

Simplified Block Diagram

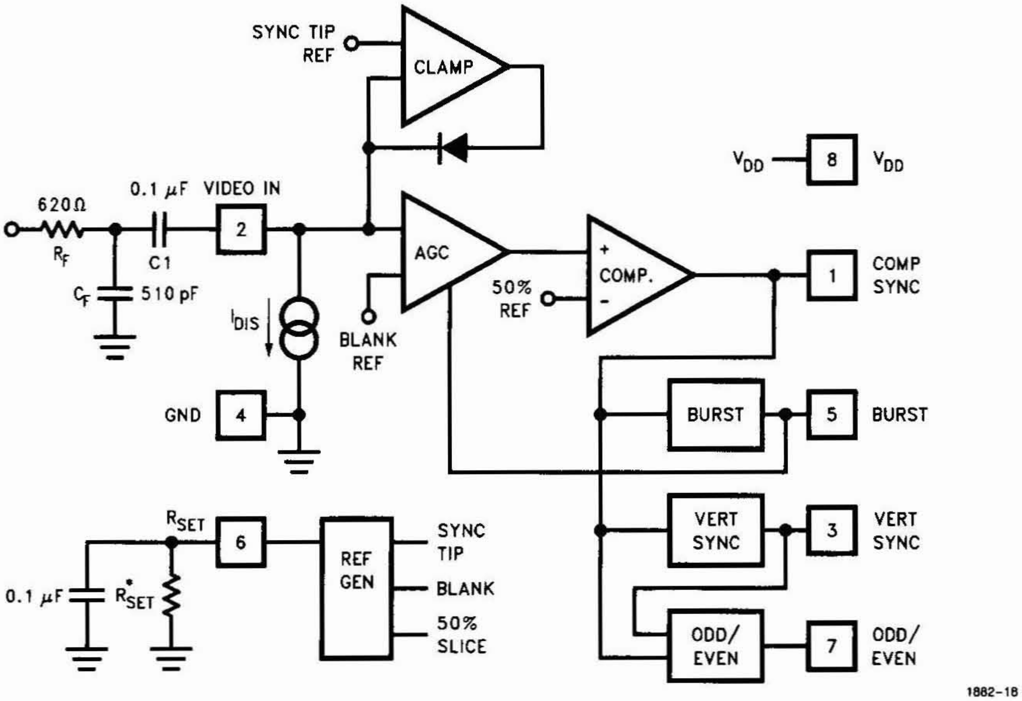

SYNC TIP REF
CLAMP
620Ω
R_F
0.1 μF
VIDEO IN
C1
C_F
510 pF
2
I_{DIS}
AGC
BLANK REF
GND
4
50% REF
COMP.
+
-
V_{DD}
8
V_{DD}
1
COMP SYNC
BURST
5
BURST
VERT SYNC
3
VERT SYNC
ODD/ EVEN
7
ODD/ EVEN
R_{SET}
6
0.1 μF
R_{SET}*
REF GEN
SYNC TIP
BLANK
50% SLICE
1882-18

Figure 6

* Note: R_{SET} must be a 1% resistor.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2082C

Current-Mode Multiplier

Features

- Flexible inputs and outputs, all ground referred
- 150 MHz large and small-signal bandwidth
- 46 dB of calibrated gain control range
- 70 dB isolation in disable mode @ 10 MHz
- 0.15% diff gain and 0.05° diff phase performance at NTSC using application circuit
- Operates on ±5V to ±15V power supplies
- Outputs may be paralleled to function as a multiplexer

Applications

- Level adjust for video signals
- Video faders and mixers
- Signal routing multiplexers
- Variable active filters
- Video monitor contrast control
- AGC
- Receiver IF gain control
- Modulation/demodulation
- General "cold" front-panel control of AC signals

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2082CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2082CS	0°C to +75°C	8-Pin SO	MDP0027

General Description

The EL2082 is a general purpose variable gain control building block, built using an advanced proprietary complementary bipolar process. It is a two-quadrant multiplier, so that zero or negative control voltages do not allow signal feedthrough and very high attenuation is possible. The EL2082 works in current mode rather than voltage mode, so that the input impedance is low and the output impedance is high. This allows very wide bandwidth for both large and small signals.

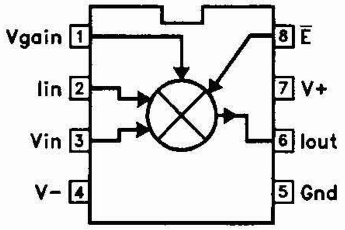
The I_{IN} pin replicates the voltage present on the V_{IN} pin; therefore, the V_{IN} pin can be used to reject common-mode noise and establish an input ground reference. The gain control input is calibrated to 1 mA/mA signal gain for 1V of control voltage. The disable pin ($\overline{E}$) is TTL-compatible, and the output current can comply with a wide range of output voltages.

Because current signals rather than voltages are employed, multiple inputs can be summed and many outputs wire-or'ed or mixed.

The EL2082 operates from a wide range of supplies and is available in standard 8-pin plastic DIP or 8-lead SO.

Connection Diagram

8-Pin DIP/SO



2082-1

Top View

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between $V_S{}^+$ and $V_S{}^-$	+33V	P_D	Maximum Power Dissipation	See Curves
V_{IN}, I_{OUT}	Voltage	±V_S	T_A	Operating Temperature Range	0°C to +75°C
V_E, V_{GAIN}	Input Voltage	−1 to +7V	T_J	Operating Junction Temperature	150°C
I_{IN}	Input Current	±5 mA	T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

(V_S = ±15V, V_G = 1V, V_E = 0.8V, V_{OUT} = 0, V_{IN} = 0, I_{IN} = 0)

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{IO}	Input Offset Voltage	Full	−20		20	II	mV
I_{OO}	Output Offset Current	Full	−100		100	II	µA
R_{INI}	I_{IN} Input Impedance; I_{IN} = 0, 0.35 mA	Full	75	95	115	II	Ω
V_{CMRR}	Voltage Common-Mode Rejection Ratio V_{IN} = −10V, +10V	Full	45	55		II	dB
I_{CMRR}	Offset Current Common-Mode Rejection Ratio, V_{IN} = −10V, +10V	Full		0.5	5	II	µA/V
V_{PSRR}	Offset Voltage Power Supply Rejection Ratio, V_S = ±5V to ±15V	Full	60	80		II	dB
I_{PSRR}	Offset Current Power Supply Rejection Ratio, V_S = ±5V to ±15V	Full		1	10	II	µA/V
I_{BVIN}	V_{IN} Bias Current	Full	−10		10	II	µA
R_{INV}	V_{IN} Input Impedance; V_{IN} = −10V, +10V	Full	0.5	1.0		II	MΩ
Nlini	Signal Nonlinearity; I_{IN} = −0.7 mA, −0.35 mA, 0 mA, +0.35 mA, +0.7 mA	Full		0.10	0.4	II	%
R_{OUT}	Output Impedance V_{OUT} = −10V, +10V	Full	0.25	0.5		II	MΩ

DC Electrical Characteristics — Contd.

($V_S = \pm 15V, V_G = 1V, V_E = 0.8V, V_{OUT} = 0, V_{IN} = 0, I_{IN} = 0$)

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OUT}	Output Swing; $V_{GAIN} = 2V$, I_{IN} ±2 mA, $R_L = 4.0K$	Full	−11		+11	II	V
V_{IOG}	V_{OS}, Gain Control, Extrapolated from $V_{GAIN} = 0.1V, 1V$	Full	−15		15	II	mV
A_I	Current Gain, I_{IN} ±350 μA	Full	0.9	1.0	1.1	II	mA/mA
Nling	Nonlinearity of Gain Control, $V_{GAIN} = 0.1V, 0.5V, 1V$	Full		2	5	II	%
I_{SO}	Input Isolation with $V_{GAIN} = -0.1V$	Full	−80	−96		II	dB
V_{INH}	$\overline{E}$ Logic High Level	Full	2.0			II	V
V_{INL}	$\overline{E}$ Logic Low Level	Full			0.8	II	V
I_{LH}	Input Current of $\overline{E}$, $V_E = 5V$	Full	−50		50	II	μA
I_{LL}	Input Current of $\overline{E}$, $V_E = 0$	Full	−50		50	II	μA
I_{ODIS}	I_{OUT}, Disabled $\overline{E} = 2.0V$	Full			±10	II	μA
I_S	Supply Current	Full		13	16	II	mA

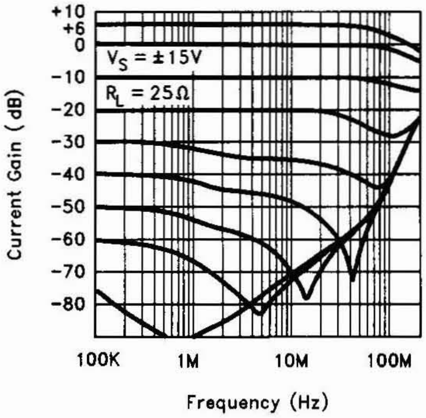
AC Electrical Characteristics

($R_L = 25\Omega, C_L = 4$ pF, $C_{IIN} = 2$ pF, $T_A = 25°C, V_G = 1V, V_S = \pm 15V$)

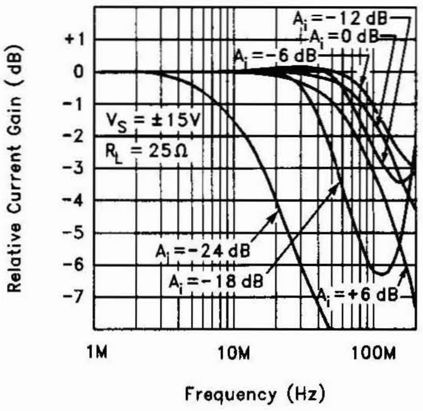
Parameter	Description	Min	Typ	Max	Test Level	Units
BW1	Current Mode Bandwidth −3 dB		150		V	MHz
BW2	±0.1 dB		30		V	MHz
BWp	Power, $I_{IN} = 1$ mA p-p		150		V	MHz
BWg	Gain Control Bandwidth		20		V	MHz
SRG	Gain Control Slew Rate V_G from 0.2V to 2V		12		V	(mA/mA)/μs
T_{REC}	Recovery Time from $V_G < 0$		250		V	ns
T_{EN}	Enable Time from $\overline{E}$ Pin		200		V	ns
T_{DIS}	Disable Time from $\overline{E}$ Pin		30		V	ns
D_G	Differential Gain, NTSC with $I_{IN} = -0.35$ mA to $+0.35$ mA		0.25		V	%
D_P	Differential Phase, NTSC with $I_{IN} = -0.35$ mA to $+0.35$ mA		0.05		V	Degree

Typical Performance Curves

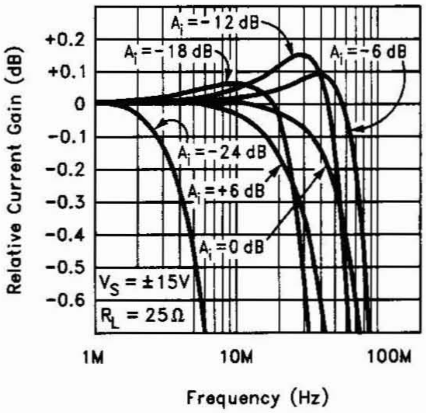
Current Gain vs Frequency for Different Gains



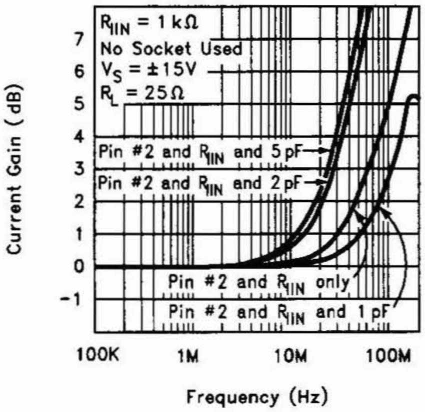
Current Gain vs Frequency



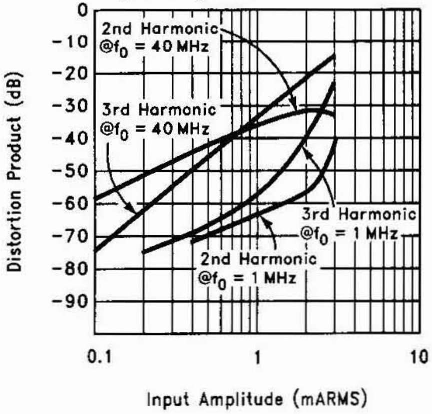
Current Gain Flatness



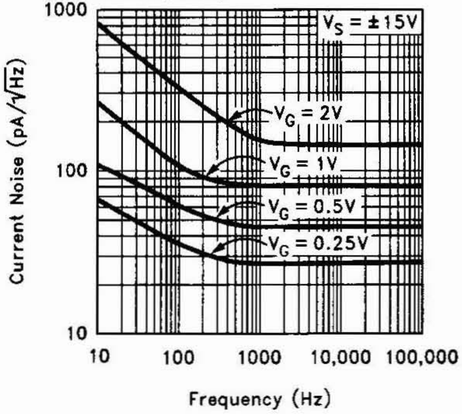
Frequency Response in Voltage Input Mode



Harmonic Distortion vs Input Amplitude

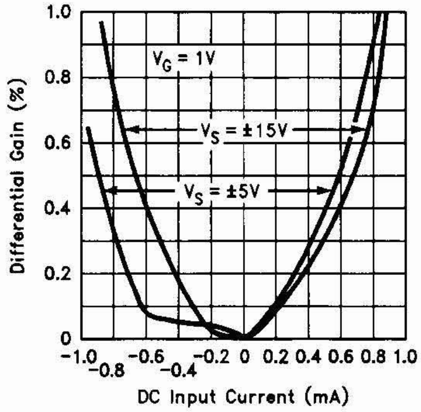


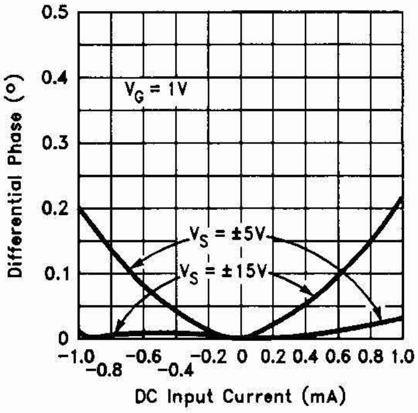
Output Current Noise vs Frequency



2082-2

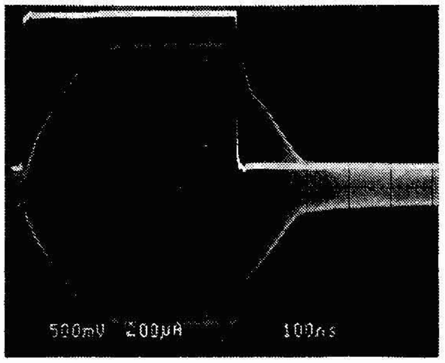
Typical Performance Curves — Contd.


Differential Gain Error vs DC Offset Current


Differential Phase Error vs DC Offset Current

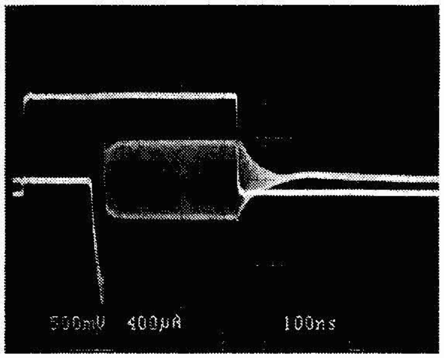
2082-3

Gain Pin Transient Response

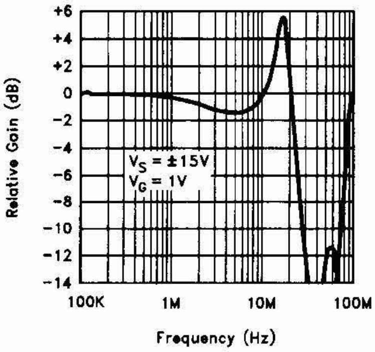


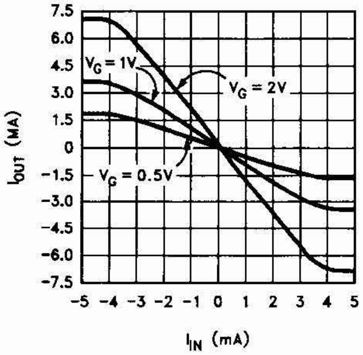
2082-4

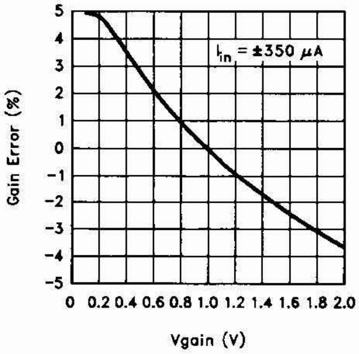
Gain Control Recovery From Vg = −0.1V



2082-5


Gain Control Pin Frequency Response

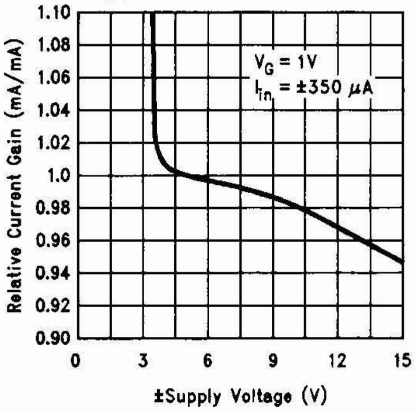

I_{OUT} vs I_{IN}


Normalized Gain Error vs V_{GAIN} Voltage

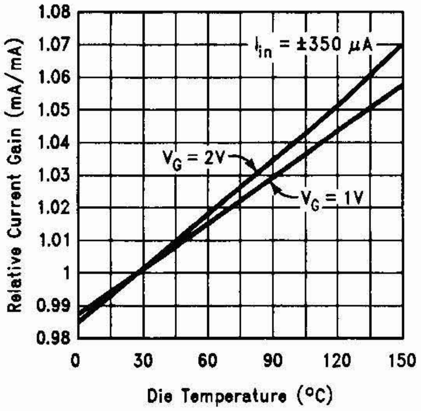
2082-6

Typical Performance Curves — Contd.

Current Gain vs Supply Voltage

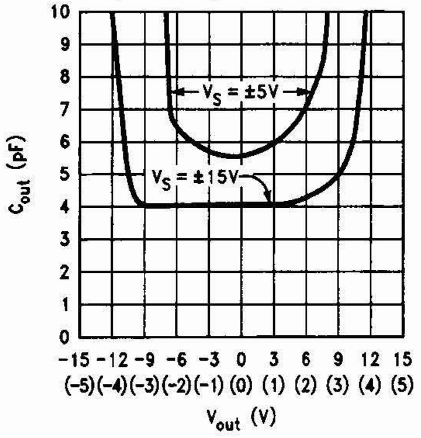


Current Gain vs Temperature



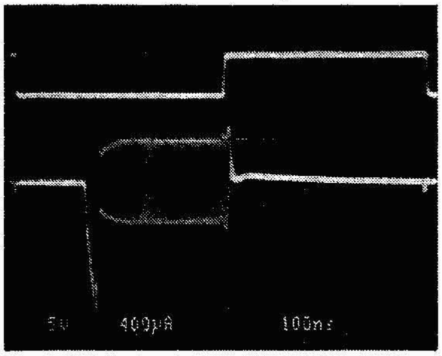
2082-7

Output Capacitance vs Output Voltage



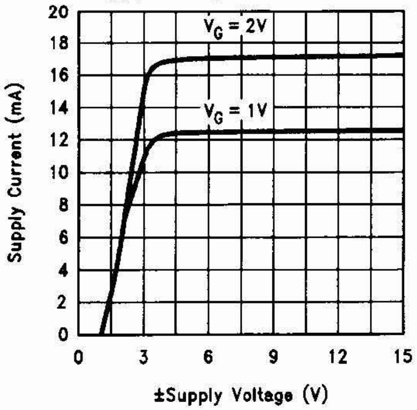
2082-8

Enable Pin Response

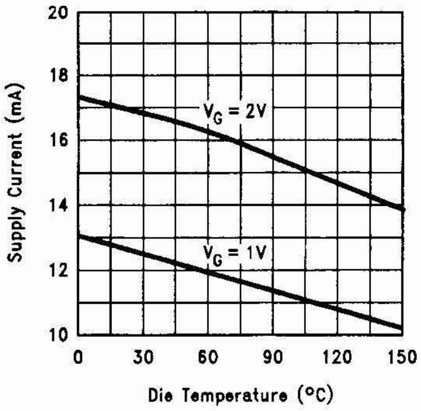


2082-9

Supply Current vs Supply Voltage

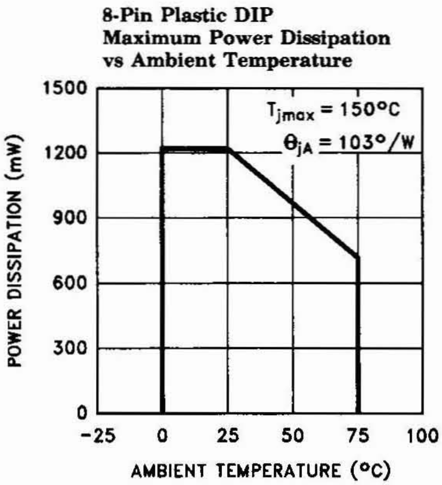


Supply Current vs Die Temperature

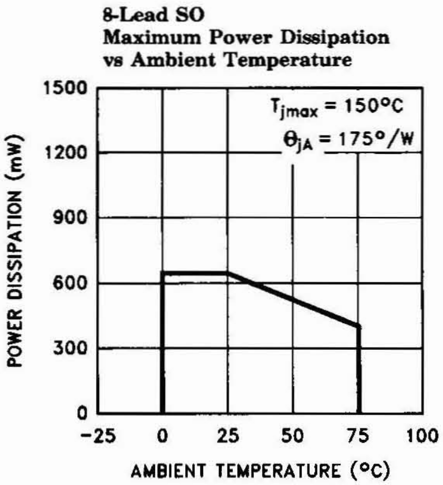


2082-10

Typical Performance Curves — Contd.



2082-11



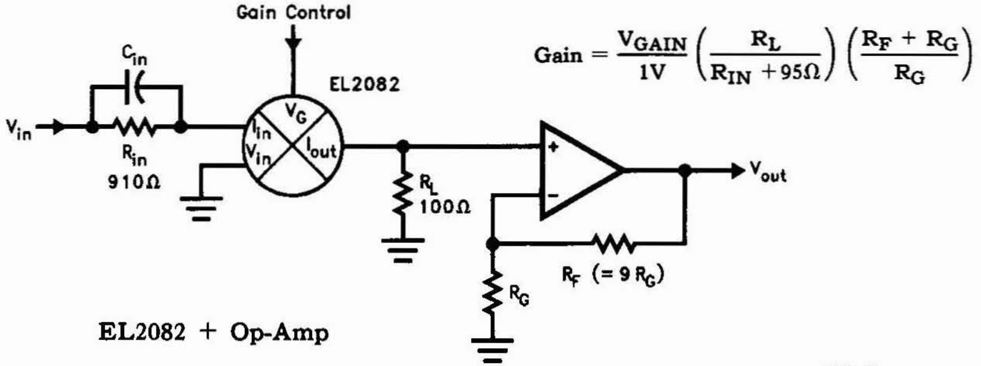
2082-12

Applications Information

The EL2082 is best thought of as a current-conveyor with variable current gain. A current input to the I_{IN} pin will be replicated as a current driven out the I_{OUT} pin, with a gain controlled by V_{GAIN}. Thus, an input of 1 mA will produce an output current of 1 mA for V_{GAIN} = 1V. An input of 1 mA will produce an output of 2 mA for V_{GAIN} = 2V. The useable V_{GAIN} range is zero to +2V. A negative level on V_{GAIN}, even only −20 mV, will yield very high signal attenuation.

The EL2082 in Conjunction with Op-Amps

This resistor-load circuit shows a simple method of converting voltage signals to currents and vice versa:



$$\text{Gain} = \frac{V_{GAIN}}{1V}\left(\frac{R_L}{R_{IN}+95\Omega}\right)\left(\frac{R_F+R_G}{R_G}\right)$$

EL2082 + Op-Amp

2082-13

R_{IN} would typically be 1 kΩ for video level inputs, or 10 kΩ for ±10V instrumentation signals. The higher the value of R_{IN} (the lower the input current), the lower the distortion levels of the EL2082 will be. An approximate expression of the nonlinearity of the EL2082 is:

$$\text{Nonlinearity (\%)} = 0.3 * I_{IN}\,(\text{mA})^2$$

Optimum input current level is a tradeoff between distortion and signal-to-noise-ratio. The distortion and input range do not change appreciably with V_{GAIN} levels; distortion is set by input currents alone.

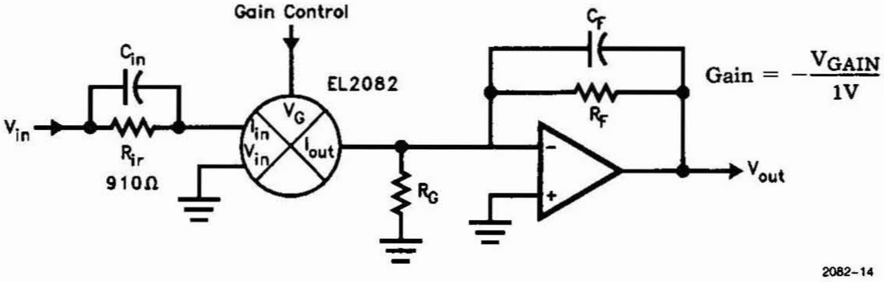
Applications Information — Contd.

The output current could be terminated with a 1 kΩ load resistor to achieve a nominal voltage gain of 1 at the EL2082, but the I_{OUT}, load, and stray capacitances would limit bandwidth greatly. The lowest practical total capacitance at I_{OUT} is about 12 pF, and this gives a 13 MHz bandwidth with a 1 kΩ load. In the above example a 100Ω load is used for an upper limit of 130 MHz. The operational amplifier gives a gain of +10 to bring the overall gain to unity. Wider bandwidth yet can be had by installing C_{IN}. This is a very small capacitor, typically 1 pf–2 pF, and it bolsters the gain above 100 MHz. Here is a table of results for this circuit used with various amplifiers:

Operational Amplifier	Power Supplies	Rf	Rg	C_{IN}	−3 dB Bandwidth	0.1 dB Bandwidth	Peaking
EL2020	±5V	620	68	—	34 MHz	5.6 MHz	0
EL2020	±15V	620	68	—	40 MHz	7.4 MHz	0
EL2130	±5V	620	68	—	73 MHz	11 MHz	1.0 dB
EL2030	±15V	620	68	—	93 MHz	12 MHz	1.3 dB
EL2090	±15V	240	27	—	60 MHz	10 MHz	0.5 dB
EL2120	±5V	220	24	—	57 MHz	10 MHz	0.4 dB
EL2120	±15V	220	24	—	65 MHz	11 MHz	0.3 dB
EL2070	±5V	200	22	2 pF	150 MHz	30 MHz	0.4 dB
EL2071	±5V	1.5K	240	2 pF	200 MHz	30 MHz	0
EL2075	±5V	620	68	2 pF	270 MHz	30 MHz	1.5 dB

Maximum bandwidth is maintained over a gain range of +6 to −16 dB; bandwidth drops at lower gains. If wider gain range with full bandwidth is required, two or more EL2082's can be cascaded with the I_{OUT} of one directly driving the I_{IN} of the next.

The EL2082 can also be used with an I ⟶ V operational circuit:



$$\text{Gain} = -\frac{V_{GAIN}}{1V}\left(\frac{R_F}{R_{IN}+95\Omega}\right)$$

Inverting
EL2082 + Op-Amp

The circuit above gives a negative gain. The main concern of this connection involves the total I_{OUT} and stray capacitances at the amplifier's input. When using traditional op-amps, the pole caused by these capacitances can make the amplifier less stable and even cause oscillations in amplifiers whose gain-bandwidth is greater than 5 MHz. A typical cure is to add a capacitor Cf in the 2 pF–10 pF range. This will reduce overall bandwidth, so a capacitor C_{IN} can be added to regain frequency response. The ratio Cf/C_{IN} is made equal to R_{IN}/R_f.

Applications Information — Contd.

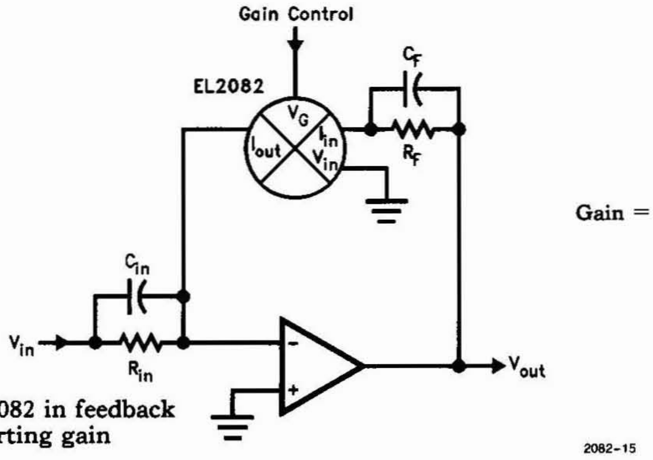
Current-feedback amplifiers eliminate this difficulty. Because their -input is a very low impedance, capacitance at the summing point of an inverting operational circuit is far less troublesome. Here is a table of results of various current-feedback circuits used in the inverting circuit:

Operational Amplifier	Power Supplies	Rf	R_{IN}	Rg	−3 dB Bandwidth	0.1 dB Bandwidth	Peaking
EL2020	±5V	1k	910	—	29 MHz	4.3 MHz	0
EL2020	±15V	1k	910	—	34 MHz	5.3 MHz	0
EL2130	±5V	1k	910	—	61 MHz	9.7 MHz	0
EL2030	±15V	1k	910	—	82 MHz	12.3 MHz	0
EL2171	±5V	2k	1.8k	1k	114 MHz	11 MHz	1.2 dB

with the EL2171 the EL2082 had ±15V supplies and the EL2171 required a 150Ω output load.

The EL2120 and EL2090 are suitable in this circuit but they are compensated for 300Ω feedback resistors. R_{IN} would have to be reduced greatly to obtain unity gain and the increased signal currents would cause the EL2082 to display much increased distortion. They could be used if the input resistor were maintained at 910Ω and Rf reduced for a $-1/3$ gain, or if Rf = 1k and an overall bandwidth of 25 MHz were acceptable.

The EL2082 can also be used within an op-amp's feedback loop:



EL2082 in feedback inverting gain

$$\text{Gain} = -\frac{1V}{V_{GAIN}}\left(\frac{R_F + 95\Omega}{R_{IN}}\right)$$

With voltage-mode op-amps, the same concern about capacitance at the summing node exists, so Cf and C_{IN} should be used. As before, current-feedback amplifiers tend to solve the problem. However, in this circuit the inherent phase lag of the EL2082 detracts from the phase margin of the op-amp, and some overall bandwidth reduction may result. The EL2082 appears as a 3.0 ns delay, well past 100 MHz. Thus, for a 20 MHz loop bandwidth, the EL2082 will subtract 20 MHz × 3.0 ns × 360 degrees = 21.6 degrees. The loop path should have at least 55 degrees of phase margin for low ringing in this connection. Loop bandwidth is always reduced by the ratio $R_{IN}/(R_{IN} + Rf)$ with voltage mode op-amps.

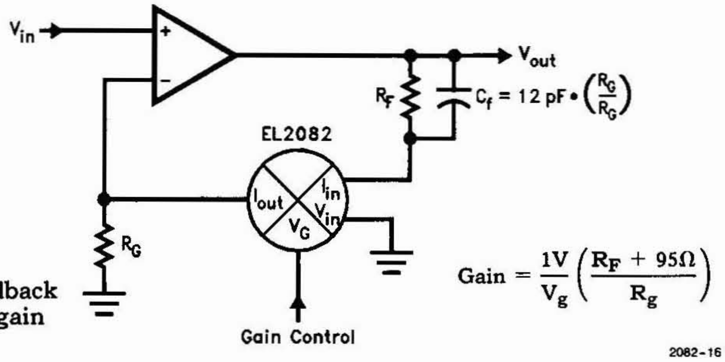
Applications Information — Contd.

Current-feedback op-amps again solve the summing-junction capacitance problem in this connection. The loop bandwidth here becomes a matter of transimpedance over frequency and its phase characteristics. Unfortunately, this is generally poorly documented in amplifier data sheets. A rule of thumb is that the transimpedance falls to the value of the recommended feedback resistor at a frequency of $F_{-3\ dB}/4$ to $F_{-3\ dB}/2$, where $F_{-3\ dB}$ is the unity-gain closed-loop bandwidth of the amplifier. The phase margin of the op-amp is usually close to 90 degrees at this frequency.

In general, Rf is initially the recommended value for the particular amplifier and is then empirically adjusted for amplifier stability at maximum V_{GAIN}, then R_{IN} is set for the overall circuit gain required. Sometimes a very small Cf can be used to improve loop stability, but it often must be in series with another resistor of value around Rf/2.

A virtue of placing the EL2082 in feedback is that the input-referred noise will drop as gain increases. This is ideal for level controls that are used to set the output to a constant level for a variety of inputs as well as AGC loops. Furthermore, the EL2082 has a relatively constant input signal amplitude for a variety of input levels, and its distortion will be relatively constant and controllable by setting Rf. Note that placing the EL2082 in the feedback path causes the circuit bandwidth to vary inversely with gain.

The next circuit shows use of the EL2082 in the feedback path of a non-inverting op-amp:


V_{in}
+
−
V_{out}
R_F
$C_f = 12\ pF \cdot \left(\frac{R_G}{R_G}\right)$
EL2082
I_{in}
I_{out}
V_{in}
V_G
R_G
$\text{Gain} = \frac{1V}{V_g}\left(\frac{R_F + 95\Omega}{R_g}\right)$
Gain Control
2082-16

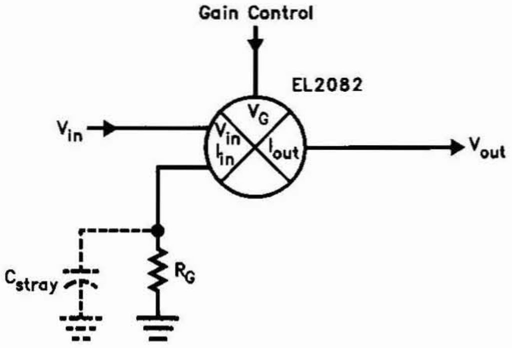
EL2082 in feedback
non-inverting gain

This example has the same virtues with regards to noise and distortion as the preceding circuit; and its bandwidth shrinks with increasing gain as well. The typical 12 pF sum of EL2082 output capacitance in parallel with stray capacitance necessitates the inclusion of Cf to prevent a feedback pole. Because of this 12 pF capacitance at the op-amp -input, current-feedback op-amps will generally not be useable. As before, the loop bandwidth and phase margin must accommodate the extra phase lag of the EL2082.

Applications Information — Contd.

Using the V_{IN} Pin

The V_{IN} pin can be used instead of the I_{IN} pin so:


Gain Control
EL2082
V_G
V_{in}
I_{in}
I_{out}
V_{in}
V_{out}
C_{stray}
R_G

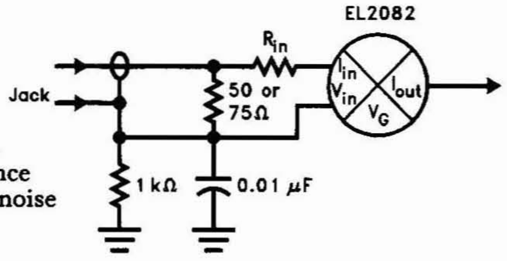
The V_{IN} pin used as signal input

$$Gm = \frac{I_{OUT}}{V_{IN}} = \frac{-Vg}{1v}\left(\frac{1}{R_g + 95\Omega}\right)$$

2082-17

This connection is useful when a high input impedance is required. There are a few caveats when using the V_{IN} pin. The first is that V_{IN} has a 250 V/µs slew rate limitation. The second is that the inevitable C_{STRAY} across Rg causes a gain zero and gain INCREASES above the $1/(2\pi\ C_{STRAY}\ Rg)$ frequency and can peak as much as 20 dB with large C_{STRAY}. A graph of gain vs. frequency for several C_{STRAYS} is included in the typical performance curves. In general, if wide bandwidth and frequency flatness is desired, the I_{IN} pin should be used.

The V_{IN} pin does make an excellent ground reference pin, for instance when low-frequency noise is to be rejected. The next schematic shows the EL2082 V_{IN} pin rejecting possible 60 Hz hum induced on an RF input cable:


EL2082
R_{in}
Jack
50 or 75Ω
1 kΩ
0.01 µF
I_{in}
V_{in}
I_{out}
V_G

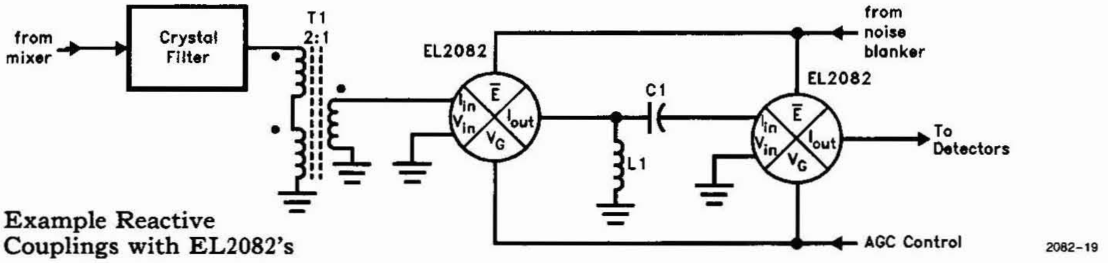
Using the V_{IN} pin as a ground reference to reject hum and noise

2082-18

This example shows V_{IN} rejecting low-frequency field-induced noise but not adding peaking since the 0.01 µF bypass capacitor shunts high-frequency signals to local ground.

Reactive Couplings with the EL2082

The following sketch is an excerpt of a receiver IF amplifier showing methods of connecting the EL2082 to reactive networks:


from mixer
Crystal Filter
T1
2:1
EL2082
$\bar{E}$
I_{in}
V_{in}
I_{out}
V_G
C1
L1
from noise blanker
EL2082
To Detectors
AGC Control

Example Reactive Couplings with EL2082's

2082-19

Applications Information — Contd.

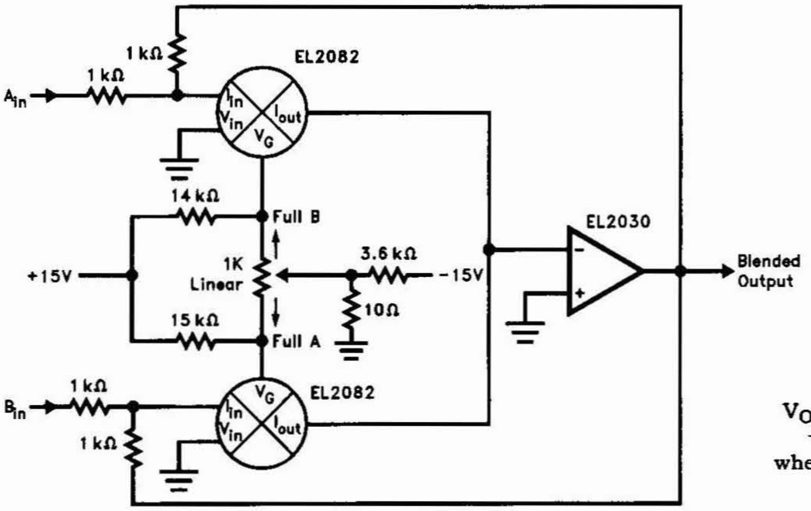
The I_{IN} pin of the EL2082 looks like 95Ω well past 100 MHz, and the output looks like a simple current-source in parallel with about 5 pF. There is no particular problem with any resistance or reactance connected to I_{IN} or I_{OUT}. The mixer output is generally sent to a crystal filter, which required a few hundred ohm terminating impedance. The impedance of the I_{IN} pin of the first EL2082 is transformed to about 400Ω by the 2:1 transformer T1. The two EL2082's are used as variable-gain IF amplifiers, with small gains offered by each. The output of the first EL2082 is coupled to the second by the resonant matching network L1–C1. For a Q of 5, Xc1 = x11 = 5 × 95Ω, approximately. The impedance seen at the first EL2082's I_{OUT} will be about $Q^2 \times 95\Omega$, or 2.5k, and by impedance transformation alone the first gain cell delivers 28 dB of gain at Vg = 1V. More gain cells can be used for a wider range of (calibrated) AGC compliance.

The $\overline{E}$ input can be used as a high-speed noise blanker gate.

Linearized Fader/Gain Control

The following circuit is an example of placing two EL2082's in the feedback network of an op-amp to significantly reduce their distortions:

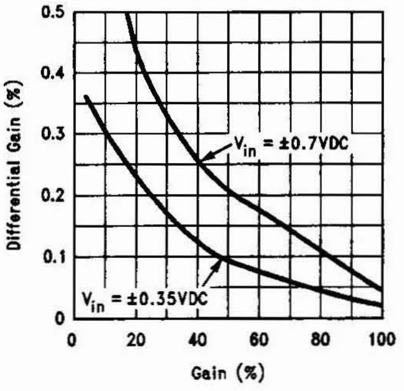
Linearized Gain Control/Fader



$$V_{OUT} = K \bullet V_A + (1-K) \bullet V_B$$
where $0 \le K \le 1$

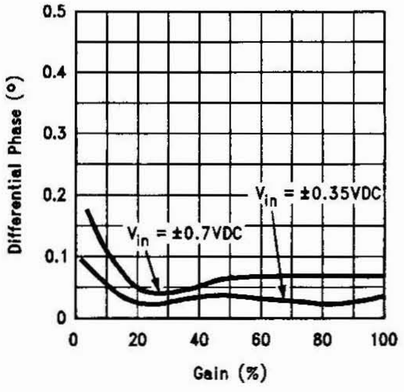
2082-20

Dual EL2082 Fader with EL2030
NTSC Differential Gain Error



2082-21

Dual EL2082 Fader with EL2030
NTSC Differential Phase Error



2082-22

Applications Information — Contd.

The circuit sums two inputs A and B, such that the sum of their respective path gains is unity, as controlled by the potentiometer. When the potentiometer's wiper is fully down, the slightly negative voltage at the Vg of the B-side EL2082 cuts off the B signal to better than 70 dB attenuation at 3.58 MHz. The A-side EL2082 is at unity gain, so the only (error) signal presented to the op-amp's -input is the same (error) signal at the I_{IN} of the A-side EL2082. The circuit thus outputs -A_{IN}. Since the error signal required by the op-amp is very small, even at video frequencies, the current through the A-side EL2082 is small and distortion is minimized.

At 50% potentiometer setting, equal error output signals flow from the EL2082's, since the op-amp still requires little net -input current. The EL2082's essentially buck each other to establish an output, and 50% gain occurs for both the A and B inputs. The EL2082's now contribute distortion, but less than in previous connections. The op-amp sees a constant 1k feedback resistor regardless of potentiometer setting, so frequency response is stable for all gain settings.

A single-input gain control is implemented by simply grounding B_{IN}.

Distortion can be improved by increasing the input resistors to lower signal currents. This will lower the overall gain accordingly, but will not affect bandwidth, which is dependent upon the feedback resistors. Reducing the signal input amplitude is an analagous tactic, but the noise floor will effectively rise.

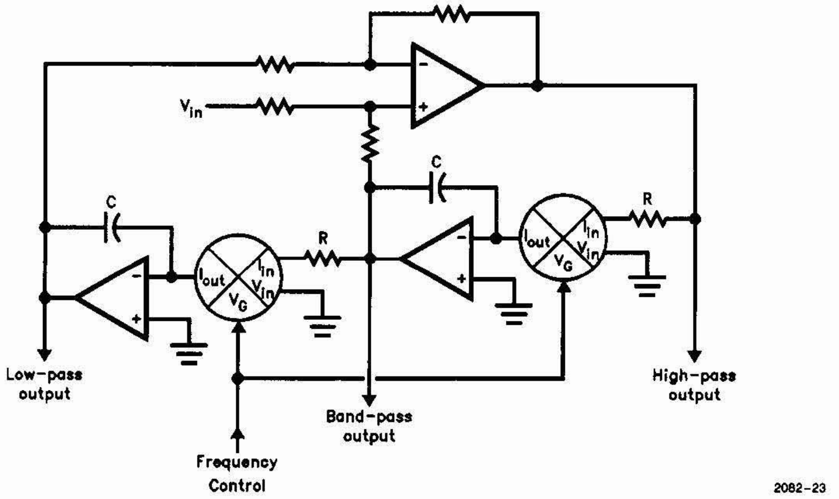
Another strategy to reduce distortion in video systems is to use DC restoration circuitry, such as the EL2090 ahead of the fader inputs to reduce the range of signals to be dealt with; the −0.7V to +0.7V possible range of inputs (due to capacitor coupling) would be changed to a stabilized −0.35V to +0.35V span.

The EL2020, EL2030, and EL2120 (at reduced bandwidth since it is compensated for 300Ω feedback resistors) all give the same video performance at NTSC operation.

Variable Filters

This circuit is the familiar state-variable configuration, similar to the bi-quad:

Voltage Tuneable Bi-Quad Filter

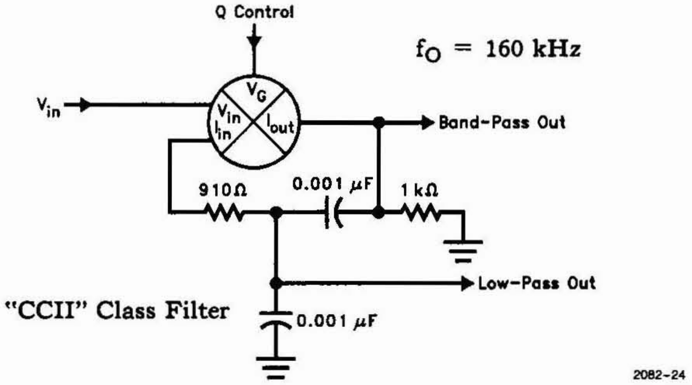


$$F_0 = \frac{V_g}{1V}\left(\frac{1}{2\pi(R + 95\Omega)C}\right)$$

Applications Information — Contd.

Frequency-setting resistors R are each effectively adjusted in value by an EL2082 to effect voltage-variable tuning. Two gain controls yields a linear frequency adjustment; using one gives a square-root-of-control voltage tuning. The EL2082's could be placed in series with the integrator capacitors instead to yield a tuning proportional to 1/Vg.

The next circuit is one of a new class of "CCII" filters that use the current-conveyor element. Basic information is available in the April 1991, volume 38, number 4 edition of the IEEE Transactions on Circuits and Systems journal, pages 456 through 461 of the article "The Single CCII Biquads with High-Input Impedance", by Shen-Iuan Liu and Hen-Wai Tsao.



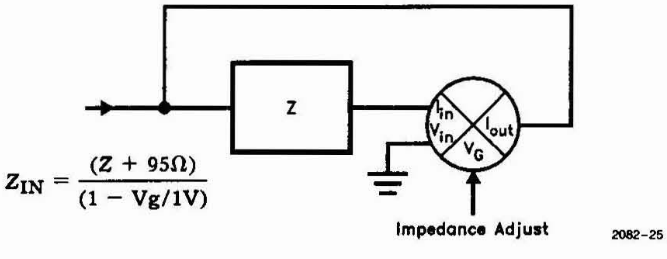
"CCII" Class Filter

This interesting filter uses the current output of the EL2082 to generate a bandpass voltage output and the intermediate node provides a second-order low-pass filter output. Both outputs should be buffered so as not to warp characteristics, although the V_{IN} of the next EL2082 can be driven directly in the case of cascaded filters. The V_{GAIN} input acts as a Q and peaking adjust point around the nominal 1V value. The resistor at I_{OUT} could serve as the frequency trim, and Q trimmed subsequently with V_{GAIN}.

Negative Components

The following circuit converts a component or two-terminal network to a variable and even negative replica of that impedance:

Variable or Negative Impedance Converter



$$Z_{IN} = \frac{(Z + 95\Omega)}{(1 - Vg/1V)}$$

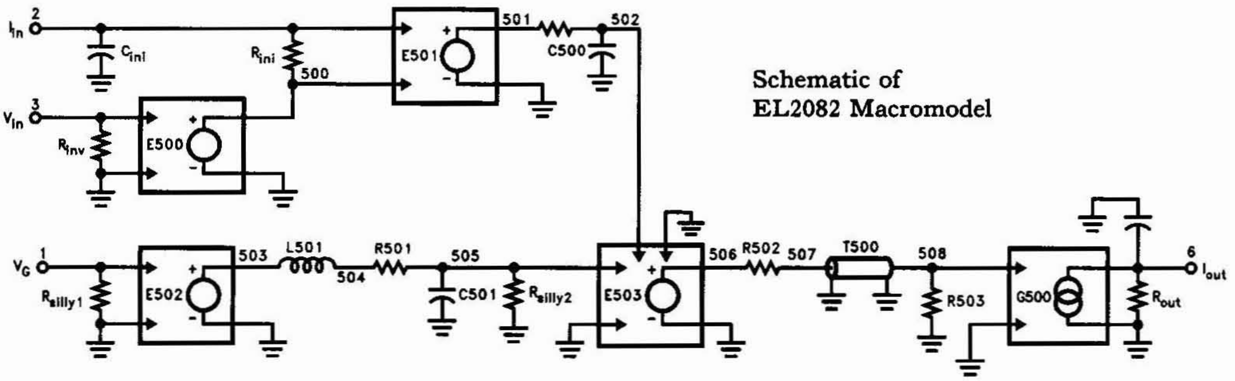
Applications Information — Contd.

A negative impedance is simply an impedance whose current flows reverse to the normal sense. In the above circuit, the current through Z is replicated by the EL2082 and inverted (I_{OUT} flows inverted to the sense of I_{IN} in the EL2082) and summed back to the input. When $Vg = 0$ or $Vg < 0$, the input impedance is simply $Z + 95\Omega$. When $Vg = 1V$, the negative of the current through Z is summed with the input and the input impedance is "infinite". When $Vg = 2V$, twice the negative of the current through Z is summed with the input resulting in an input impedance of $-Z-95\Omega$.

Thus variable capacitors can be simulated by substituting the capacitor as Z. "Negative" capacitors result for $Vg > 1V$, and capacitance needs to be present in parallel with the input to prevent oscillations. Inductors or complicated networks also work for Z, but a net negative impedance will result in oscillations.

EL2082 Macromodel

This macromodel has been designed to work with PSPICE (copywritten by the Microsim Corporation). E500 buffers in the V_{IN} voltage and presents it to the R_{INI} resistor to emulate the I_{IN} pin. E501 supplies the non-linearity of the current channel and replicates the I_{IN} current to a ground referenced voltage. R500 and C500 provide the bandwidth limitation on the current signal. E502 supplies the V_{GAIN} non-linearity and drives the L501/R501/C501 to shape the gain control frequency response. E503 does the actual gain-control multiplication, and drives delay line T500 to better simulate the actual phase characteristics of the part G500 creates the current output, and R_{OUT} with C_{OUT} provide proper output parasitics.



Schematic of
EL2082 Macromodel

The model is good at frequency and linearity estimates around $Vg = 1V$ and nominal temperatures, but has several limitations:

The Vg channel does not give zero gain for $Vg < 0$; the output gain reverses–don't use $Vg < 0$
The Vg channel is not slew limited
Frequency response does not vary with supply voltage

The V_{IN} channel is not slew limited
Noise is not modeled
Temperature effects are not modeled
CMRR and PSRR are not modeled
Frequency response does not vary with Vg

Unfortunately, the polynomial expressions and two-input multiplication may not be available on every simulator. Results have been confirmed by laboratory results in many situations with this macromodel, within its capabilities.

EL2082 Macromodel

```
*:                     Vgain
*                      |     Iin
*                      |     |     Vin
*                      |     |     |                 Iout
*                      |     |     |                 |
.SUBCKT EL2082macro   (1     2     3     4     5     6     7     8)
***
*** I-to-I gain cell macromodel ***
***
******
Cini 2 0 2P
C500 502 0 0.9845P
C501 505 0 1000P
Cout 6 0 5P
******
L501 503 504 0.1U
******
Rsilly1 1 0 1E9
Rsilly2 505 0 1E9
Rini 2 500 95
Rinv 3 0 2Meg
Rout 6 0 1Meg
R500 501 502 1000
R501 504 505 5
R502 506 507 50
R503 508 0 50
******
E500 500 0 3 0 1
E501 501 0 POLY(1) (2,500) 0 2  0 -.8
E502 503 0 POLY(1) (1,0) 0 1.05 -.05
E503 506 0 POLY(2) (505,0) (502,0) 0 0 0 0 1
G500 6 0 508 0 -0.0105
T500 508 0 507 0 Z0=50 TD=1.95N
******
.ENDS
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2090C

100 MHz DC-Restored Video Amplifier

Features

- Complete video level restoration system
- 0.01% differential gain and 0.02° differential phase accuracy at NTSC
- 100 MHz bandwidth
- 0.1 dB flatness to 20 MHz
- Sample-and-hold has 15 nA typical leakage and 1.5 pC charge injection
- System can acquire DC correction level in 10 μs, or 5 scan lines of 2 μs each, to ½ IRE
- $V_S = \pm 5V$ to $\pm 15V$
- TTL/CMOS hold signal

Applications

- Input amplifier in video equipment
- Restoration amplifier in video mixers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2090CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2090CM	0°C to +75°C	16-Lead SOL	MDP0027

General Description

The EL2090C is the first complete DC-restored monolithic video amplifier sub-system. It contains a very high-quality video amplifier and a nulling sample-and-hold amplifier specifically designed to stabilize video performance. When the HOLD logic input is set to a logic 0 during a horizontal sync, the sample-and-hold amplifier may be used as a general-purpose op-amp to null the DC offset of the video amplifier. When the HOLD input goes to a logic 1 the sample-and-hold stores the correction voltage on the hold capacitor to maintain DC correction during the subsequent scan line.

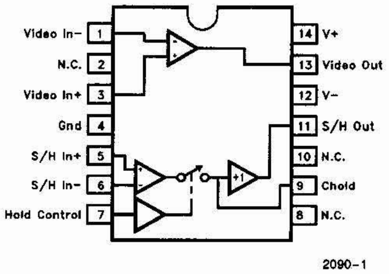
The video amplifier is optimized for video characteristics, and performance at NTSC is nearly perfect. It is a current-feedback amplifier, so that −3 dB bandwidth changes little at various closed-loop gains. The amplifier easily drives video signal levels into 75Ω loads. With 100 MHz bandwidth, the EL2090 is also useful in HDTV applications.

The sample-and-hold is optimized for fast sync pulse response. The application circuit shown will restore the video DC level in five scan lines, even if the HOLD pulse is only 2 μs long. The output impedance of the sample-and-hold is low and constant over frequency and load current so that the performance of the video amplifier is not compromised by connections to the DC restore circuitry.

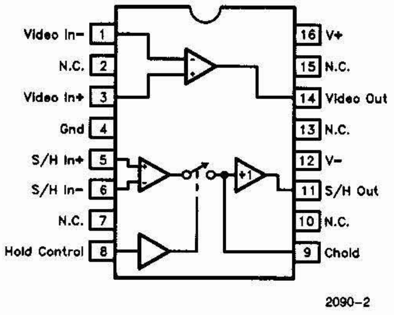
The EL2090C is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL2090C is specified for operation over the 0°C to 75°C temperature range.

Connection Diagrams

14-Pin DIP Package



16-Pin SOL Package



January 1996 Rev D

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V
Voltage between $V_{IN}+$, $S/H_{IN}+$, $S/H_{IN}-$, C_{HOLD}, and GND pins	(V+) + 0.5V to (V−) −0.5V
V_{OUT} Current	60 mA
Current into $V_{IN}-$ and HOLD Pins	5 mA
Current S/H_{OUT}	16 mA
Internal Power Dissipation	See Curves
Operating Ambient Temperature Range	0°C to 75°C
Operating Junction Temperature Plastic DIP or SOL	150°C
Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V; R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_S	Total Supply Current	Full		14	17	II	mA
Video Amplifier Section (Not Restored)							
V_{OS}	Input Offset Voltage	Full		8	70	II	mV
I_{B+}	$+V_{IN}$ Input Bias Current	Full		2	15	II	μA
I_{B-}	$-V_{IN}$ Input Bias Current	Full		30	150	II	μA
R_{OL}	Transimpedance	25°C		300		V	V/mA
A_{VOL}	Open-Loop Voltage Gain; V_{OUT} = ±2V	Full	56	65		II	dB
V_O	Output Voltage Swing V_S = ±15V; R_L = 2 kΩ	Full	±12	±13		II	V
	V_S = ±5V; R_L = 150Ω	Full	±3.0	±3.5		II	V
I_{SC}	Short-Circuit Current; $+V_{IN}$ Set to ±2V; $-V_{IN}$ to Ground through 1 kΩ	25°C	±50	±90	±160	II	mA
Sample-And-Hold Section							
V_{OS}	Input Offset Voltage	Full		2	10	II	mV
I_B	Input Bias Current	Full		0.5	2.5	II	μA
I_{OS}	Input Offset Current	Full		0.05	0.5	II	μA
$R_{IN, DIFF}$	Input Differential Resistance	25°C		200		V	kΩ
$R_{IN, COMM}$	Input Common-Mode Resistance	25°C		100		V	MΩ
V_{CM}	Common-Mode Input Range	Full	±11	±12.5		II	V

Open Loop DC Electrical Characteristics

V_S = ±15V; R_L = 150Ω, T_A = 25°C unless otherwise specified — Contd.

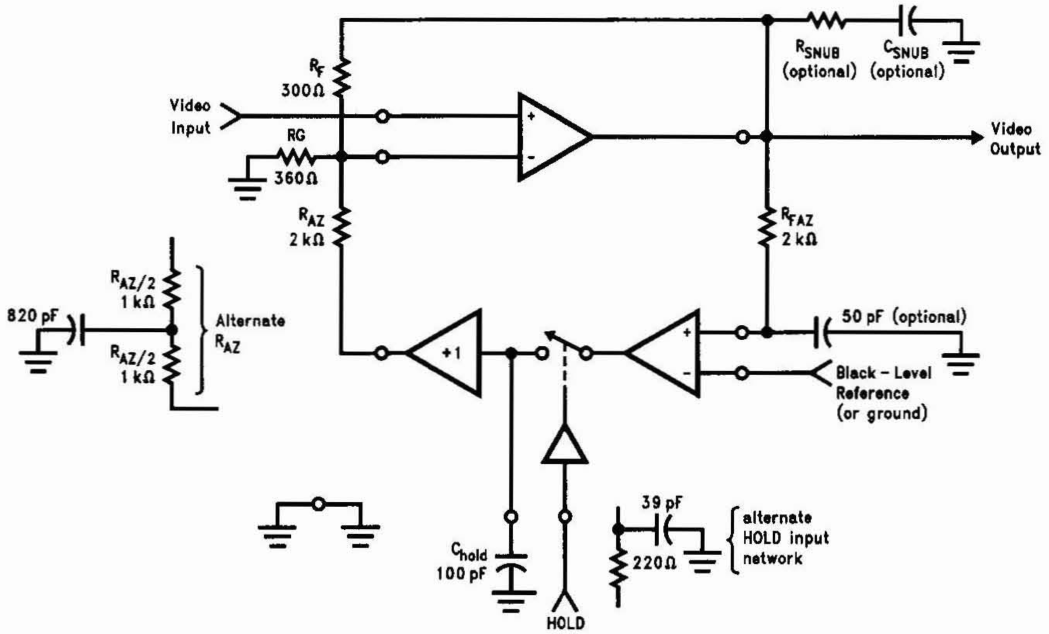
Parameter	Description	Temp.	Min	Typ	Max	Test Level	Units
Sample-And-Hold Section — Contd.							
A_{VOL}	Large Signal Voltage Gain	Full	15k	50k		II	V/V
CMRR	Common-Mode Rejection Ratio V_{CM} = ±11V	Full	75	95		II	dB
PSRR	Power-Supply Rejection Ratio V_S = ±5V to ±15V	Full	75	95		II	dB
V_{thresh}	HOLD Pin Logic Threshold	Full	0.8	1.4	2.0	II	V
I_{droop}	Hold Mode Droop Current	Full		10	50	II	nA
I_{charge}	Charge Current Available to Chold	Full	±90	±135		II	µA
V_O	Output Swing; R_L = 2k	Full	±10	±13		II	V
I_{SC}	Short-Circuit Current	25°C	±10	±17	±40	II	mA

Closed Loop AC Electrical Characteristics

V_S = ±15V; C_L = 15 pF; C_{stray} ($-V_{IN}$) = 2.5 pF; R_F = R_G = 300Ω; R_L = 150Ω; C_{hold} = 100 pF; T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
Video Amplifier Section						
SR	SlewRate; V_{OUT} from −2 to +2V		600		V	V/µs
BW	Bandwidth; −3 dB ±1 dB ±0.1 dB	75 35 10	100 60 20		III III III	MHz MHz MHz
Peaking dG	Differential Gain; V_{IN} from −0.7V to 0.7V; F = 3.58 MHz		0.01		V	%
dθ	Differential Phase; V_{IN} from −0.7V to 0.7V; F = 3.58 MHz		0.02		V	°
Sample-And-Hold Section						
BW	Gain-Bandwidth Product		1.3		V	MHz
ΔQ	Sample to Hold Charge Injection (Note 1)		1.5	5	III	pC
ΔT	Sample to Hold or Hold to Sample Delay Time		20		V	ns
T_s	Sample to Hold Settling Time to 2 mV		200		V	ns

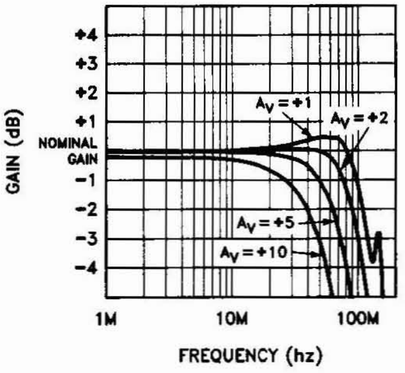
Note 1: The logic input is between 0V and 5V, with a 220Ω resistor in series with the HOLD pin and 39 pF capacitor from HOLD pin to ground.


R_SNUB (optional)
C_SNUB (optional)
R_F 300Ω
Video Input
RG 360Ω
+
−
Video Output
R_AZ 2 kΩ
R_FAZ 2 kΩ
R_AZ/2 1 kΩ
820 pF
R_AZ/2 1 kΩ
Alternate R_AZ
+1
50 pF (optional)
+
−
Black - Level Reference (or ground)
39 pF
C_hold 100 pF
220Ω
alternate HOLD input network
HOLD

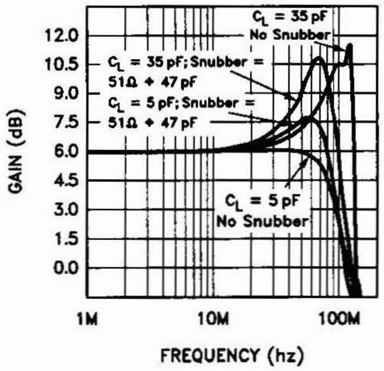
2090-3

Figure 1. Typical Application ($A_V = +2$)

Typical Performance Curves

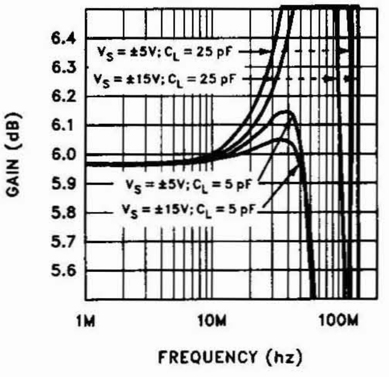


Relative Frequency Response for Various Gains

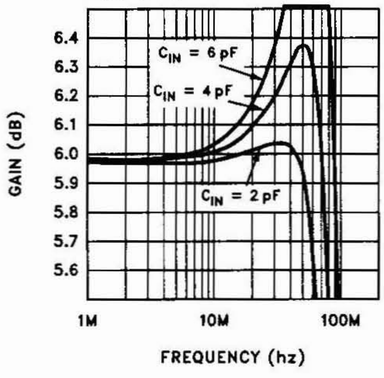


Frequency Response with Different Loads ($A_V = +2$)

2090-4



Frequency Response Flatness for Various Load and Supply Conditions

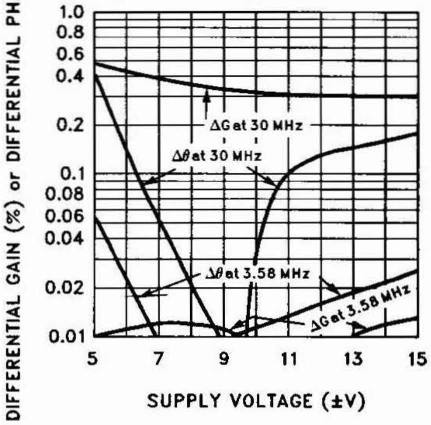


Frequency Response Flatness vs C_{IN-}, $A_V = +2$

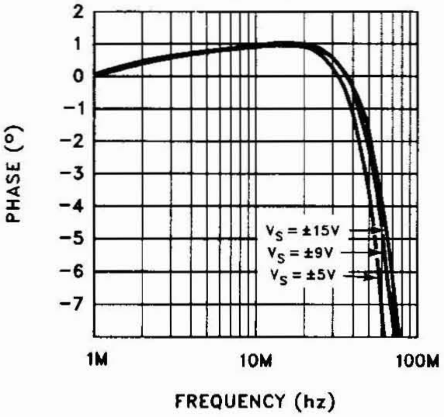
2090-5

Typical Performance Curves — Contd.

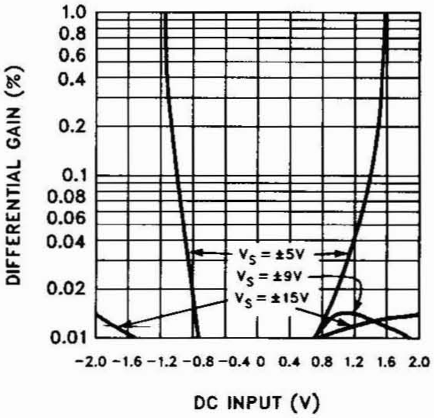
Differential Gain and Phase vs Supply Voltage; $A_V = +2$, $R_L = 150\Omega$, V_{IN} from 0 to +0.7 V_{DC}



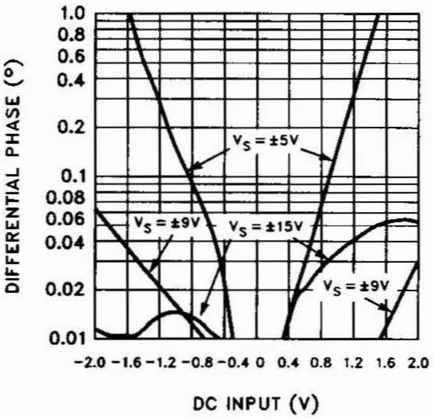
Deviation from Linear Phase vs Frequency



Differential Gain vs DC Input Offset; $A_V = +2$, $F_O = 3.58$ MHz, $R_L = 150\Omega$

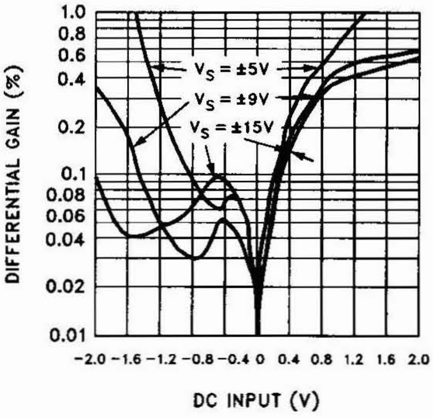


Differential Phase vs DC Input Offset; $A_V = +2$, $F_O = 3.58$ MHz, $R_L = 150\Omega$

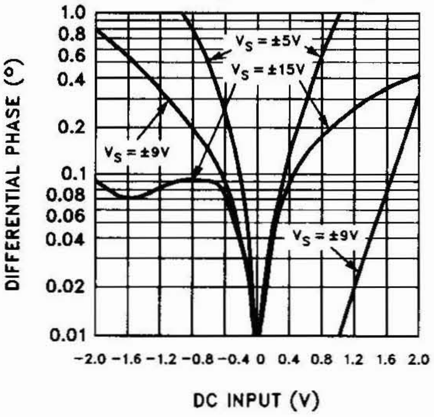


2090-12

Differential Gain vs DC Input Offset; $A_V = +2$ and $F_O = 30$ MHz, $R_L = 150\Omega$



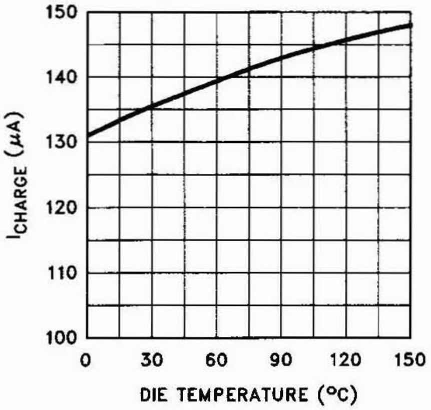
Differential Phase vs DC Input Offset; $A_V = +2$, $F_O = 30$ MHz, $R_L = 150\Omega$



2090-6

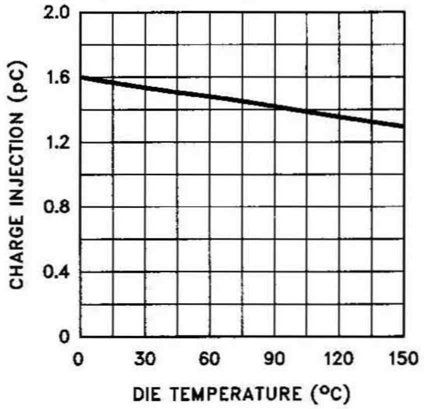
Typical Performance Curves — Contd.

S/H Available Charge Current vs Temperature

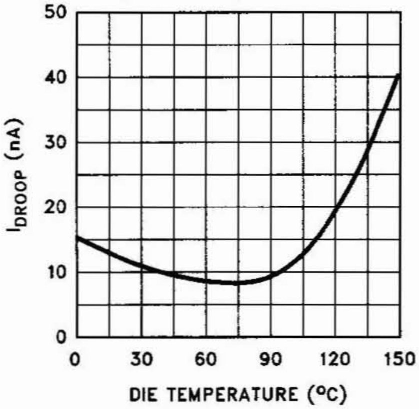


2090-7

Sample-to-Hold Change Injection vs Temperature

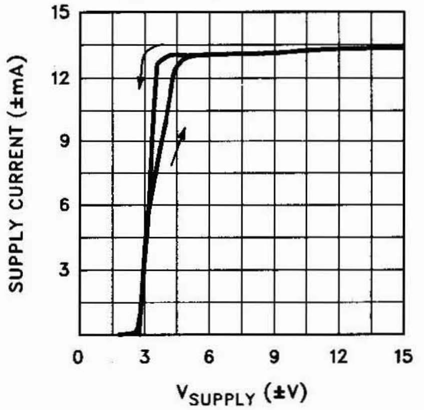


Typical Droop Current vs Temperature, V_S = ±15V

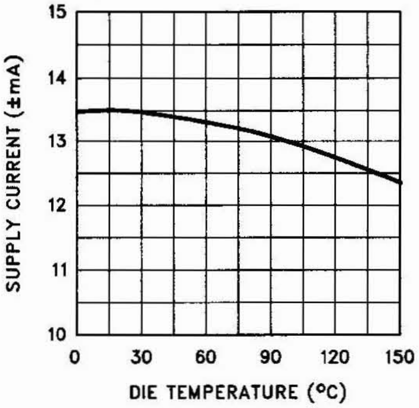


2090-8

Supply Current vs Supply Voltage



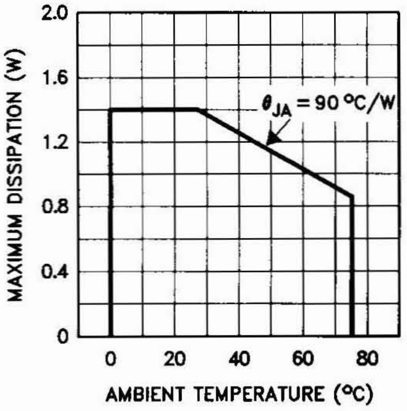
Supply Current vs Temperature; V_S = ±15V



2090-9

Typical Performance Curves — Contd.

Maximum Power Dissipation vs Ambient Temperature— 14-Pin PDIP and 16-Pin SOL



2090-10

Applications Information

The EL2090C is a general purpose component and thus the video amplifier and sample-and-hold pins are uncommitted. Therefore much of the ultimate performance as a DC-restored video amplifier will be set by external component values and parasitics. Some application considerations will be offered here.

The DC feedback from the sample-and-hold can be applied to either positive or negative inputs of the video amplifier (with appropriate phasing of the sample-and-hold amplifier inputs). We will consider feedback to the inverting video input. During a sample mode (the HOLD input at a logic low), the sample-and-hold acts as a simple nulling op-amp.

Ideally, the DC feedback resistor Raz is a high value so as not to couple a large amount of the AC signal on the video input back to the sample-and-hold amplifier output. The sample-and-hold output is a low impedance at high frequencies, but variations of the DC operating point will change the output impedance somewhat. No more than a few ohms output impedance change will occur, but this can cause gain variations in the 0.01% realm. This DC-dependent gain change is in fact a differential gain effect. Some small differential phase error will also be added. The best approach is to maximize the DC feedback resistor value so as to isolate the sample-and-hold from the video path as much as possible. Values of 1 kΩ or above for Raz will cause little to no video degradation. This suggests that the largest applicable power supply voltages be used so that the output swing of the sample-and-hold can still correct for the variations of DC offset in the video input with large values of Raz. The typical application circuit shown will allow correction of ±1V inputs with good isolation of the sample-and-hold output. Good isolation is defined as no video degradation due to the insertion of the sample-and-hold loop. Lower supply voltages will require a smaller value of DC feedback resistor to retain correction of the full input DC variation. The EL2090 differential phase performance is optimum at ±9V supplies, and differential gain only marginally improves above this voltage. Since all video characteristics mildly degrade with increasing die temperature, the ±9V levels are somewhat better than ±15V supplies. However, ±15V supplies are quite usable.

Ultimate video performance, especially in HDTV applications, can also be optimized by setting the black-level reference such that the signal span at the video amplifier's output is set to its optimum range. For instance, setting the span to ±1V of output is preferable to a span of 0V to +2V. The curves of differential gain and phase versus input DC offset will serve as guides.

The DC feedback resistor may be split so that a bypass capacitor is added to reduce the initially small sample-and-hold transients to even smaller levels. The corruption can be reduced to as low as 1 mV peak seen at the video amplifier output. The size of the capacitor should not be so large as to de-stabilize the sample-and-hold feedback loop, nor so small as to reduce the video amplifier's gain flatness. A resistor or some other video isolation network should be inserted between the video amplifier output and the sample-and-hold input to prevent excessive video from bleeding through the autozero section, as well as preventing spurious DC correction due to video signals confusing the sample-and-hold during autozero events. Figure 1 shows convenient component values. A full 3.58 MHz trap is not necessary for suppressing NTSC chroma burst interaction with the sample-and-hold input; the simple R-C network suggested in Figure 1 suffices.

Applications Information — Contd.

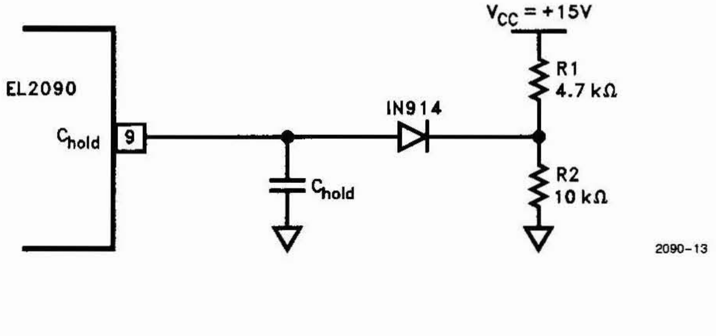
The HOLD input to the sample-and-hold has a 1.4V threshold and is clamped to a diode below ground and 6V above ground. The hold step characteristics are not sensitive to logic high nor low levels (within TTL or CMOS swings), but logic slewrates greater than 1000V/μs can couple noise and hold step into the sample-to-hold output waveforms. The logic slewrate should be greater than 50V/μs to avoid hold jitter. To avoid artificially high droop in hold mode, the Chold pin and Chold itself should be guarded with circuit board traces connected to the output of the sample-and-hold. Low-leakage hold capacitors should be used, such as mica or mylar, but not ceramic. The excellent properties of more expensive polystyrene, polypropylene, or teflon capacitors are not needed.

The user should be aware of a combination of conditions that may make the EL2090 operate incorrectly upon power-up. The fault condition can be described by noticing that the sample-and-hold output (pin 11) appears locked at a voltage close to V_{CC}. This voltage is maintained regardless of changes at the inputs to the sample-and-hold (pins 5 and 6) or to the HOLD control input (pin 7). Two conditions must occur to bring this about:

1. A large value of Chold—usually values of 1000 pF or more. This is not an unusual situation. Many users want to reduce the size of the hold step and increasing Chold is the most direct way to do this. Increasing Chold also reduces the slew rate of the sample and hold section but because of the limited size of the video signal, this is usually not a limitation.
2. A sampling interval (dictated by the HOLD pin) that is too small. By small, we mean less than 2 μs.

For a sampling interval that is wide enough, there is enough time for the loop to close and for the amplifier to discharge whatever charge was dumped onto Chold it during the initial power spike and to then ramp up (or down) to the voltage that is proper for a balanced loop. When the sampling interval is too small, there is insufficient time for internal devices to recover from their initial saturated state from power-up because the feedback is not closed long enough. Therefore, typical recovery times for the loop are 2 μs or greater. Summarizing, the two things that could prevent proper saturation recovery are (as mentioned above) too large a capacitor which slows the charge and discharge rate of the stored voltage at Chold and too small a sampling interval in which the entire feedback loop is closed.

The circuit shown below prevents the fault condition from occurring by preventing the node from ever saturating. By clamping the value of Chold to some value lower than the supply voltage less



Applications Information — Contd.

a saturation voltage, we prevent this node from approaching the positive rail. The maximum voltage is set by the resistive voltage divider (between V+ and GND) R1 and R2 plus a diode. This value can be adjusted if the maximum size of the input signal is known. The diode used is an off-the-shelf 1N914 or 1N916.

As is true of all 100 MHz amplifiers, good bypassing of the supplies to ground is mandatory. 1 μF tantalums are sufficient, and 0.01 μF leaded chip capacitors in parallel with medium value electrolytics are also good. Leads longer than ½ can induce a characteristic 150 MHz resonance and ringing.

The V_{IN-} of the video amplifier should have the absolute minimum of parasitic capacitance. Stray capacitance of more than 3 pF will cause peaking and compromise the gain flatness. The bandwidth of the amplifier is fundamentally set by the value of Rf. As demonstrated by the frequency response versus gain graph, the peaking and bandwidth is a weak function of gain. The EL2090 was designed for Rf = 300Ω giving optimum gain flatness at Av = +2. Unity-gain response is flattest for Rf = 360Ω; gains of +5 can use Rf = 270Ω. In situations where the peaking is accentuated by load capacitance or −input capacitance the value of Rf will have to be increased, and some bandwidth will be sacrificed.

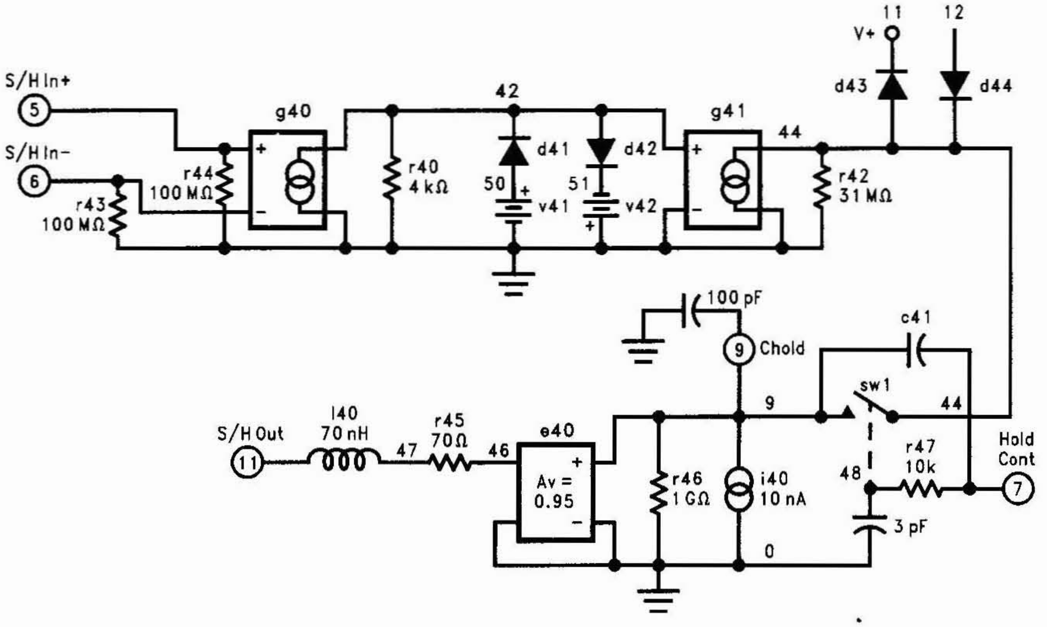
The V_{IN+} of the video amplifier should not look into an inductive source impedance. If the source is physically remote and a terminated input line is not provided, it may be necessary to connect an input "snubber" to ground. A snubber is a resistor in series with a capacitor which de-Q's the input resonance. Typical values are 100Ω and 30 pF.

The output of the video amplifier is sensitive to capacitive loads greater than 25 pF, and a snubber to ground or a resistor in series with the output is useful to isolate reactive loads.

EL2090 Macromodel

```
* Revision A, October 1992
.param vclamp = {-0.002 * (TEMP-25)}
*
* Connections:      Vidin+
*                   |    Vidin-
*                   |    |    +Vsupply
*                   |    |    |    -Vsupply
*                   |    |    |    |    Vid Out
*                   |    |    |    |    |    S/H In+
*                   |    |    |    |    |    |    S/H In-
*                   |    |    |    |    |    |    |    S/H Out
*                   |    |    |    |    |    |    |    |    Hold Control
*                   |    |    |    |    |    |    |    |    |    Chold
*                   |    |    |    |    |    |    |    |    |    |
.subckt EL2090/EL   3    1    14   12   13   5    6    11   7    9
*
******** Video Amplifier *******************
*
e1 20 0 3 0 1.0
vis 20 34 0V
h2 34 38 vxx 1.0
r10 1 36 25
l1 36 38 20nH
iinp 3 0 10µA
iinm 1 0 5µA
h1 21 0 vis 600
r2 21 22 1K
d1 22 0 dclamp
d2 0 22 dclamp
e2 23 0 22 0 0.00166666666
l5 23 24 0.7µH
c5 24 0 0.5pF
r5 24 0 600
g1 0 25 24 0 1.0
rol 25 0 400K
cdp 25 0 7.7pF
q1 12 25 26 qp
q2 14 25 27 qn
q3 14 26 28 qn
q4 12 27 29 qp
r7 28 13 4
r8 29 13 4
ios1 14 26 2.5mA
ios2 27 12 2.5mA
ips 14 12 7.2mA
ivos 0 33 5mA
vxx 33 0 0V
r11 33 0 1K
*
************ Sample & Hold *************************
*
g40 49 0 5 6 1e-3
vcur 49 42 0v
r43 6 0 100Meg
r44 5 0 100Meg
r40 42 0 4K
d41 50 42 diode
d42 42 51 diode
v41 50 0 {vclamp}
v42 0 51 {vclamp}
g41 44 0 42 0 200e-6
r42 44 0 31Meg
d45 9 14 diode
d46 12 9 diode
s1 44 9 48 0 swa
e40 46 0 9 0 0.95
i40 0 9 10nA
r45 46 47 70
l40 47 11 70nH
c40 7 9 0.32pF
r47 7 48 10K
c41 48 0 3pF
*
* Models
*
.model qn npn(is=5e-15 bf=500 tf=0.1nS)
.model qp pnp(is=5e-15 bf=500 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.02 bv=2.75 n=4)
.model diode d
.model swa vswitch(von=1.2v voff=1.6v roff=1e12 ron=100)
.ends
```

EL2090 Macromodel — Contd.

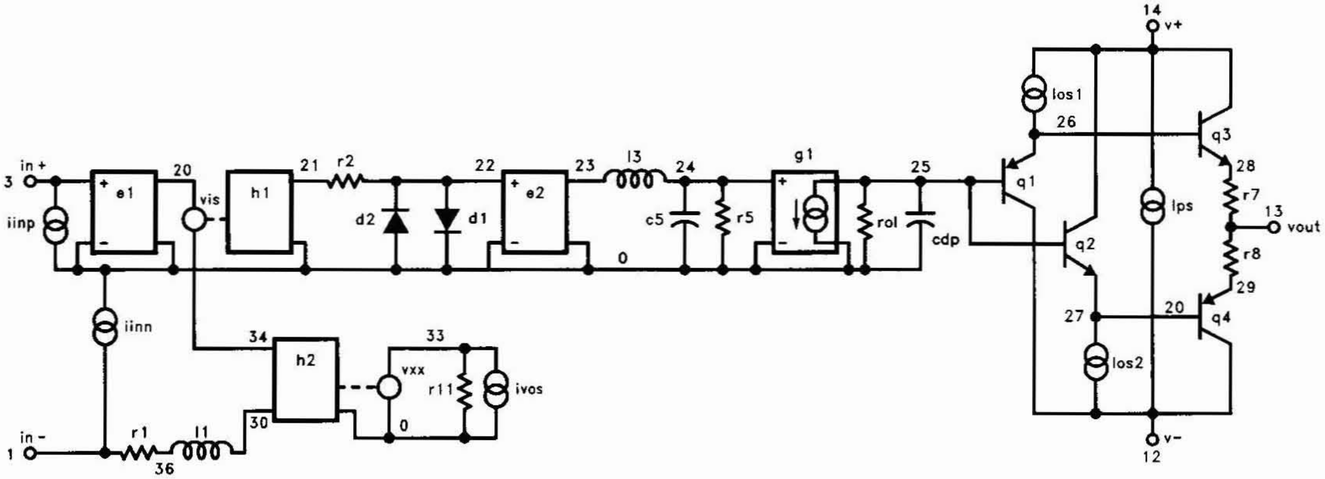

S/H In+
5
S/H In−
6
r44
100 MΩ
r43
100 MΩ
g40
+
−
42
r40
4 kΩ
d41
50
+
v41
51
d42
+
v42
g41
+
−
44
r42
31 MΩ
11
V+
12
d43
d44
100 pF
9
Chold
c41
sw1
9
44
S/H Out
11
l40
70 nH
47
r45
70Ω
46
e40
Av =
0.95
+
−
r46
1 GΩ
i40
10 nA
48
r47
10k
Hold
Cont
7
3 pF
0

2090-15

Sample and Hold Amplifier

3

EL2090 Macromodel — Contd.


in +
3
iinp
e1
+
-
20
vis
h1
21
r2
d2
d1
22
e2
+
-
23
l3
24
c5
r5
g1
+
-
rol
25
cdp
0
iinn
34
h2
33
vxx
r11
ivos
0
30
in -
1
r1
l1
36
14
v+
Ios1
26
q3
q1
28
r7
Ips
13
vout
q2
r8
29
27
20
q4
Ios2
v-
12

2090-14

Video Amplifier

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4083C

Current Mode Four Quadrant Multiplier

December 1995 Rev B

3

Features

- Novel current mode design
  Virtual ground current summing inputs
  Differential ground referenced current outputs
- High speed (both inputs)
  200 MHz bandwidth
  12 ns 1% settling time
- Low distortion
  THD < 0.03% @ 1 MHz
  THD < 0.1% @ 10 MHz
- Low noise ($R_L = 50\Omega$)
  100 dB dynamic range
  10 Hz to 20 kHz
  73 dB dynamic range
  10 Hz to 10 MHz
- Wide supply conditions
  ±5 to ±15V operation
  Programmable bias current
- 0.2 dB gain tolerance to 25 MHz

Applications

- Four quadrant multiplication
- Gain control
- Controlled signal summing and multiplexing
- HDTV video fading and switching
- Mixing/modulating/demodulating (phase detection)
- Frequency doubling
- Division
- Squaring
- Square rooting
- RMS and power measurement
- Vector addition-RMS summing
- CRT focus and geometry correction
- Polynomial function generation
- AGC circuits

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL4083CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL4083CS	−40°C to +85°C	8-Pin SO	MDP0027

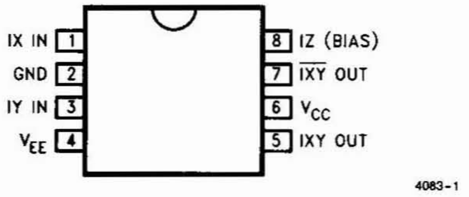
General Description

The 4083C makes use of an Elantec fully complimentary oxide isolated bipolar process to produce a patent pending current in, current out four quadrant multiplier. Input and output signal summing and direct interface to other current mode devices can be accomplished by simple connection to reduce component count and preserve bandwidth. The selection of an appropriate series resistor value allows an input to accept a voltage signal of any size and optimize dynamic range. The differential outputs offer significant performance improvements which greatly extend the usable gain control range at high frequencies. The bias current is programmable to accommodate the voltage and power dissipation constraints of the package and available systems supplies.

The devices can implement all the classic four quadrant multiplier applications and are uniquely well suited to gain control and signal summing of broadband signals.

Connection Diagram

EL4083
8-Pin SO/P DIP



Top View

Manufactured under U.S. Patent No. 5,389,840

EL4083C

Current Mode Four Quadrant Multiplier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V_S+ and V_S-	+33V
$I_{Z(BIAS)}$	Z, Bias Current	+2.4 mA
I_X	X Input Current	±2.4 mA
I_Y	Y Input Current	±2.4 mA
P_D	Maximum Power Dissipation	See Curves
T_A	Operating Temperature Range	
	EL4083	−40°C to +85°C
T_J	Operating Junction Temperature	
	EL4083	150°C
T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics (T_A = 25°C, V_S = ±5, I_Z = 1.6 mA) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Test Level	Units
Power Supplies						
Operating Supply Voltage Range		±4.5		±16.5	I	V
I_{CC}	V_S = ±15V, I_Z = 0.2 mA	7.2	8.5	9.5	I	mA
I_{CC}	V_S = ±5V, I_Z = 1.6 mA	42.0	44.0	45	I	mA
I_{EE}	V_S = ±15V, I_Z = 0.2 mA	9.5	10.0	12	I	mA
I_{EE}	V_S = ±5V, I_Z = 1.6 mA	45	47	48	I	mA
Multiplier Performance						
Transfer Function (Note 5)	$(I_{XY} - I_{\overline{XY}}) = K(I_X \times I_Y)/I_Z$					
K Value		0.92	0.965	1.01	I	
Total Error (Note 1)	-2 mA < I_X, I_Y < 2 mA		±0.5	±2	I	%FS
vs. Temp	T_{MIN} to T_{MAX}		±1.5	±3	IV	%FS
Linearity (Note 2)			0.25	0.5	I	%FS
Bandwidth (Note 3)	−3 dB (See Figure 2)	200	225		III	MHz
X Feedthrough DC to I_{XY} or $I_{\overline{XY}}$ (Note 5)	I_X = ±2 mA, I_Y = 0 (unnulled)		0.15	1.6	I	%FS
Y Feedthrough DC to I_{XY} or $I_{\overline{XY}}$ (Note 5)	I_Y = ±2 mA, I_X = 0 (unnulled)		0.15	1.6	I	%FS
AC Feedthrough, X to I_{XY} or $I_{\overline{XY}}$ (Note 4)	I_X = 4 mApp, I_Y = nulled					
	f = 3.58 MHz		−80		V	dB
	f = 100 MHz		−28		V	dB
AC Feedthrough, X to $(I_{XY} - I_{\overline{XY}})$ (Note 4)	I_X = 4 mApp, I_Y = nulled DC < f < 1 GHz		−50		V	dB
AC Feedthrough, Y to I_{XY} or $I_{\overline{XY}}$ (Note 4)	I_Y = 4 mApp, I_X = nulled					
	f = 3.58 MHz		−64		V	dB
	f = 100 MHz		−26		V	dB
AC Feedthrough, Y to $(I_{XY} - I_{\overline{XY}})$ (Note 4)	I_Y = 4 mApp, I_X = nulled					
	DC < f < 1 GHz		−50		V	dB

Electrical Characteristics — Contd. (T_A = 25°C, V_S = ±5, I_Z = 1.6 mA) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Test Level	Units
Inputs (I_X, I_Y)						
Full Scale Range	FRS = 1.25 × I_Z (Nominal)		±2		I	mA
Clipping Level	$C_L = 2 \times I_Z$	2.85	3.2		I	mA
Z_{IN} (I_X)		30	40	48	I	Ω
Z_{IN} (I_Y)		30	36	48	I	Ω
Input Offset Voltages	at Input Pins, I_Z = 1.6 mA	−4		+4		mV
(V_{OSX},V_{OSY})	I_Z = 0.2 mA	−12		+12		mV
Input Offset Currents (Note 5)	$R_{SX} = R_{SY}$ = 1K, $V_X = V_Y = 0$,		±10	±40	I	μA
I_{XOS}, I_{YOS}	T_{MIN} to T_{MAX}		±20		V	nA/°C
Nonlinearity						
I_X	I_Y = 2 mA, − 2 mA < I_X < 2 mA		0.1	0.6	I	%FS
I_Y	I_X = 2 mA, − 2 mA < I_Y < 2 mA		0.1	0.4	I	%FS
Distortion, I_X (to I_{XY} or $I_{\overline{XY}}$)	I_Y = 2 mA, − 2 mA < I_X < 2 mA					
	f = 3.58 MHz		−55		V	dB
	f = 100 MHz		−25		V	dB
Distortion, I_Y (to I_{XY} or $I_{\overline{XY}}$)	I_X = 2 mA, − 2 mA < Iy < 2 mA					
	f = 3.58 MHz		−56		V	dB
	f = 100 MHz		−26		V	dB
Distortion, I_X (to ($I_{XY} - I_{\overline{XY}}$)	I_Y = 2 mA, −2 mA < I_X < 2 mA					
	f = 3.58 MHz		−66		V	dB
	f = 100 MHz		−35		V	dB
Distortion, I_Y (to ($I_{XY} - I_{\overline{XY}}$)	I_X = 2 mA, −2 mA < I_Y < 2 mA					
	f = 3.58 MHz		−66		V	dB
	f = 100 MHz		−34		V	dB
Diff Gain	@3.58 MHz					
I_X	I_Z = 0.2 mA, I_Y = 0.25 mA		0.2		V	%
I_Y	I_Z = 0.2 mA, I_X = 0.25 mA		0.17		V	%
I_X	I_Z = 1.6 mA, I_Y = 2 mA		0.1		V	%
I_Y	I_Z = 1.6 mA, I_X = 2 mA		0.05		V	%
Diff Phase	@3.58 MHz					
I_X	I_Z = 0.2 mA, I_Y = 0.25 mA		0.5		V	deg °
I_Y	I_Z = 0.2 mA, I_X = 0.25 mA		0.5		V	deg °
I_X	I_Z = 1.6 mA, I_Y = 2 mA		0.05		V	deg °
I_Y	I_Z = 1.6 mA, I_X = 2 mA		0.05		V	deg °
Outputs (I_{XY}, I_{YX})						
Output I_{OS} (Note 5)	$I_X = I_Y = 0$		−15	±120	I	μA
Diff Output I_{OS} (Note 5)	$I_X = I_Y = 0$, (I_{XY}−$I_{\overline{XY}}$)		±0.1	±80	I	μA
Voltage Compliance		±1.5	±2.0		V	V
Max Output Current Swing		±2.85	±3.2		I	mA
Noise Spectral Density						
10 Hz < f < 10 MHz	R_L = 50Ω		125		V	pA/rootHz
I_Z (Bias)						
Current Range	Tested	0.2		1.6	I	mA
Input Voltage	I_Z = 0.2 mA			±25	I	mV
Input Voltage	I_Z = 1.6 mA			±25	I	mV

Note 1: Error is defined as the maximum deviation from the ideal transfer function expressed as a percentage of the full scale output.

Note 2: Linearity is defined as the error remaining after compensating for scale factor (gain) variation and input and output referred offset errors.

Note 3: Bandwidth is guaranteed using the squaring mode test circuit of Figure 4.

Note 4: Relative to full scale output with full scale sinewave on signal input and zero port input nulled. Specification represents feedthrough of the fundamental.

Note 5: Specifications are provisional for the EL4083.

EL4083 Block Diagram

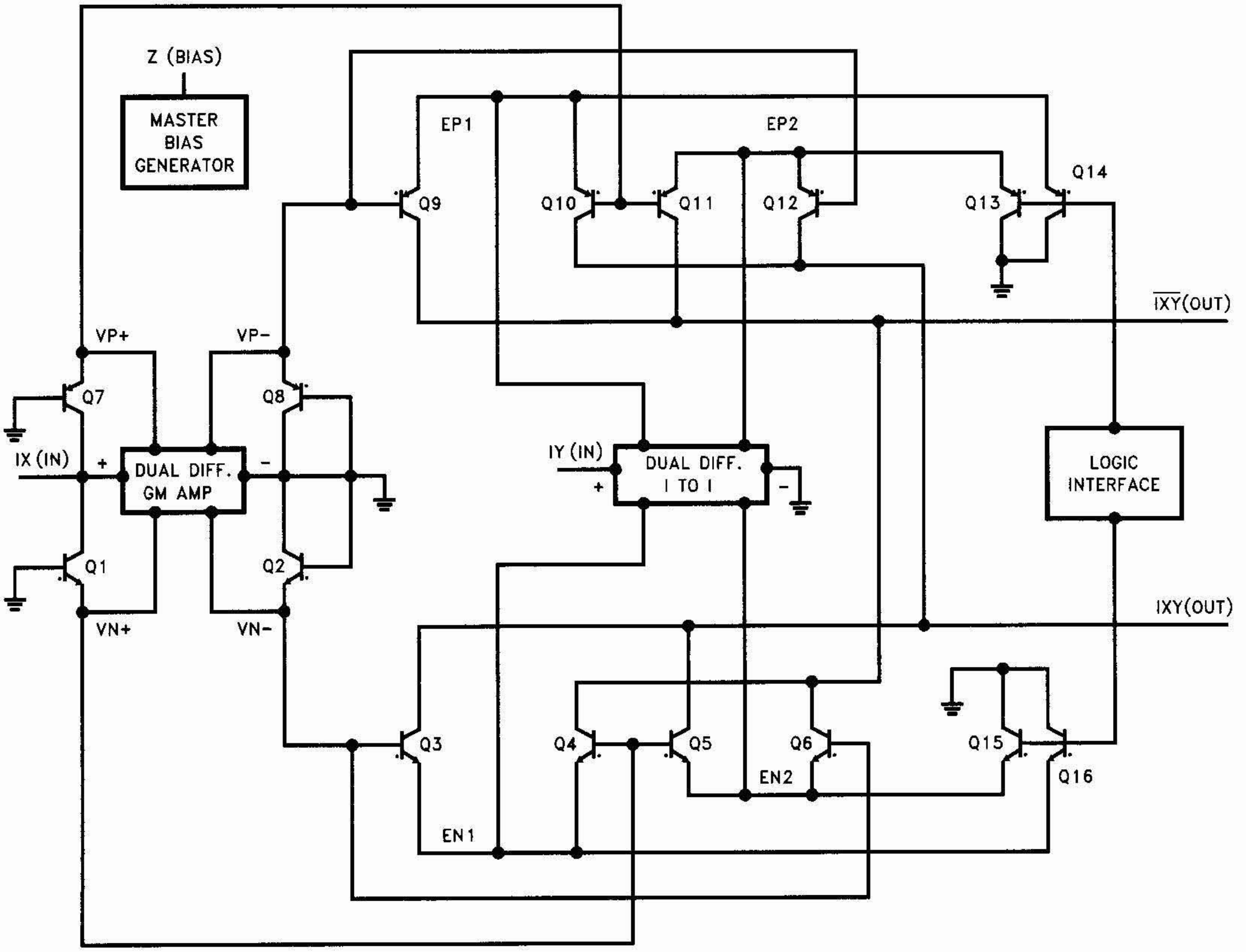
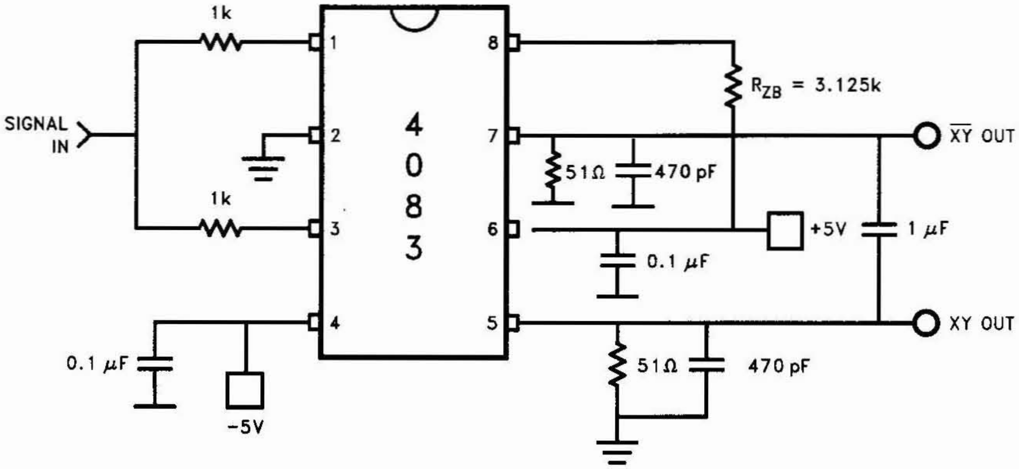

Z (BIAS)
MASTER BIAS GENERATOR
EP1
EP2
Q9
Q10
Q11
Q12
Q13
Q14
IXY(OUT)
VP+
VP−
Q7
Q8
IX (IN)
+
DUAL DIFF. GM AMP
−
Q1
Q2
VN+
VN−
IY (IN)
+
DUAL DIFF. I TO I
−
LOGIC INTERFACE
IXY(OUT)
Q3
Q4
Q5
Q6
EN2
Q15
Q16
EN1
4083-3

Figure 1

AC Test Fixture


1k
1k
SIGNAL IN
1
2
3
4
8
7
6
5
4083
R_{ZB} = 3.125k
51Ω
470 pF
$\overline{XY}$ OUT
+5V
1 µF
0.1 µF
XY OUT
0.1 µF
-5V
51Ω
470 pF

4083-4

Figure 2. AC Bandwidth Test Fixture

Burn-In Circuit

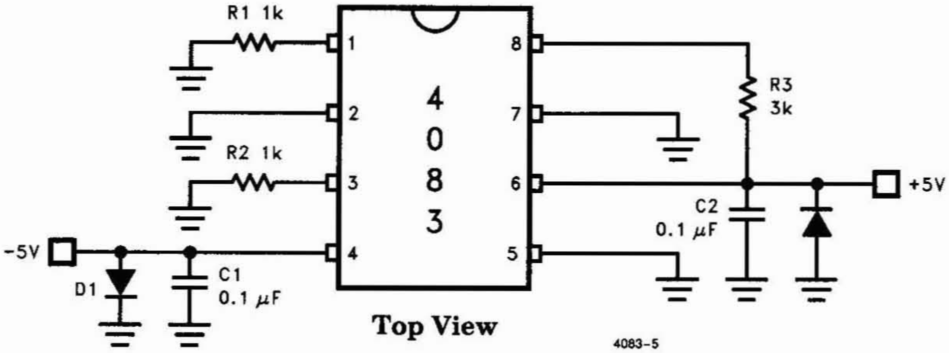
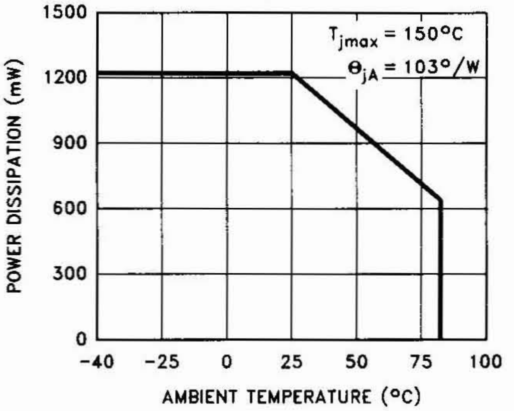
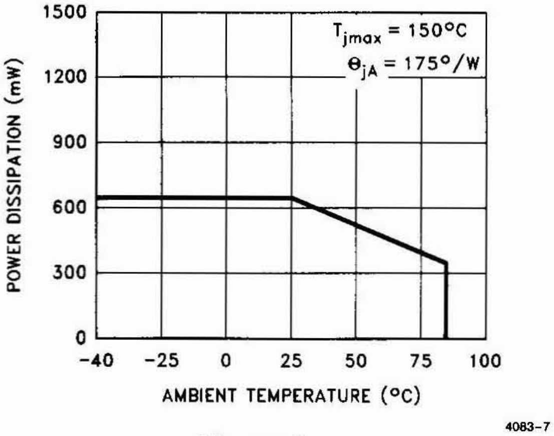

R1 1k
R2 1k
1
2
3
4
8
7
6
5
4083
R3
3k
C2
0.1 µF
+5V
-5V
D1
C1
0.1 µF
Top View
4083-5

Figure 3. Burn-In Circuit P-DIP



8-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

Figure 4



8-Lead SO
Maximum Power Dissipation
vs Ambient Temperature

Figure 5

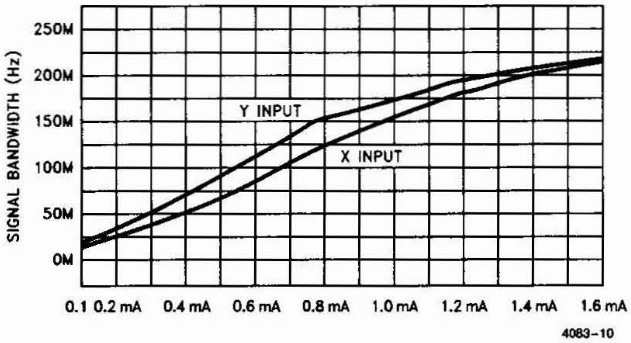


Figure 6. (I_X, I_Y Bandwidth vs I_Z)

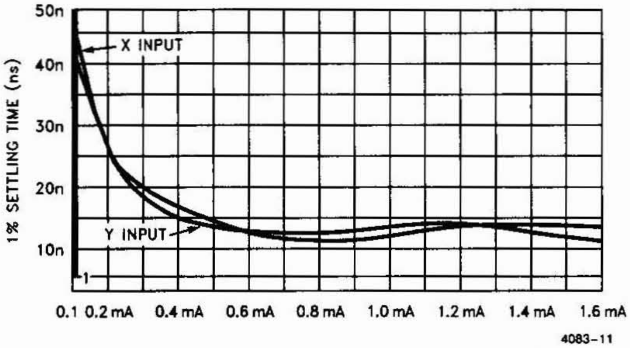
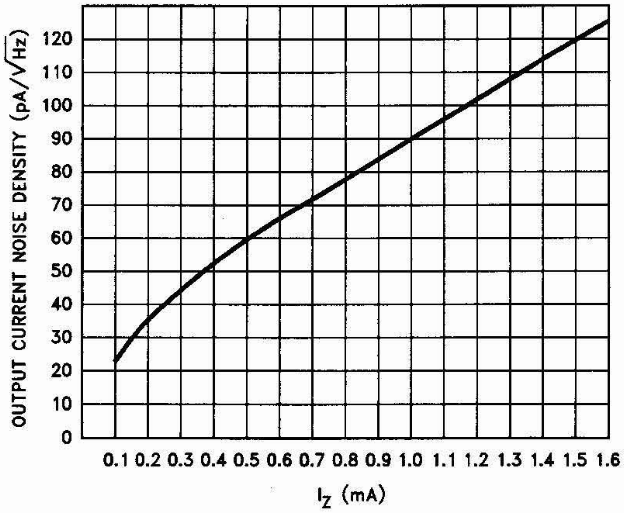
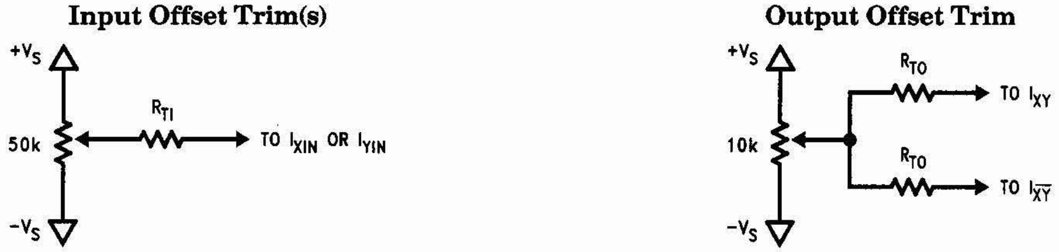


Figure 7. (I_X, I_Y 1% Settling Time vs I_Z)



4083-12

Figure 8. Output Noise Density vs I_Z Bias


Input Offset Trim(s)
+V_S
R_{TI}
50k
TO I_{XIN} OR I_{YIN}
−V_S
Output Offset Trim
+V_S
R_{TO}
TO I_{XY}
10k
R_{TO}
TO $I_{\overline{XY}}$
−V_S

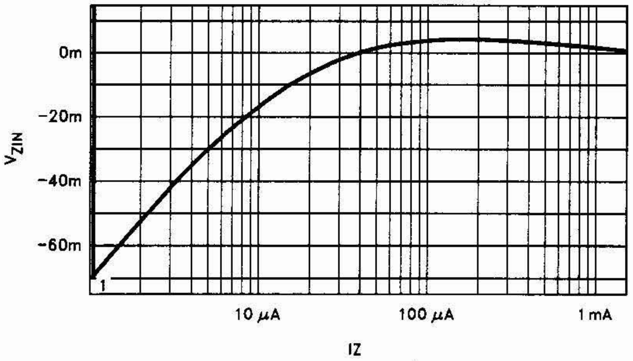
4083-13

4083-14

$R_{TI} = (V_S \times 1.6\ \text{mA})/(16\ \mu\text{A} \times I_Z)$

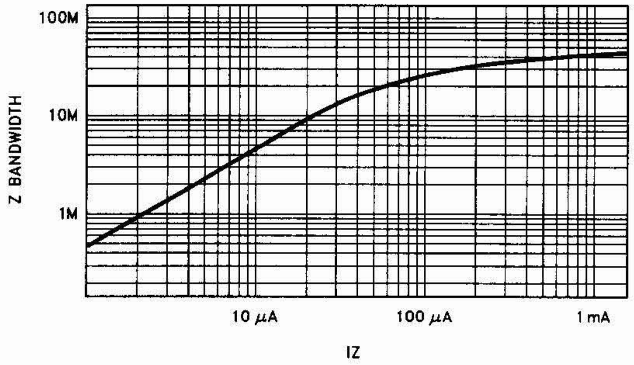
$R_{TO} = (V_S \times 1.6\ \text{mA})/(30\ \mu\text{A} \times I_Z)$

Figure 9. Optional External Trim Networks



4083-15

Figure 10. V_{ZIN} vs I_Z (Typical)



4083-16

Figure 11. I_{ZIN} Bandwidth vs I_Z

General Operating Information

I_Z Input (Bias, Divisor) and Power Supplies

The I_Z pin is a low impedance ($<20\Omega$) virtual ground current input. It can accept positive current from a resistor connected to a positive voltage source or the positive supply. The instantaneous bias for the multiplier gain core is proportional to this current value. Negative applied current will put the multiplier portion of the circuit in a zero bias state and the voltage at the pin will be clamped at a diode drop below ground. The part will respond in a similar manner to currents from a current source such as the output of a transconductance amplifier or one of its own outputs. The overall transfer equation for the EL4083 is:

$K(I_X \times I_Y)/I_Z = (I_{XY} - I_{\overline{XY}})$, $K \sim 1$

As can be seen from the equation, the Z input can serve as a divisor input. However, it is different from the other two inputs in that the value of its current determines the supply current of the part and the bandwidth and compliance range of the outputs and other two inputs. Table 1 gives the equations describing these and other important relationships. These dependencies can complicate and/or limit the usefulness of this pin as a computational input. The I_Z dependence of the impedance of the multiplying inputs can be particularly troublesome. See the I_Z divider and the RMS #2 circuit sections of the application note for some ways of dealing with this.

The primary intended use for the Z input is as a programming pin similar in function to those on programmable op amps. This enables one to trade off power consumption against bandwidth and settling time and allow the part to function within its power dissipation rating over its full operational supply range ($\pm 4.5V$ – $\pm 16.5V$). The E4083 has been designed to function well for I_Z values in the range of $200\ \mu A < I_Z < 1.6$ mA which corresponds to I_X and I_Y signal bandwidths of about 50 MHz to over 200 MHz. Higher values of I_Z may cause problems at temperature extremes while lower values down to zero will progressively degrade the input referred D.C. offsets and reduce speed. Below about 50 μA of bias current the internal servo amplifier loop which maintains the I_Z pin at ground will lose regulation and the voltage at the pin will start to move negative (see Figure 10). This is accompanied by a significant increase in input impedance of the pin. Figure 11 shows the A.C. bandwidth of the I_Z input as a function of the D.C. value of I_Z. Figures 6 and 7 show the bandwidth and 1% settling time of the multiplying inputs, I_X and I_Y, as functions of I_Z.

I_X and I_Y (Multiplier) Inputs and Offset Trimming

The I_X and I_Y pins are low impedance (I_Z dependent) virtual ground current inputs that accept bipolar signals. The input referred clip value is equal to $I_Z \times 2$ while the full scale value has been chosen to be $1.25 \times I_Z$ to maintain excellent distortion and linearity performance. Operating at higher full scale values will degrade these two pa-

Table 1. Basic Design Equations and Relationships

Positive Supply Current	$I_S+ = 3.4\text{ mA} + I_Z \times 26$
Negative Supply Current	$I_S- = 4.5\text{ mA} + I_Z \times 27$
Power Dissipation (See Figures 4 and 5)	$PWR = (+V_S - (-V_S)) \times (4\text{ mA} + I_Z \times 26.5)$
Multipling Input(s) Impedance	$R_{ZX} = R_{ZY} = (32\Omega) \times 1.6\text{ mA}/I_Z$
Multiplying Input(s) Clip Point	$I_X\text{ (clip)} = I_Y\text{ (clip)} = I_Z \times 2$
Multiplying Input(s) Full Scale Value	$I_X\text{ (fs)} = I_Y\text{ (fs)} = I_Z \times 1.25$ (nominal)
Multiplying Input Resistor Values (In Terms of Peak Input Signal)	$R_X = V_X\text{ (peak)}/I_X\text{ (fs)}$ $R_Y = V_Y\text{ (peak)}/I_Y\text{ (fs)}$
Full Scale Output (Single Ended)	$I_{XY} = I_{\overline{XY}} = I_X\text{ (fs)} \times I_Y\text{ (fs)}/(I_Z \times 2)$
Full Scale Output (Differential)	$(I_{XY} - I_{\overline{XY}}) = I_X\text{ (fs)} \times I_Y\text{ (fs)}/I_Z$
I_Z (Bias) Input Voltage vs I_Z	(See Figure 10)
I_Z Signal Bandwidth vs I_Z	(See Figure 11)
I_X, I_Y Signal Bandwidth vs I_Z	(See Figure 6)
I_X, I_Y 1% Settling Time vs I_Z	(See Figure 7)

General Operating Information

— Contd.

rameters and, to some extent, bandwidth while improving the signal to noise performance, feedthrough and control range.

The EL4083 is fundamentally different from conventional voltage mode multipliers in that the available input range can be tailored to accommodate voltage sources of almost any size by selecting appropriate input series resistor values. If desired, one can interface with voltages that are much greater than the supplies from which the part is powered. Current source signals can be connected directly to the multiplier inputs. The parts' dynamic range can also be tailored to a large extent for a current signal by the appropriate selection of I_Z. These inputs act in the same manner as a virtual ground input of an operational amplifier and thus can serve as a summing node for any number of voltage and/or current signals. Outputs of components such as current output DACs, transconductance amplifiers and current conveyors can be directly connected to the inputs.

Ideally, a multiplier should give zero output if either one of its multiplying inputs is zero. A nonzero output under these conditions is caused by a combination of input and output referred offsets. An output referred offset can be thought of as a fixed value added to the output and thus only affects D.C. accuracy. An input referred offset at a multiplying input allows signal to feedthrough from the other multiplying input to the output(s). The EL4083 is trimmed during testing at Elantec for X and Y input referred offset for $I_Z = 1.6$ mA. The internal trim networks provide a current to each input which nulls the feedthrough caused by internal device mismatches. These current values are ratioed to the value of I_Z so that the input referred nulls are largely maintained at different values of I_Z. However, there will be some mistracking in the trim networks so that the input referred null point will deviate away from zero at values of I_Z lower than 1.6 mA. Figure 9 shows optional external input and output referred offset trim networks which can be used as needed to improve performance.

As mentioned, the output referred offset only affects D.C. accuracy which may not be an issue in A.C. applications. In gain control applications one may only need to null feedthrough with respect to the gain control input.

In gain control (VCA) applications the X input should be used as the control input and the signal applied to the Y input since it has slightly higher bandwidth and better linearity and distortion performance.

Current Outputs (I_{XY}, $I_{\overline{XY}}$), Feedthrough and Distortion

Another unique feature of the EL4083 is the differential ground referenced current output structure. These outputs can drive 50Ω terminated lines and reactive loads such as transformers, baluns, and LC tank and filter circuits directly.* Unlike low impedance follower buffers, these outputs do not interact with the load to produce ringing or instability. If a high level low impedance output is required, the outputs can be recovered differentially and converted to a single ended output with a fast op amp such as the EL2075 (see Figure 19). The outputs can also drive current input devices such as CMF amps, current conveyors and its own inputs directly by simple connection.

Figures 12 and 14 show the nulled gain and feedthrough characteristics of the I_{XY} and $I_{\overline{XY}}$ outputs which are virtually identical and differ only in phase. Figure 12 is with the A.C. signal applied to the X input with Y used as the gain control and in Figure 14 these signals are reversed. Note that in both cases the signal feedthrough rolls up and peaks near the cutoff frequency. This is quite typical of the performance of all previous four quadrant multipliers. Figures 13 and 15 show the corresponding gain/feedthrough characteristics for the differentially recovered output signal I_{XY}-$I_{\overline{XY}}$. Note that in this case the peak feedthrough at high frequencies is lower by more than 40 dB.

---

* See EL2082 Data Sheet—Receiver IF Amplifier (Figure 19). The EL2082 also has a current output.

General Operating Information

— Contd.

Figures 16 and 17 show the total harmonic distortion for the single-ended and differential recovered outputs for a full scale A.C. input signal on one input and a full scale D.C. control signal on the other. Note that above about one megahertz to the cutoff frequency the THD of the differentially recovered signal is as much as 10 dB lower than the single-ended signals.

General Operating Information — Contd.

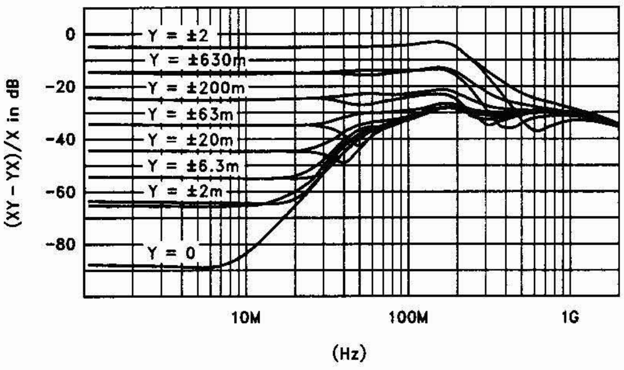


Figure 12. Nulled I_{XY} and $I_{\overline{XY}}$ Frequency Response (Signal on XIN, Gain Controlled by YIN)

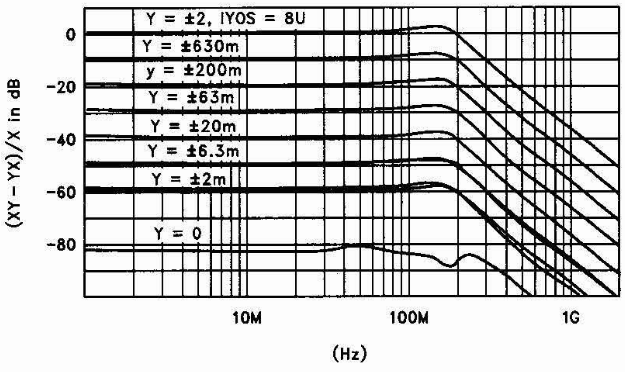


Figure 13. Nulled (I_{XY}-$I_{\overline{XY}}$) Frequency Response (Signal on XIN, Gain Controlled by YIN)

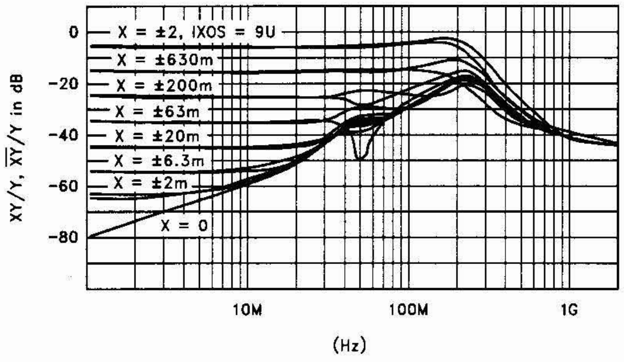


Figure 14. Nulled I_{XY} and $I_{\overline{XY}}$ Frequency Response (Signal on YIN, Gain Controlled by XIN)

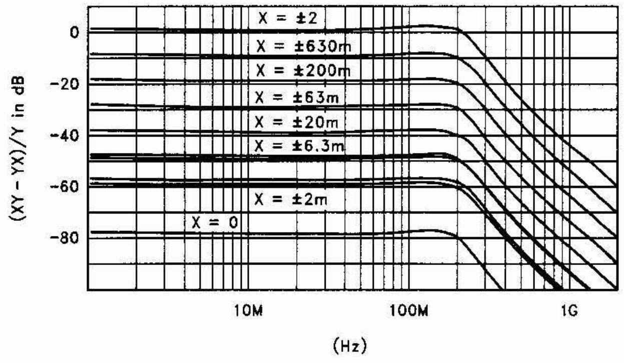


Figure 15. Nulled (I_{XY}−$I_{\overline{XY}}$) Frequency Response (Signal on YIN, Gain Controlled by XIN)

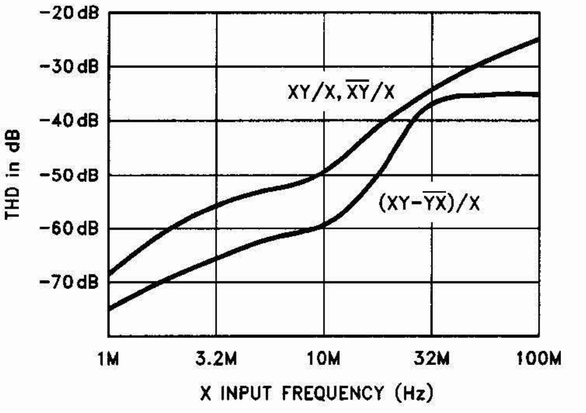


Figure 16. (Full Level XIN THD vs Frequency)

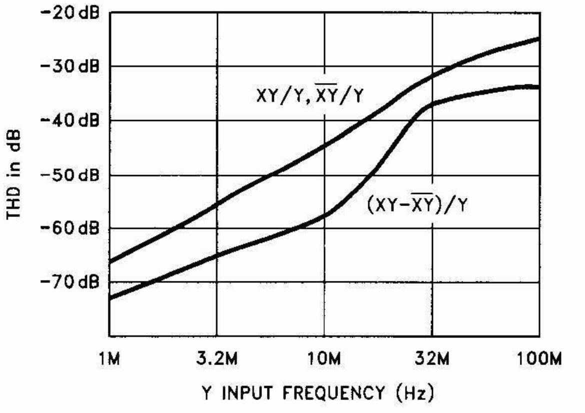


Figure 17. (Full Level YIN THD vs Frequency)

EL4083C

Current Mode Four Quadrant Multiplier

Applications

Basic Product Functions

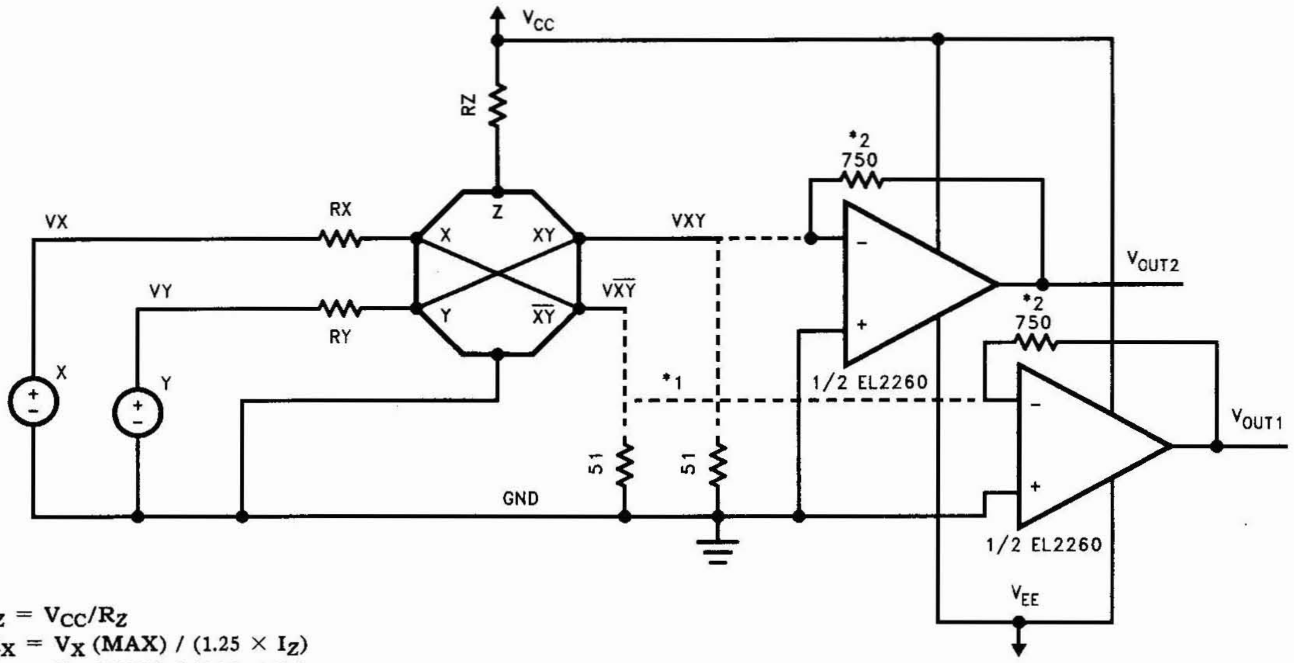
Figures 18 and 19 are the basic schematics for many of the applications of the EL4083. These can perform signal mixing, frequency doubling, modulation, demodulation, gain control/voltage-controlled amplification, multiplication and squaring. Figure 18 has resistively terminated differential outputs and has the widest bandwidth. The figure also shows the option of using the EL2260 dual CMF amplifier to recover the outputs differentially at very low impedance. This has a maximum 3 dB bandwidth of 130 MHz and settles to 1% in 25 ns. Figure 19 uses an EL2075 at the outputs as a differential to single ended converter with gain to take advantage of the performance enhancements of the differentially recovered output mentioned above and to provide a high level low impedance drive. The −3 dB bandwidth of this circuit is over 150 MHz using good layout techniques. However, to achieve this bandwidth one must restrict the output swing to little more than 1 Vpp to avoid running into the 500V/µs minimum slew rate of the EL2075. Table 2 shows the input signal assignments for the applications listed above.

Table 2. Input Signal Assignments for Figures 18 and 19 Circuits

Application	V_X	V_Y
Mixer	Signal 1	Signal 2
Frequency Doubler	Signal	Signal
Modulator	Modulating Signal	Carrier
Demodulator	Local Oscillator	Modulated Signal
Gain Control/VCA	Gain Control	Signal
Multiplier	Signal 1	Signal 2
Squarer	Signal	Signal

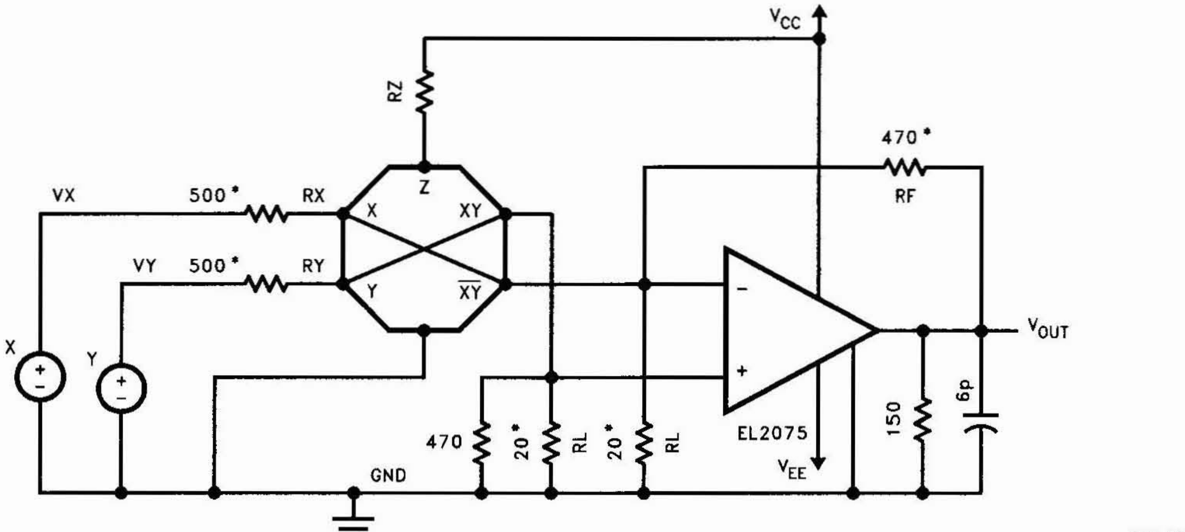
*X means not connected if function is not used.

Applications — Contd.


VCC
RZ
Z
VX
RX
X
XY
VXY
VY
RY
Y
$\overline{XY}$
$V\overline{XY}$
X
Y
*1
51
51
GND
*2
750
*2
750
VOUT2
VOUT1
1/2 EL2260
1/2 EL2260
VEE
4083-27

$I_Z = V_{CC}/R_Z$
$R_X = V_X\ (MAX) / (1.25 \times I_Z)$
$R_Y = V_Y\ (MAX) / (1.25 \times I_Z)$
*1. 51Ω Resistors omitted when using EL2260
*2. Optimum value of RF determined by supplies and amount or tolerable peaking
(−3 dB BW ~ 90 MHz @ V_S = ±5V, BW ~ 150 MHz @ ±15V)

Figure 18. Basic Schematic (Dual Diff Outs)


VCC
RZ
470*
RF
Z
VX
500*
RX
X
XY
VY
500*
RY
Y
$\overline{XY}$
X
Y
VOUT
470
20*
RL
20*
RL
EL2075
VEE
150
6p
GND
4083-28

$I_Z = V_{CC}/R_Z$
$R_X = V_X\ (MAX) / (1.25 \times I_Z)$
$R_Y = V_Y\ (MAX) / (1.25 \times I_Z)$
*Optimized for Wide Bandwidth

Figure 19. Basic Schematic (Single Ended Converted) (150 MHz VCA)

Other Applications

Elantec has also published an applications note covering other applications of the EL4083. These include dividers, squaring and square rooting circuits, several RMS and power measurement circuits, and a wideband AGC circuit. Also presented are two polynomial computation examples for video and some HDTV quality fader and summing circuits. The EL4083 has been found flexible enough to easily implement all of the classic four quadrant multiplier applications and also offer interesting new applications possibilities.

EL4083 Macromodel

This macromodel is compatible with PSPICE (copywritten by Microsim Corporation) . It has been designed to work accurately for fixed values of I_Z (bias) in the range of 200 μA to 1.6 mA. The additional simulation burden imposed by including provision for a time varying I_Z was thought not worthwhile. The value of I_Z is specified to the model by the parameter NS. The relation between I_Z and NS is; $I_Z = 200\ \mu A \times NS$. All other inputs can accept time varying signals.

The model will provide good transient and frequency response and settling time estimates as well as time domain switching results. Input and output impedance and overload responses are correctly modeled. The D.C. current drawn from supplies for a given value of I_Z is also correct.

Noise, PSRR and the temperature dependence of A.C. parameters such as frequency response and settling time are not modeled. Linearity and distortion results from the model will be worse than the real part by about a factor of three and do not show the correct frequency dependence.

The macromodel is constructed from simple controlled sources, passive components and stripped transistor and diode models. As such it should be usable, perhaps with slight modification, on all but student or demonstration simulators where the model's size may be a problem.

Macromodel

```
*EL4083 Macromodel
*Revision A, August 22, 1994
*
*Connection: IZ(BIAS)
*        |  IX(in)
*        |  |  IY(in)
*        |  |  |  VEE
*        |  |  |  |  VCC
*        |  |  |  |  |  IXY
*        |  |  |  |  |  |  /IXY
*        |  |  |  |  |  |  |
.subckt EL4083 ZIN XIN YIN VEE VCC IXY IYX
.MODEL M1MP5DIODE D TT=60p IS=1f CJO=300f
VJ=600m XTI=3 EG=1.11 RS=80m
.MODEL M2MDCAP D TT=100n IS=2e-17 CJO=1p
VJ=800m RS=300
.MODEL M3MNPN1 NPN CJC=1.3p TF=120p IS=1.04f
BF=120 CJS=480f
.MODEL M4MPNP1 PNP CJC=1.79p TF=50.166666666667p
IS=1f BF=90 CJS=480f
C1 N9 N7 9p
C2 N7 0 350f
C3 N19 N16 9p
C4 N16 0 350f
D1 0 N15 M2MDCAP 12
D10 0 N26 M1MP5DIODE 1
D11 N26 N27 M1MP5DIODE 1
D12 N29 N30 M1MP5DIODE 1
D13 0 N31 M1MP5DIODE 1
D14 VBP N34 M1MP5DIODE 2
D15 N34 VBP M1MP5DIODE 2
D16 0 N34 M2MDCAP 12.5
D17 N35 0 M2MDCAP 12.5
D18 N35 VBN M1MP5DIODE 2
D19 VBN N35 M1MP5DIODE 2
D2 N15 0 M2MDCAP 12
D20 N42 N10 M2MDCAP 4
D21 N10 0 M2MDCAP 4
D22 0 N20 M2MDCAP 4
D23 N20 N45 M2MDCAP 4
D3 0 N12 M1MP5DIODE 8
D4 N55 N13 M1MP5DIODE 8
D5 0 N25 M2MDCAP 6
D6 N25 0 M2MDECAP 6
D7 0 N22 M1MP5DIODE 8
D8 N54 N23 M1MP5DIODE 8
D9 0 N28 M1MP5DIODE 1
EV94 0 VBN 0 N45 1
```

Macromodel — Contd.

```
EV95 VBP 0 N42 0 1
EV96 N54 0 N21 0 650m
EV97 N55 0 N11 0 650m
EV98 N27 0 N28 0 1
EV99 N29 0 SWIN 0 1
FI10 VN-VEE VFI10 1
FI11 VCC VP-VFI11 1
FI12 VCC N39 VFI12 1
FI13 N37 VEE VFI13 1
FI14 VCC N38 VFI14 1
FI15 N36 VEE VFI15 1
FI16 N45 VEE VFI16 1
FI17 VCC N42 VFI17 1
FI18 N37 N36 VFI18 500m
FI19 N38 N39 VFI19 500m
FI20 VN+ VN- VFI20 500m
FI21 VP+ VP- VFI21 500m
FI22 0 N21 VFI22 1
FI23 N21 0 VFI23 1
FI24 N24 0 VFI24 2
FI25 N14 0 VFI25 2
FI26 N11 0 VFI26 1
FI27 0 N11 VFI27 1
FI28 VCC VEE VFI28 21
FI 29 N28 ZB1 VFI29 1
FI5 N33 0 VFI5 1
FI6 0 N33 VFI6 1
FI7 N35 N34 VFI7 1
FI8 VN+ VEE VFI8 1
FI9 VCC VP+ VFI9 1
IIBGN 0 VEE 2.2m
IIBGP VCC 0 2.46m
IIISWB N32 VEE 629u
IIISWI SWIN VEE 555u
IIZSU N28 VEE 10u
L1 N7 IXA 71n
L2 XIN N7 4n
L3 N16 IYA 71n
L4 YIN N16 4n
L5 N46 IYX 4n
L6 N47 IXY 4n
Q10 N10 VP+[VEE] M4MPNP1 2
Q10 N46 VN+ N36[VEE] M3MNPN1 2
Q11 N47 VN+ N37 [VEE] M3MNPN1 2
Q12 N46 VN- N37 [VEE] M3MNPN1 2
Q13 0 N34 N56 [VEE] M4MPNP1 400m
Q14 0 N34 N57 [VEE] M4MPNP1 400m
Q15 0 N35 N58 [VEE] M3MNPN1 400m
Q16 0 N35 N59 [VEE] M3MNPN1 400m
Q2 0 N10 VP- [VEE] M4MPNP1 2
Q3 0 N20 VN+ [VEE] M3MNPN1 2
Q4 0 N20 VN- [VEE] M3MNPN1 2
Q5 N46 VP- N39 [VEE] M4MPNP1 2
Q6 N47 VP+ N39 [VEE] M4MPNP1 2
Q7 N46 VP+ N38 [VEE] M4MPNP1 2
Q8 N47 VP- N38 [VEE] M4MPNP1 2
Q9 N47 VN- N36 [VEE] M3MNPN1 2
R1 N15 N7 60 TC=824u 7.67u
R10 N16 N17 450 TC=0 0
R11 YIN N16 100 TC=0 0
R12 0 SWIN 500 TC=824u 7.67u
R13 N56 N38 35 TC=0 0
R14 N57 N39 35 TC=0 0
R15 N37 N58 35 TC=0 0
R16 N36 N59 35 TC=0 0
R17 N46 IYX 100 TC=0 0
R18 N47 IXY 100 TC=0 0
R2 N11 IXC 6.25 TC=0 0
R3 N9 IXC 4.5 TC=0 0
R4 N7 IXA 1.5K TC=0 0
R5 XIN N7 100 TC=0 0
R6 N25 N16 156 TC=824u 7.67u
R7 N21 IYC 6.25 TC=0 0
R8 ITC N19 45 TC=0 0
R9 N17 IYA 45 TC=0 0
RSU VEE 0 16K TC=0 0
VFI10 N43 N44 0.0
VFI11 N40 N41 0.0
VFI12 ZB4 ZB5 0.0
VFI13 ZB5 ZB6 0.0
VFI14 ZB3 ZB4 0.0
VFI15 ZB6 ZB7 0.0
VFI16 N44 ZB9 0.0
VFI17 N41 ZB8 0.0
VFI18 IYB IYC 0.0
VFI19 IYA IYB 0.0
VFI20 IXB IXC 0.0
VFI21 IXA IXB 0.0
VFI22 N22 N24 0.0
VFI23 N23 N24 0.0
VFI24 ZB2 ZB3 0.0
VFI25 ZB1 ZB2 0.0
VFI26 N13 N14 0.0
VF127 N12 N14 0.0
VFI28 ZB9 VEE 0.0
VFI29 ZIN N26 0.0
VF15 N30 N32 0.0
VFI6 N31 N32 0.0
VFI7 N33 0 0.0
VFI8 ZB8 N43 0.0
VFI9 ZB7 N40 0.0
.ENDS
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4089C
DC Restored Video Amplifier

Features

- Complete video level restoration system
- 0.02% differential gain and 0.05° differential phase accuracy at NTSC
- 60 MHz bandwidth
- 0.1 dB flatness to 10 MHz
- $V_S = \pm 5V$ to $\pm 15V$
- TTL/CMOS hold signal

Applications

- Input amplifier in video equipment
- Restoration amplifier in video mixers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4089CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL4089CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

The EL4089C is an 8-pin complete DC-restored monolithic video amplifier sub-system. It contains a high quality video amplifier and a nulling, sample-and-hold amplifier specifically designed to stabilize video performance.

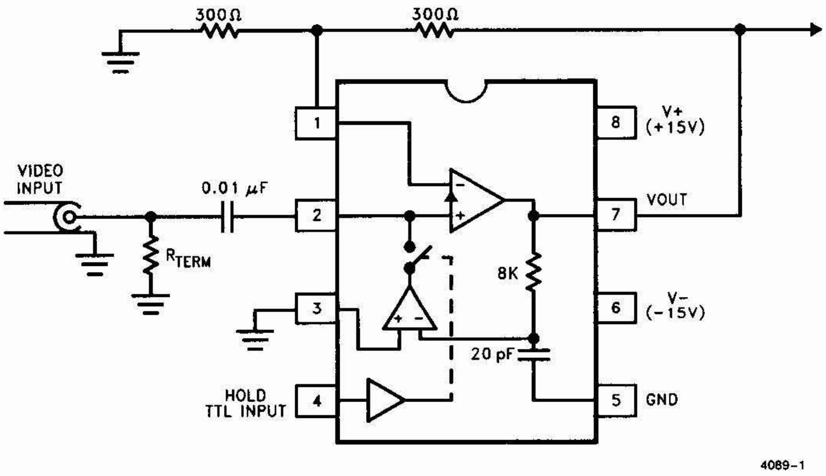
When the HOLD logic input is set to a TTL/CMOS logic 0, the sample- and-hold amplifier can be used to null the DC offset of the video amplifer.

When the HOLD input goes to a TTL/CMOS logic 1, the correcting voltage is stored on the video amplifier's input coupling capacitor. The correction voltage can be further corrected as need be, on each video line.

The video amplifier is optimized for video performance and low power. Its current feedback design allows the user to maintain essentially the same bandwidth over a gain range of nearly 10:1. The amplifier drives back-terminated 75Ω lines.

The EL4089C is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL4089C is specified for operation over 0°C to +75°C temperature range.

Connection Diagram



DC restoring amplifier with a gain of 2, restoring to ground.

January 1996 Rev B

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	33V
Voltage between V_{IN+}, S/H_{IN+}, and GND pins	(V+) +0.5V to (V−) −0.5V
V_{OUT} Current	60 mA
Current into V_{IN-} and HOLD Pins	5 mA
Internal Power Dissipation	See Curves
Operating Ambient Temperature Range	0°C to +75°C
Operating Junction Temperature Plastic DIP or SOL	150°C
Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

Provisional Supplies at ±15V, Load = 1 kΩ; T_A = +25°C

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Amplifier Section (HOLD = 5V)							
V_{OS}	Input Offset Voltage	+25°C		12	25	II	mV
Ib+	IN+ Input Bias Current	+25°C		1	5	II	μA
Ib−	IN− Input Bias Current	+25°C		18	150	II	μA
R_{OL}	Transimpedance (Note 1)	+25°C	180	800		II	kΩ
R_{IN-}	IN− Resistance	+25°C		20		V	Ω
CMRR	Common Mode Rejection Ratio (Note 2)	+25°C	44	60		II	dB
V_O	Output Voltage Swing	+25°C	±12	±13		II	V
I_{SC}	Short Circuit Current (IN+ Only Driven to 0.5V)	+25°C	45	100		II	mA
Restore Section							
V_{OS}, Comp	Composite Input Offset Voltage (Note 3)	+25°C		3	7	II	mV
Ib+,r	Restore In+ Input Bias Current	+25°C		3	12	II	μA
I_{OUT}	Restoring Current Available	+25°C	180	300		II	μA
CMRR	Common Mode Rejection Ratio (Note 2)	+25°C	60	70		II	dB

Open Loop DC Electrical Characteristics — Contd.

Provisional Supplies at ±15V, Load = 1 kΩ; T_A = +25°C

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Restore Section —Contd.							
PSRR	Power Supply Rejection Ratio (Note 4)	+25°C	60	90		II	dB
$V_{THRESHOLD}$	HOLD Logic Threshold	+25°C	0.8		2.0	II	V
I_{IH}, Hold	HOLD Input Current @ Logic High	+25°C		1	5	II	µA
I_{IL}, Hold	HOLD Input Current @ Logic Low	+25°C		5	15	II	µA
Supply Current							
Isy, Hold	Supply Current (HOLD = 5V)	+25°C	4.8	6.0	9.0	II	mA
Isy, Sampling	Supply Current (HOLD = 0V)	+25°C	5.0	6.5	11.0	II	mA

Closed Loop AC Electrical Characteristics

Provisional Supplies at ±15V, Load = 150Ω and 15 pF. R_f and R_g = 300Ω; A_V = 2, T_A = 25°C. (See Note 7 about Test Fixture)

Parameter	Description	Min	Typ	Max	Test Level	Units
Amplifier Section						
SR	Slew Rate (Note 5)		500		V	V/µs
SR	Slew Rate with ±5V Supplies (Note 5)		275		V	V/µs
BW	Bandwidth −3 dB ±5V Supplies −3 dB		60 55		V V	MHz MHz
BW	Bandwidth ±0.1 dB ±5V Supplies ±0.1 dB		25 23		V V	MHz MHz
dG	Differential Gain V_S = ±15V at 3.58 MHz (Note 6) V_S = ±5V		0.02 0.03		V V	% %
dPh	Differential Phase V_S = ±15V at 3.58 MHz (Note 6) V_S = ±5V		0.05 0.06		V V	° °
Restore Section						
SR	Restore Amplifier Slew Rate (Test Circuit) 20%–80%		25		V	V/µs
T_{HE}	Time to Enable Hold		25		V	ns
T_{HD}	Time to Disable Hold		40		V	ns

Note 1: For current feedback amplifiers, $A_{VOL} = R_{OL}/R_{IN-}$.

Note 2: V_{CM} = ±10V for V_S = ±15V.

Note 3: Measured from S/H Input to amplifier output, while restoring.

Note 4: V_{OS} is measured at V_S = ±4.5V and V_S = ±16V, both supplies are changed simultaneously.

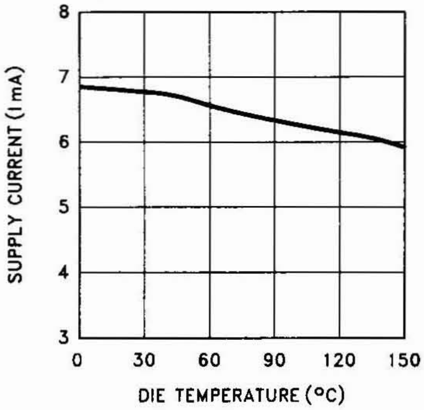
Note 5: SR measured at 20% to 80% of a 4V pk-pk square wave.

Note 6: DC offset from −0.714V through +0.714V, ac amplitude is 286 mVp-p, equivalent to 40 ire.

Note 7: Test fixture was designed to minimize capacitance at the IN− input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.

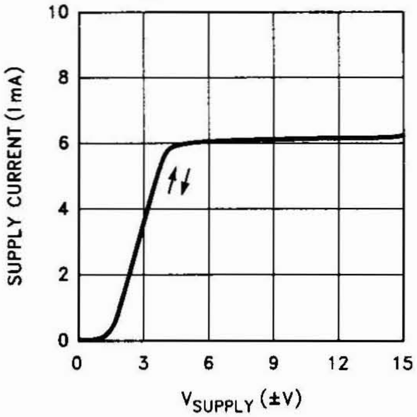
Typical Performance Curves

Supply Current vs Temperature
$V_S = \pm 15V$



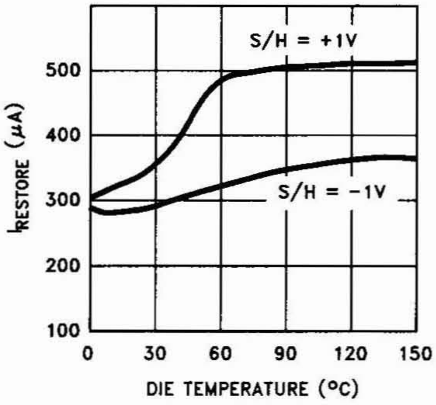
4089-2

Supply Current vs Supply Voltage



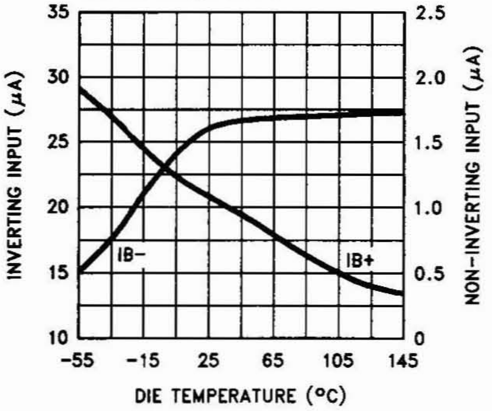
4089-3

Restoring Current vs Temperature



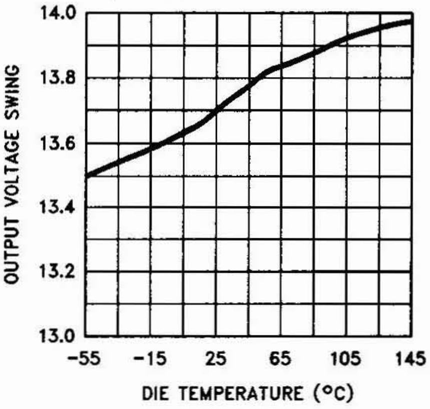
4089-4

Amplifier Input Current vs Die Temperature



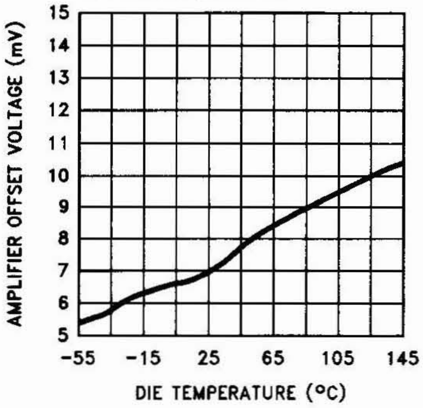
4089-5

Amplifier Output Voltage vs Die Temperature;
$V_S = \pm 15V$



4089-6

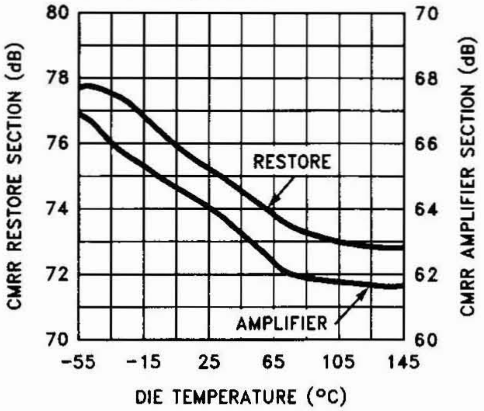
Amplifier Offset Voltage vs Die Temperature



4089-7

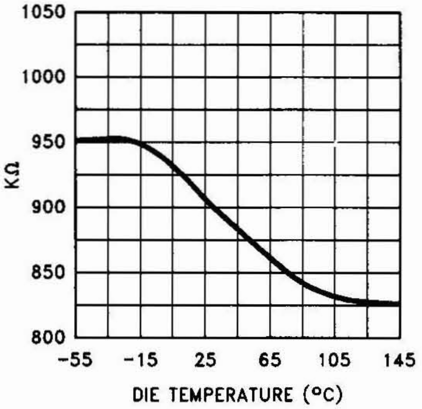
Typical Performance Curves — Contd.

CMRR for Amplifier and Restore Section vs Die Temperature



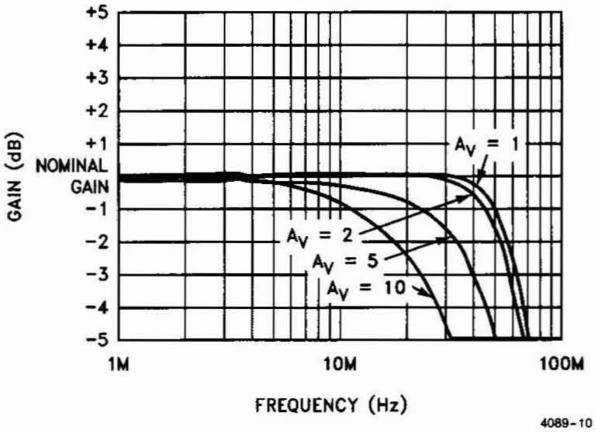
4089-8

Transimpedance (R_{OL}) vs Die Temperature



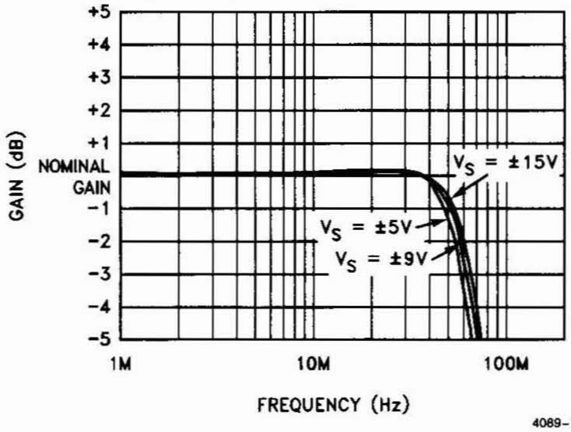
4089-9

Relative Frequency Response for Various Gains, R_F = 300Ω



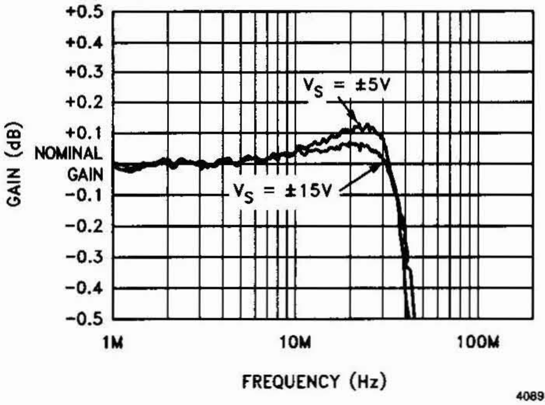
4089-10

Frequency Response vs Supply A_V = 2; R_F = 300



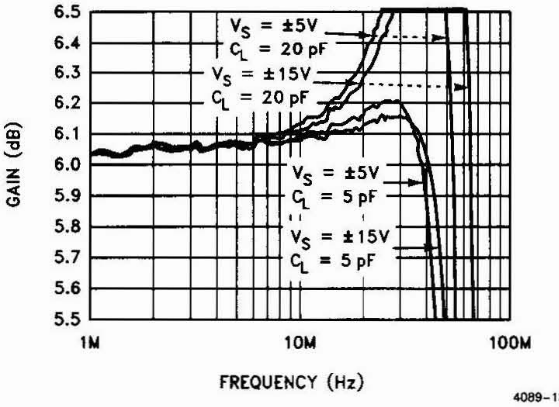
4089-11

Frequency Response Flatness vs Supply A_V = 2; R_F = 300



4089-12

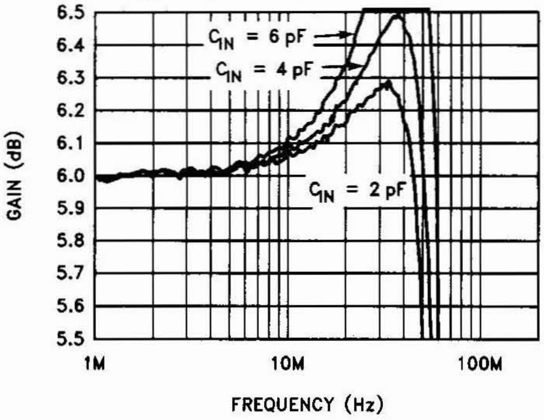
Frequency Response Flatness for Various Load and Supply Conditions A_V = 2; R_F = 300



4089-13

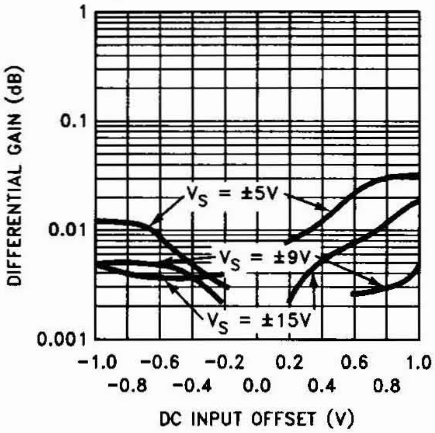
Typical Performance Curves — Contd.

Frequency Response Flatness vs C_{IN-}; $A_V = 2$; $R_F = 300$



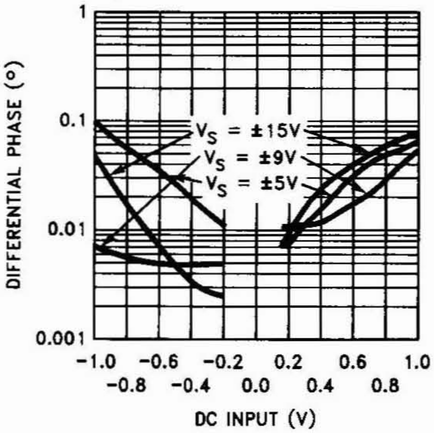
4089-14

Differential Gain vs DC Input Offset; $A_V = 2$, $F_O = 3.58$ MHz, $R_L = 150\Omega$



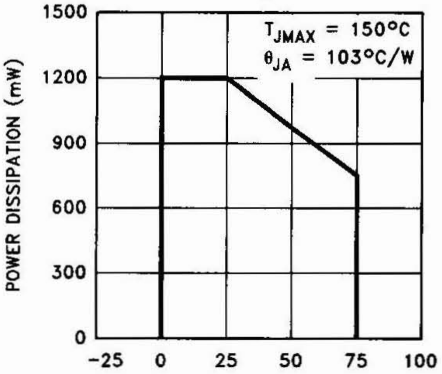
4089-15

Differential Phase vs DC Input Offset; $A_V = 2$; $F_O = 3.58$ MHz; $R_L = 150\Omega$



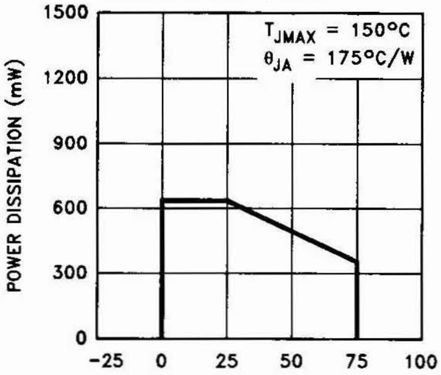
4089-16

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



4089-17

8-Lead SO Maximum Power Dissipation vs Ambient Temperature



4089-18

Typical Application

The EL4089 can be used to DC-restore a video waveform (see Fig. 1). The above circuit forces the cable driving video amplifier's output to ground when the HOLD pin is at a logic low.

The "correction voltage" is stored on capacitor CX1, an external ceramic capacitor. The capacitor value is chosen from the system requirements. The typical input bias current to the video amplifier is 1 μA, so for a 62 μs hold time, and a 0.01 μF capacitor, the output voltage drift is 6.2 mV in one line.

The S/H amplifier can provide a typical current of 300 μA to charge capacitor CX1, so with a 1.2 μs sampling time, the output can be corrected by 36 mV in each line.

Using a smaller value of CX1 increases both the voltage that can be corrected, and the drift while being held, likewise, using a larger value of CX1, reduces the voltages.

The RX1 resistor is in the circuit purely to simulate some external source impedance, and is not needed as a real component. Likewise for RX2. The 75Ω back terminating resistor RXT is recommended when driving 75Ω cables.

The board layout should have a ground plane underneath the EL4089, with the ground plane cut away from the vicinity of the V_{IN-} pin, (pin 1). This helps to minimize the stray capacitance on pin 1.

Power supply bypassing is important, and a 0.1 μF ceramic capacitor, from each power pin to ground, placed very close to the power pins, together with a 4.7 μF tantalum bead capacitor, is recommended.

When both digital and Analog grounds are on the same board, the EL4089 should be on the Analog ground. The digital ground can be connected to the Analog ground through a 100Ω–300Ω resistor, near the EL4089. This allows the digital signal a return path, while preventing the digital noise from corrupting the analog ground.

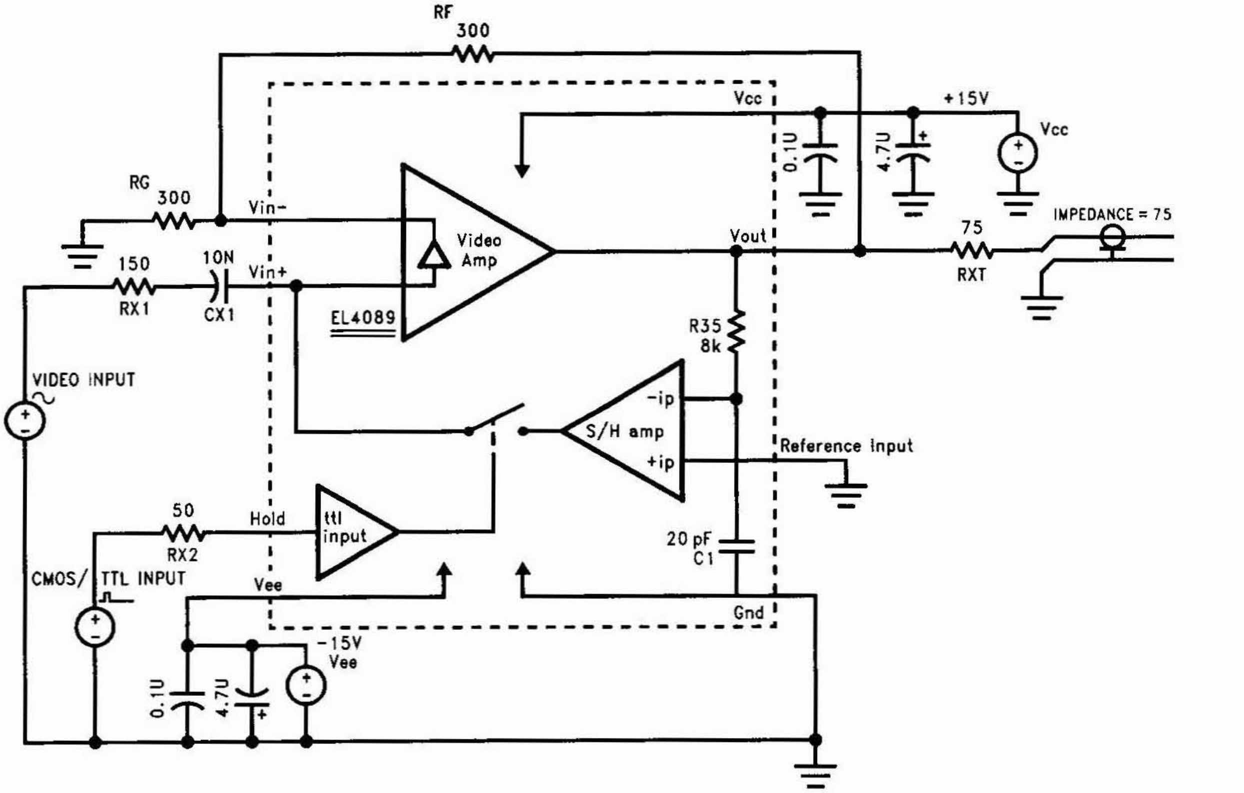

RF
300
Vcc
+15V
0.1U
4.7U
Vcc
RG
300
Vin−
Video
Amp
Vout
75
RXT
IMPEDANCE = 75
150
RX1
10N
CX1
Vin+
EL4089
R35
8k
VIDEO INPUT
−ip
S/H amp
+ip
Reference input
50
RX2
Hold
ttl
input
20 pF
C1
CMOS/TTL INPUT
Vee
Gnd
−15V
Vee
0.1U
4.7U
4089-19

Figure 1

Table of Charge Storage Capacitor vs Droop Charging Rates

Cap Value nF	Droop in 60 µs mV	Charge in 1.2 µs mV	Charge in 4 µs mV
10	6	36	120
33	1.8	11	36
100	0.6	3.6	12

Basic formulae are:
V (droop) = Ib+ * (Line time − Sample time) / Capacitor
and V (charge) = I_{OUT} * Sample time / Capacitor

For best results the source impedance should be kept low, using a buffer for example.

Because the S/H effectively shorts the input signal during Sample, the input should not be sampled during active video. Typically the sample is made during the back porch period of horizontal blanking. For this reason color composite signals, which have color burst on the back porch, can not be passed. See EL2090 or EL4093 for this application.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4093C

300 MHz DC-Restored Video Amplifier

Features

- High accuracy DC restoration for video
- Low supply current of 9.5 mA typ.
- 300 MHz bandwidth
- 1500V/μs slew rate
- 0.04% differential gain and 0.02° differential phase into 150Ω for NTSC
- 1.5 mV max. restored DC offset
- Sample and hold amplifier with fast enable and low leakage
- TTL-compatible HOLD logic input

Applications

- Input amplifier in video equipment
- Restoration amplifier in video mixers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4093CN	-40°C to +85°C	16-pin P-DIP	MDP0031
EL4093CS	-40°C to +85°C	16-Lead SOIC	MDP0027

Demo Board

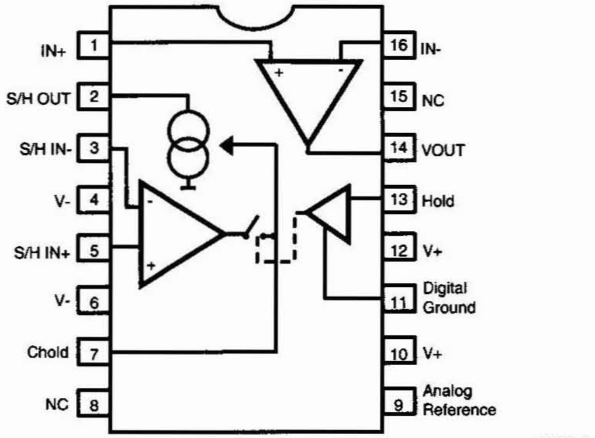
A demo PCB is available for this product. Request "EL4093 Demo Board."

General Description

The EL4093C is a complete DC-restored video amplifier subsystem, featuring low power consumption and high slew rate. It contains a current feedback amplifier and a sample and hold amplifier designed to stabilize video performance. When the HOLD logic input is low, the sample and hold may be used as a general purpose op amp to null the DC offset of the video amplifier. When the HOLD input goes high the sample and hold stores the correction voltage on the hold capacitor to maintain DC correction during the subsequent video scan line.

The sample and hold amplifier contains a current output stage that greatly simplifies its connection to the video amplifier. Its high output impedance also helps to preserve video linearity at low supply voltages. For ease of interfacing, the HOLD input is TTL-compatible. This device has an operational temperature of −40°C to +85°C and is packaged in plastic 16-pin DIP and 16-lead SOIC.

Connection Diagram



44093-1

Absolute Maximum Ratings

V_S	V+ to V− Supply Voltage	12.6V
V_{HOLD}	Voltage at HOLD input	(DGND−0.7) to (DGND+5.5V)
V_{IN}	Voltage at any other input	V+ to V−
ΔV_{IN}	Difference between Sample and Hold inputs	±8V
I_{OUT1}	Video amplifier output current	±30 mA
I_{OUT2}	S/H amplifier output current	±10 mA
I_{IN}	Maximum current into other pins	±6 mA
P_D	Maximum Power Dissipation	See Curves
T_A	Operating Ambient Temperature Range	−40°C to +85°C
T_J	Operating Junction Temperature	150°C
T_{ST}	Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics Power supplies at ±5V, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
$I_{S,HOLD}$	Total Supply current in HOLD mode		9.5	11.5	I	mA
$I_{S,SAMPLE}$	Total Supply current in SAMPLE mode		8.5	10.5	I	mA

Video Amplifier Section (Not Restored)

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		10	110	I	mV
I_{B+}	Non-Inverting Input Bias Current		10	25	I	μA
I_{B-}	Inverting Input Bias Current		15	50	I	μA
R_{OL}	Transimpedance $V_{OUT} = \pm 2.5V, R_L = 150\Omega$	150	400		I	kΩ
V_O	Output Voltage Swing $R_L = 150\Omega$	±3	±3.5		I	V
I_{SC}	Output Short-Circuit Current	60	100		I	mA

Open-Loop DC Electrical Characteristics

Power supplies at ±5V, T_A = 25°C — Contd.

Sample and Hold Section

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		0.5	1.5	I	mV
TCV_{OS}	Average Offset Voltage Drift		6		V	µV/°C
I_B	Input Bias Current		1	2	I	µA
I_{OS}	Input Offset Current		10	200	I	nA
TCI_{OS}	Average Offset Current Drift		0.1		V	nA/°C
V_{CM}	Common Mode Input Range	±2.5	±2.8		I	V
g_m	Transconductance (R_L = 500Ω)	5	15		I	A/V
CMRR	Common Mode Rejection Ratio (V_{CM} −2.5V to +2.5V)	70	90		I	dB
V_{IL}	HOLD Logic Input Low (referenced to Digital GND)			0.8	I	V
V_{IH}	HOLD Logic Input High (referenced to Digital GND)	2.0			I	V
V_{GND}	Digital GND Reference Voltage	(V−)		(V+) − 4.0	I	V
I_{DROOP}	Hold Mode Droop Current		10	70	I	nA
I_{CHARGE}	Charge Current Available to C_{HOLD}	±5.5	±8.5		I	mA
V_O	Output Voltage Swing (R_L = 10kΩ)	±3	±3.5		I	V
I_O	Output Current Swing (R_L = 0Ω)	±4.5	±5.5		I	mA

Closed-Loop AC Electrical Characteristics

Power supplies at ±5V, T_A = 25°C, R_F = R_G = 750Ω, R_L = 150Ω, C_L = 5 pF, C_{IN-}(parasitic) = 1.8 pF

Video Amplifier Section

Parameter	Description	Min	Typ	Max	Test Levels	Units
BW, −3 dB	−3 dB Small-Signal Bandwidth		300		V	MHz
BW, ±0.1 dB	0.1 dB Flatness Bandwidth		50		V	MHz
Peaking	Frequency Response Peaking		0		V	dB
SR	Slew rate, V_{OUT} between −2V and +2V		1500		V	V/µs
dG	Differential Gain Error, Voffset between −714 mV and +714 mV		0.04		V	%
dθ	Differential Phase Error, Voffset between −714 mV and +714 mV		0.02		V	°

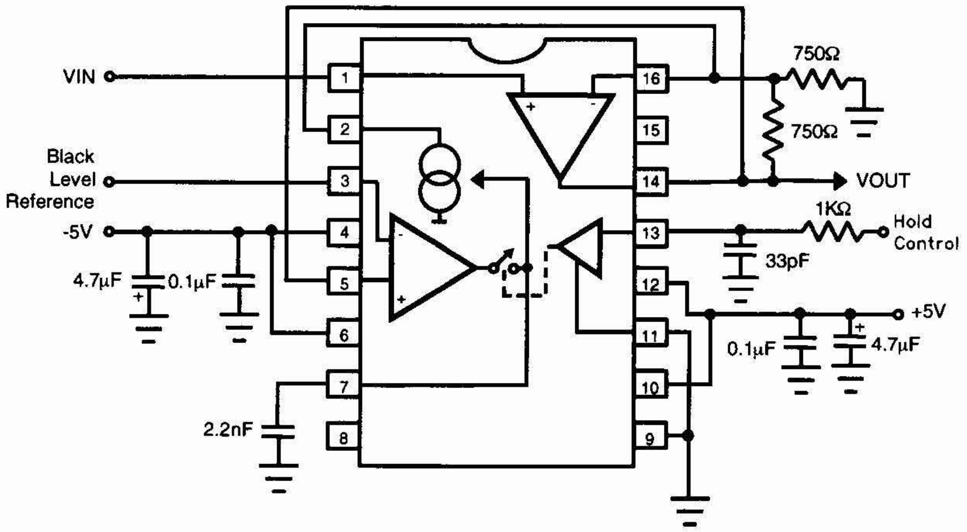
Closed-Loop AC Electrical Characteristics

Power supplies at ±5V, $T_A = 25°C$, $R_F = R_G = 750\Omega$, $R_L = 150\Omega$, $C_L = 5$ pF, $C_{HOLD} = 2.2$ nF

Sample and Hold Section

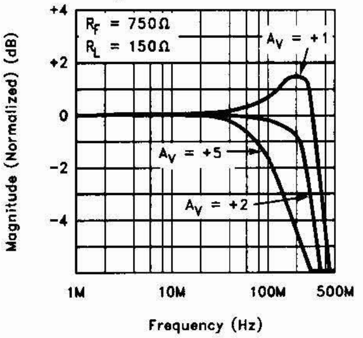
Parameter	Description	Min	Typ	Max	Test Levels	Units
ΔI_{STEP}	Change in Sample to Hold Output Current Due to Hold Step		0.1		V	μA
ΔT_{SH}	Sample to Hold Delay Time		15		V	ns
ΔT_{HS}	Hold to Sample Delay Time		40		V	ns
T_{AC}	Settling Time to 1% (DC Restored Amplifier Output) Video Amplifier Input from 0 to 1V		2.2		V	μs

Typical Application


VIN
Black Level Reference
-5V
4.7μF
0.1μF
2.2nF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
750Ω
750Ω
VOUT
1KΩ
Hold Control
33pF
+5V
0.1μF
4.7μF
44093-2

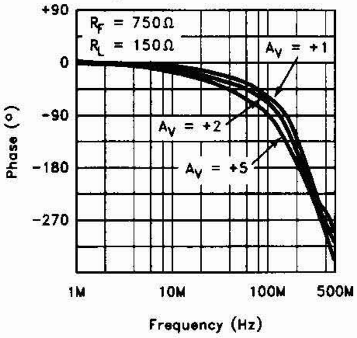
Typical Performance Curves

Non-inverting Frequency Response (Gain)



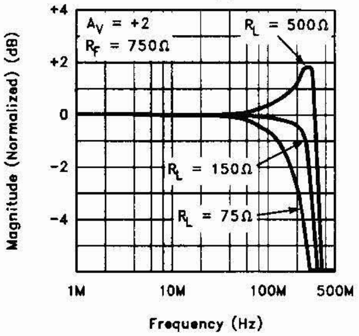
44093-4

Non-inverting Frequency Response (Phase)



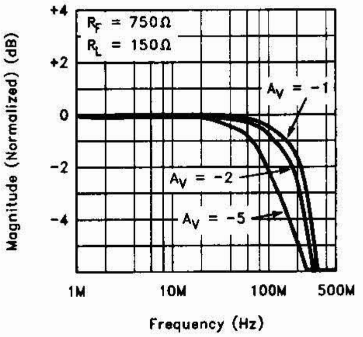
44093-5

Frequency Response for Various R_L



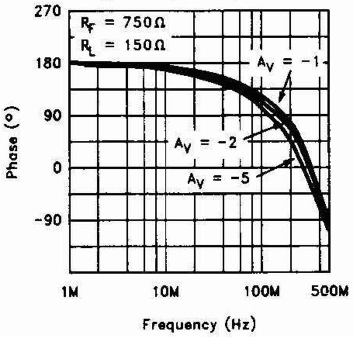
44093-6

Inverting Frequency Response (Gain)



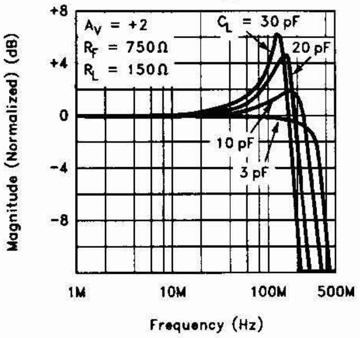
44093-7

Inverting Frequency Response (Phase)



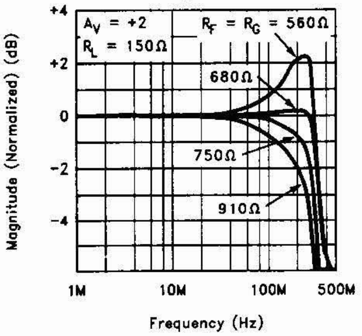
44093-8

Frequency Response for Various C_L



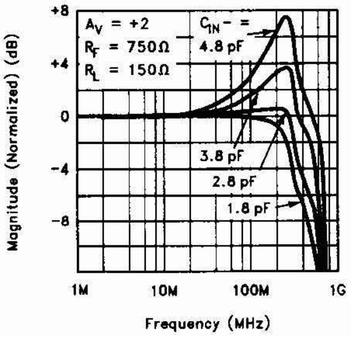
44093-9

Frequency Response for Various R_F and R_G



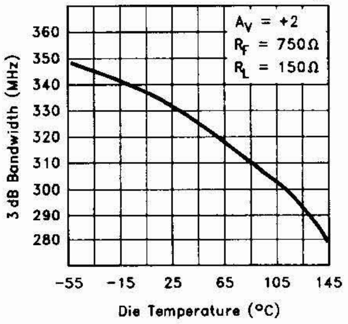
44093-10

Frequency Response for Various C_{IN}



44093-11

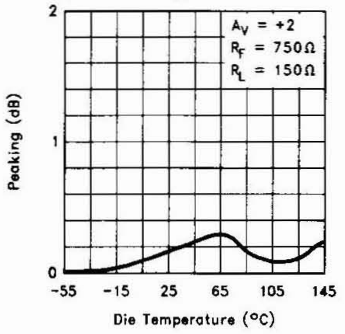
3 dB Bandwidth vs Temperature (Video Amp)



44093-12

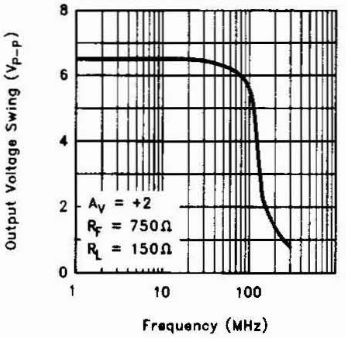
Typical Performance Curves — Contd.

Peaking vs Temperature (Video Amp)



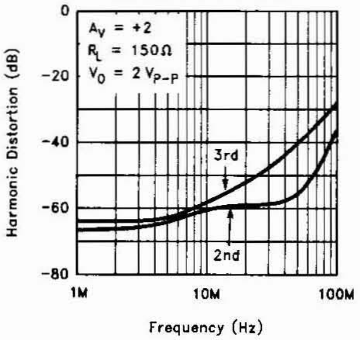
44093-13

Output Voltage Swing vs Frequency



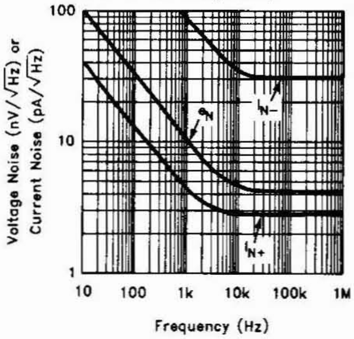
44093-14

2nd and 3rd Harmonic Distortion vs Frequency



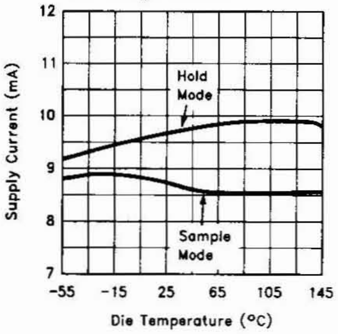
44093-15

Voltage and Current Noise vs Frequency



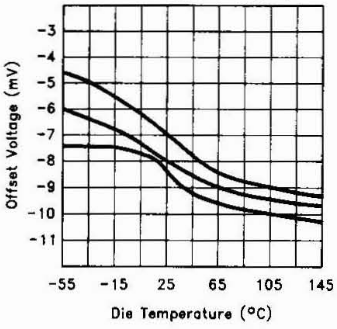
44093-16

Supply Current vs Temperature



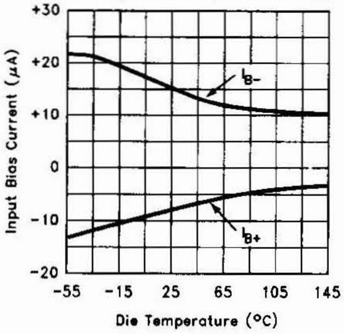
44093-17

Input Offset Voltage vs Die Temperature (Video Amp, 3 Sample)



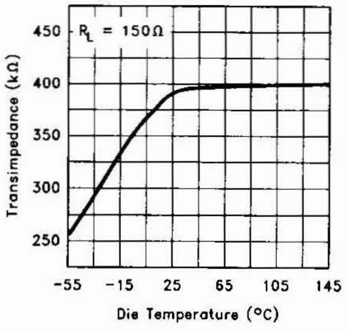
44093-18

Input Bias Current vs Temperature (Video Amp)



44093-19

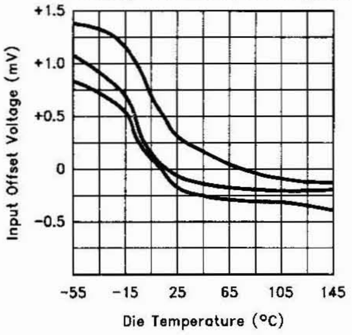
Transimpedance vs Temperature (Video Amp)



44093-20

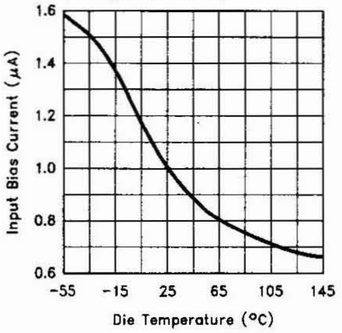
Typical Performance Curves — Contd.

Input Offset Voltage vs Die Temperature (Sample & Hold, 3 Samples)



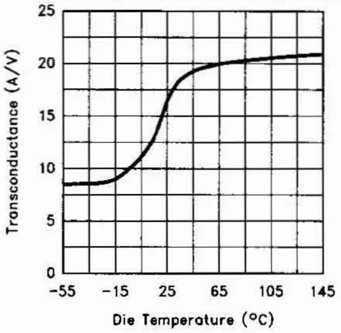
44093-21

Input Bias Current vs Die Temperature (Sample & Hold)



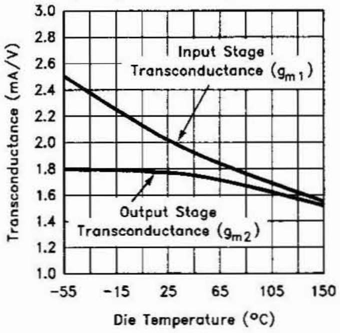
44093-22

Transconductance vs Temperature (Sample & Hold)



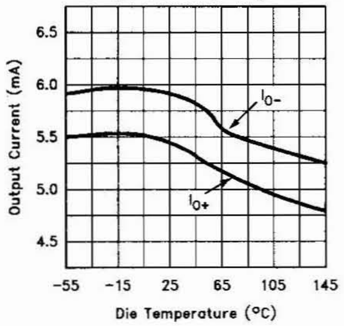
44093-23

Transconductance vs Die Temperature (Sample & Hold)



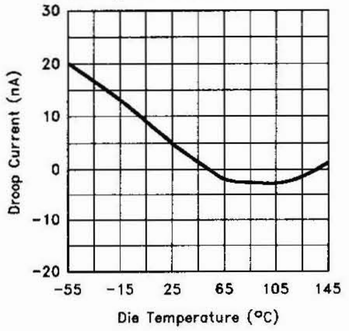
44093-38

Output Current Swing vs Temperature (Sample & Hold)



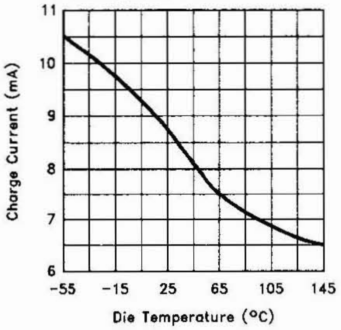
44093-25

Droop Current vs Temperature (Sample & Hold)



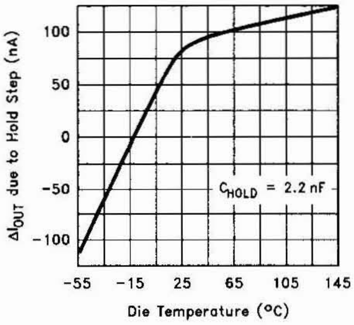
44093-26

Charge Current vs Temperature (Sample & Hold)



44093-27

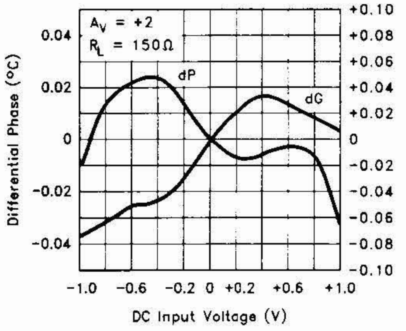
Hold Step (ΔI_{OUT}) vs Temperature



44093-28

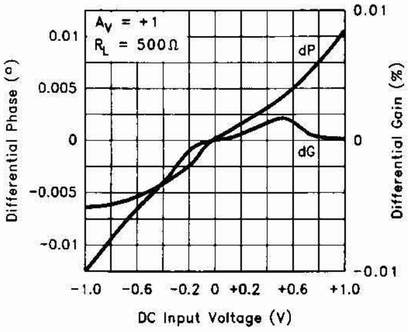
Typical Performance Curves — Contd.

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



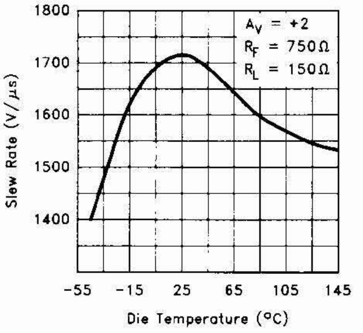
44093-29

Differential Gain and Phase vs DC Input Voltage at 3.58 MHz



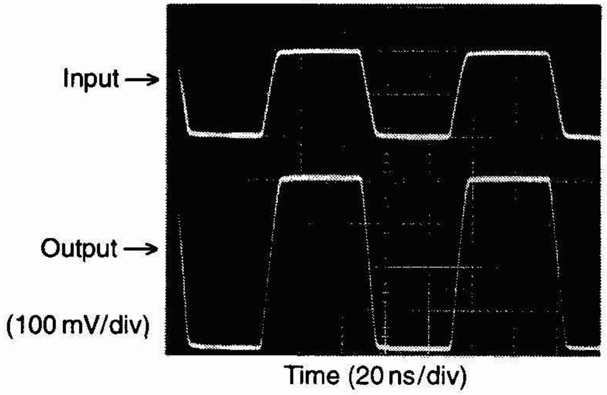
44093-30

Slew Rate vs Die Temperature (Video Amp)



44093-31

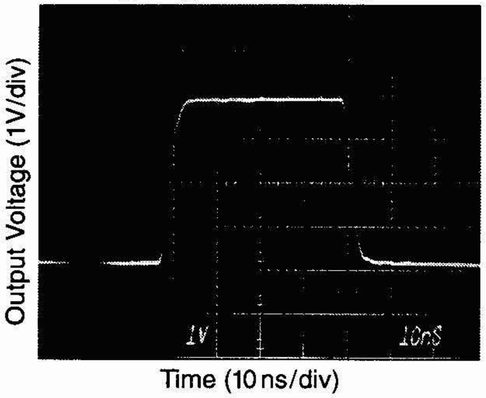
Small-Signal Step Response



$A_V = +2$, $R_F = R_G = 750\Omega$, $R_L = 150\Omega$

44093-32

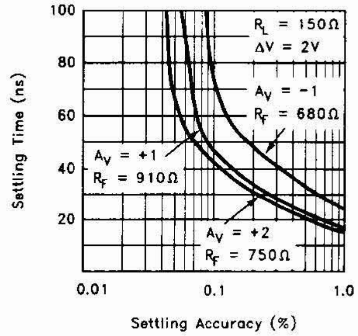
Large-Signal Step Response



$A_V = +2$, $R_F = R_G = 750\Omega$, $R_L = 150\Omega$

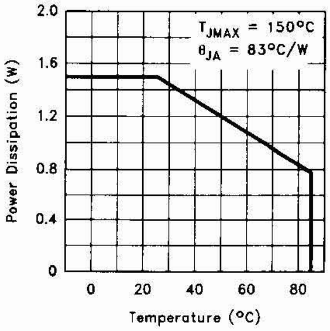
44093-33

Settling Time vs Settling Accuracy (Video Amp)



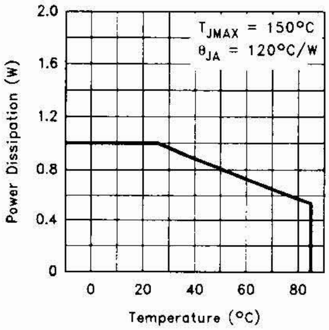
44093-34

Maximum Power Dissipation vs Ambient Temperature, 16-Pin P-DIP Package



44093-35

Maximum Power Dissipation vs Ambient Temperature, 16-Pin SO Package



44093-36

Applications Information

Product Description

The EL4093C is a high speed DC-restore system containing a current feedback amplifier (CFA) and a sample & hold (S/H) amplifier. The CFA offers a wide 3 dB bandwidth of 300 MHz and a slew rate of 1500 V/μs, making it ideal for high speed video applications such as SVGA. The CFA's excellent differential gain and phase at 3.58 MHz also makes it suitable for NTSC applications. Drawing only 9.5 mA on ±5V supplies, the EL4093C serves as an excellent choice for those applications requiring both low power and high bandwidth.

The connection between the CFA and sample & hold (the Autozero interface) has been greatly simplified. The output of the sample & hold is a high impedance current source, allowing direct connection to the CFA inverting input for autozero purposes. In addition, special circuitry within the sample & hold provides a charge current of 8.5 mA in sample mode, resulting in a sample hold current ratio (ratio of charging current to droop current) of approx. 1,000,000.

Theory of Operation

In video applications, DC restoration moves the backporch or black level to a fixed DC reference. The EL4093C uses a CFA in feedback with a sample & hold to provide DC restoration. Figure 1 shows how the two are connected to provide this function; the S/H compares the output of the CFA to a DC reference, and any difference between them causes an output current from the S/H. This "autozero" current is fed to the CFA inverting input, the effect of which is to move the CFA output towards the reference voltage. This autozero mechanism settles when the CFA output is one V_{OS} away from the reference (the V_{OS} here refers to the S/H offset voltage).

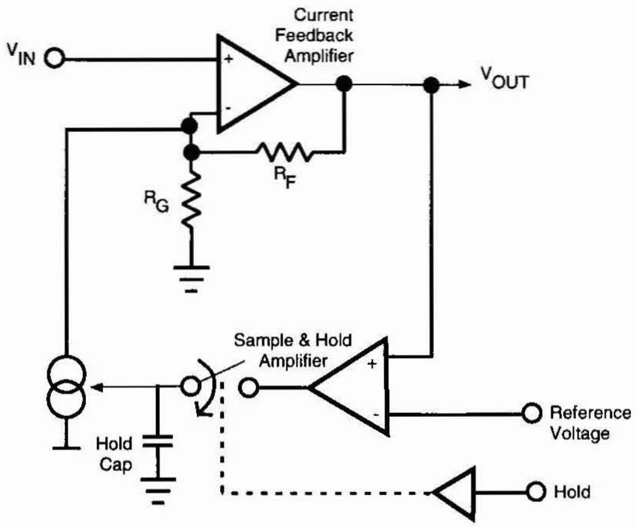


Figure 1

The autozero mechanism is typically active for only a short period of each video line. Figure 2 shows a NTSC video signal along with the EL4581C back porch output. The back porch signal is used to drive the HOLD input of the EL4093C, and we see that the EL4093C is in sample mode for only 3.5 μs of each line. It is during this time that the autozero mechanism attempts to drive the CFA output towards the reference voltage, at the same time putting a correction voltage onto the hold capacitor C_{HOLD}. During the rest of the line (60 μs) the EL4093C is in hold mode, but DC correction is maintained by the voltage on C_{HOLD}.

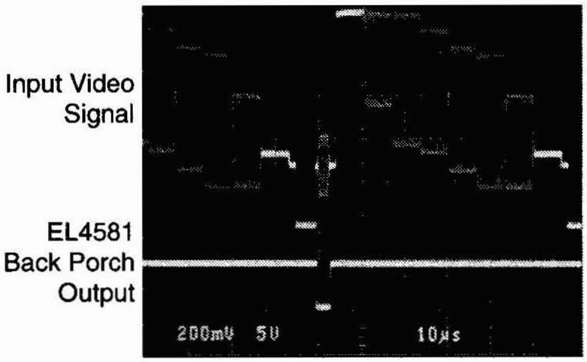


Figure 2

Applications Information — Contd.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. In the EL4093C there are two sets of supply pins: V+1/V−1 provide power for the CFA, and V+2/V−2 are for the S/H amplifier. Good performance can be achieved using only one set of bypass capacitors, although they must be close to the V+1/V-1 pins since that is where the high frequency currents flow. The combination of a 4.7 μF tantalum capacitor in parallel with a 0.01 μF capacitor has been shown to work well. Chip capacitors are recommended for the 0.01 μF bypass to minimize lead inductance.

For good AC performance, parasitic capacitance should be kept to a minimum, especially at the CFA inverting input. Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Chip resistors are recommended for R_F and R_G, and use of sockets should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

If the CFA is configured for non-inverting gain, then one should also pay attention to the trace leading to the +input. The inductance of a long trace (> 3") can form a resonant network with the amplifier input, resulting in high frequency oscillations around 700 MHz. In such cases a 50Ω−100Ω series resistor placed close to the +input would isolate this inductance and damp out the resonance.

Capacitance at the Inverting Input

Any manufacturer's high-speed voltage or current feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. Hence it is important to minimize the stray capacitance at this node by removing the nearby ground plane. In addition, since the S/H output connects to this node, it is important to minimize the trace capacitance. Good practice here would be to connect the two pins with a short trace directly underneath the chip.

Feedback Resistor Values

The EL4093C has been optimized for a gain of +2 with R_F = 750Ω. This value of feedback resistor gives a 3 dB bandwidth of 300 MHz at a gain of +2 driving a 150Ω load. Since the amplifier inside the EL4093C uses current mode feedback, it is possible to change the value of R_F to adjust the bandwidth. Shown in the table below are optimum feedback resistor values for different closed loop gains.

Gain	Optimum RF	BW (MHz)	Peaking (dB)
+1	910	314	0.2
+2	750	300	0
+5	470	294	0.2
−1	680	300	0

Autozero Interface

The autozero interface refers to the connection between the S/H output and the CFA inverting input. This interface has been greatly simplified compared to that of the EL2090C, in that the S/H output is a high impedance current source. The S/H output can be connected directly to the inverting input, and its high impedance greatly reduces the interaction between the sample & hold and the gain setting resistors. Another virtue of this interface is better gain linearity as the autozero current changes. For example, at an autozero current of 0 mA the output impedance is about 5 MΩ, dropping to 1 MΩ as the autozero current increases to 3 mA. Using R_F = R_G = 750Ω, the closed loop gain changes only by 0.025% in this interval.

Applications Information — Contd.

Autozero Range

The autozero range is defined as the difference between the input DC level and the reference voltage to restore to. The size of this range is a function of the gain setting resistors used and the S/H output current swing. For a gain of +2 the optimum feedback resistor is 750Ω, and the available S/H output current is ±5.5 mA minimum. To determine the autozero range for this case, we refer to Figure 3 below.

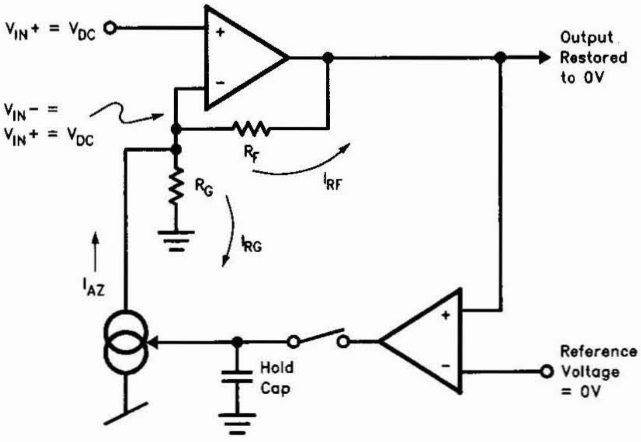


Figure 3

Suppose that the input DC level is $+V_{DC}$, and that the reference voltage is 0V. We know that in feedback, the following two conditions will exist on the CFA: first, its output will be equal to 0V (due to autozero), and second, its $V_{IN}-$ voltage is equal to the $V_{IN}+$ voltage (i.e. $V_{IN}- = +V_{DC}$). So we have a potential difference of $+V_{DC}$ across both R_F and R_G, resulting in a current $I_{RF} = I_{RG} = V_{DC}/750\Omega$ that must flow into each of them. This current $I_{AZ} = (I_{RF} + I_{RG})$ must come from the S/H output. Since the maximum that I_{AZ} can be is 5.5 mA, we can solve for V_{DC} using the following:

$$I_{AZ} = \pm 5.5 \text{ mA} = 2\left(\frac{V_{DC}}{750\Omega}\right)$$

and see that $V_{DC} = \pm 2V$. This range can easily accommodate most video signals.

As another example, consider the case where we are restoring to a reference voltage of +0.75V. Using the same reasoning as above, a current $I_{RF} = (V_{DC} - 0.75V)/R_F$ must flow through R_F, and a current $I_{RG} = V_{DC}/R_G$ must go into R_G. Again, our boundary condition is that $I_{RF} + I_{RG} \leq \pm 5.5$ mA, and we can solve for the allowable V_{DC} values using the following:

$$\pm 5.5 \text{ mA} = \frac{V_{DC} - 0.75V}{750\Omega} + \frac{V_{DC}}{750\Omega}$$

Hence V_{DC} must be between +2.4V to −1.7V. This example illustrates that when the reference changes, the autozero range also changes. In general, the user should determine the autozero range for his/her application, and ensure that the input signal is within this range during the autozero period.

Autozero Loop Bandwidth

The gain-bandwidth product (GBWP) of the autozero loop is determined by the size of the hold capacitor, the value of R_F, and the transconductances (gm's) of the S/H amplifier. To begin, the S/H amplifier is modeled as in Figure 4 below. First, the input stage transconductance is represented by gm1, with the compensation capacitor given by C_{HOLD}. This stage's GBWP is thus $gm1/(2\pi \bullet C_{HOLD}) = 1/(2\pi \bullet (350\Omega)(2.2\text{ nF})) = 207$ kHz. Next, since the S/H has a current output, its output stage can be modeled as a transconductance gm2, in this case having a value of 1/(500Ω). The current from gm2 then flows through the I to V converter made up of the CFA and R_F to produce a voltage gain. Thus the GBWP of the overall loop is given by:

$$\text{GBWP} = \frac{gm1}{2\pi \bullet C_{HOLD}} (gm2 \bullet R_F)$$

Applications Information — Contd.

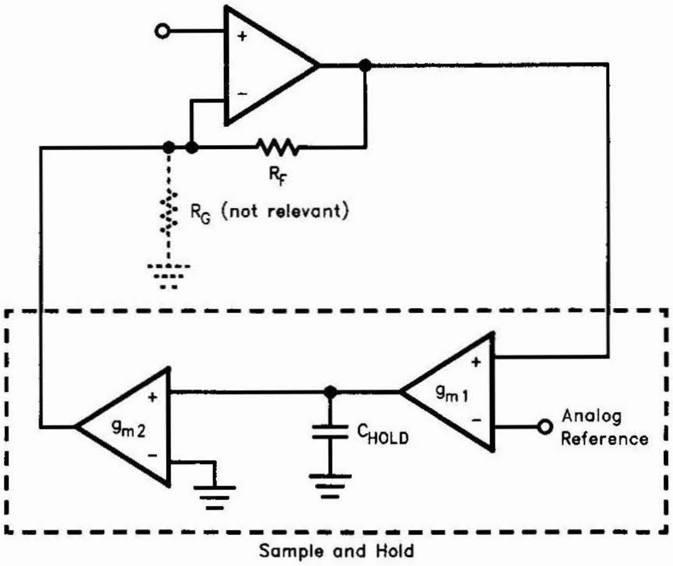


Figure 4

With $R_F = 750\Omega$, a GBWP of 310 kHz is obtained. Note however that this is the small signal GBWP. As mentioned earlier, the sample and hold has special boost circuits built in which provides ±8.5 mA of charge current during full slew. These boost circuits turn on when the S/H input differential voltage exceeds ±50 mV. When the boosters are turned on, gm1 greatly increases and the circuit becomes nonlinear. Thus some stability issues are associated with the boosters, and they will be addressed in a later section.

Charge Injection and Hold Step

Charge injection refers to the charge transferred to the hold capacitor when switching to the HOLD mode. The charge should ideally be 0, but due to stray capacitive coupling and other effects, is typically 0.1 pC in the EL4093. This charge changes the hold capacitor voltage by $\Delta V = \Delta Q / C_{HOLD}$, and this ΔV is multiplied by the output stage transconductance (gm2) to produce a change in S/H output current. This last quantity is listed as the spec ΔI_{STEP}, and is calculated using the following:

$$\Delta I_{STEP} = \left(\frac{\Delta Q}{C_{HOLD}}\right) \bullet gm2$$

For $C_{HOLD} = 2.2$ nF and $gm2 = 1/(500\Omega)$, ΔI_{STEP} has a typical value of 100 nA. This change in S/H output current flows through R_F, shifting the CFA output voltage. However, as we shall soon see, this shift is negligible. Assuming $R_F = 750\Omega$, ΔI_{STEP} is impressed across R_F to give $(750\Omega)(100\text{ nA}) = 0.08$ mV of change at the CFA output.

Droop Rate

When the S/H amplifier is in HOLD mode, there is a small current that leaks from the switch into the hold capacitor. This quantity is termed the droop current, and is typically 10 nA in the EL4093. This droop current produces a ramp in the hold capacitor voltage, which in turn produces a similar effect at the CFA output. The Droop Rate at the CFA output can be found using the equation below:

$$\text{Droop} = \frac{I_{DROOP}}{C_{HOLD}} (gm2 \bullet R_F)$$

Assuming $R_F = 750\Omega$ and $C_{HOLD} = 2.2$ nF, the drift in the CFA output due to droop current is about 7 µV/µs. Recall that in NTSC applications, there is about 60 µs between autozero periods. Thus there is 7 µV/µs)(60 µs) = 0.4 mV, or less than 0.1 IRE, of drift over each NTSC scan line. This drift is negligible in most applications.

Applications Information — Contd.

Choice of Hold Capacitor

The EL4093 has been designed to work with a hold capacitor of 2.2 nF. With this value of C_{HOLD}, the droop rate and hold step are negligibly small for most applications. In addition, with the special boost circuits inside the S/H, fast acquisition is possible even using a hold capacitor of this size. Figure 5 below shows the input and output of the DC-restored amplifier while the S/H is in sample mode. Applying a +1V step to the non-inverting input of the CFA, the output of the CFA jumps to +2V. The S/H, however, then tries to autozero the system by driving the CFA output back to the reference voltage. Since the input differential across the S/H is initially +2V, the boost circuits turn on and supply 8.5 mA of charge current to the hold capacitor. The boost circuit remains on until the CFA output has come to within 50 mV of the reference. Note that this event took only 320 ns; settling to within 1% of the final value takes another 2 μs. Thus for a 1V input step, acquisition takes only one to two NTSC scan lines.

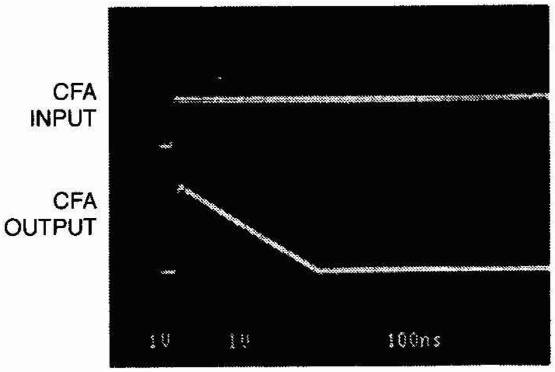


Figure 5. Autozero Mechanism Restores Amplifier Output to Ground after +1V Step at Input

A natural question arises as to whether there are other C_{HOLD} values that can be used. In one direction, increasing C_{HOLD} will further reduce the droop and hold step, but lengthen the acquisition time. Since the droop and hold step are already small to begin with, there is no apparent advantage to increasing C_{HOLD}.

In the other direction, decreasing C_{HOLD} would increase the droop and hold step but shorten the acquisition time. There is, however, a caveat to reducing C_{HOLD}: too small a C_{HOLD} would cause the autozero loop to oscillate. The reason is that when the S/H boost circuit turns on, the input stage gm increases drastically and the circuit becomes nonlinear. A sufficiently large C_{HOLD} must be used to suppress the non-linearity and force the loop to settle. For example, it has been found that a C_{HOLD} of 470 pF results in 1 $V_{P\text{-}P}$ oscillation around 10 MHz at the CFA output.

The minimum recommended value for C_{HOLD} is 2.2 nF. With this value the loop remains stable over the entire operating temperature range (−40°C to +85°C). The greatest instability occurs at low temperatures, where we observe from the performance curves that the S/H gm's, and hence the GBWP, are at their maximum. If the operating range is restricted to room temperature or above, then 1.5 nF is sufficient to keep the loop stable. At this value of C_{HOLD} the acquisition time reduces to about 1.5 μs.

Video Performance and Application

Although the EL4093 is intended for high speed video applications such as SVGA, it also offers excellent performance for NTSC, with 0.04% dG and 0.02° dP at 3.58 MHz. Some application considerations, however, are required for handling NTSC signals.

Referring back to Figure 2, recall that typically, the autozero interval lies in the back porch portion of video containing the colorburst pulse. When the S/H compares the video to the reference voltage during this period, the colorburst (40 $IRE_{P\text{-}P}$) triggers the S/H boost circuit and prevents the autozero loop from settling.

Applications Information — Contd.

A remedy for this situation is to attenuate the colorburst before applying it to the S/H input. Figure 6 below shows a 3.58 MHz chroma trap which would notch out the colorburst while preserving the video DC level.

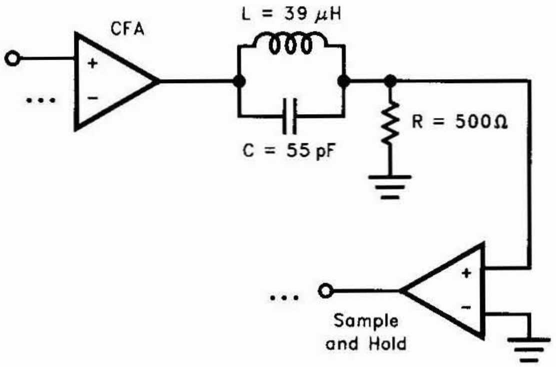


Figure 6. Colorburst Trap for NTSC Applications

One may be tempted to use a RC lowpass filter to suppress the colorburst, as shown in Figure 7 below. This technique, however, poses several problems. First, to obtain enough attenuation, we need to set the pole frequency 10 to 20 times lower than 3.58 MHz. This pole, being close to the auto zero loop pole, would destabilize the system and cause the loop to oscillate.

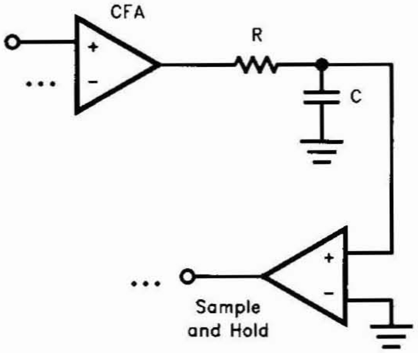


Figure 7. Caution: Lowpass Filter Does Not Work in NTSC Applications

Although we can cancel this pole by introducing a zero, the RC network introduces a time delay between the CFA output and the S/H input. This has undesirable effects in some NTSC applications, as Figure 8 below illustrates. There is only 0.6 μs from the rising edge of sync to the colorburst. If we are autozeroing over the back porch, the autozero period would begin somewhere in this 0.6 μs interval. Since the edge of sync is now delayed by the RC network, autozero begins before the video back porch reaches its final value. Consequently, the autozero loop performs a correction on every line and never settles.

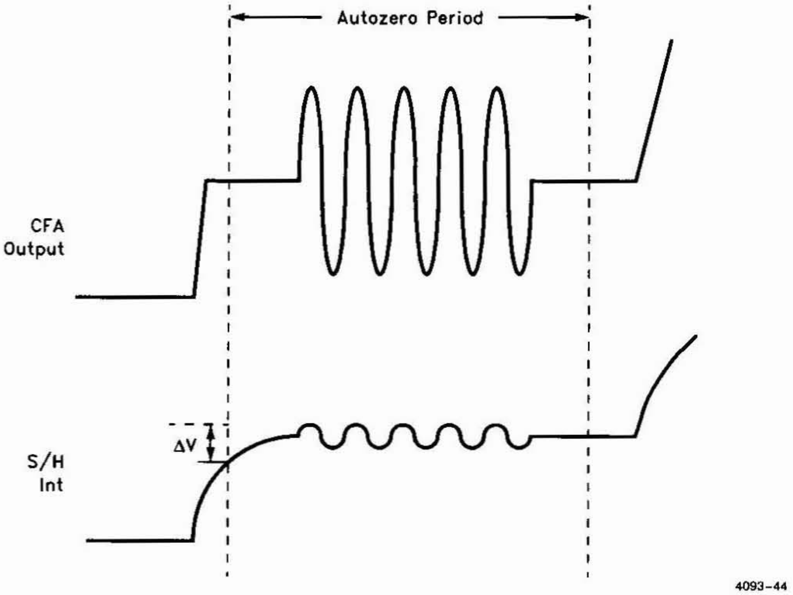


Figure 8. Lowpass Filter Delays Input to Sample and Hold

Applications Information — Contd.

If the video does not contain any AC components during the autozero level (e.g. RGB video), then the above networks are not needed and the CFA output can be connected directly to the S/H input.

Power Dissipation

The EL4093 current feedback amplifier has an absolute maximum of ±30 mA output current drive. This is slightly more than the current required to drive ±2V into 75Ω. To see how much the junction temperature is raised in this worst case, we refer to the equations below:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \bullet PD_{MAX})$$

where:

T_{MAX} = Maximum Ambient Temperature
θ_{JA} = Thermal Resistance of the Package
PD_{MAX} = Maximum Power Dissipation of the CFA and S/H amplifier in the Package

PD_{MAX} for either the CFA or the S/H amplifier can be calculated as follows:

$$PD_{MAX} = (2 \bullet V_S \bullet I_{SMAX}) + (V_S - V_{OUTMAX}) \bullet (V_{OUTMAX}/R_L)$$

where:

V_S = Supply Voltage
I_{SMAX} = Maximum Supply Current of Amplifier
V_{OUTMAX} = Maximum Output Voltage of Application
R_L = Load Resistance

For the EL4093, the maximum supply current is 11.5 mA on V_S = ±5V. Assume that in the worst case, the CFA output swings ±2V into 75Ω. Since the S/H has a current output, we assume that it is at maximum current swing (±5.5 mA) but at a mid-rail output voltage (0V). With the above assumptions, PD_{MAX} for the EL4093 is 223 mW, and using the thermal resistance of a narrow SO package (120°C/W), this yields a temperature increase of 27°C. Since the maximum ambient temperature is 85°C, the resulting junction temperature of 112°C is still below the maximum.

Please note that there is no short-circuit protection on the EL4093 CFA output, and hence the minimum short circuit current (60 mA) is greater than the absolute maximum output current. Maintaining the EL4093 in this state for more than a few seconds may cause the part to exceed T_{JMAX}, in addition to metal migration problems.

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EL4094C
Video Gain Control/Fader

Features
- Complete video fader
- 0.02%/0.04° differential gain/ phase @100% gain
- Output amplifier included
- Calibrated linear gain control
- ±5V to ±15V operation
- 60 MHz bandwidth
- Low thermal errors

Applications
- Video faders/wipers
- Gain control
- Video text insertion
- Level adjust
- Modulation

Ordering information

Part No.	Temp. Range	Package	Outline #
EL4094CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL4094CS	−40°C to +85°C	8-Pin SO	MDP0027

General Description
The EL4094C is a complete two-input fader. It combines two inputs according to the equation:

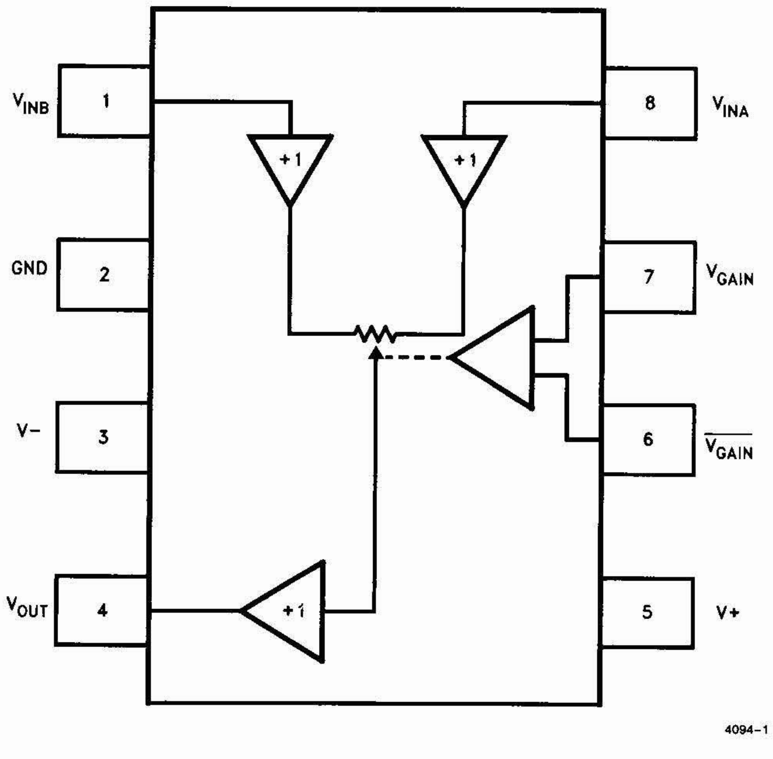
$$V_{OUT} = V_{INA}(0.5V + Vg) + V_{INB}(0.5V - Vg),$$

where V_{GAIN} is the difference between V_{GAIN} and $\overline{V_{GAIN}}$ pin voltages and ranges from −0.5V to +0.5V. It has a wide 60 MHz bandwidth at −3 dB, and is designed for excellent video distortion performance. The EL4094C is the same circuit as the EL4095, but with feedback resistors included on-chip to implement unity-gain connection. An output buffer is included in both circuits.

The gain-control input is also very fast, with a 20 MHz small-signal bandwidth and 70 ns recovery time from overdrive.

The EL4094C is compatible with power supplies from ±5V to ±15V, and is available in both the 8-pin plastic DIP and SO-8.

Connection Diagram



Manufactured under U.S. Patent No. 5,321,371, 5,374,898

January 1996, Rev C

EL4094C
Video Gain Control/Fader

Absolute Maximum Ratings (T_A = 25°C)

V_S+	Voltage between $V_S{}^+$ and GND	+18V
V_S	Voltage between $V_S{}^+$ and $V_S{}^-$	+33V
V_{INA}, V_{INB}	Input Voltage	$(V_S{}^-) - 0.3V$ to $(V_S{}^+) + 0.3V$
V_{GAIN}	Input Voltage	$\overline{V_{GAIN}} \pm 5V$
$\overline{V_{GAIN}}$	Input Voltage	$V_S{}^-$ to $V_S{}^+$

I_{OUT}	Output Current	±35 mA
Internal	Power Dissipation	See Curves
T_A	Operating Ambient Temp. Range	−40°C to +85°C
T_J	Operating Junction Temperature	150°C
T_{ST}	Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V, T_A = 25°C, V_{GAIN} = +0.6V to measure channel A, V_{GAIN} = −0.6V to measure channel B, $\overline{V_{GAIN}}$ = 0V, unless otherwise specified

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
V_{OS}	Input Offset Voltage		4	30	I	mV
I_{B+}	V_{IN} Input Bias Current		2	10	I	μA
PSRR	Power Supply Rejection Ratio	60	80		I	dB
EG	Gain Error, 100% Setting		−0.5	−0.8	I	%
V_{IN}	V_{IN} Range	(V−) +2.5		(V+) −2.5	I	V
V_O	Output Voltage Swing	(V−) +2.5		(V+) −2.5	I	V
I_{SC}	Output Short-Circuit Current	50	95	150	I	mA
V_{GAIN}, 100%	Minimum Voltage at V_{GAIN} for 100% Gain	0.45	0.5	0.55	I	V
V_{GAIN}, 0%	Maximum Voltage at V_{GAIN} for 0% Gain	−0.55	−0.5	−0.45	I	V
NL, Gain	Gain Control Non-linearity, V_{IN} = ±0.5V		1.5	4	I	%
NL, A_V = 1	Signal Non-linearity, V_{IN} = 0 to ±1V, V_{GAIN} = 0.55V		0.01		V	%
A_V = 0.5	Signal Non-linearity, V_{IN} = 0 to ±1V, V_{GAIN} = 0V		0.05		V	%
A_V = 0.25	Signal Non-linearity, V_{IN} = 0 to ±1V, V_{GAIN} = −0.25V		0.2	0.5	I	%
R_{GAIN}	Resistance between V_{GAIN} and $\overline{V_{GAIN}}$	4.6	5.5	6.6	I	kΩ
I_S	Supply Current	12	14.5	17	I	mA
F_T	Off-Channel Feedthrough		−75	−50	I	dB

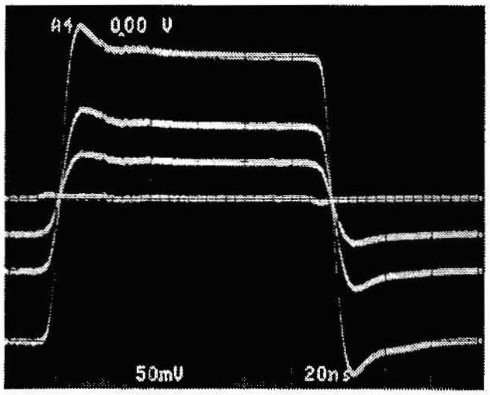
Closed Loop AC Electrical Characteristics

$V_S = \pm 15V, C_L = 15$ pF, $T_A = 25°C, A_V = 100\%$ unless otherwise noted

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
SR	Slew Rate; V_{OUT} from −3V to +3V measured at −2V and +2V	370	500		V	V/µs
BW	Bandwidth, −3 dB	45	60		III	MHz
	−1 dB		35		V	MHz
	−0.1 dB		6		V	MHz
dG	Differential Gain, AC amplitude of 286 $mV_{p\text{-}p}$ at 3.58 MHz on DC offset of −0.7, 0, and +0.7V $A_V = 100\%$		0.02		V	%
	$A_V = 50\%$		0.20		V	%
	$A_V = 25\%$		0.40		V	%
dθ	Differential Phase, AC ampitude of 286 $mV_{p\text{-}p}$ at 3.58 MHz on DC offset of −0.7, 0, and +0.7V $A_V = 100\%$		0.04		V	(°)
	$A_V = 50\%$		0.20		V	(°)
	$A_V = 25\%$		0.20		V	(°)
BW, GAIN	−3 dB Gain Control Bandwidth, V_{GAIN} Amplitude 0.5 $V_{p\text{-}p}$		20		V	MHz
T_{REC}, GAIN	Gain Control Recovery from Overload; V_{GAIN} from −0.6V to 0V		70		V	ns

Typical Performance Curves

Small-Signal Step Response for Gain = 100%, 50%, 25%, and 0%. V_S ±5V



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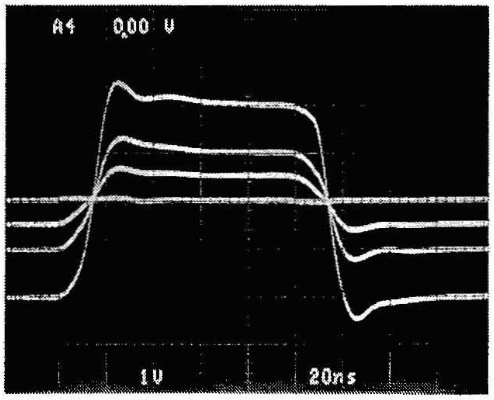
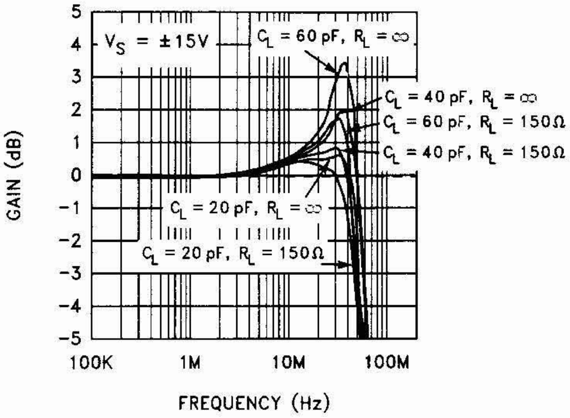
Large-Signal Step Response for Gain = 100%, 50%, 25%, and 0%. V_S ±12V



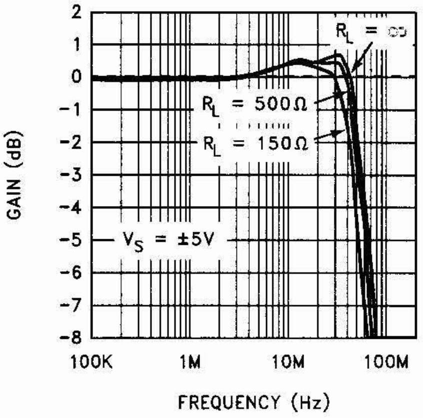
4094-3

Typical Performance Curves — Contd.

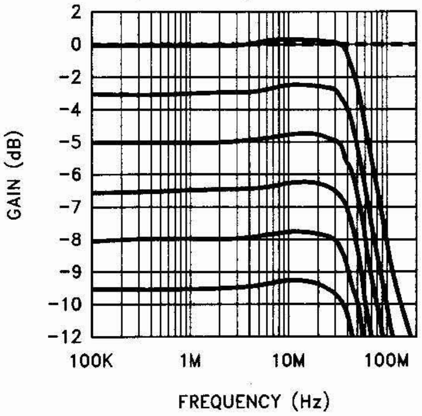
Frequency Response vs Capacitive Loading



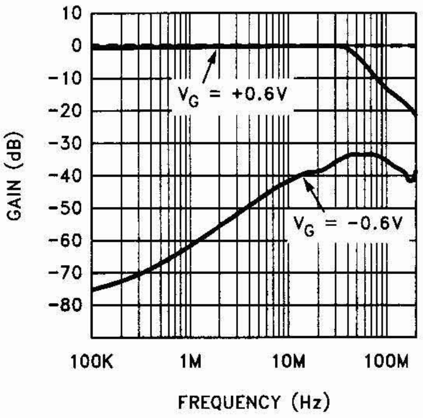
Frequency Response vs Resistive Loading



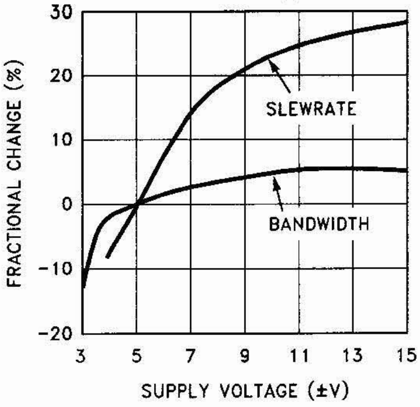
Frequency Response vs Gain



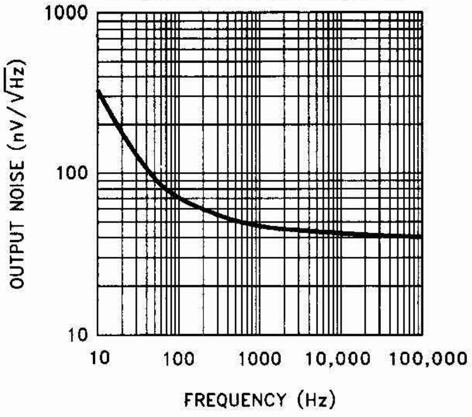
Off-Channel Isolation Over Frequency



Change in Slewrate and Bandwidth with Supply Voltage

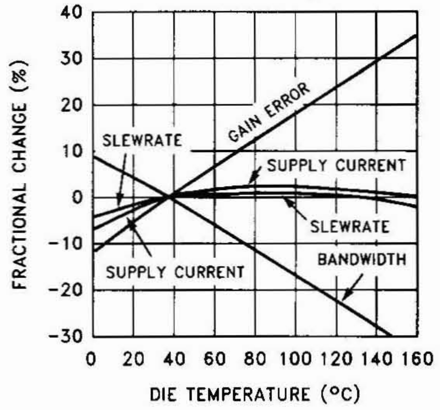


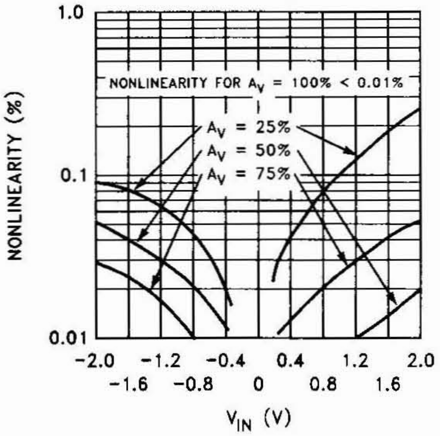
Output Noise Over Frequency

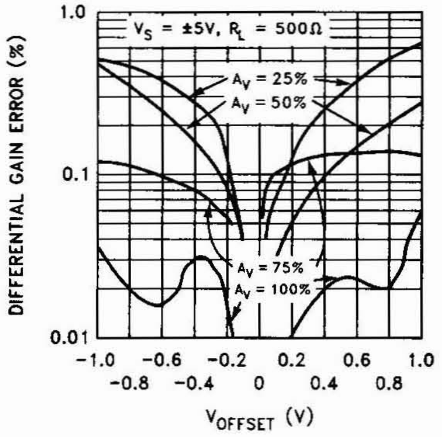


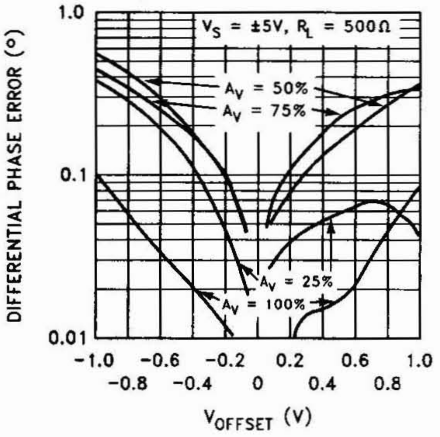
4094-4

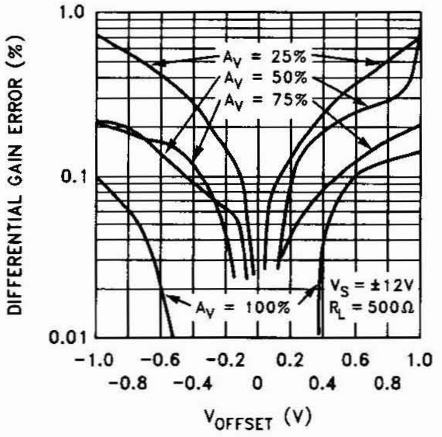
Typical Performance Curves — Contd.

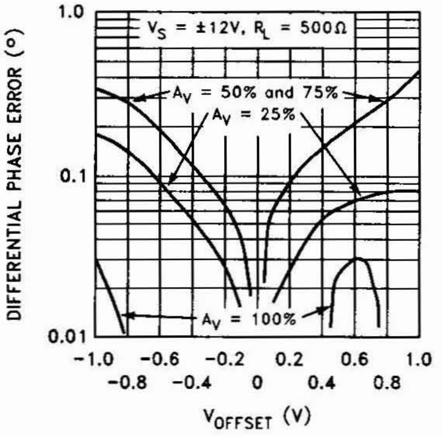

Change in 100% Gain Error, Supply Current, Slewrate and Bandwidth over Temperature


Nonlinearity vs V_{IN} for Gain = 100%, 75%, 50% and 25%


Differential Gain Error vs V_{offset} for Gain = 100%, 75%, 50% and 25%. F = 3.58 MHz

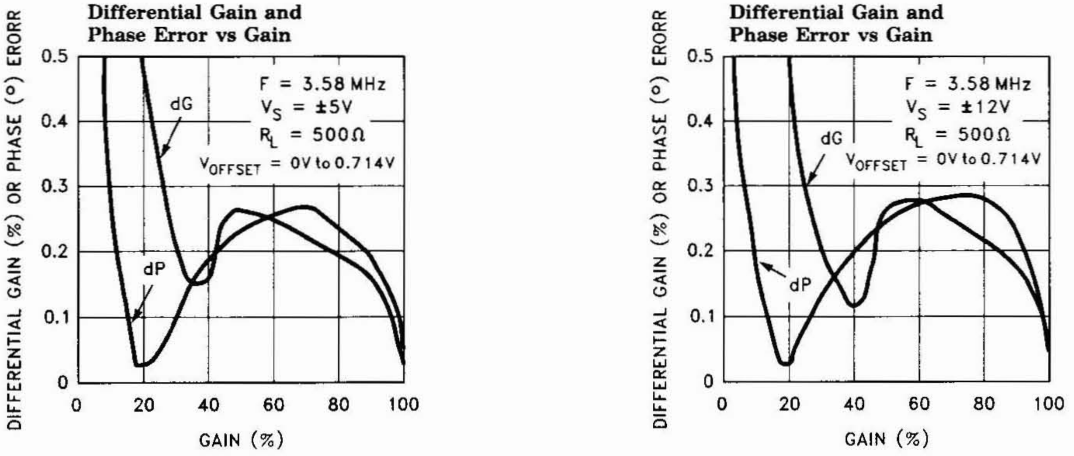

Differential Phase Error vs V_{offset} for Gain = 100%, 75%, 50% and 25%. F = 3.58 MHz


Differential Gain Error vs V_{offset} for Gain = 100%, 75%, 50% and 25%. F = 3.58 MHz


Differential Phase Error vs V_{offset} for Gain = 100%, 75%, 50% and 25%. F = 3.58 MHz

4094-5

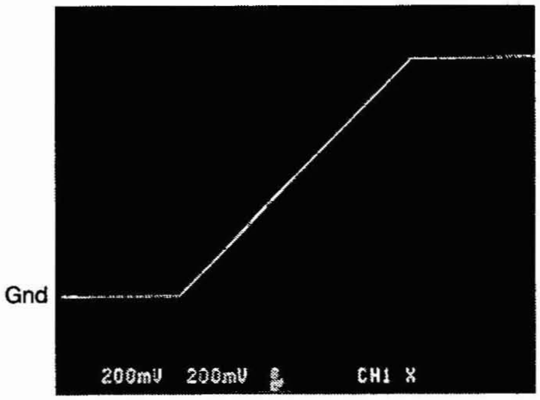
Typical Performance Curves — Contd.


Differential Gain and Phase Error vs Gain

Differential Gain and Phase Error vs Gain

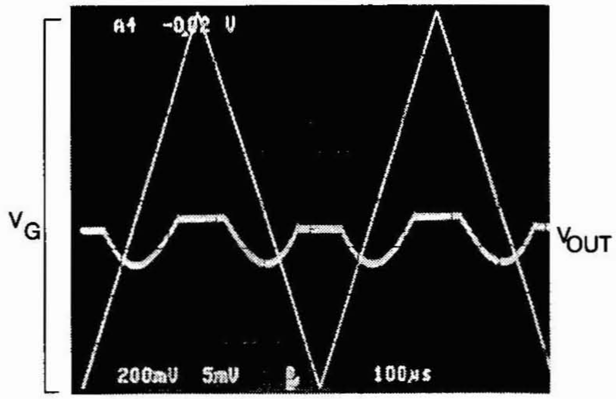
4094-6

Gain vs V_G. $1V_{DC}$ at V_{INA}



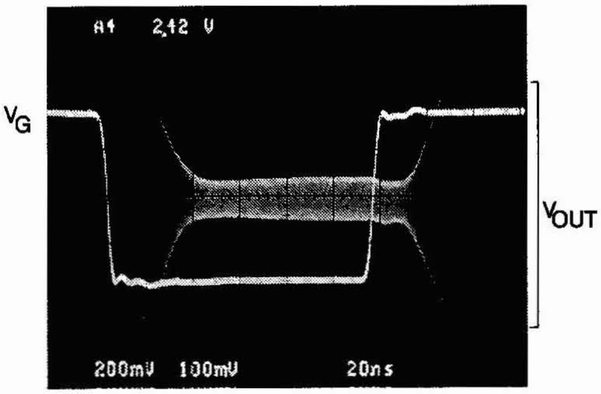
4094-7

Cross-Fade Balance. $V_{INA} = V_{INB} = 0V$



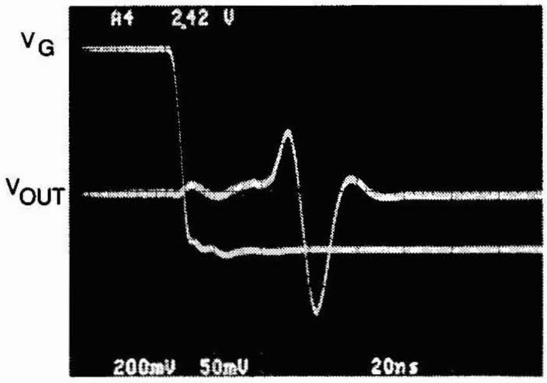
4094-8

Gain Control Response to a Non-Overloading Step, Constant Sinewave at V_{INA}



4094-9

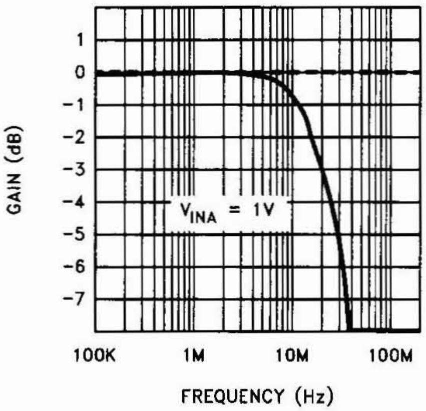
V_{GAIN} Overload Recovery Response



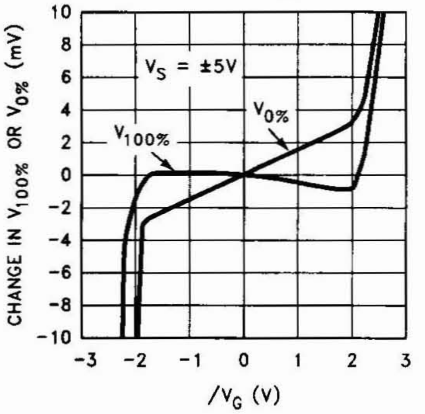
4094-10

Typical Performance Curves — Contd.

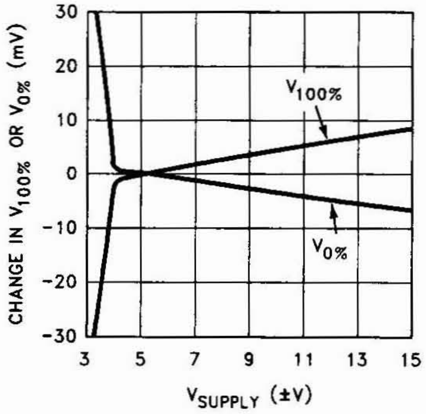
Gain Control Gain vs Frequency



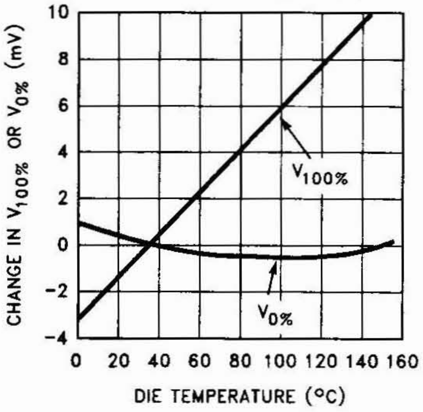
Change in V(100%) and V(0%) of Gain Control vs /V_G Offset



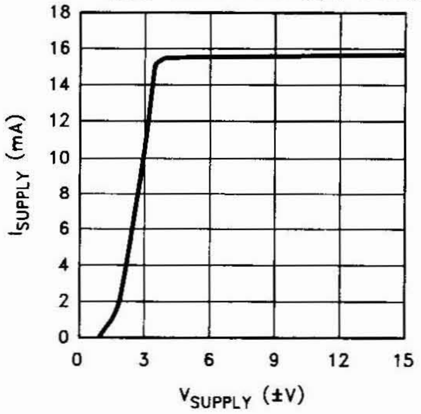
Change in V(100%) and V(0%) of Gain Control vs Supply Voltage



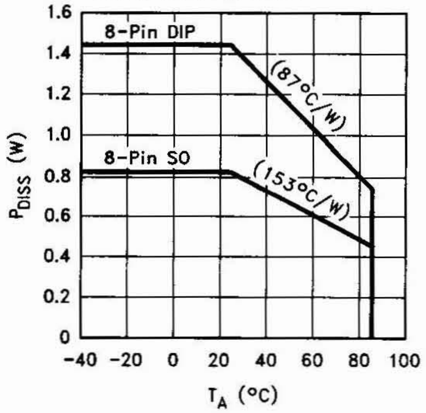
Change in V(100%) and V(0%) of Gain Control vs Die Temperature



Supply Current vs Supply Voltage



Maximum Dissipation vs Ambient Temperature



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Applications Information

The EL4094 is a self-contained and calibrated fader subsystem. When a given channel has 100% gain the circuit behaves as a current-feedback amplifier in unity-gain connection. As such, video and transfer distortions are very low. As the gain of the input is reduced, a 2-quadrant multiplier is gradually introduced into the signal path and distortions increase with reducing gain.

The input impedance also changes with gain setting, from about 1 MΩ at 100% gain down to 16 kΩ at zero gain. To maximize gain accuracy and linearity, the inputs should be driven from source impedances of 500Ω or less.

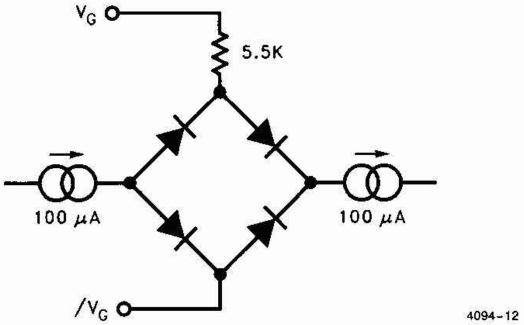
Linearity

The EL4094 is designed to work linearly with ±2V inputs, but lowest distortion occurs at ±1V levels and below. Errors are closer to those of a good current-feedback amplifier above 90% gain.

Low-frequency linearity is 0.1% or better for gains 25% to 100% and inputs up to 1V. NTSC differential gain and phase errors are better than 0.3% and 0.3° for the 25% to 100% gain range. These distortions are not strongly affected by supply voltage nor output loading, at least down to 150Ω. For settling to 0.1%, however, it is best to not load the output heavily and to run the EL4094 on the lowest practical supply voltages, so that thermal effects are minimized.

Gain Control Inputs

The gain control inputs are differential and may be biased at any voltage as long as $/V_{GAIN}$ is less than 2.5V below V+ and 3V above V−. The differential input impedance is 5.5 kΩ, and the common-mode impedance is more than 500 kΩ. With zero differential voltage on the gain inputs, both signal inputs have a 50% gain factor. Nominal calibration sets the 100% gain of V_{INA} input at +0.5V of gain control voltage, and 0% at −0.5V of gain control. V_{INB}'s gain is complementary to that of V_{INA}; +0.5V of gain control sets 0% gain at V_{INB} and −0.5V gain control sets 100% V_{INB} gain. The gain control does not have a completely abrupt transition at the 0% and 100% points. There is about 10 mV of "soft" transfer at the gain endpoints. To obtain the most accurate 100% gain factor or best attenuation at 0% gain, it is necessary to overdrive the gain control input by 30 mV or more. This would set the gain control voltage range as −0.565V to +0.565V, or 30 mV beyond the maximum guaranteed 0% to 100% range. In fact, the gain control inputs are very complex. Here is a representation of the terminals:



Representation of Gain Control Inputs V_G and $/V_G$

For gain control inputs between ±0.5V (±90 µA), the diode bridge is a low impedance and all of the current into Vg flows back out through $/V_g$. When gain control inputs exceed this amount, the bridge becomes a high impedance as some of the diodes shut off, and the V_g impedance rises sharply from the nominal 5.5KΩ to about 500KΩ. This is the condition of gain control overdrive. The actual circuit produces a much sharper overdrive characteristic than does the simple diode bridge of this representation.

The gain input has a 20 MHz −3 dB bandwidth and 17 ns risetime for inputs to ±0.45V. When the gain control voltage exceeds the 0% or 100% values, a 70 ns overdrive recovery transient will occur when it is brought back to linear range. If quicker gain overdrive response is required, the Force control inputs of the EL4095 can be used.

Output Loading

The EL4094 does not work well with heavy capacitive loads. Like all amplifier outputs, the output impedance becomes inductive over frequency resonating with a capacitive load. The effective output inductance of the EL4094 is about 350 nH. More than 50 pF will cause excessive frequency response peaking and transient ringing. The problem can be solved by inserting a low-value resistor in series with the load, 22Ω or more. If a series resistance cannot be used, then adding a 300Ω or less load resistor to ground or a "snubber" network may help. A snubber is a re-

Applications Information — Contd.

sistor in series with a capacitor, 150Ω and 100 pF being typical values. The advantage of a snubber is that it does not draw DC load current.

Unterminated coaxial line loads can also cause resonances, and they should be terminated either at the far end or a series back-match resistor installed between the EL4094 and the cable.

The output stage can deliver up to 140 mA into a short-circuit load, but it is only rated for a continuous 35 mA. More continuous current can cause reliability problems with the on-chip metal interconnect. Video levels and loads cause no problems at all.

Noise

The EL4094 has a very simple noise characteristic: the output noise is constant (40 nV/√Hz wideband) for all gain settings. The input-referred noise is then the output noise divided by the gain. For instance, at a gain of 50% the input noise is 40 nV/√Hz/0.5, or 80 nV/√Hz.

Bypassing

The EL4094 is fairly tolerant of power-supply bypassing, but best multiplier performance is obtained with closely connected 0.1 μF ceramic capacitors. The leaded chip capacitors are good, but neither additional tantalums nor chip components are necessary. The signal inputs can oscillate locally when connected to long lines or unterminated cables.

Power Dissipation

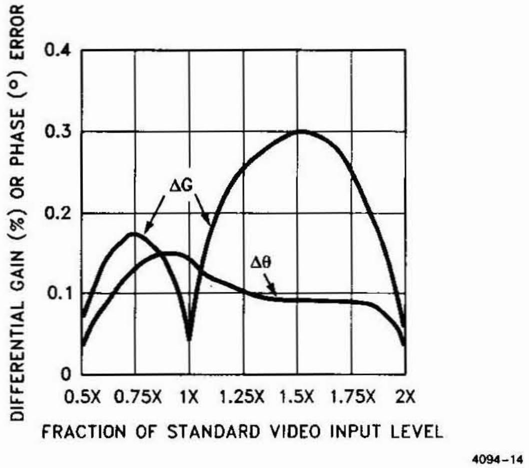
Peak die temperature must not exceed 150°C. At this temperature, the epoxy begins to soften and becomes unstable, chemically and mechanically. This allows 75°C internal temperature rise for a 75°C ambient. The EL4094 in the 8-pin PDIP package has a thermal resistance of 87°/W, and can thus dissipate 862 mW at a 75°C ambient temperature. The device draws 17 mA maximum supply current, only 510 mW at ±15V supplies, and the circuit has no dissipation problems in this package.

The SO-8 surface-mount package has a 153°/W thermal resistance with the EL4094, and only 490 mW can be dissipated at 75°C ambient temperature. The EL4094 thus cannot be operated with ±15V supplies at 75°C in the surface-mount package; the supplies should be reduced to ±5V to ±12V levels, especially if extra dissipation occurs when driving a load.

The EL4094 as a Level Adjust

A common use for gain controls is as an input signal leveller—a circuit that scales too-large or too-small signals to a standard amplitude. A typical situation would be to scale a variable video input by +6 dB to −6 dB to obtain a standard amplitude. The EL4094 cannot provide more than 0 dB gain, but it can span the range of 0 dB to −12 dB with another amplifier gaining the output up by 6 dB. The simplest way to obtain the range is to simply ground the B input and vary the gain of the signal applied to the A input. The disadvantage of this approach is that linearity degrades at low gains. By connecting the signal to the A input of the EL4094 and the signal attenuated by 12 dB to the B input, the gain control offers the highest linearity possible at 0 dB and −12 dB extremes, and good performance between. The circuit is shown on the following page.

The EL4095 can be used to provide the required gains without the extra amplifier. In practice, the gain control is adjusted to set a standard video level regardless of the input level. The EL4583 sync-separator has a recovered amplitude output that can be used to servo the gain control voltage. Here is the curve of differential gain and phase distortion for varying inputs, with the output set to standard video level:



Differential Gain and Phase of Linearized Level Control

Applications Information — Contd.

The differential gain error is kept to 0.3% and the differential phase to 0.15° or better over the entire input range.

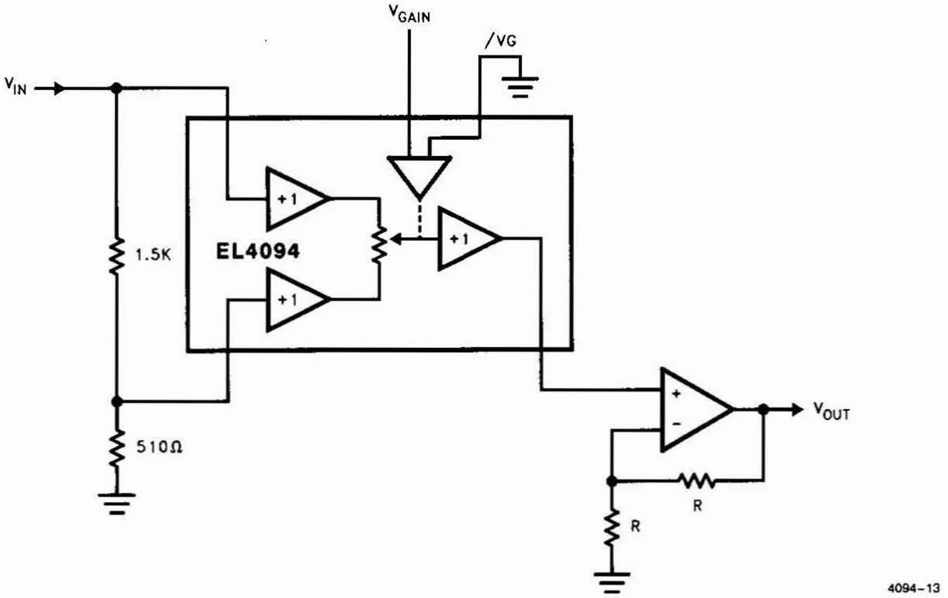
The EL4094 as an Adjustable Filter

Equalizers are used to adjust the delay or frequency response of systems. A typical use is to compensate for the high-frequency loss of a cable system ahead of the cable so as to create a flat response at the far end. A generalized scheme with the EL4094 is shown below.

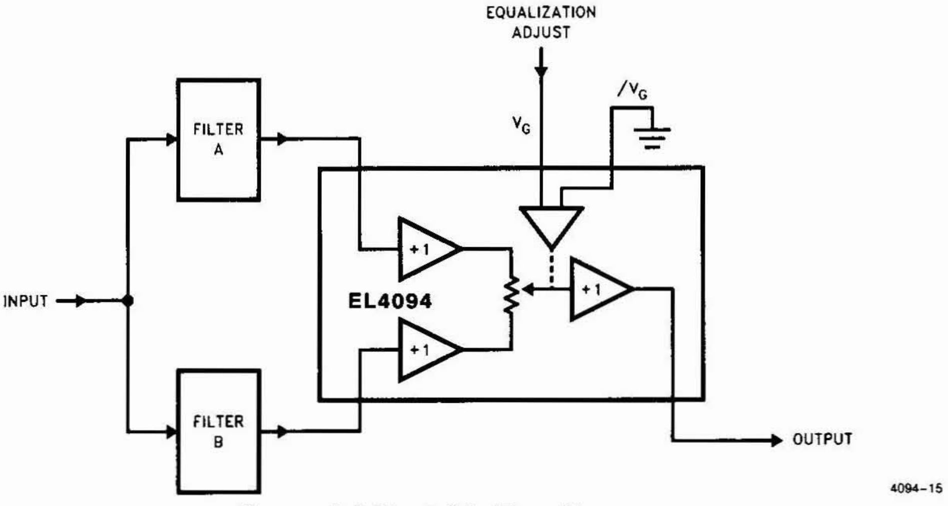
For an adjustable preemphasis filter, for instance, filter A might be an all-pass filter to compensate for the delay of filter B, a peaking filter. Fading the gain from A to B provides a variable amount of peaking, but constant delay.

The EL4094 as a Phase Modulator

To make a phase modulator, filter A might be a leading-phase network, and filter B a lagging network. The wide bandwidth of the gain-control input allows wideband phase modulation of the carrier applied to the main input. Of course, the carrier and gain inputs must not be digital but be reasonably clean sinewaves for the modulation to be accurate.



+6 dB to −6 dB Linearized Level Control



General Adjustable Equalizer

EL4094C Macromodel

This macromodel is offered to allow simulation of general EL4094 behavior. We have included these characteristics:

Small-signal frequency response
Output loading effects
Input impedance
Off-channel feedthrough
Output impedance over frequency

Signal path DC distortions
V_{GAIN} I-V characteristics
V_{GAIN} overdrive recovery delay
100% gain error

These will give a good range of results for various operating conditions, but the macromodel does not behave identically as the circuit in these areas:

Temperature effects
Signal overload effects
Signal and $/V_G$ operating range
Current-limit
Video and high-frequency distortions
Supply voltage effects
Slewrate limitations
Noise
Power supply interactions

The macromodel's netlist is based on the Pspice simulator (copywritten by the Microsim Company). Other simulators may not support the POLY function, which is used to implement multiplication as well as square-low nonlinearities.

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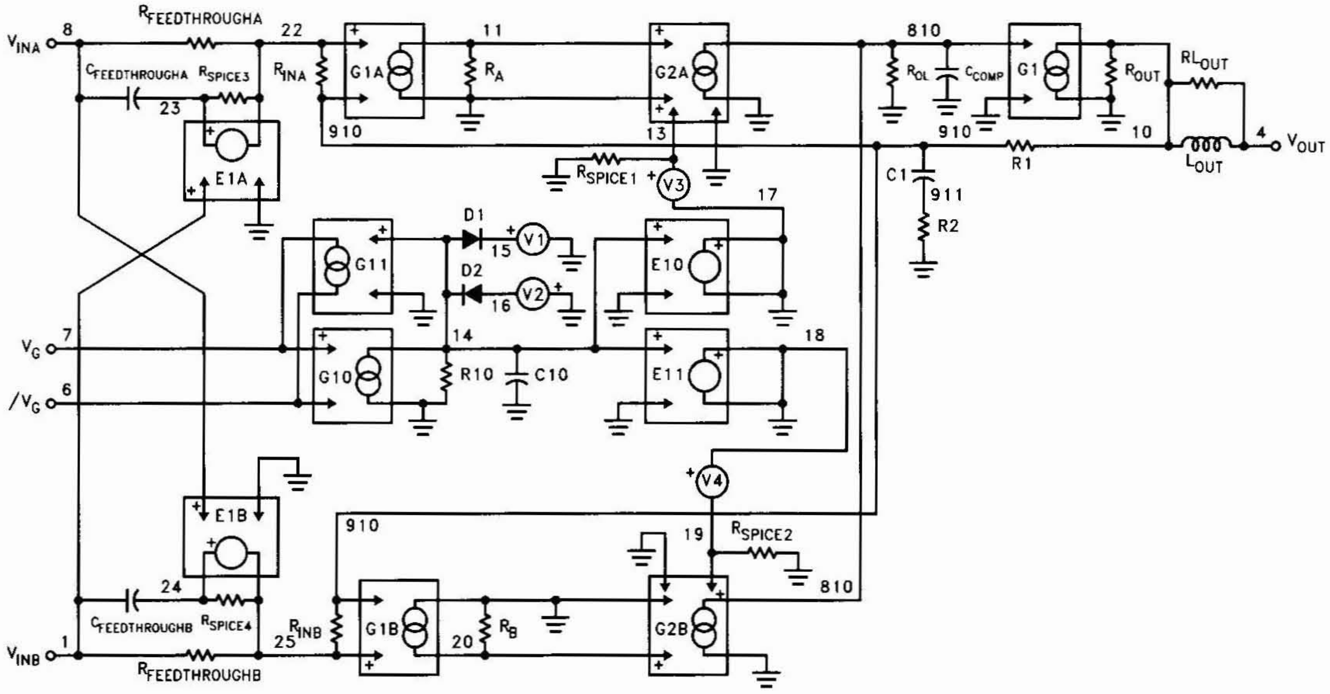
******
******
*                      VINB
*                      |      VOUT
*                      |      |      /VG
*                      |      |      |     VG
*                      |      |      |     |     VINA
*                      |      |      |     |     |
.subckt EL4094subckt   (1     4      6     7     8)
***
ROL 810 0 290k
Ccomp 810 0 3.5p
G1 10 0 810 0 -10
ROUT 10 0 0.1
LOUT 10 4 350.200n
RLOUT 10 4 80
r1 10 910 10
c1 910 911 300p
r2 911 0 90
***
*** Input channel A
***
RINA 22 910 16k
ra 11 0 1k
Cfeedthrougha 23 8 130p
Rfeedthrougha 8 22 1.0
E1a 23 22 1 0 1.0
Rspice3 23 22 1E12
G1a 11 0 POLY(1) (22, 910) 0.0 0.001 -3E-6
G2a 810 0 POLY(2) (11,0) (13, 0) 0.0 0.0 0.0 0.0 0.001
***
***Input channel B
***
RINB 25 910 16k
rb 20 0 1k
Cfeedthroughb 24 1 130p
Rfeedthroughb 1 25 1.0
E1b 24 25 8 0 1.0
Rspice4 24 25 1E12
G1b 20 0 POLY(1) (25, 910) 0.0 0.001 -3E-6
G2b 810 0 POLY(2) (20,0) (19, 0) 0.0 0.0 0.0 0.0 0.001
***
***Gain control
***
Rspice1 13 0 1E12
Rspice2 18 0 1E12
R10 14 0 1E7
C10 14 0 8E-16
D1 14 15 Dclamp
D2 16 14 Dclamp
.model Dclamp D (TT=200n)
V1 15 0 4999.3
V2 0 16 4999.3
V3 13 17 0.5
V4 19 18 0.5
G10 14 0 7 6 -0.001
G11 7 6 14 0 -2E-8
E10 17 0 14 0 1E-4
E11 18 0 14 0 -1E-4
***
.ends
******
```

EL4094C Macromodel — Contd.


V_{INA}
8
$R_{FEEDTHROUGHA}$
22
11
810
$C_{FEEDTHROUGHA}$
R_{SPICE3}
R_{INA}
G1A
R_A
G2A
R_{OL}
C_{COMP}
G1
R_{OUT}
RL_{OUT}
23
910
13
910
10
4
V_{OUT}
R1
L_{OUT}
E1A
R_{SPICE1}
V3
C1
911
R2
17
D1
G11
15
V1
E10
D2
16
V2
V_G
7
14
18
G10
R10
C10
E11
$/V_G$
6
V4
E1B
910
19
R_{SPICE2}
810
24
$C_{FEEDTHROUGHB}$
R_{SPICE4}
R_{INB}
G1B
R_B
G2B
V_{INB}
1
25
20
$R_{FEEDTHROUGHB}$

4094-16

EL4094 Macromodel Schematic

EL4095C

Video Gain Control/Fader/Multiplexer

Features

- Full function video fader
- 0.02%/0.02° differential gain/phase @ 100% gain
- 25 ns multiplexer included
- Output amplifier included
- Calibrated linear gain control
- ± 5V to ± 15V operation
- 60 MHz bandwidth
- Low thermal errors

Applications

- Video faders/wipers
- Gain control
- Graphics overlay
- Video text insertion
- Level adjust
- Modulation

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL4095CN	−40°C to +85°C	14 Pin P-DIP	MDP0031
EL4095CS	−40°C to +85°C	SO-14	MDP0027

General Description

The EL4095C is a versatile variable-gain building block. At its core is a fader which can variably blend two inputs together and an output amplifier that can drive heavy loads. Each input appears as the input of a current-feedback amplifier and with external resistors can separately provide any gain desired. The output is defined as:

$$V_{OUT} = A^*V_{INA}\,(0.5V + V_{GAIN}) + B^*V_{INB}\,(0.5V - V_{GAIN}),$$

where A and B are the fed-back gains of each channel.

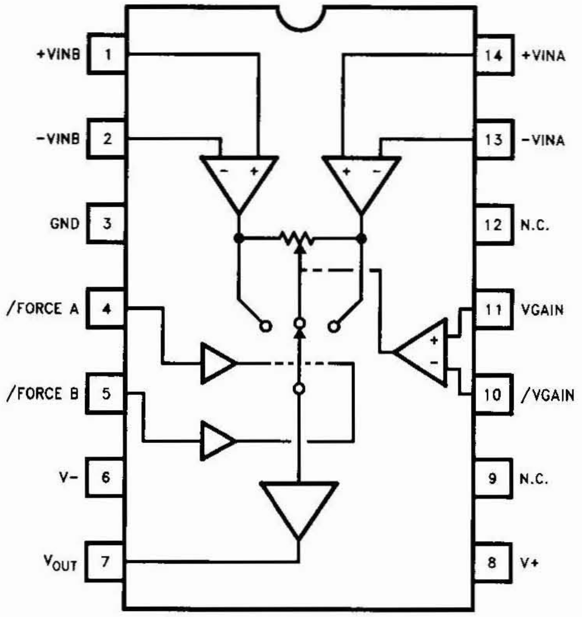
Additionally, two logic inputs are provided which each override the analog V_{GAIN} control and force 100% gain for one input and 0% for the other. The logic inputs switch in only 25 ns and provide high attenuation to the off channel, while generating very small glitches.

Signal bandwidth is 60 MHz, and gain-control bandwidth 20 MHz. The gain control recovers from overdrive in only 70 ns.

The EL4095C operates from ± 5V to ± 15V power supplies, and is available in both 14-pin DIP and narrow surface mount packages.

Connection Diagram

14-Pin DIP, SO



Top View

Manufactured under U.S. Patent No. 5,321,371, 5,374,898

EL4095C

Video Gain Control/Fader/Multiplexer

Absolute Maximum Ratings (T_A = 25°C)

V_S+	Supply Voltage	+18V
V_S	Voltage between V_S+ and V_S-	+33V
$+V_{INA}$, $+V_{INB}$	Input Voltage	$(V_S-) - 0.3V$ to $(V_S+) + 0.3V$
I_{IN}	Current Into $-V_{INA}$, $-V_{INB}$	5 mA
V_{GAIN}	Input Voltage	$V_{\overline{GAIN}} \pm 5V$
$V_{\overline{GAIN}}$	Input Voltage	V_S- to V_S+
V_{FORCE}	Input Voltage	−1V to +6V
I_{OUT}	Output Current	±35 mA
T_A	Operating Temperature Range	−40°C to +85°C
T_J	Operating Junction Temperature	0°C to +150°C
T_{ST}	Storage Temperature Range	−65°C to +150°C
Internal Power Dissipation		See Curves

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, T_A = 25°C, $V_{\overline{GAIN}}$ ground unless otherwise specified

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
V_{OS}	Input Offset Voltage		1.5	5	I	mV
I_{B+}	$+V_{IN}$ Input Bias Current		5	10	I	μA
I_{B-}	$-V_{IN}$ Input Bias Current		10	50	I	μA
CMRR	Common Mode Rejection	65	80		I	dB
−CMRR	$-V_{IN}$ Input Bias Current Common Mode Rejection		0.5	1.5	I	μA/V
PSRR	Power Supply Rejection Ratio	65	95		I	dB
−IPSR	$-V_{IN}$ Input Current Power Supply Rejection Ratio		0.2	2	I	μA/V
R_{OL}	Transimpedance	0.2	0.4		I	MΩ
R_{IN-}	$-V_{IN}$ Input Resistance		80		V	Ω
V_{IN}	$+V_{IN}$ Range	(V−) + 3.5		(V+) −3.5	I	V
V_O	Output Voltage Swing	(V−) +2		(V+) −2	I	V
I_{SC}	Output Short-Circuit Current	80	125	160	I	mA
V_{IH}	Input High Threshold at Force A or Force B Inputs			2.0	I	V
V_{IL}	Input Low Threshold at Force A or Force B Inputs	0.8			I	V
I_{FORCE}, High	Input Current of Force A or Force B, V_{FORCE} = 5V			−50	I	μA
I_{FORCE}, Low	Input Current of Force A or Force B, V_{FORCE} = 0V		−440	−650	I	μA

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 15V, T_A = 25°C$, unless otherwise specified

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
Feedthrough, Forced	Feedthrough of Deselected Input to Output, Deselected Input at 100% Gain Control	60	75		I	dB
V_{GAIN}, 100%	Minimum Voltage at V_{GAIN} for 100% Gain	0.45	0.5	0.55	I	V
V_{GAIN}, 0%	Maximum Voltage at V_{GAIN} for 0% Gain	−0.55	−0.5	−0.45	I	V
NL, Gain	Gain Control Non-linearity, $V_{IN} = \pm 0.5V$		2	4	I	%
R_{IN}, VG	Impedance between V_{GAIN} and $\overline{V_{GAIN}}$	4.5	5.5	6.5	I	kΩ
NL, $A_V = 1$ $A_V = 0.5$ $A_V = 0.25$	Signal Non-linearity, $V_{IN} = \pm 1V, V_{GAIN} = 0.55V$ Signal Non-linearity, $V_{IN} = \pm 1V, V_{GAIN} = 0V$ Signal Non-linearity, $V_{IN} = \pm 1V, V_{GAIN} = -0.25V$		<0.01 0.03 0.07	 0.4	V V I	% % %
I_S	Supply Current		17	20	I	mA

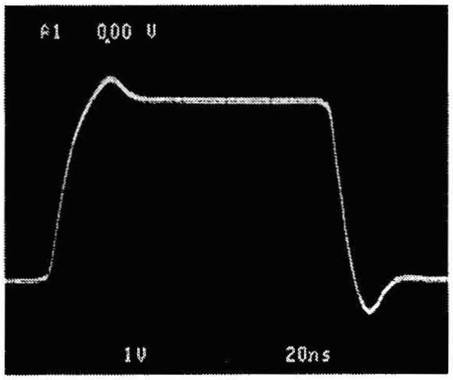
Closed Loop AC Electrical Characteristics

$V_S = \pm 15V, A_V = +1, R_F = R_{IN} = 1\ k\Omega, R_L = 500\Omega, C_L = 15\ pF, C_{IN-} = 2\ pF, T_A = 25°C, A_V = 100\%$ unless otherwise noted

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
SR	Slew Rate; V_{OUT} from −3V to +3V Measured at −2V and +2V		330		V	V/µs
BW	Bandwidth −3 dB −1 dB −0.1 dB		60 30 6		V	MHz MHz MHz
dG	Differential Gain; AC Amplitude of 286 mV_{p-p} at 3.58 MHz on DC Offset of −0.7V, 0V and +0.7V $A_V = 100\%$ $A_V = 50\%$ $A_V = 25\%$		 0.02 0.07 0.07		V	 % % %
dθ	Differential Phase; AC Amplitude of 286 mV_{p-p} at 3.58 MHz on DC Offset of −0.7V, 0V and +0.7V $A_V = 100\%$ $A_V = 50\%$ $A_V = 25\%$		 0.02 0.05 0.15		V	 ° ° °
T_S	Settling Time to 0.2%; V_{OUT} from −2V to +2V $A_V = 100\%$ $A_V = 25\%$		 100 100		V	 ns ns
T_{FORCE}	Propagation Delay from $V_{FORCE} = 1.4V$ to 50% Output Signal Enabled or Disabled Amplitude		25		V	ns
BW, Gain	−3 dB Gain Control Bandwidth, V_{GAIN} Amplitude 0.5 V_{P-P}		20		V	MHz
T_{REC}, Gain	Gain Control Recovery from Overload; V_{GAIN} from −0.7V to 0V		70		V	ns

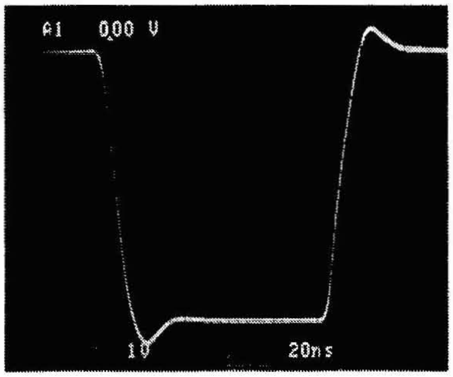
Typical Performance Curves

Large-Signal Pulse Response Gain = +1



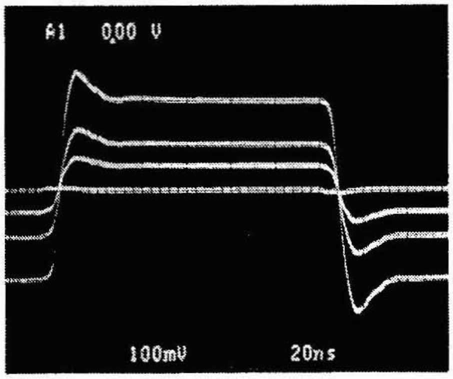
4095-6

Large-Signal Pulse Response Gain = −1



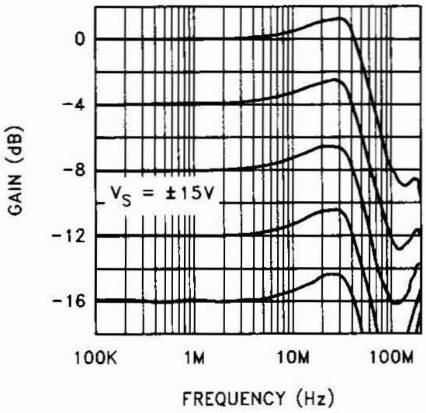
4095-7

Small-Signal Pulse Response for Various Gains



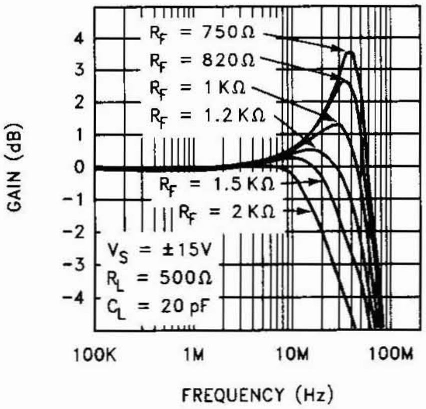
4095-8

Frequency Response for Different Gains-A_V = +1



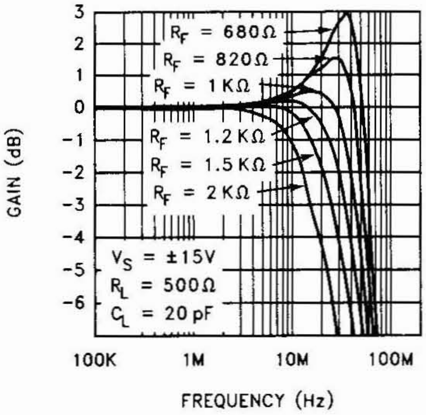
4095-9

Frequency Response with Different Values of R_F − Gain = +1



4095-10

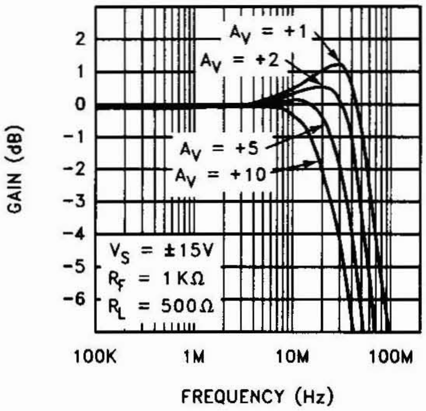
Frequency Response with Different Values of R_F − Gain = −1



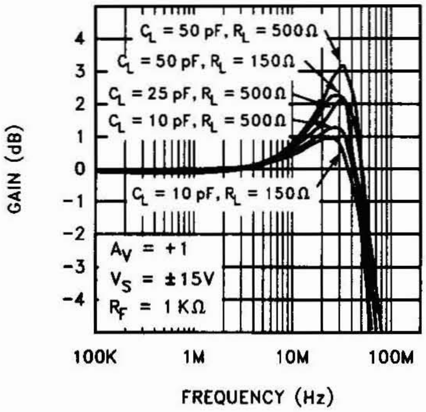
4095-11

Typical Performance Curves — Contd.

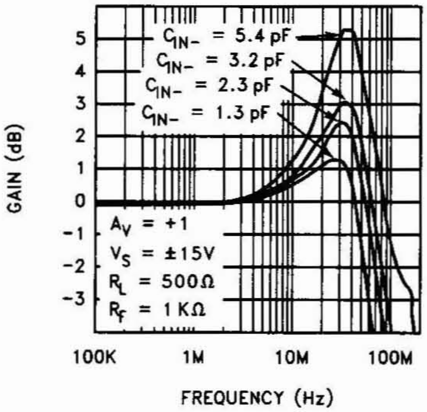
Frequency Response with Different Gains



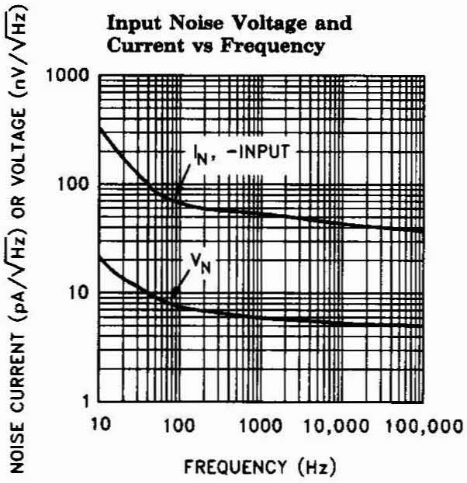
Frequency Response with Various Load Capacitances and Resistances



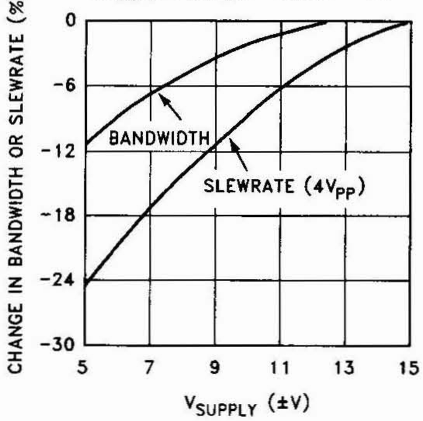
Frequency Response with Various Values of Parasitic C_{IN-}



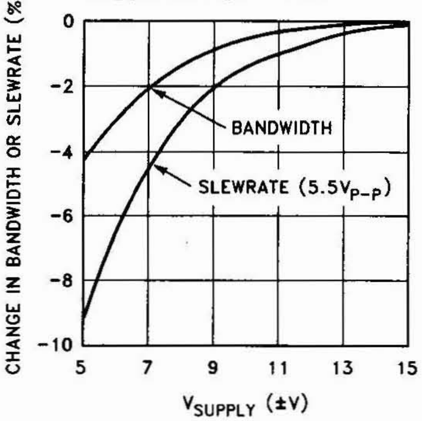
Input Noise Voltage and Current vs Frequency



Change in Bandwidth and Slewrate with Supply Voltage − Gain = +1



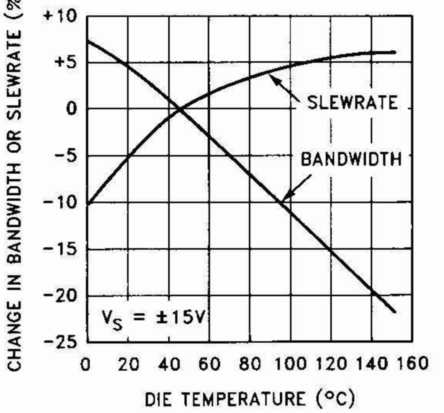
Change in Bandwidth and Slewrate with Supply Voltage − Gain = −1



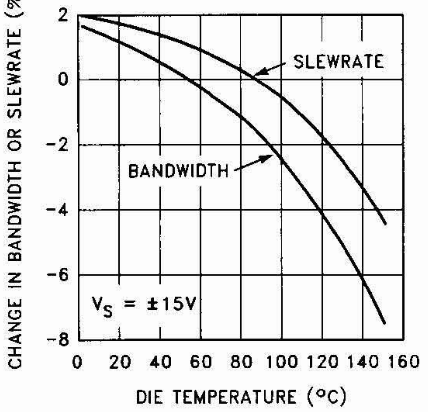
4095-12

Typical Performance Curves — Contd.

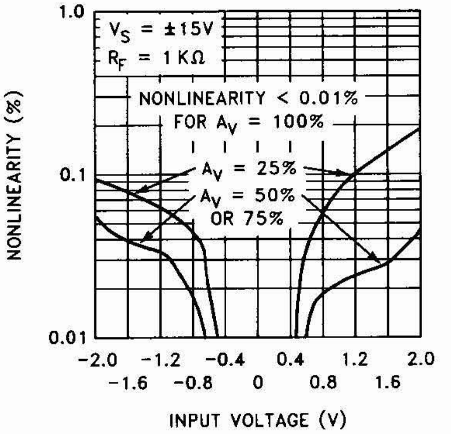
Change in Bandwidth and Slewrate with Temperature − Gain = +1



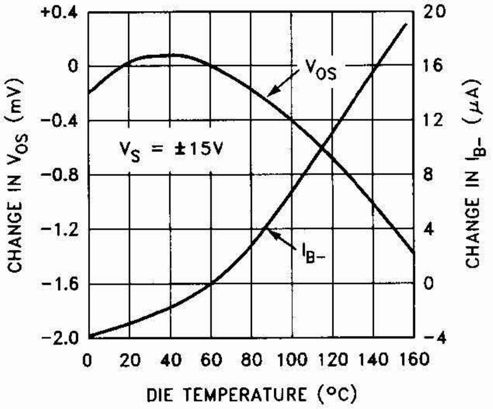
Change in Bandwidth and Slewrate with Temperature − Gain = −1



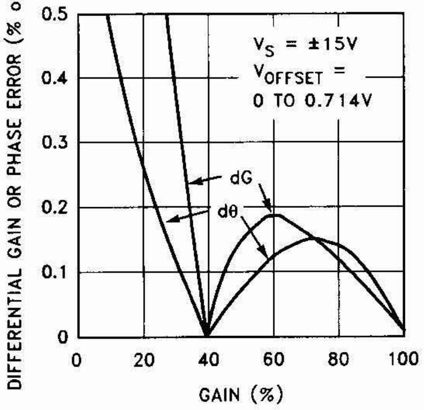
DC Nonlinearity vs Input Voltage − Gain = +1



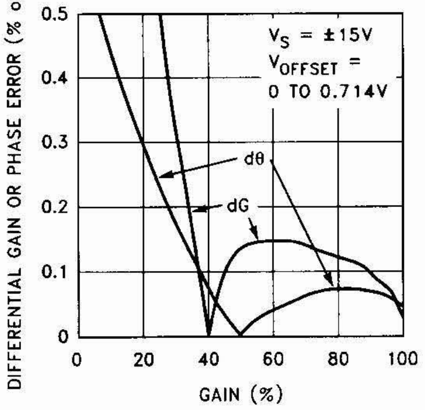
Change in V_{OS} and I_{B-} vs die Temperature



Differential Gain and Phase Errors vs Gain Control Setting − Gain = +1



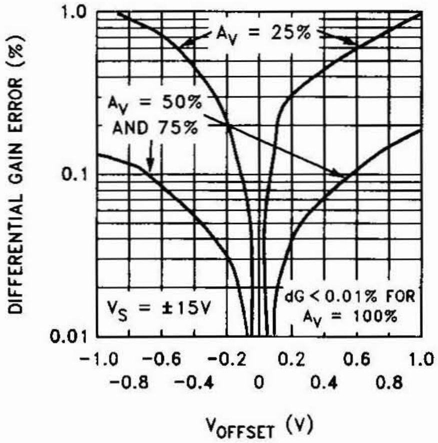
Differential Gain and Phase Errors vs Gain Control Setting − Gain = −1



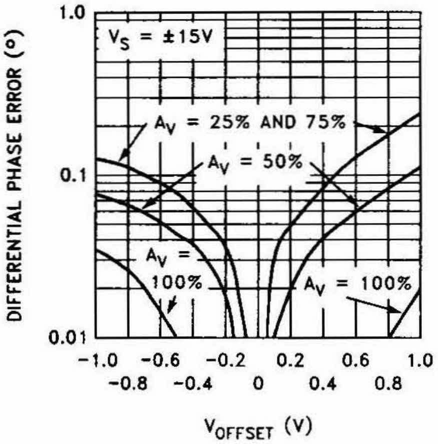
4095-13

Typical Performance Curves — Contd.

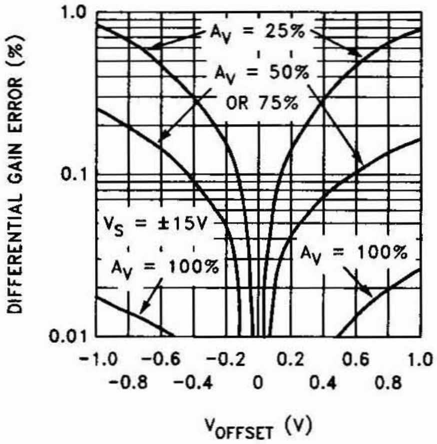
Differential Phase Error vs DC Offset − Gain = +1



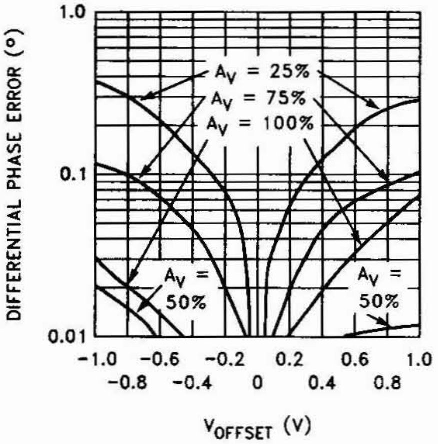
Differential Phase Error vs DC Offset − Gain = +1



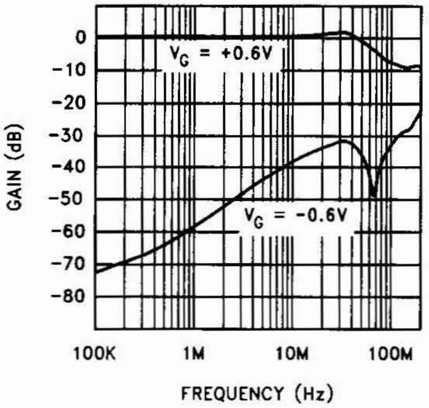
Differential Phase Error vs DC Offset − Gain = −1



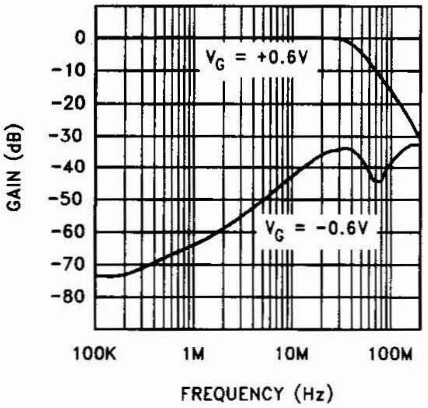
Differential Phase Error vs DC Offset − Gain = −1



Attenuation over Frequency − Gain = +1



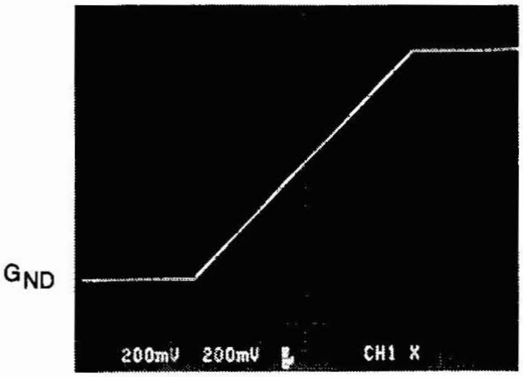
Attenuation over Frequency − Gain = −1



4095-14

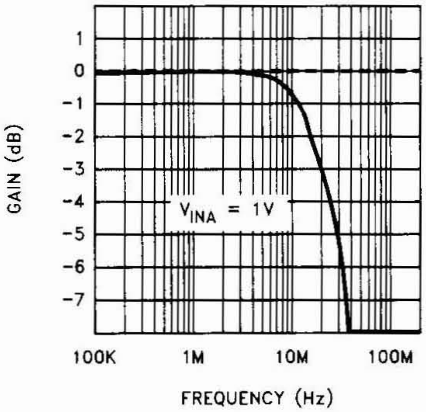
Typical Performance Curves — Contd.

Gain vs V_G (1 V_{DC} at V_{INA})



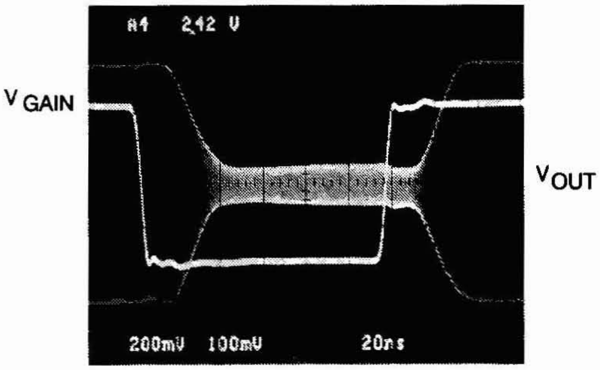
4095-15

Gain Control Gain vs Frequency



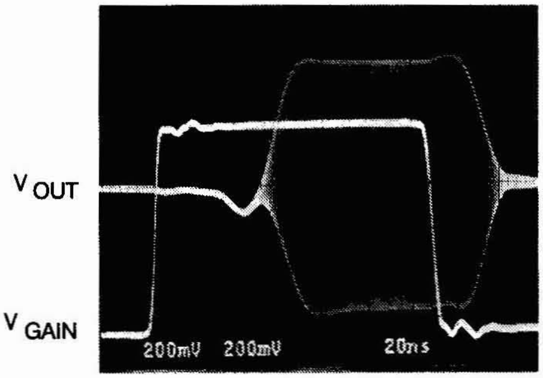
4095-16

Gain Control Response to a Non-Overloading Step, Constant Sinewave at V_{INA}



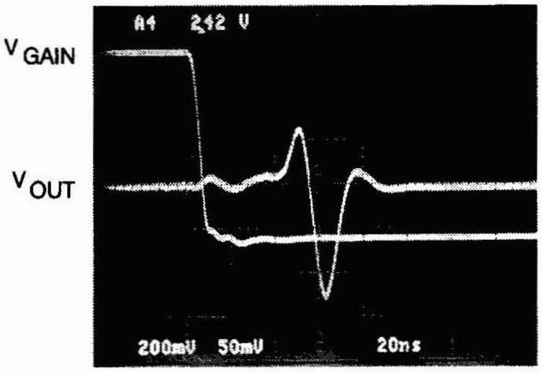
4095-17

V_{GAIN} Overload Recovery Delay



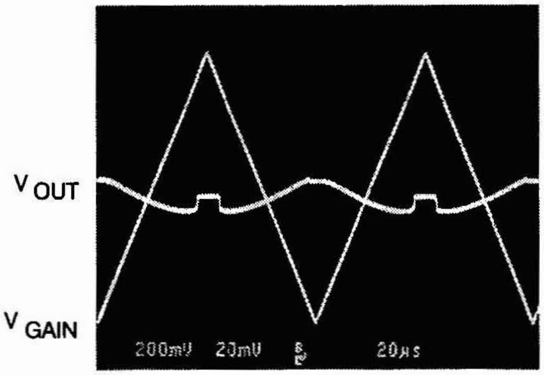
4095-18

V_{GAIN} Overload Recovery Response—No AC Input



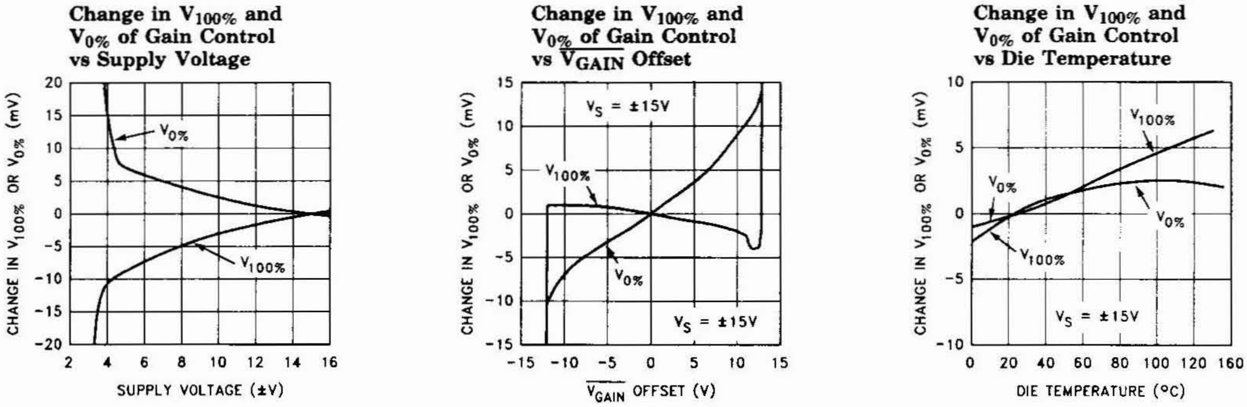
4095-19

Cross-Fade Balance −0V on A_{IN} and B_{IN}; Gain = +1



4095-20

Typical Performance Curves — Contd.



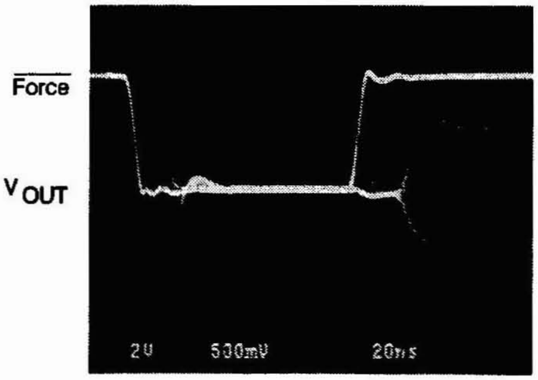
Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs Supply Voltage

Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs $\overline{V_{GAIN}}$ Offset

Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs Die Temperature

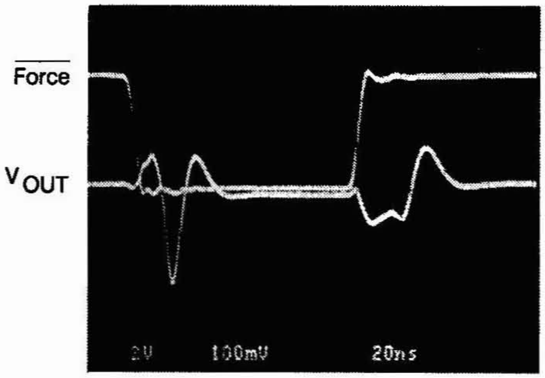
4095-21

$\overline{\text{Force}}$ Response

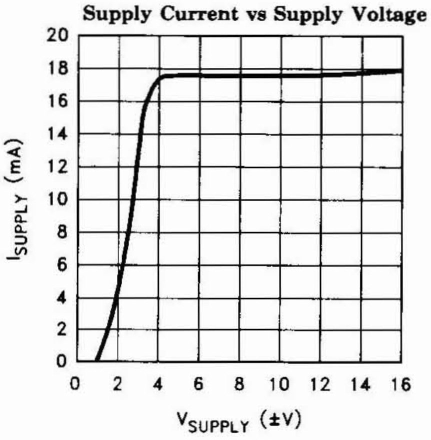


4095-22

$\overline{\text{Force}}$-Induced Output Transient

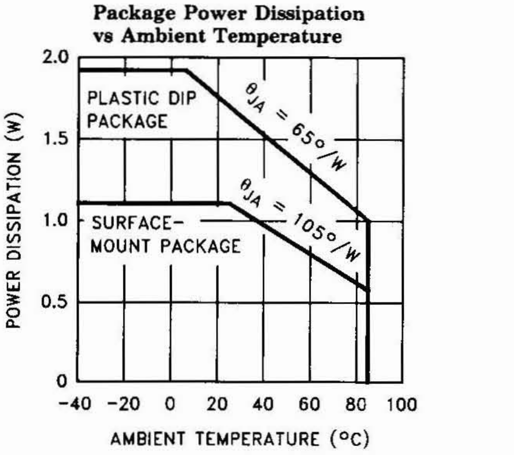


4095-23



Supply Current vs Supply Voltage

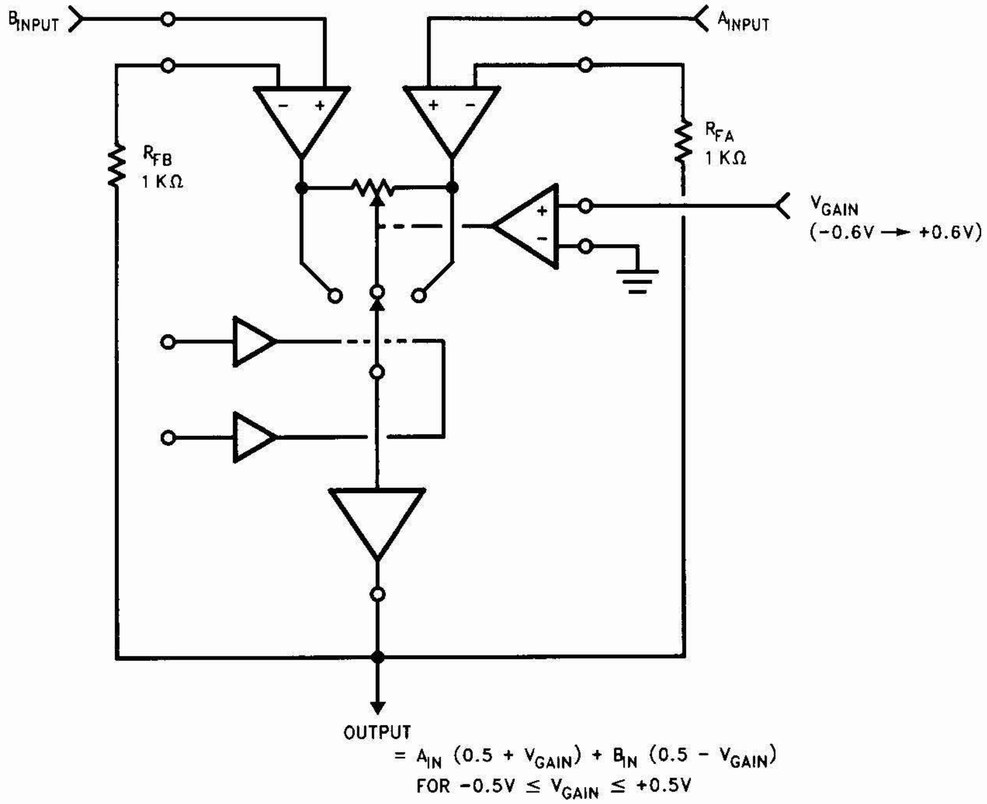
4095-24



Package Power Dissipation vs Ambient Temperature

4095-25

Test Circuit, $A_V = +1$


B_{INPUT}
A_{INPUT}
R_{FB}
1 KΩ
R_{FA}
1 KΩ
V_{GAIN}
(−0.6V → +0.6V)
OUTPUT
= A_{IN} (0.5 + V_{GAIN}) + B_{IN} (0.5 − V_{GAIN})
FOR −0.5V ≤ V_{GAIN} ≤ +0.5V

4095-26

Applications Information

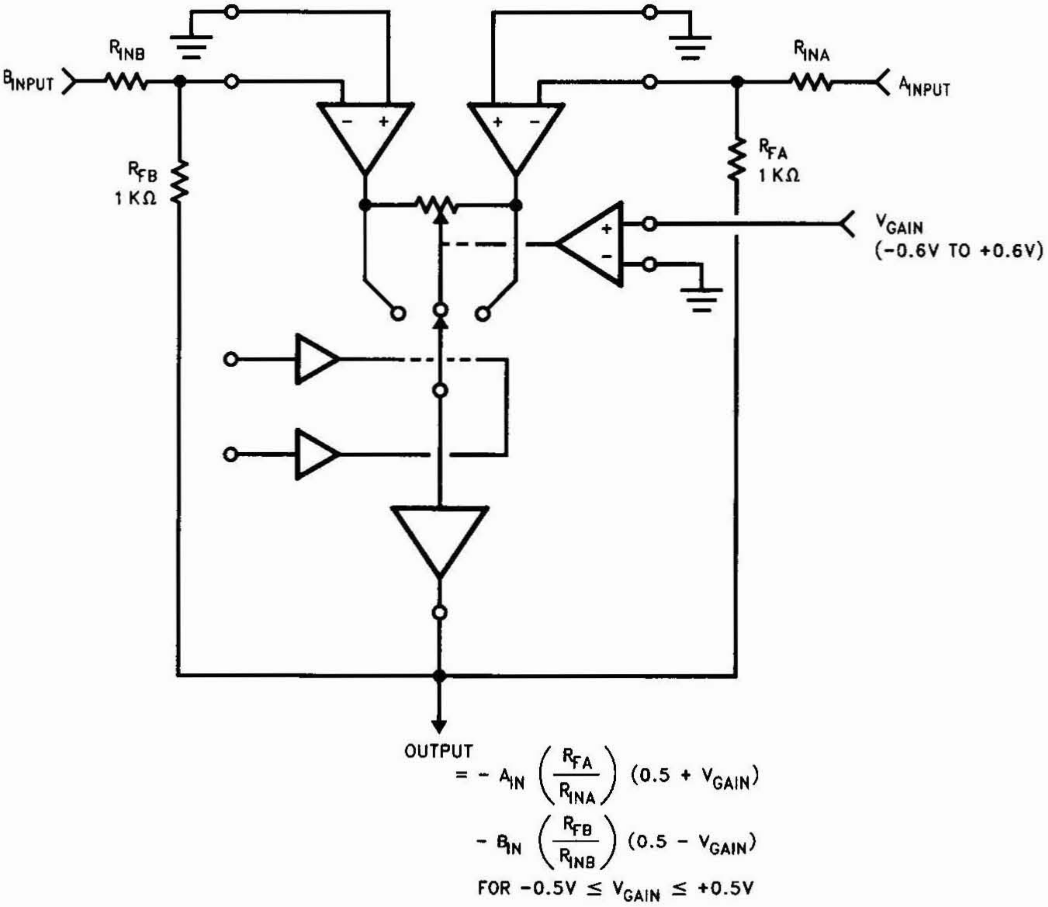
The EL4095 is a general-purpose two-channel fader whose input channels each act as a current-feedback amplifier (CFA) input. Each input can have its own gain factor as established by external resistors. For instance, the Test Circuit shows two channels each arranged as +1 gain, with the traditional single feedback resistor R_F connected from V_{OUT} to the $-V_{IN}$ of each channel.

The EL4095 can be connected as an inverting amplifier in the same manner as any CFA:

Frequency Response

Like other CFA's, there is a recommended feedback resistor, which for this circuit is 1 KΩ. The value of RF sets the closed-loop −3 dB bandwidth, and has only a small range of practical variation. The user should consult the typical performance curves to find the optional value of R_F for a given circuit gain. In general, the bandwidth will decrease slightly as closed-loop gain is increased; R_F can be reduced to make up for bandwidth loss. Too small a value of R_F will cause frequency response peaking and ringing during transients. On the other hand, increasing R_F will reduce bandwidth but improve stability.

EL4095C In Inverting Connection


R_{INB}
B_{INPUT}
R_{FB}
1 KΩ
R_{INA}
A_{INPUT}
R_{FA}
1 KΩ
V_{GAIN}
(−0.6V TO +0.6V)
OUTPUT
$= -A_{IN}\left(\frac{R_{FA}}{R_{INA}}\right)(0.5 + V_{GAIN})$
$- B_{IN}\left(\frac{R_{FB}}{R_{INB}}\right)(0.5 - V_{GAIN})$
FOR $-0.5V \leq V_{GAIN} \leq +0.5V$

4095-27

Applications Information — Contd.

Stray capacitance at each $-V_{IN}$ terminal should absolutely be minimized, especially in a positive-gain mode, or peaking will occur. Similarly, the load capacitance should be minimized. If more than 25 pF of load capacitance must be driven, a load resistor from 100Ω to 400Ω can be added in parallel with the output to reduce peaking, but some bandwidth degradation may occur. A "snubber" load can alternatively be used. This is a resistor in series with a capacitor to ground, 150Ω and 100 pF being typical values. The advantage of a snubber is that it does not draw DC load current. A small series resistor, low tens of ohms, can also be used to isolate reactive loads.

Distortion

The signal voltage range of the $+V_{IN}$ terminals is within 3.5V of either supply rail.

One must also consider the range of error currents that will be handled by the $-V_{IN}$ terminals. Since the $-V_{IN}$ of a CFA is the output of a buffer which replicates the voltage at $+V_{IN}$, error currents will flow into the $-V_{IN}$ terminal. When an input channel has 100% gain assigned to it, only a small error current flows into its negative input; when low gain is assigned to the channel the output does not respond to the channel's signal and large error currents flow.

Here are a few idealized examples, based on a gain of +1 for channels A and B and $R_F = 1\ k\Omega$ for different gain settings:

Gain	V_{INA}	V_{INB}	$I(-V_{INA})$	$I(-V_{INB})$	V_{OUT}
100%	1V	0	0	1 mA	1V
75%	1V	0	−250 μA	750 μA	0.75V
50%	1V	0	−500 μA	500 μA	0.5V
25%	1V	0	−750 μA	250 μA	0.25V
0%	1V	0	−1 mA	0	0V

Thus, either $-V_{IN}$ can receive up to 1 mA error current for 1V of input signal and 1 kΩ feedback resistors. The maximum error current is 3 mA for the EL4095, but 2 mA is more realistic. The major contributor of distortion is the magnitude of error currents, even more important than loading effects. The performance curves show distortion versus input amplitude for different gains.

If maximum bandwidth is not required, distortion can be reduced greatly (and signal voltage range enlarged) by increasing the value of R_F and any associated gain-setting resistor.

100% Accuracies

When a channel gain is set to 100%, static and gain errors are similar to those of a simple CFA. The DC output error is expressed by

$$V_{OUT}\text{, Offset} = V_{OS}{}^{*}\ A_V + (I_B-)^{*}R_F.$$

The input offset voltage scales with fed-back gain, but the bias current into the negative input, $I_B{}^{-}$, adds an error not dependent on gain. Generally, $I_B{}^{-}$ dominates up to gains of about seven.

The fractional gain error is given by

$$E_{GAIN} = (R_F + A_V{}^{*}R_{IN}-)\,R_F + A_V\,R_{IN})/R_{OL}$$

The gain error is about 0.3% for a gain of one, and increases only slowly for increasing gain. $R_{IN}-$ is the input impedance of the input stage buffer, and R_{OL} is the transimpedance of the amplifier, 80 kΩ and 350 kΩ respectively.

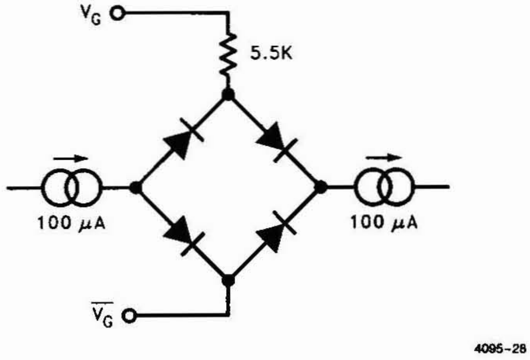
Gain Control Inputs

The gain control inputs are differential and may be biased at any voltage as long as $\overline{V_{GAIN}}$ is less than 2.5V below V+ and 3V above V−. The differential input impedance is 5.5 kΩ, and a common-mode impedance is more than 500 kΩ. With zero differential voltage on the gain inputs, both signal inputs have a 50% gain factor. Nominal calibration sets the 100% gain of V_{INA} input at +0.5V of gain control voltage, and 0% at −0.5V of gain control. V_{INB}'s gain is complementary to that of V_{INA}; +0.5V of gain control sets 0% gain at V_{INB} and −0.5V gain control sets 100% V_{INB} gain. The gain control does not have a completely abrupt transition at the 0% and 100% points. There is about 10 mV of "soft" transfer at the gain endpoints. To obtain the most accurate 100% gain factor or best attenuation of 0% gain, it is necessary to overdrive the gain control input by about 30 mV. This would set the gain control voltage range as −0.565 mV to +0.565V, or 30 mV beyond the maximum guaranteed 0% to 100% range.

Applications Information — Contd.

In fact, the gain control internal circuitry is very complex. Here is a representation of the terminals:

Representation of Gain Control Inputs V_G and $\overline{V_G}$



For gain control inputs between ±0.5V (±90 µA), the diode bridge is a low impedance and all of the current into V_G flows back out through $\overline{V_G}$. When gain control inputs exceed this amount, the bridge becomes a high impedance as some of the diodes shut off, and the V_G impedance rises sharply from the nominal 5.5 KΩ to over 500 KΩ. This is the condition of gain control overdrive. The actual circuit produces a much sharper overdrive characteristics than does the simple diode bridge of this representation.

The gain input has a 20 MHz −3 dB bandwidth and 17 ns risetime for inputs to ±0.45V. When the gain control voltage exceeds the 0% or 100% values, a 70 ns overdrive recovery transient will occur when it is brought back to linear range. If quicker gain overdrive response is required, the Force control inputs of the EL4095 can be used.

Force Inputs

The Force inputs completely override the V_{GAIN} setting and establish maximum attainable 0% and 100% gains for the two input channels. They are activated by a TTL logic low on either of the $\overline{\text{FORCE}}$ pins, and perform the analog switching very quickly and cleanly. $\overline{\text{FORCEA}}$ causes 100% gain on the A channel and 0% on the B channel. $\overline{\text{FORCEB}}$ does the reverse, but there is no defined output state when $\overline{\text{FORCEA}}$ and $\overline{\text{FORCEB}}$ are simultaneously asserted.

The Force inputs do not incur recovery time penalties, and make ideal multiplexing controls. A typical use would be text overlay, where the A channel is a video input and the B channel is digitally created text data. The $\overline{\text{FORCEA}}$ input is set low normally to pass the video signal, but released to display overlay data. The gain control can be used to set the intensity of the digital overlay.

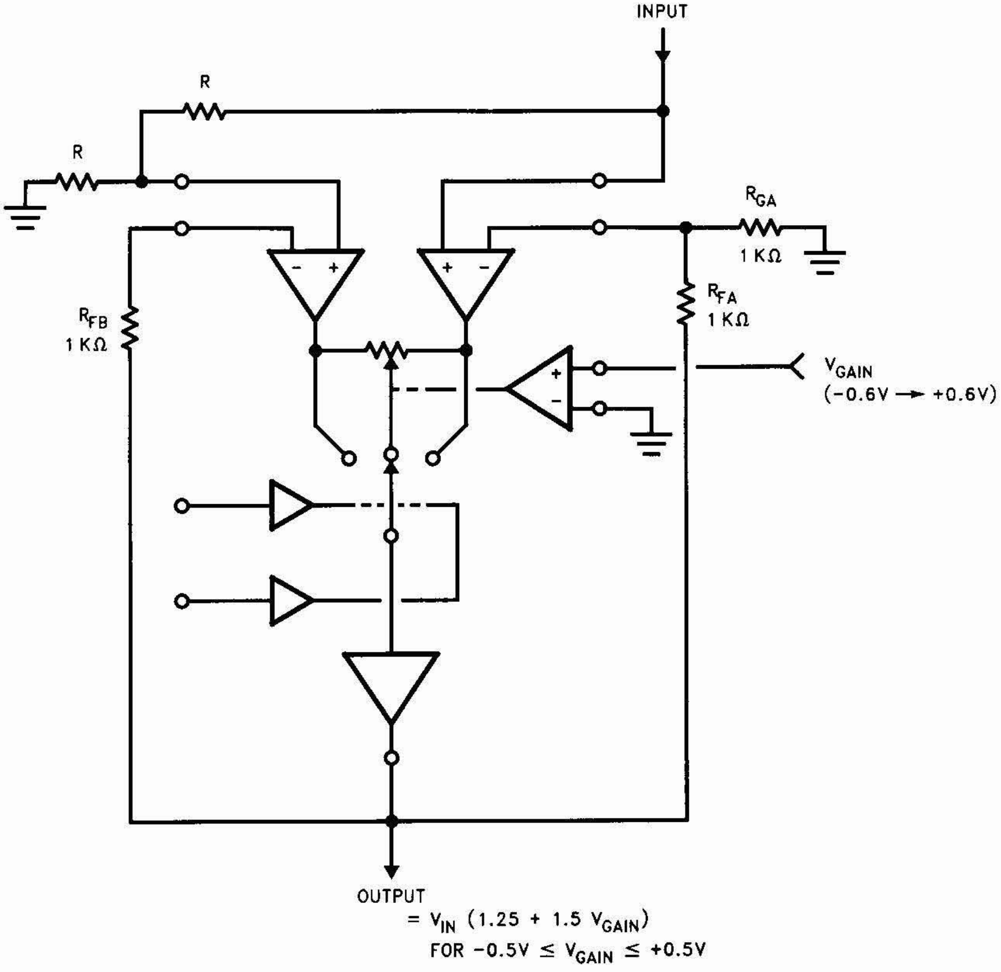
Other Applications Circuits

The EL4095 can also be used as a variable-gain single input amplifier. If a 0% lower gain extreme is required, one channel's input should simply be grounded. Feedback resistors must be connected to both $-V_{IN}$ terminals; the EL4095 will not give the expected gain range when a channel is left unconnected.

This circuit gives +0.5 to +2.0 gain range, and is useful as a signal leveller, where a constant output level is regulated from a range of input amplitudes:

Application Information — Contd.

Leveling Circuit with $0.5 \leq A_V \leq 2$


INPUT
R
R
R_{GA}
1 KΩ
R_{FA}
1 KΩ
R_{FB}
1 KΩ
V_{GAIN}
(−0.6V → +0.6V)
OUTPUT
$= V_{IN}\ (1.25 + 1.5\ V_{GAIN})$
FOR $-0.5V \leq V_{GAIN} \leq +0.5V$
4095-29

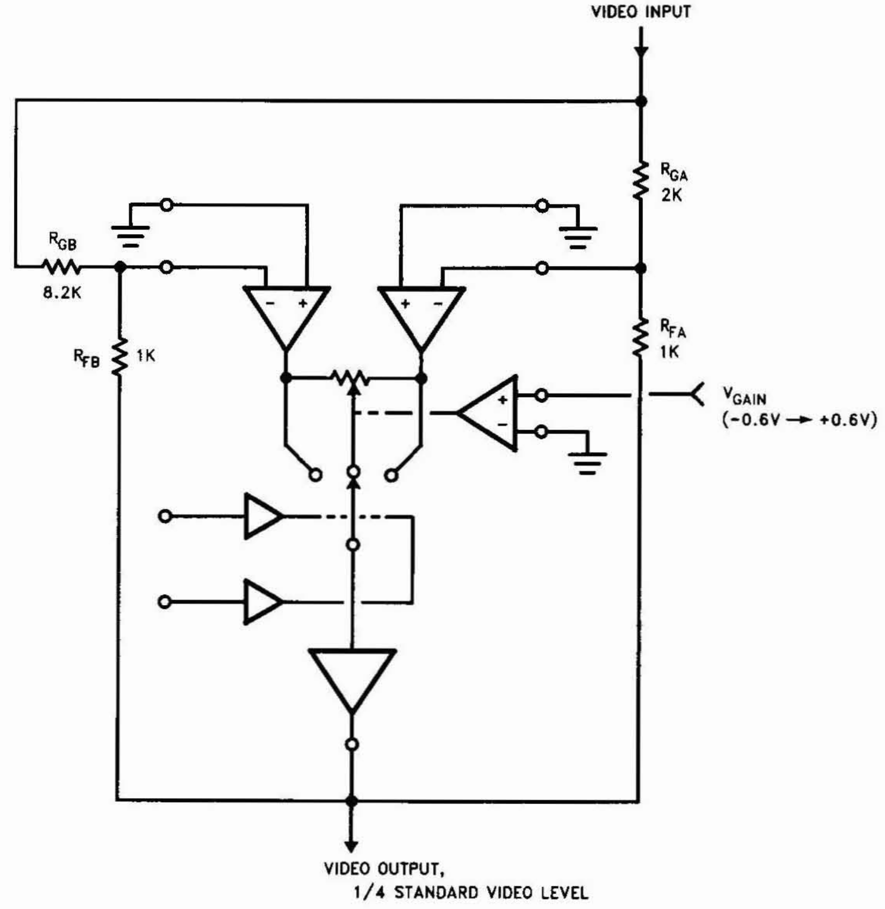
Here the A input channel is configured for a gain of +2 and the B channel for a gain of +1 with its input attenuated by ½. The connection is virtuous because the distortions do not increase monotonically with reducing gain as would the simple single-input connecton.

For video levels, however, these constants can give fairly high differential gain error. The problem occurs for large inputs. Assume that a "twice-size" video input occurs. The A-side stage sees the full amplitude, but the gain would be set to 100% B-input gain to yield an overall gain of

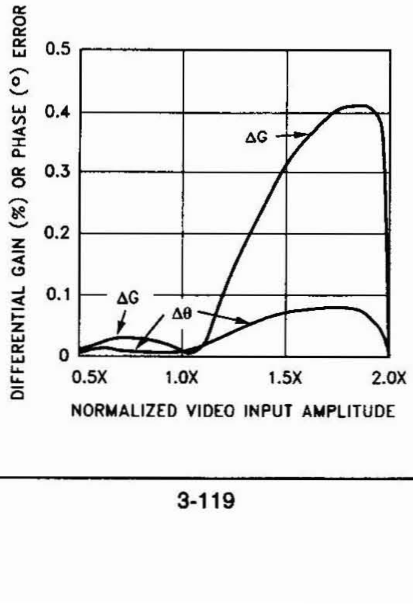
Application Information — Contd.

½ to produce a standard video output. The $-V_{IN}$ of the A side is a buffer output that reproduces the input signal, and drives R_{GA} and R_{FA}. Into the two resistors 2.1 mA of error current flows for a typical 1.4V of input DC offset, creating distortion in a A-side input stage. R_{GA} and R_{FA} could be increased together in value to reduce the error current and distortions, but increasing R_{FA} would lower bandwidth. A solution would be to simply attenuate the input signal magnitude and restore the EL4095 output level to standard level with another amplifier so:

Reduced-Gain Leveler for Video Inputs and Differential Gain and Phase Performance (see text)


VIDEO INPUT
R_{GA} 2K
R_{GB} 8.2K
R_{FB} 1K
R_{FA} 1K
V_{GAIN} (−0.6V → +0.6V)
VIDEO OUTPUT,
1/4 STANDARD VIDEO LEVEL

4095-30



4095-31

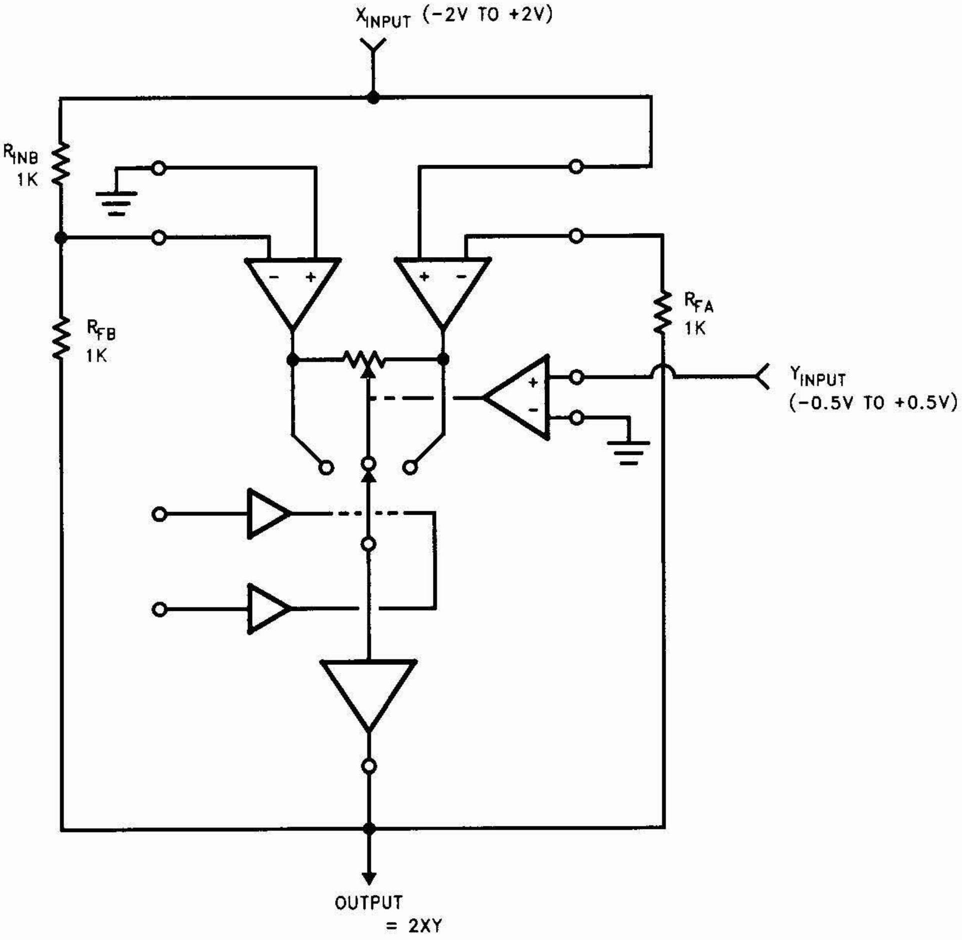
Application Information — Contd.

Although another amplifier is needed to gain the output back to standard level, the reduced error currents bring the differential phase error to less than 0.1′ over the entire input range.

A useful technique to reduce video distortion is to DC-restore the video level going into the EL4095, and offsetting black level to −0.35V so that the entire video span encompasses ±0.35V rather than the unrestored possible span of ±0.7V (for standard-sized signals). For the preceding leveler circuit, the black level should be set more toward −0.7V to accommodate the largest input, or made to vary with the gain control itself (large gain, small offset; small gain, larger offset).

The EL4095 can be wired as a four quadrant multiplier:

EL4095 Connected as a Four-Quadrant Multiplier

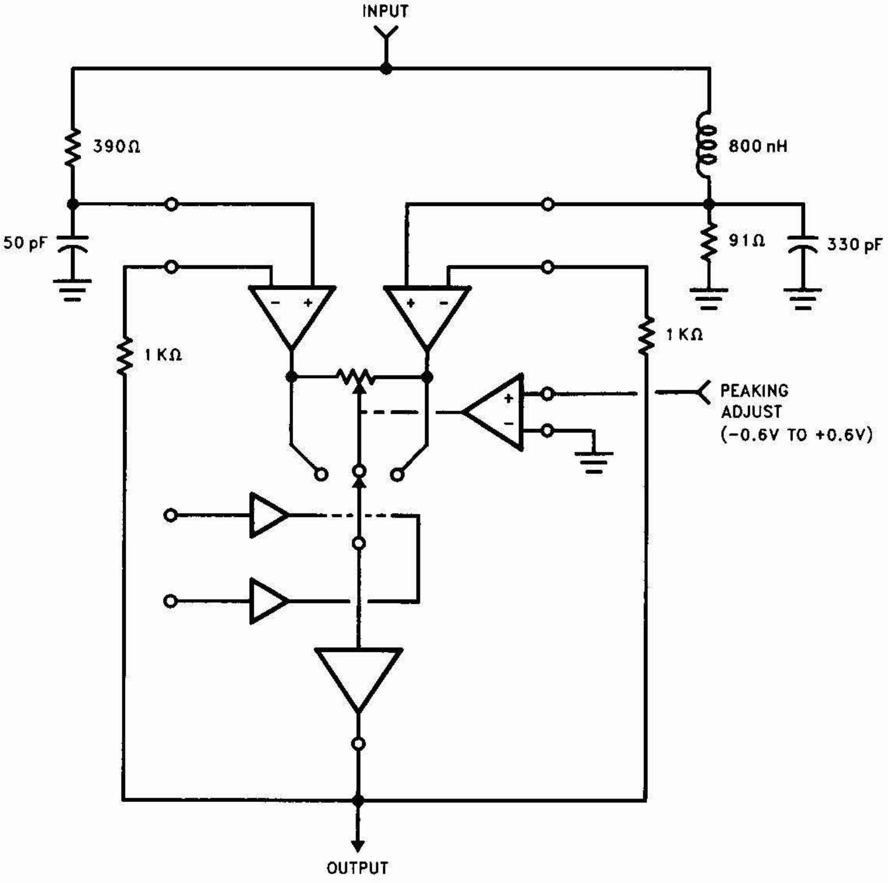


Application Information — Contd.

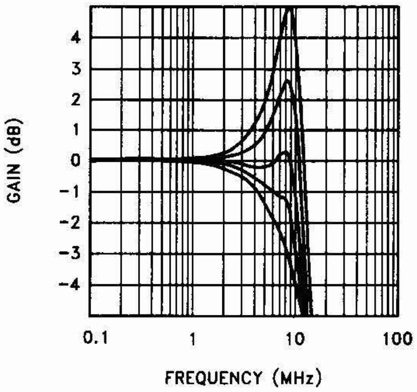
The A channel gains the input by +1 and the B channel by −1. Feedthrough suppression of the Y input can be optimized by introducing an offset between channel A and B. This is easily done by injecting an adjustable current into the summing junction ($-V_{IN}$ terminal) of the B input channel.

The two input channels can be connected to a common input through two dissimilar filters to create a DC-controlled variable filter. This circuit provides a controlled range of peaking through rolloff characteristics:

Variable Peaking Filter


INPUT
390Ω
800 nH
50 pF
91Ω
330 pF
1 KΩ
1 KΩ
PEAKING
ADJUST
(−0.6V TO +0.6V)
OUTPUT

4095-33



4095-34

Applications Information — Contd.

The EL4095 is connected as a unity-gain fader, with an LRC peaking network connected to the A-input and an RC rolloff network connected to the B-input. The plot shows the range of peaking controlled by the V_{GAIN} input. This circuit would be useful for flattening the frequency response of a system, or for providing equalization ahead of a lossy transmission line.

Noise

The electrical noise of the EL4095 has two components: the voltage noise in series with $+V_{IN}$ is $5\ nV\sqrt{Hz}$ wideband, and there is a current noise injected into $-V_{IN}$ of $35\ pA\sqrt{Hz}$. The output noise will be

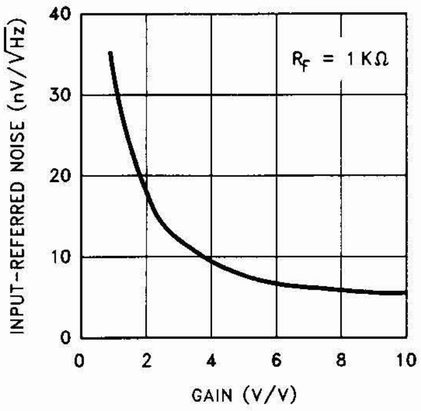
$$\overline{V_{n,\,out}} = \sqrt{(A_V \bullet \overline{V_{n,\,input}})^2 + (\overline{I_{n,\,input}} \bullet R_F)^2},$$

and the input-referred noise is

$$\overline{V_{n,\,input\text{-}referred}} = \sqrt{(\overline{V_{n,\,input}})^2 + (\overline{I_{n,\,input}} \bullet R_F/A_V)^2}$$

where A_V is the fed-back gain of the EL4095. Here is a plot of input-referred noise vs A_V:

Input-Referred Noise vs Closed-Loop Gain



4095-35

Thus, for a gain of three or more the fader has a noise as good as an op-amp. The only trade-off is that the dynamic range of the input is reduced by the gain due to the nonlinearity caused by gained-up output signals.

Power Dissipation

Peak die temperature must not exceed 150°C. This allows 75°C internal temperature rise for a 75°C ambient. The EL4095 in the 14-pin PDIP package has a thermal resistance of 65°C/W, and can thus dissipate 1.15W at a 75°C ambient temperature. The device draws 20 mA maximum supply current, only 600 mW at ±15V supplies, and the circuit has no dissipation problems in this package.

The SO-14 surface-mount package has a 105°C/W thermal resistance with the EL4095, and only 714 mW can be dissipated at 75°C ambient temperature. The EL4095 thus can be operated with ±15V supplies at 75°C, but additional dissipation caused by heavy loads must be considered. If this is a problem, the supplies should be reduced to ±5V to ±12V levels.

The output will survive momentary short-circuits to ground, but the large available current will overheat the die and also potentially destroy the circuit's metal traces. The EL4095 is reliable within its maximum average output currents and operating temperatures.

EL4095C Macromodel

This macromodel is offered to allow simulation of general EL4095 behavior. We have included these characteristics:

- Small-signal frequency response
- Output loading effects
- Input impedance
- Off-channel feedthrough
- Output impedance over frequency
- $-V_{IN}$ characteristics and sensitivity to parasitic capacitance
- Signal path DC distoritons
- V_{GAIN} I-V characteristics
- V_{GAIN} overdrive recovery delay
- 100% gain error
- $\overline{\text{FORCE}}$ operation

These will give a good range of results of various operating conditions, but the macromodel does not behave identically as the circuit in these areas:

- Temperature effects
- Signal overload effects
- Signal and $\overline{V_G}$ operating range
- Current-limit
- Video and high-frequency distortions
- Glitch and delay from $\overline{\text{FORCE}}$ inputs
- Manufacturing tolerances
- Supply voltage effects
- Slewrate limitations
- Noise
- Power supply interactions

EL4095C Macromodel — Contd.

```
*** EL4095 macromodel ***
******
******
*                       +VinB
*                        |   -VinB
*                        |    |    /ForceA
*                        |    |     |    /ForceB
*                        |    |     |     |    Vout
*                        |    |     |     |     |   /Vgain
*                        |    |     |     |     |    |   Vgain
*                        |    |     |     |     |    |    |   -VinA
*                        |    |     |     |     |    |    |    |   +VinA
*                        |    |     |     |     |    |    |    |    |
.SUBCKT 4095macromodel ( 1    2     4     5     7   10   11   13   14 )
***
Rol 810 0 290k
Ccomp 810 0 4.3p
G1 110 0 810 0 -10
Rout 110 0 0.1
Lout 110 7 350n
RLout 110 7 80
***
Rina+ 14 0 5E6
Rinb+ 1 0 5E6
Rvg 11 0 2E6
Rvgg 10 0 2E6
Rforcea 4 0 1E9
Rforceb 5 0 1E9
******
*** Input channel A
***
Rina 22 313 79
Ra 111 0 1k
Rfeedthrougha 13 313 1.0
Cfeedthrougha 23 13 2500p
Ccompa 111 0 2p
E1a 23 313 302 25 -1
E2a 22 0 14 0 0.9999
Rspice3 23 313 1E12
G1a 111 0 POLY(1) (22,313) 0.0 0.0125 -150E-6
G2a 810 0 POLY(2) (111,0) (113,0) 0.0 0.0 0.0 0.0 0.001
***
***Input channel B
***
Rinb 25 302 79
Rb 120 0 1k
Rfeedthroughb 2 302 1.0
Cfeedthroughb 24 2 2500p
Ccompb 120 0 2p
E1b 24 302 22 313 -1
E2b 25 0 1 0 0.9999
Rspice4 24 302 1E12
G1b 120 0 POLY(1) (25,302) 0.0 0.0125 -150E-6
G2b 810 0 POLY(2) (120,0) (119,0) 0.0 0.0 0.0 0.0 0.001
***
***Gain control
***
Rspice1 113 0 1E12
Rspice2 119 0 1E12
R10 114 0 1E7
R11 204 206 2.5E6
R12 205 206 2.5E6
C10 201 0 9.5E-16
D1 114 115 Dclamp
D2 116 114 Dclamp
D3 204 4 Dclamp
```

4095-36

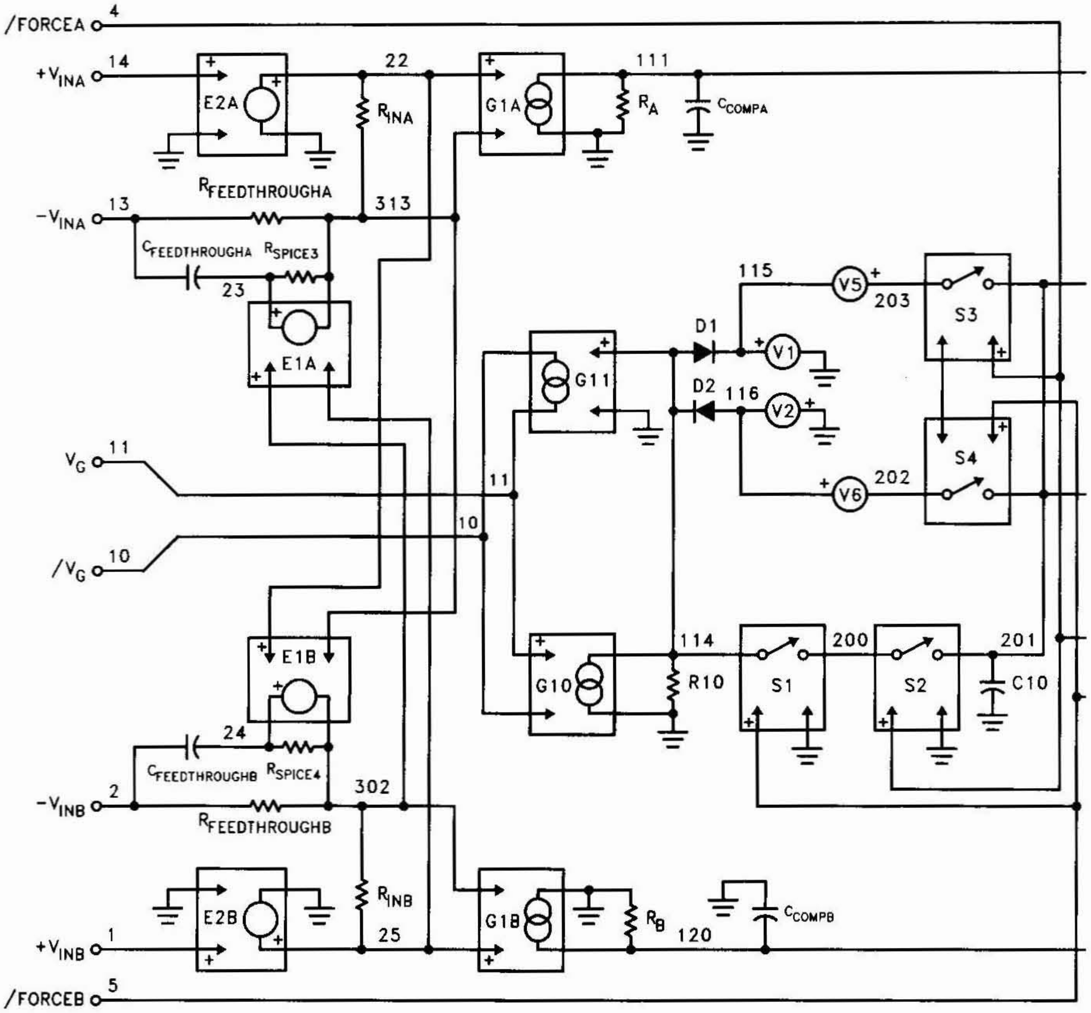
EL4095C Macromodel — Contd.

```
D4 205 5 Dclamp
.model Dclamp D(TT=200n)
Vttl 206 0 2.4
V1 115 0 4999.3
V2 0 116 4999.3
V3 113 117 0.5
V4 119 118 0.5
V5 203 115 0.7
V6 116 202 0.7
G10 114 0 11 10 -0.001
G11 11 10 114 0 -2E-8
E10 117 0 201 0 1E-4
E11 118 0 201 0 -1E-4
S1 114 200 5 0 Nopen
S2 200 201 4 0 Nopen
S3 203 201 4 0 Nclosed
S4 202 201 5 0 Nclosed
.model Nopen VSWITCH(Ron=100 Roff=1E12 Von=1.6 Voff=1.2)
.model Nclosed VSWITCH( Ron=100 Roff=1E12 Von=1.2 Voff=1.6)
***
.ENDS
******
```

4095-37

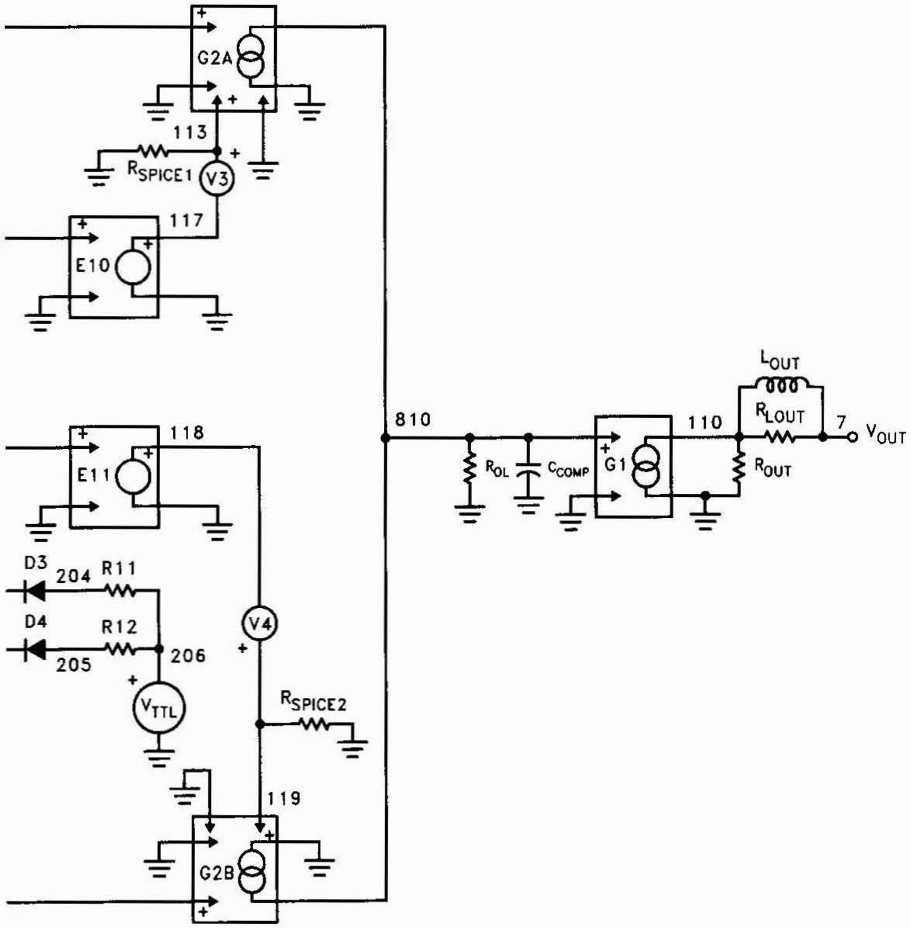
EL4095C Macromodel — Contd.

The EL4095 Macromodel Schematic


/FORCEA 4
+V_{INA} 14
E2A
22
R_{INA}
G1A
111
R_A
C_{COMPA}
R_{FEEDTHROUGHA}
−V_{INA} 13
313
C_{FEEDTHROUGHA}
R_{SPICE3}
23
E1A
115
V5
203
S3
D1
V1
G11
D2
116
V2
S4
V6
202
V_G 11
11
10
/V_G 10
E1B
G10
114
R10
S1
200
S2
201
C10
24
C_{FEEDTHROUGHB}
R_{SPICE4}
302
−V_{INB} 2
R_{FEEDTHROUGHB}
E2B
R_{INB}
G1B
R_B
C_{COMPB}
120
+V_{INB} 1
25
/FORCEB 5

4095-38

EL4095C Macromodel — Contd.


G2A
113
R_{SPICE1}
V3
117
E10
E11
118
810
D3
204
R11
D4
R12
205
206
V_{TTL}
V4
R_{SPICE2}
119
G2B
R_{OL}
C_{COMP}
G1
110
L_{OUT}
R_{LOUT}
R_{OUT}
7
V_{OUT}

4095-39

EL4332C

Triple 2:1 300 MHz Mux-Amp $A_V = 2$

Features

- 3 ns A-B switching
- 300 MHz bandwidth
- Fixed gain of 2, for cable driving
- > 650V/µs slew rate
- TTL/CMOS compatible switch

Applications

- RGB multiplexing
- Picture-in-picture
- Cable driving
- HDTV processing
- Switched gain amplifiers
- ADC input multiplexer

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4332CS	−40°C to 85°C	SO16	MDP0027

Demo Board

A demo PCB is available for this product. Request "EL4332/1 Demo Board."

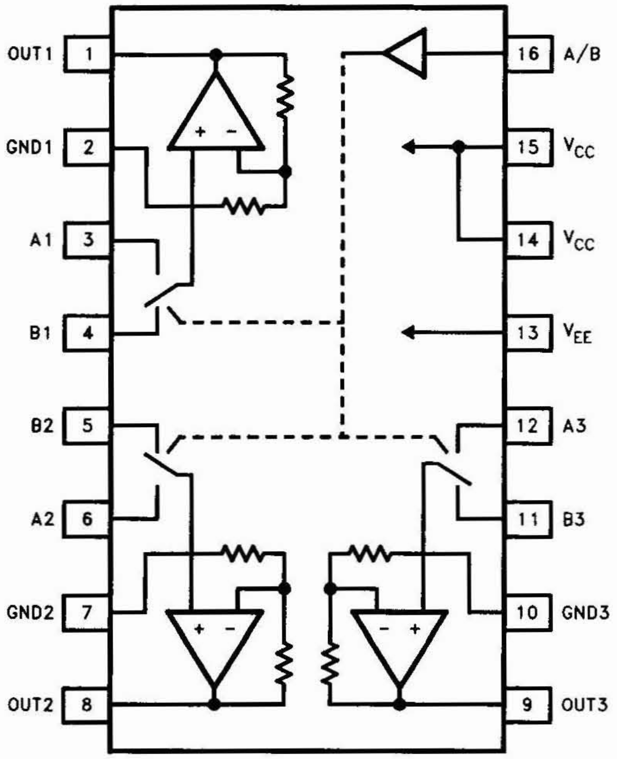
General Description

The EL4332C is a triple very high speed 2:1 Multiplexer-Amplifier. It is intended primarily for component video multiplexing and is especially suited for pixel switching. The amplifiers have their gain set to 2 internally, which reduces the need for many external components. The gain-of-2 facilitates driving back terminated cables. All three amplifiers are switched simultaneously from their A to B inputs by the TTL/CMOS compatible, common A/B control pin.

A −3 dB bandwidth of 300 MHz together with 3 ns multiplexing time enable the full performance of the fastest component video systems to be realized.

The EL4332C runs from standard ±5V supplies, and is available in the narrow 16-pin small outline package.

Connection Diagram



4332-1

EL4332C

Triple 2:1 300 MHz Mux-Amp $A_V = 2$

Absolute Maximum Ratings

V_{CC} to V_{EE}	14V	Input Current, Any Input	5 mA
V_{CC} to any GND	12V	Power Dissipation	See Curves
V_{EE} to any GND	12V	Operating Temperature	−40°C to 85°C
Continuous Output Current	45 mA	Junction Temperature	170°C
Any Input	$V_{EE} - 0.3V$ to $V_{CC} + 0.3V$	Storage Temperature	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

DC Electrical Characteristics $V_{CC} = +5V$, $V_{EE} = -5V$, Temperature = 25°C, $R_L = \infty$

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Referred Offset Voltage		8	20	II	mV
dV_{OS}	Input Referred Offset Voltage Delta (Note 1)		2	5	II	mV
R_{IN}	Input Resistance		30		V	kΩ
I_B	Input Bias Current		−7	−30	II	μA
dI_B	Input Bias Current Delta (Note 1)		0.5	2.5	II	μA
A_V	Gain	1.94	2.00	2.06	II	V/V
dA_V	Gain Delta (Note 1)		0.5	2.5	II	%
C_{IN}	Input Capacitance		3.3		V	pF
PSRR	Power Supply Rejection Ratio	50	70		II	dB
V_O	Output Voltage Swing into 500Ω load Output Voltage Swing into 150Ω load	±2.7	±3.6 +3/−2.7		II V	V V
I_{OUT}	Current Output, Measured with 75Ω Load (Note 2)	30	40		II	mA
$Xtalk_{AB}$	Crosstalk from Non-selected Input (at DC)	−70	−100		III	dB
$Xtalk_{CH\text{-}CH}$	Crosstalk from one Amplifier to another Amplifier	−70	−100		V	dB
V_{IH}	Input Logic High Level	2.0			II	V
V_{IL}	Input Logic Low Level			0.8	II	V
I_{IL}	Logic Low Input Current ($V_{IN} = 0V$)	−0.3	−40	−80	II	μA
I_{IH}	Logic High Input Current ($V_{IN} = 0V$)	−3	0	3	II	μA
I_S	Total Supply Current	38	48	60	II	mA

Note 1: Each channel's A-input to its B-input.
Note 2: There is no short circuit protection on any output.

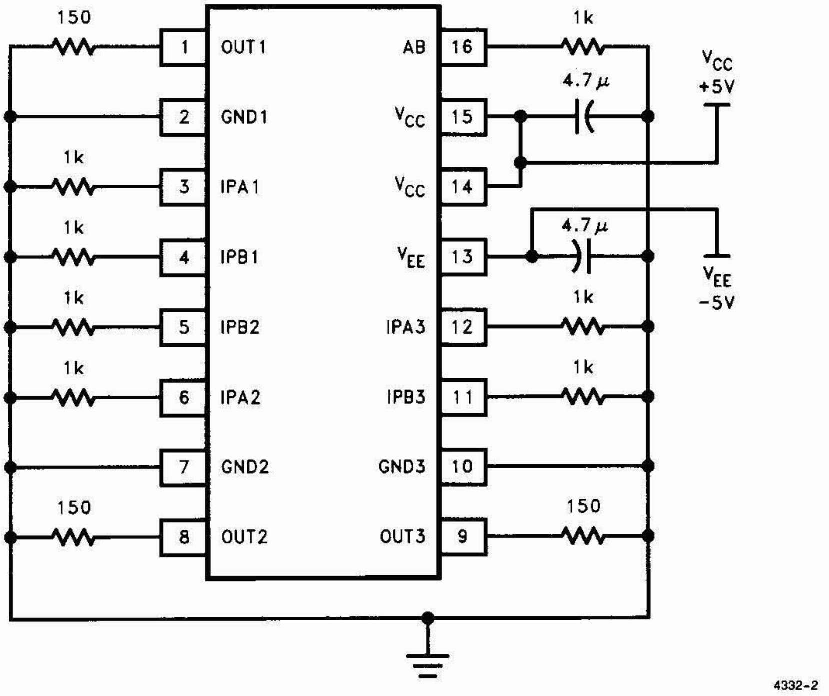
AC Electrical Characteristics $V_{CC} = +5V$, $V_{EE} = -5V$, Temperature = 25°C, $R_L = 150\Omega$, $C_L = 3$ pF.

Parameter	Description	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth		300		V	MHz
BW 0.1dB	±0.1 dB Bandwidth		105		V	MHz
DG	Differential Gain at 3.58 MHz		0.04		V	%
DP	Differential Phase at 3.58 MHz		0.08		V	°
Pkg	Peaking with Nominal Load		0.2		V	dB
SR	Slew Rate (4V Square Wave, Measured 25%–75%)		650		V	V/µs
t_s	Settling Time to 0.1% of Final Value		13		V	ns
T_{SW}	Time to Switch Inputs		3		V	ns
OS	Overshoot, $V_{OUT} = 4\ V_{P-P}$		8		V	%
I_{SO} ab 10M	Input to Input Isolation at 10 MHz		60		V	dB
100M	Input to Input Isolation at 100 MHz		40		V	dB
I_{SO} ch-ch 10M	Channel to Channel Isolation at 10 MHz		61		V	dB
100M	Channel to Channel Isolation at 100 MHz		50		V	dB

Pin Descriptions

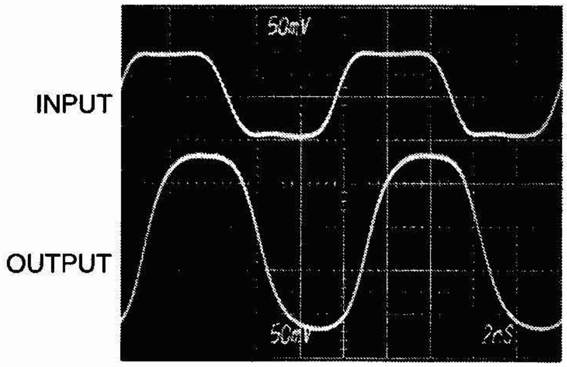
Pin Name	Function
A1, A2, A3	"A" inputs to amplifiers 1, 2 and 3 respectively
B1, B2, B3	"B" inputs to amplifiers 1, 2 and 3 respectively
GND1, GND2, GND3	These are the individual ground pins for each channel.
Out1, Out2, Out3	Amplifier outputs. Note: there is no short circuit protection on any output.
V_{CC}	Positive power supply. Typically +5V.
V_{EE}	Negative power supply. Typically −5V.
A/B	Common input select pin, a logic high selects the "A" inputs, logic low selects the "B" inputs. CMOS/TTL compatible.

Burn In Schematic


150
1 OUT1
2 GND1
1k
3 IPA1
1k
4 IPB1
1k
5 IPB2
1k
6 IPA2
7 GND2
150
8 OUT2
AB 16
1k
4.7µ
VCC 15
VCC +5V
VCC 14
4.7µ
VEE 13
VEE -5V
1k
IPA3 12
1k
IPB3 11
GND3 10
150
OUT3 9
4332-2

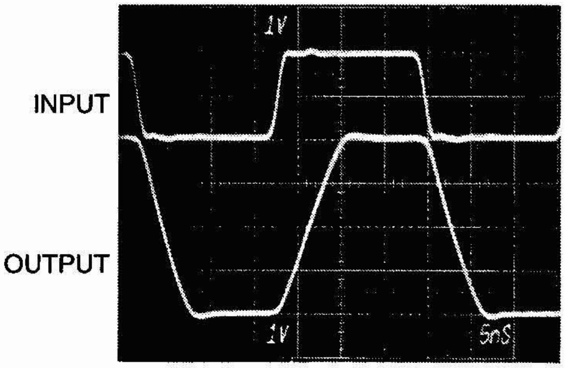
Typical Performance Curves

Small Signal Transient Response



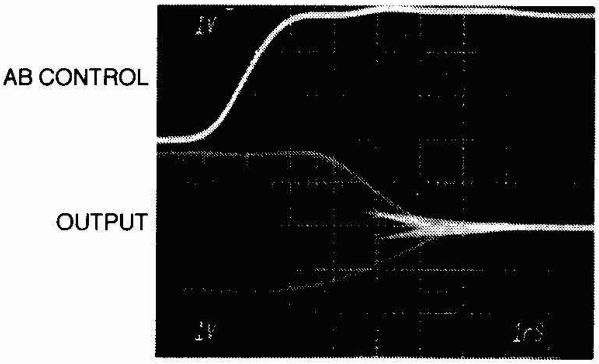
4332-3

Large Signal Transient Response



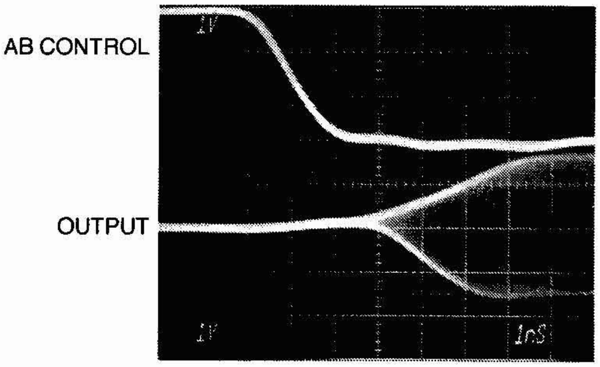
4332-4

Switching to Ground from a Large Signal Uncorrelated Sine Wave



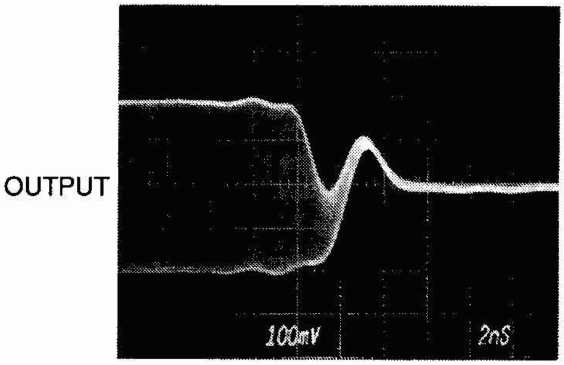
4332-5

Switching from Ground to a Large Signal Uncorrelated Sine Wave



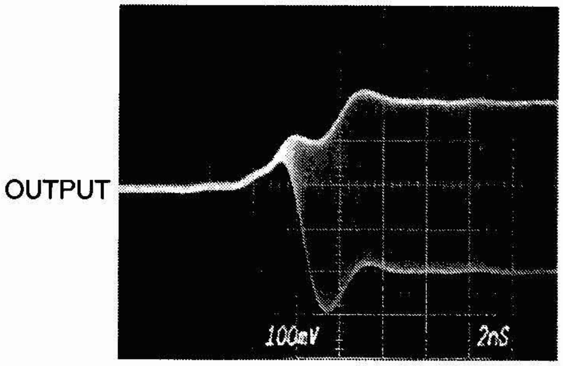
4332-6

Switching to Ground from a Small Signal Uncorrelated Sine Wave



4332-7

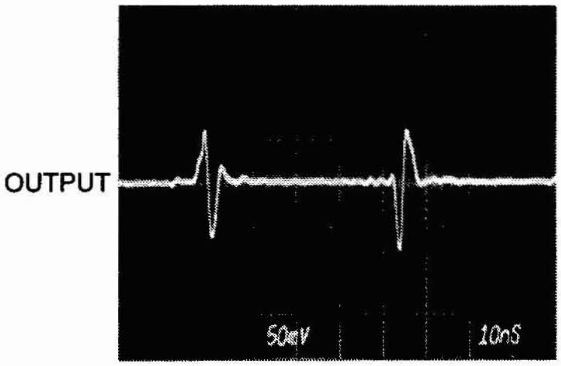
Switching from Ground to a Small Signal Uncorrelated Sine Wave



4332-8

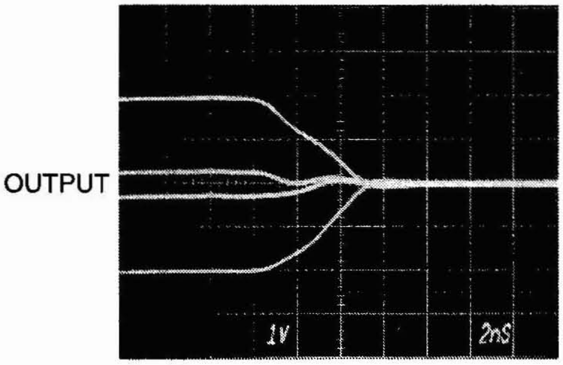
Typical Performance Curves — Contd.

Switching Glitch (Inputs at Ground)



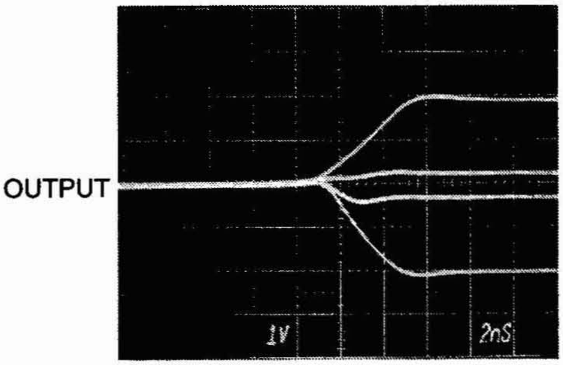
4332-9

Switching from a Family of DC Levels to Ground



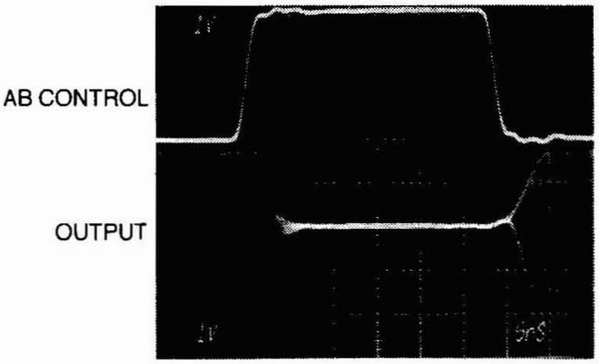
4332-10

Switching from Ground to a Family of DC Levels



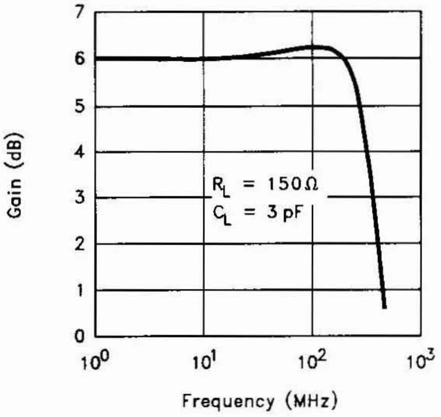
4332-11

Channel A/B Switching Delay



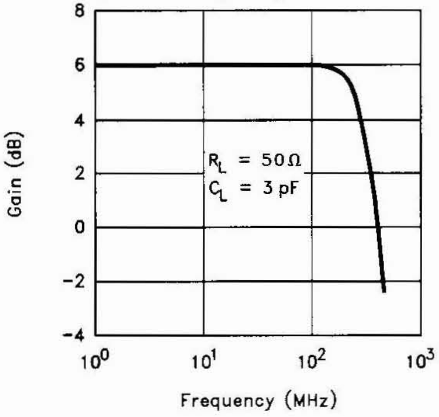
4332-31

Gain vs Frequency



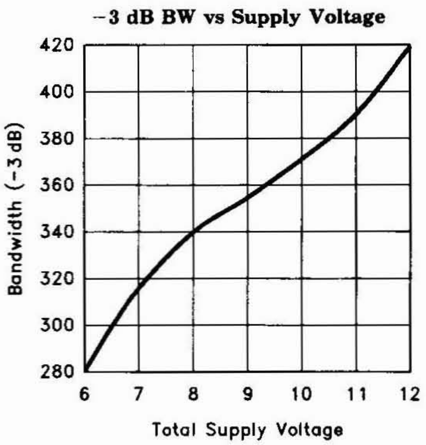
4332-12

Gain vs Frequency

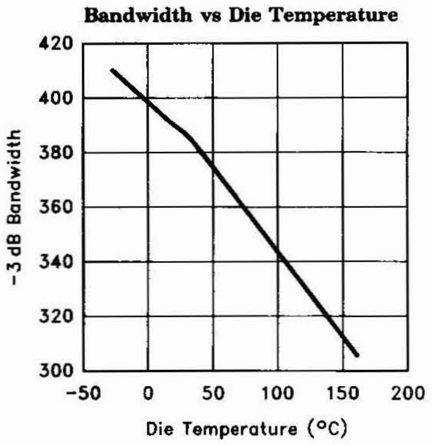


4332-13

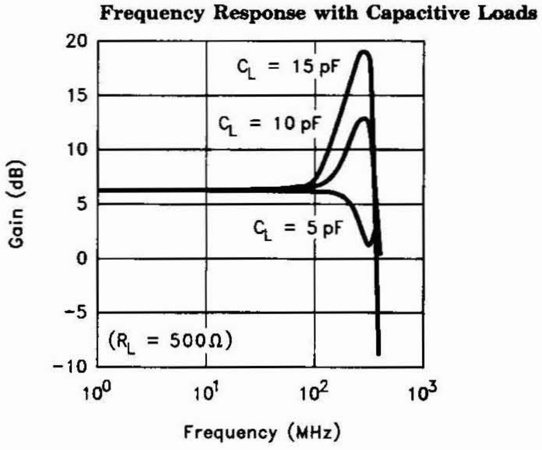
Typical Performance Curves — Contd.


−3 dB BW vs Supply Voltage

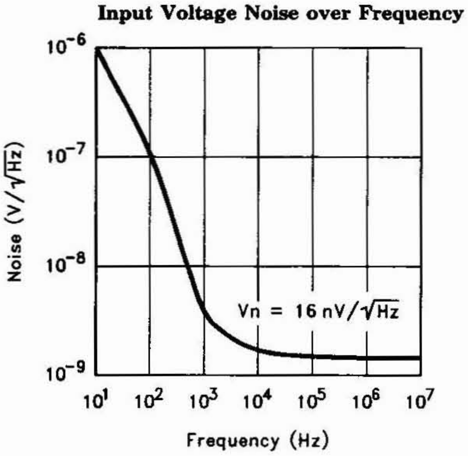
4332-14


Bandwidth vs Die Temperature

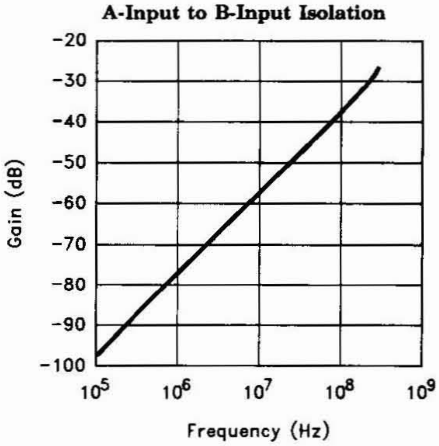
4332-15


Frequency Response with Capacitive Loads

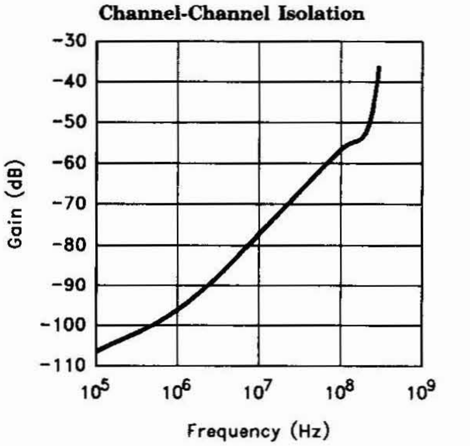
4332-16


Input Voltage Noise over Frequency

4332-17


A-Input to B-Input Isolation

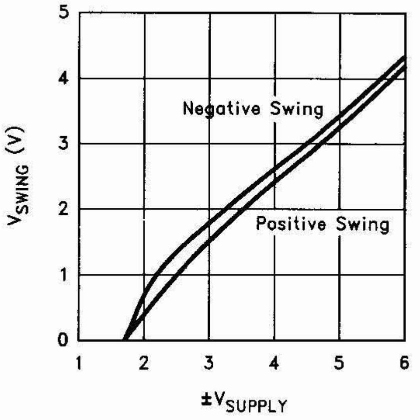
4332-18


Channel-Channel Isolation

4332-19

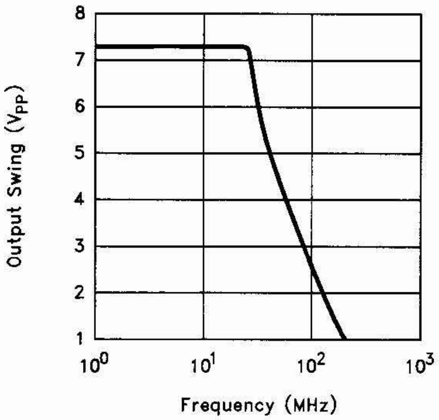
Typical Performance Curves — Contd.

Output Swing vs Supply Voltage



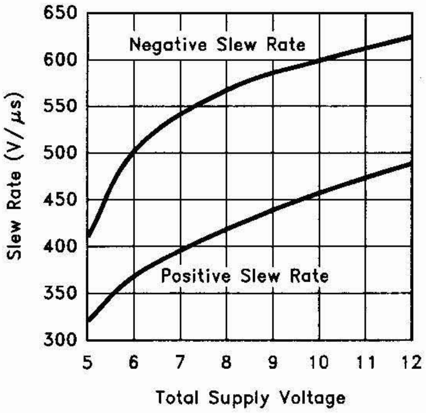
4332-20

Output Swing vs Frequency



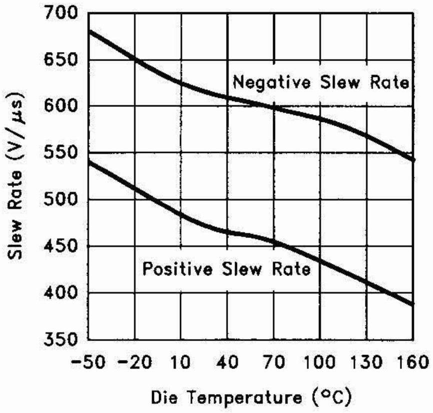
4332-21

Slew Rate vs Supply Voltage



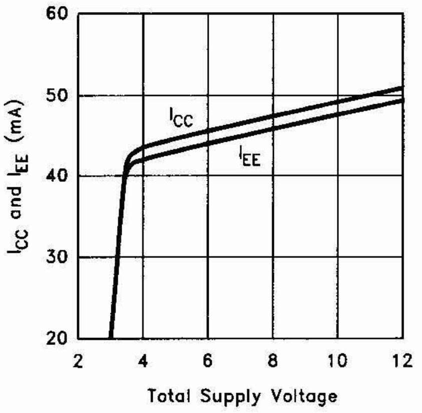
4332-22

Slew Rate vs Die Temperature



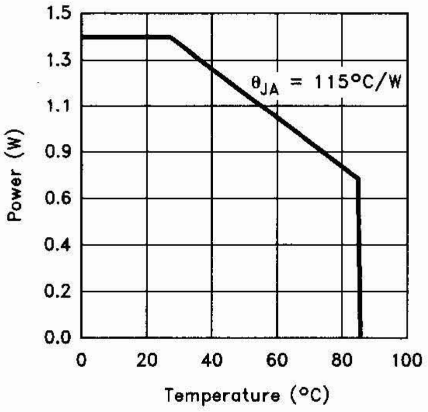
4332-23

Supply Current vs Supply Voltage



4332-24

Maximum Power Dissipation



4332-25

Typical Applications

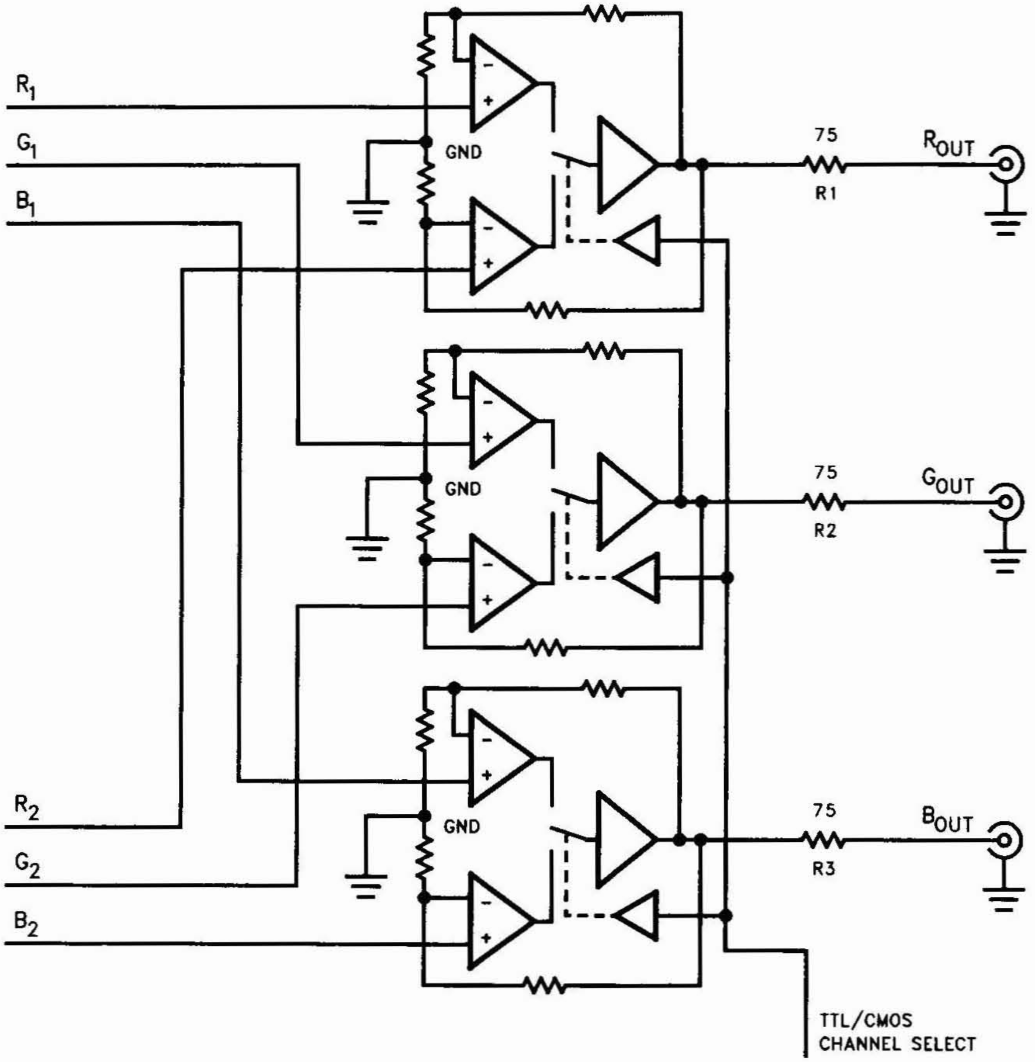

R1
G1
B1
R2
G2
B2
GND
GND
GND
75
R1
75
R2
75
R3
ROUT
GOUT
BOUT
TTL/CMOS
CHANNEL SELECT
4332-26

Figure 1. Typical Connection for a 2:1 Component Video Multiplexer

Applications

Figure 1 shows a typical use for the EL4332C. The circuit is a component video (R,G,B or Y,U,V) multiplexer. Since the gain of the internal amplifiers has been set to 2, the only extra components needed are the supply decoupling capacitors and the back terminating resistors, if transmission lines are to be driven. The EL4332 can drive backmatched 50Ω or 75Ω loads.

Grounds

It will be noticed that each mux-amp channel has its own separate ground pin. These ground pins have been kept separate to keep the channel separation inside the chip as large as possible. The feedback resistors use these ground pins as their reference. The resistors total 400Ω, so there is a significant signal current flowing from these pins to ground.

The ground pins should all be connected together, to a ground plane underneath the chip. 1 oz. copper for the ground plane is highly recommended.

Further notes and recommended practices for high speed printed circuit board layout can be found in the tutorials in the Elantec databooks.

Supplies

Supply bypassing should be as physically near the power pins as possible. Chip capacitors should be used to minimize lead inductance. Note that larger values of capacitor tend to have larger internal inductances. So when designing for 3 transmission lines or similar moderate loads, a 0.1 μF ceramic capacitor right next to the power pin in parallel with a 22 μF tantalum capacitor placed as close to the 0.1 μF is recommended. For lighter loadings, or if not all the channels are being used, a single 4.7 μF capacitor has been found quite adequate.

Note that component video signals do tend to have a high level of signal correlation. This is especially true if the video signal has been derived from 3 synchronously clocked DACs. This corresponds to all three channels drawing large slew currents simultaneously from the supplies. Thus, proper bypassing is critical.

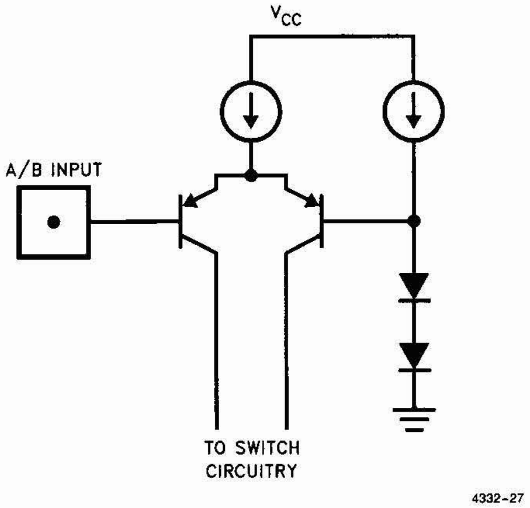


Figure 2a. Simplified Logic Input Stage

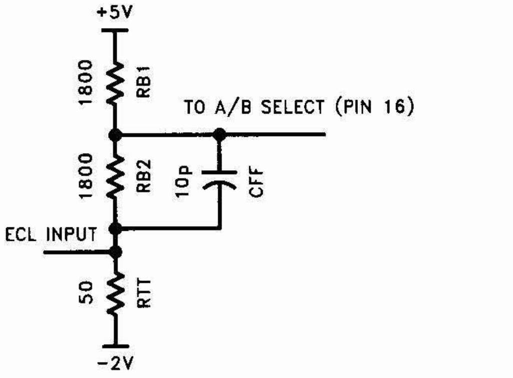


Figure 2b. Adapting the Select Pin for ECL Logic Levels

Logic Inputs

The A/B select, logic input, is internally referenced to ground. It is set at 2 diode drops above ground, to give a threshold of about 1.4V (see Figure 2a). The PNP input transistor requires that the driving gate be able to sink current, typically < 30 μA, for a logic "low". If left to float, it will be a logic "high".

The input PNP transistors have sufficient gain that a simple level shift circuit (see Figure 2b) can be used to provide a simple interface with Emitter Coupled Logic. Typically, 200 mV is enough to switch from a solid logic "low" to a "high".

The capacitor Cff is only in the network to prevent the A/B pin's capacitance from slowing the control signal. The network shown level shifts the ECL levels, −0.7V to −1.5V to +1.6V and +1.1V respectively. The terminating resistor, Rtt, is required since the open emitter of the ECL gate can not sink current. If a −2V rail is not being used, a 220Ω to 330Ω resistor to the −5.2V rail would have the same effect.

Expanding the Multiplexer

In Figure 3, a 3:1 multiplexer circuit is shown. The expansion to more inputs is very straight forward. Since the EL4332C has a fixed gain of 2, interstage attenuators may be required as shown in Figure 3. The truth table for the 3:1 multiplexer select lines is:

X	Y	Mux Output
0	0	R3, G3, B3
0	1	R2, G2, B2
1	X	R1, G1, B1

When interstage attenuators are used, the values should be kept down in the region of 50Ω–300Ω. This is to prevent a combination of circuit board stray capacitance and the EL4332C's input capacitance forming a significant pole. For example, if instead of 100Ω as shown, resistors of 1 kΩ had been used, and assuming 3 pF of stray and 3 pF of input capacitance, a pole would be formed at about 53 MHz.

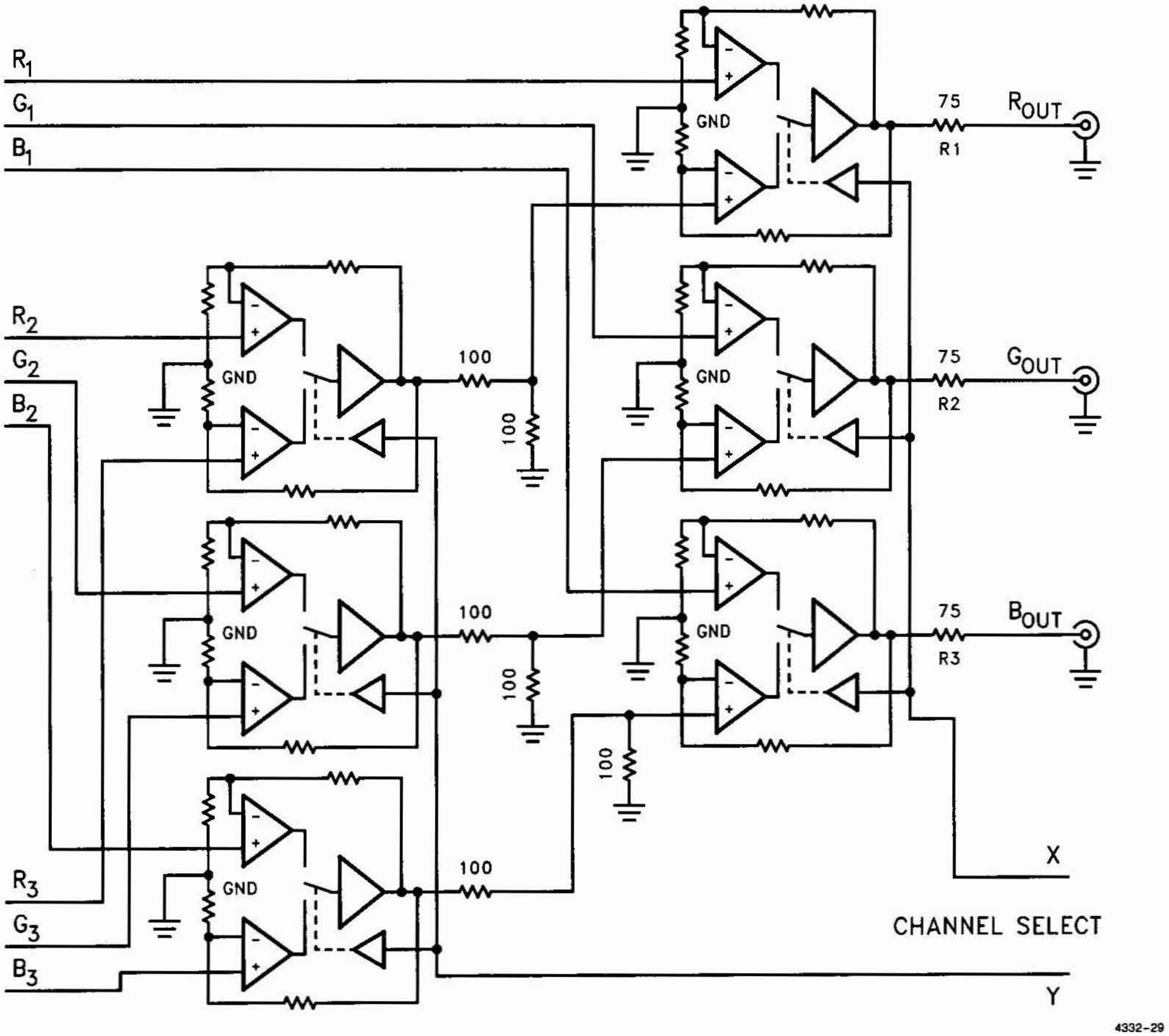

R1
G1
B1
R2
G2
B2
R3
G3
B3
GND
100
100
100
100
100
100
75
75
75
ROUT
GOUT
BOUT
R1
R2
R3
X
CHANNEL SELECT
Y
4332-29

Figure 3. Typical Connection for a 3:1 Component Video Multiplexer

A Bandwidth Selectable Circuit

In Figure 4, a circuit is shown that allows three signals to be either low pass filtered or full bandwidth.

This could be useful where an input signal is frequently noisy. The component values shown give a Butterworth LPF response, with a −3 dB frequency of 50 MHz. Note again, the resistor values are low, so that stray capacitance does not affect the desired cut-off frequency.

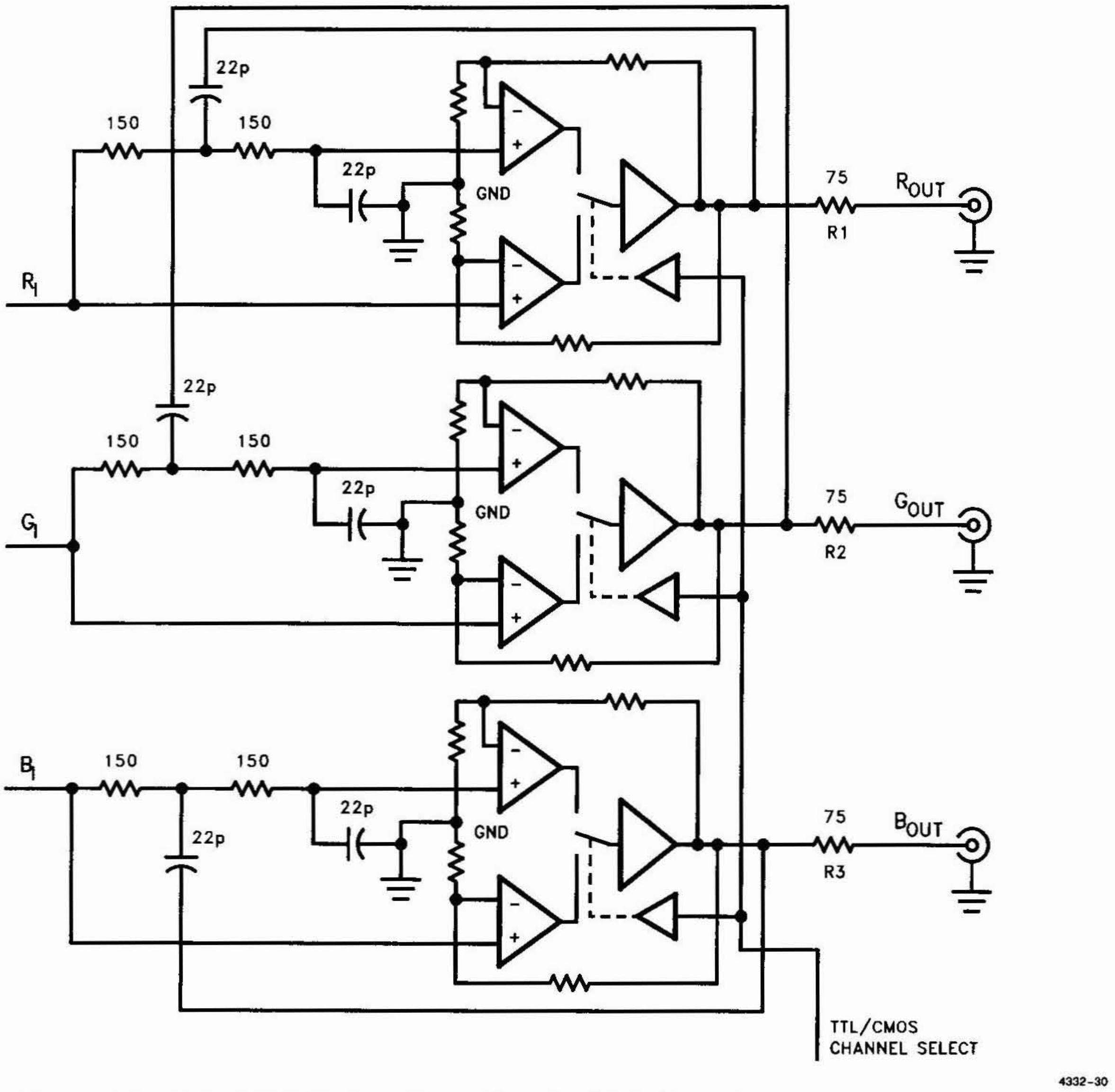

22p
150
150
22p
GND
75
R_OUT
R1
R_I
22p
150
150
22p
GND
75
G_OUT
R2
G_I
B_I
150
150
22p
22p
GND
75
B_OUT
R3
TTL/CMOS
CHANNEL SELECT
4332-30

Figure 4. Switched 50 MHz Low Pass Filter for High/Low Resolution Monitors

EL4332 Macromodel

```
* EL4332 Macromodel
* Revision A, April 1996
****************************************************************************
*Applications Hints. The EL4332 has two VCC pins, one VEE pin, and three ground
*pins. The VCC pins (pins 14 and 15 are internally shorted together in the model,
*but the ground pins (GND1, GND2, and GND3 (nodes 2, 7, and 10, repsectively)
*must be connected to ground (node 0) using a 1e-6Ω resistor. Alternatively,
* nodes 2, 7, and 10 may be connected to ground through a 25Ω resistor in parallel
* with a 4 nH inductor to simulate package and PCB parasitics.
****************************************************************************
* Connections:
* OUT1
* |     GND1
* |     |     A1
* |     |     |     B1
* |     |     |     |      B2
* |     |     |     |      |      A2
* |     |     |     |      |      |     GND2
* |     |     |     |      |      |     |     OUT2
* |     |     |     |      |      |     |     |
* |     |     |     |      |      |     |     |
* 1     2     3     4      5      6     7     8
*
* OUT3
* |     GND3
* |     |     B3
* |     |     |     A3
* |     |     |     |      VEE
* |     |     |     |      |      VCC
* |     |     |     |      |      |     VCC
* |     |     |     |      |      |     |     A/B
* |     |     |     |      |      |     |     |
* |     |     |     |      |      |     |     |
* 9     10    11    12     13     14    15    16
.subckt EL4332/EL 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
************A B Switch ***************
Rshort    14    15    1e-12
rshort1   15    0     100 Meg
Isw    14    110    1.5 mA
vref    111    0    1.6V
q1    101    16     110 qp
q2    102    111    110 qp
R1    101    13    500
R2    102    13    500
Rd1    107    0    100
Esw 107 0 table {v(102, 101)*100} (0,0) (1,1)
*
************Amplifier #1 ************
q131    103    3      112 qp
q141    104    114    113 qp
```

EL4332 Macromodel — Contd.

```
q151    105    4     115 qp
q161    106    117    116 qp
Ia11    14     112    1 mA
Ia21    14     113    1 mA
Ib11    14     115    1 mA
Ib21    14     116    1 mA
Rga1     112    113    275
Rgb1     115    116    275
R31     103    13     275
R41     104    13     275
R51     105    13     275
R61     106    13     275
R71     1     114     400
R81     114    2     400
R91     1     117     400
R110     117    2     400
Ediff1 108 0 value {(v(104,103)*v(107)) + (v(106,105)*(1-v(107)))}
rdiff1     108     0     1K
*
*Compensation Section
*
ga1     0     134     108     0     1m
rh1     134     0     5 Meg
cc1     134     0     0.6 pF
*
*     Poles
*
ep1     141     0     134     0     1.0
rpa1     141     142     200
cpa1     142     0     0.75 pF
rpb1     142     143     200
cpb1     143     0     0.75 pF
*
*     Output Stage
*
i011     15     150     1.0 mA
i021     151     13     1.0 mA
q71     13     143     150 qp
q81     15     143     151 qn
q91     15     150     152 qn
q101     13     151     153 qp
ros11     152     1     2
ros21     153     1     2
*
************Amplifier #2***********
q231     203     6     212 qp
q241     204     214     213 qp
q251     205     5     215 qp
q261     206     217     216 qp
```

EL4332 Macromodel — Contd.

```
Ia12    14    212    1 mA
Ia22    14    213    1 mA
Ib12    14    215    1 mA
Ib22    14    216    1 mA
Rga2    212    213    275
Rgb2    215    216    275
R231    203    13    275
R241    204    13    275
R251    205    13    275
R261    206    13    275
R271    8    214    400
R281    214    7    400
R291    8    217    400
R210    217    7    400
Ediff2 208 0 value {(v(204,203)*v(107)) + (v(206,205)*(1-v(107)))}
rdiff2 208 0 1K
*
* Compensation Section
*
ga2    0    234    208    0    1m
rh2    234    0    5 Meg
cc2    234    0    0.6 pF
*
* Poles
*
ep2    241    0    234    0    1.0
rpa2    241    242    200
cpa2    242    0    0.75 pF
rpb2    242    243    200
cpb2    243    0    0.75 pF
*
*    Output Stage
*
i012    15    250    1.0 mA
i022    251    13    1.0 mA
q271    13    243    250 qp
q281    15    243    251 qn
q291    15    250    252 qn
q201    13    251    253 qp
ros12    252    8    2
ros22    253    8    2
*
************Amplifier #3 ************
q331    303    12    312 qp
q341    304    314    313 qp
q351    305    11    315 qp
q361    306    317    316 qp
Ia13    14    312    1 mA
Ia23    14    313    1 mA
```

EL4332 Macromodel — Contd.

```
Ib13    14    315    1 mA
Ib23    14    316    1 mA
Rga3    312   313    275
Rgb3    315   316    275
R331    303   13     275
R341    304   13     275
R351    305   13     275
R361    306   13     275
R371    9     314    400
R381    314   10     400
R391    9     317    400
R310    317   10     400
Ediff3 308 0 value {( v(304,303)*(v(107)) + (v(306,305)*(1-v(107)))}
rdiff3 308 0 1K
*
* Compensation
*
ga3     0     334    308    0    1m
rh3     334   0      5 Meg
cc3     334   0      0.6 pF
*
* Poles
*
ep3     341   0      334    0    1.0
rpa3    341   342    200
cpa3    342   0      0.75 pF
rpb3    342   343    200
cpb3    343   0      0.75 pF
*
* Output Stage
*
i013    15    350    1.0 mA
i023    351   13     1.0 mA
q371    13    343    350 qp
q381    15    343    351 qn
q391    15    350    352 qn
q301    13    351    353 qp
ros13   352   9      2
ros23   353   9      2
*
* Power Supply Current
*
ips     15    13     22 mA
*
*    Models
*
.model   qp   pnp(is=1.5e-16   bf=300   tf=0.01 ns)
.model   qn   npn(is=0.8e-18   bf=300   tf=0.01 ns)
.ends
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4390C

Triple 80 MHz Video Amplifier with DC Restore

Features

- 80 MHz −3 dB bandwidth for gains of 1 to 10
- 800 V/μs slew rate
- 15 MHz bandwidth flat to 0.1 dB
- Excellent differential gain and phase
- TTL/CMOS compatible DC restore function
- Available in 16 lead P-DIP, 16 lead SOL

Applications

- RGB drivers requiring DC restoration
- RGB multiplexers requiring DC restoration
- RGB building blocks
- Video gain blocks requiring DC restoration
- Sync and color burst processing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4390CN	−40°C to +85°C	16-Pin P-DIP	MDP0031
EL4390CM	−40°C to +85°C	16-Lead SOL	MDP0027

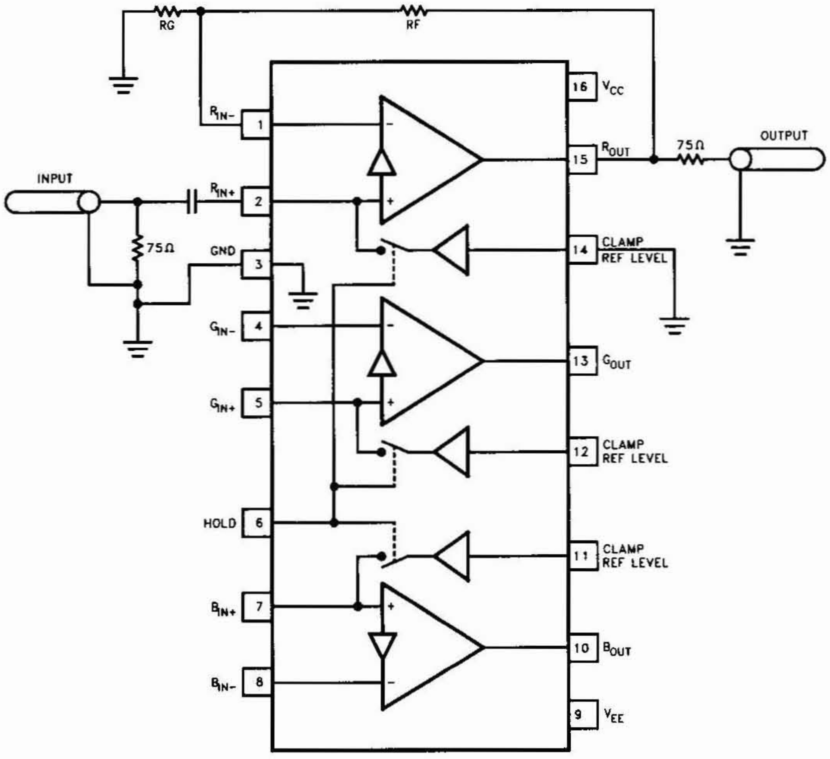
General Description

The EL4390C is three wideband current-mode feedback amplifiers optimized for video performance, each with a DC restore amplifier. The DC restore function is activated by a common TTL/CMOS compatible control signal while each channel has a separate restore reference.

Each amplifier can drive a load of 150Ω at video signal levels. The EL4390C operates on supplies as low as ±4V up to ±15V.

Being a current-mode feedback design, the bandwidth stays relatively constant at approximately 80MHz over the ±1 to ±10 gain range. The EL4390C has been optimized for use with 1300Ω feedback resistors.

Connection Diagram


RG
RF
R_{IN-}
R_{IN+}
GND
G_{IN-}
G_{IN+}
HOLD
B_{IN+}
B_{IN-}
INPUT
75Ω
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
V_{CC}
R_{OUT}
75Ω
OUTPUT
CLAMP REF LEVEL
G_{OUT}
CLAMP REF LEVEL
CLAMP REF LEVEL
B_{OUT}
V_{EE}
4390-1

November 1994, Rev A

EL4390C

Triple 80 MHz Video Amplifier with DC Restore

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+33V	Internal Power Dissipation	See Curves
Voltage at V_S+	+18V	Operating Ambient Temp. Range	−40°C to +85°C
Voltage at V_S-	−18V	Operating Junction Temperature	150°C
Voltage between $V_{IN}+$ and $V_{IN}-$	±6V	Storage Temperature Range	−65°C to +150°C
Current into $V_{IN}+$ and $V_{IN}-$	5mA		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 1KΩ

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Amplifier Section (not restored)							
V_{OS}	Input Offset Voltage	+25°C		2	15	II	mV
I_B+	$I_{IN}+$ Input Bias Current	+25°C		0.2	5	II	μA
I_B-	$I_{IN}-$ Input Bias Current	+25°C		10	65	II	μA
R_{OL}	Transimpedance (Note 1)	+25°C	100	220		II	kΩ
$R_{IN}-$	I_N- Resistance	+25°C		50		V	Ω
CMRR	Common-Mode Rejection Ratio (Note 2)	+25°C	50	56		II	dB
PSRR	Power Supply Rejection Ratio (Note 4)	+25°C	50	70		II	dB
V_O	Output Voltage Swing; R_L = 1kΩ	+25°C	±12	±13		II	V
I_{SC}	Short-Circuit Current	+25°C	45	70	100	II	mA
I_{SY}	Supply Current (Quiescent)	+25°C	10	20	32	II	mA
Restoring Section							
V_{OS}, COMP	Composite Input Offset Voltage (Note 3)	+25°C		8	35	II	mV
I_B+, R	Restore I_N+ Input Bias Current	+25°C		0.2	5	II	μA
I_{OUT}	Restoring Current Available	+25°C	2	4		II	mA
PSRR	Power Supply Rejection Ratio (Note 4)	+25°C	50	70		II	dB
G_{OUT}	Conductance	+25°C		8		V	mA/V
I_{SY}, RES	Supply Current, Restoring	+25°C	10	23	37	II	mA
V_{IL}, RES	RES Logic Low Threshold	+25°C		1.0	1.4	II	V
V_{IH}, RES	RES Logic High Threshold	+25°C	1.4	1.8		II	V

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 1KΩ — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Restoring Section							
I_{IL}, RES	RES Input Current, Logic Low	+25°C		2	10	II	μA
I_{IH}, RES	RES Input Current, Logic High	+25°C		0.5	3	II	μA

Note 1: For current feedback amplifiers, $A_{VOL} = R_{OL}/R_{IN}-$.

Note 2: $V_{CM} = \pm 10V$ for $V_S = \pm 15V$.

Note 3: Measured from V_{CL} to amplifier output, while restoring.

Note 4: V_{OS} is measured at $V_S = \pm 4.5V$ and $V_S = \pm 16V$, both supplies are changed simultaneously.

Closed Loop AC Electrical Characteristics

Supplies at ±15V, Load = 150Ω and 15 pF, $T_A = 25°C$ (See note 7 re: test fixture)

Parameter	Description	Min	Typ	Max	Test Level	Units
Amplifier Section						
SR	Slew Rate (Note 5)		800		V	V/μs
SR	Slew Rate w/ ±5V Supplies (Note 5)		550		V	V/μs
BW	Bandwidth, −3dB, $A_V = 1$ ±5V Supplies, −3dB		95 72		V V	MHz MHz
BW	Bandwidth, −0.1 dB ±5V Supplies, −0.1dB		20 14		V V	MHz MHz
dG	Differential Gain at 3.58 MHz at ±5V Supplies (Note 6)		0.02 0.02		V V	% %
dθ	Differential Phase at 3.58 MHz at ±5V Supplies (Note 6)		0.03 0.06		V V	(°) (°)
Restoring Section						
T_{RE}	Time to Enable Restore		35		V	ns
T_{RD}	Time to Disable Restore		35		V	ns

Note 5: SR is measured at 20% to 80% of 4V pk-pk square wave, with $A_V = 5$, $R_F = 820\Omega$, $R_G = 200\Omega$.

Note 6: DC offset from −0.714V to +0.714V, AC amplitude is 286m Vp-p, equivalent to 40 ire.

Note 7: Test fixture was designed to minimize capacitance at the I_N- input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.

Table 1. Charge Storage Capacitor Value vs. Droop and Charging Rates

Cap Value (nF)	Droop in 60μS (mV)	Charge in 2μS (mV)	Charge in 4μS (mV)
10	30	400	800
22	13.6	182	364
47	6.4	85	170
100	3.0	40	80
220	1.36	18	36

These numbers represent the worst case bias current, and the worst case charging current. Note that to get the full (2mA+) charging current, the clamp input must have >250mV of error voltage.

Note that the magnitude of the bias current will decrease as temperature increases.

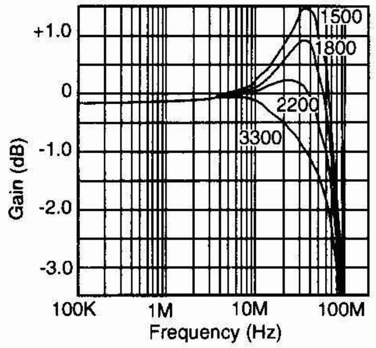
The basic droop formula is :
$V\ (\text{droop}) = I_{B+} \times (\text{Line time} - \text{Charge time}) / \text{capacitor value}$

and the basic charging formula is:
$V\ (\text{charge}) = I_{OUT} \times \text{Charge time} / \text{capacitor value}$

Where I_{OUT} is:
$I_{OUT} = (\text{Clamp voltage} - \text{IN+ voltage}) / 120$

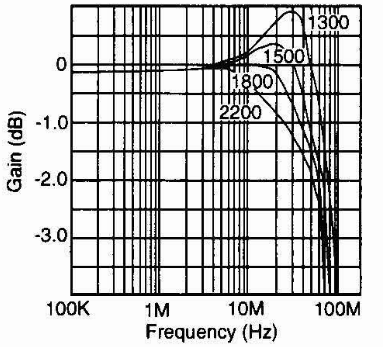
Typical Performance Curves

Gain Flatness
for Various R_F
V_S = ±15V, A_V = 0 dB



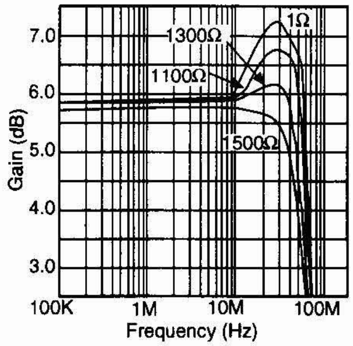
4390-2

Gain Flatness
for Various R_F
V_S = ±5V, A_V = 0 dB



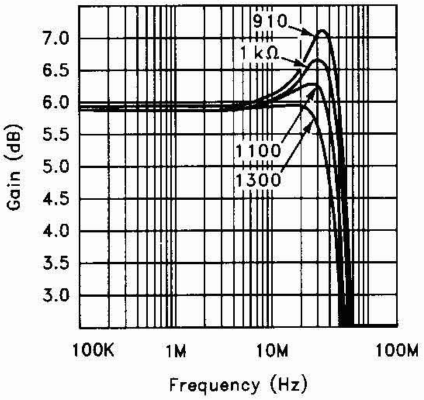
4390-3

Gain Flatness
for Various R_F and R_G Values
V_S = ±15V, A_V = 6 dB



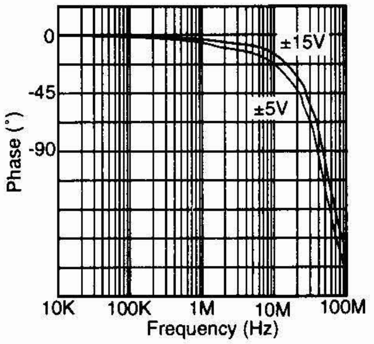
4390-4

Gain Flatness
for Various R_F and R_G Values
V_S = ±5V, A_V = 6 dB



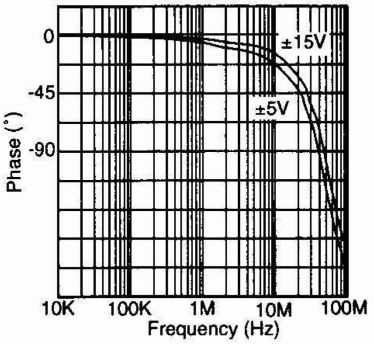
4390-6

Phase Shift
for A_V = 2,
R_F = R_G = 1300Ω



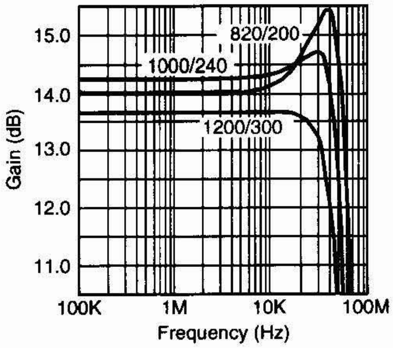
4390-5

Phase Shift for A_V = 2,
R_F = R_G = 1000Ω
at V_S = ±5V and V_S = ±15V



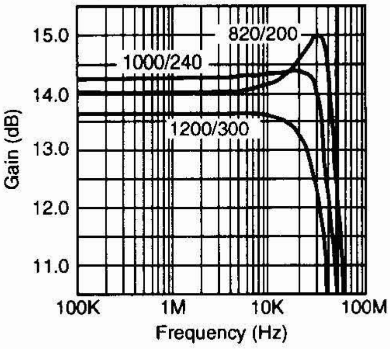
4390-7

Gain Flatness
V_S = ±15V, A_V = 14 dB,
R_F/R_G as Shown



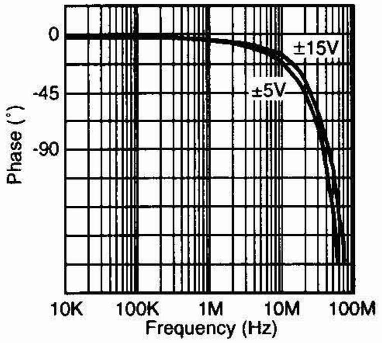
4390-8

Gain Flatness
V_S = ±5V, A_V = 14 dB,
R_F/R_G as Shown



4390-9

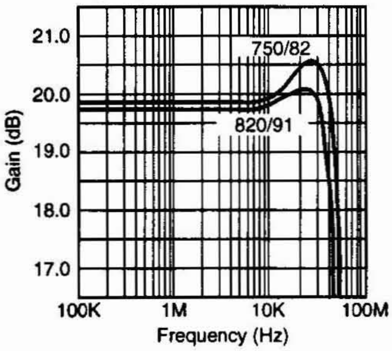
Phase Shift
for A_V = 5 dB, R_F = 820Ω,
R_G = 200Ω, V_S = ±5V



4390-10

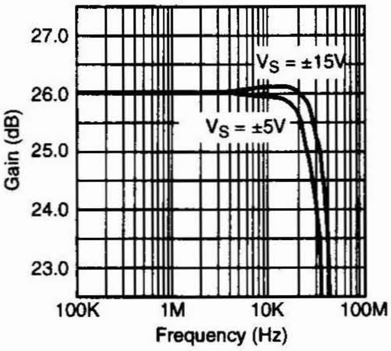
Typical Performance Curves — Contd.

Gain Flatness
$V_S = \pm 5V$, $A_V = 20$ dB, R_F/R_G as Shown



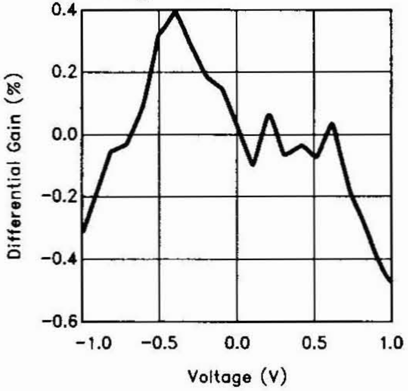
4390-11

Gain Flatness
$V_S = \pm 5V$, $A_V = 26$ dB, $R_F = 680\Omega$, $R_G = 36\Omega$



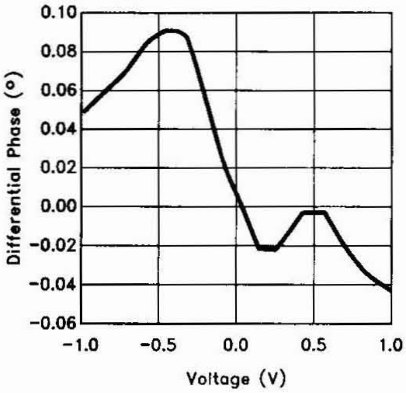
4390-12

Differential Gain at $V_S = \pm 15V$



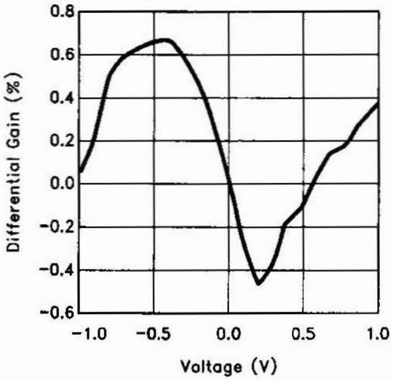
4390-17

Differential Phase at $V_S = \pm 15V$



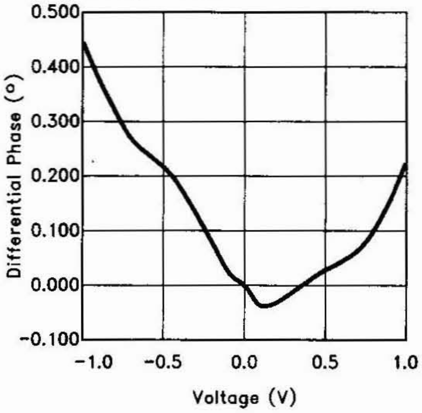
4390-18

Differential Gain at $V_S = \pm 5V$



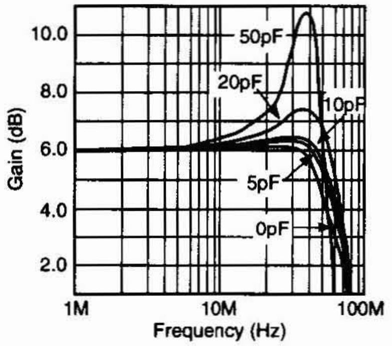
4390-19

Differential Phase at $V_S = \pm 5V$



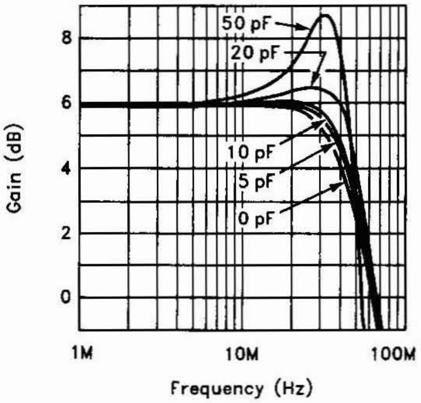
4390-20

Frequency Response for Various C_{LOAD}, $V_S = \pm 15V$, $R_F = R_G = 1300\Omega$



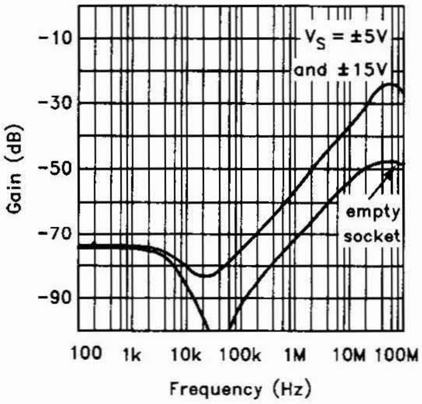
4390-13

Frequency Response for Various C_{LOAD}, $V_S = \pm 5V$, $R_F = R_G = 1300\Omega$



4390-14

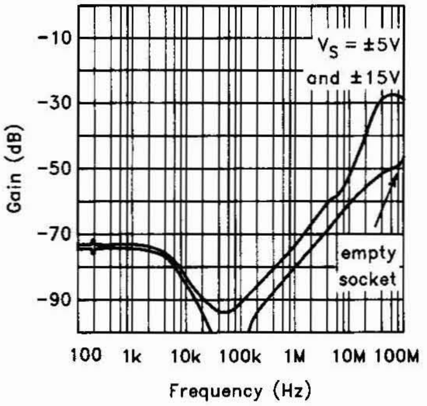
Crosstalk, Channel R and B to Channel G, $V_S = \pm 5V$, $R_F = 1300\Omega$



4390-15

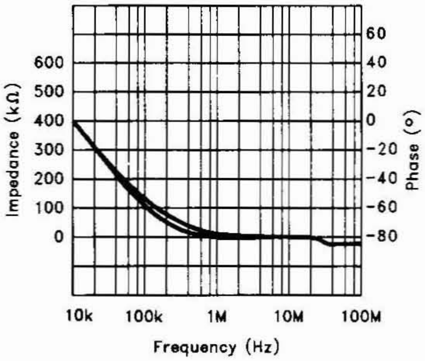
Typical Performance Curves — Contd.

Crosstalk, Channel R and G to Channel B, V_S = ±5V, R_F = 1300Ω



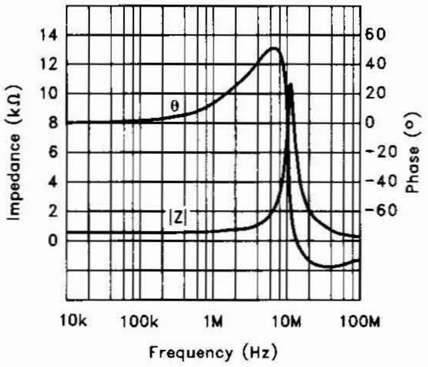
4390-16

I_N+ Input Impedance during HOLD, V_S = ±5V



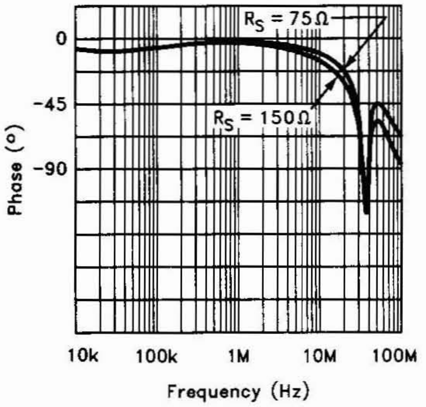
4390-21

I_N+ Input Impedance during SAMPLE, V_S = ±5V



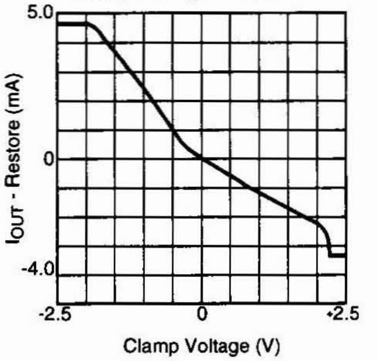
4390-22

Phase Shift at I_N+ Pin during Restore, R_S = 75Ω and 150Ω, V_S = ±5V



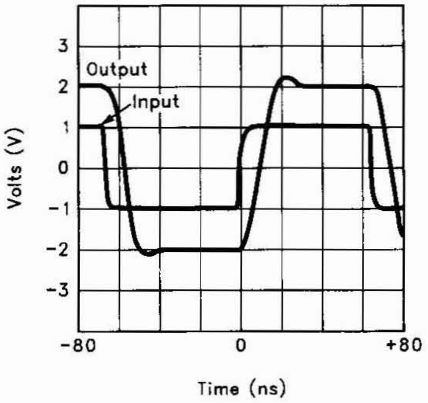
4390-23

I_{OUT} Restoring vs Clamp, Voltage at V_S = ±5V



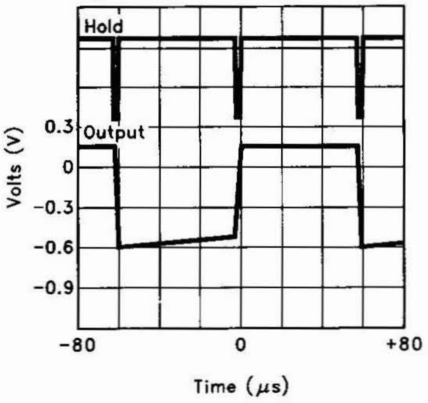
4390-24

Pulse Response with A_V = 2, R_F = R_G = 1300Ω at V_S = ±5V



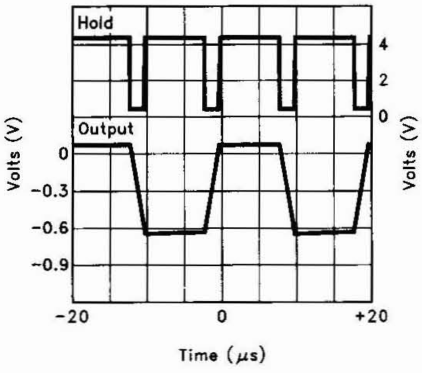
4390-25

Output during DC-Restoration, Showing DC Droop R_F = R_G = 1300Ω, V_S = ±5V



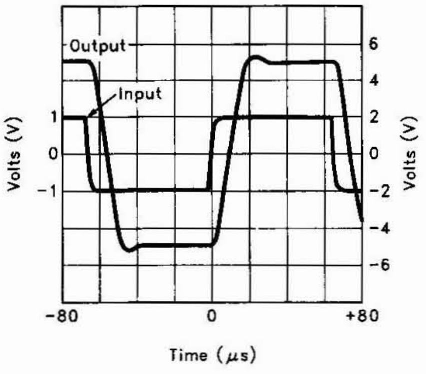
4390-26

Output during DC-Restoration, R_F = R_G = 1300Ω, V_S = ±5V



4390-27

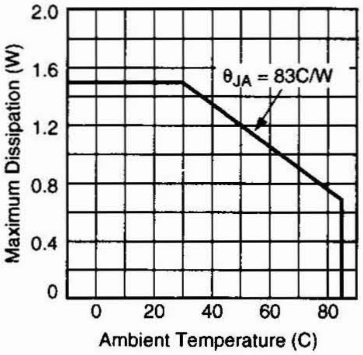
Pulse Response with A_V = 5, R_F = 820Ω and R_G = 200Ω at V_S = ±15V



4390-28

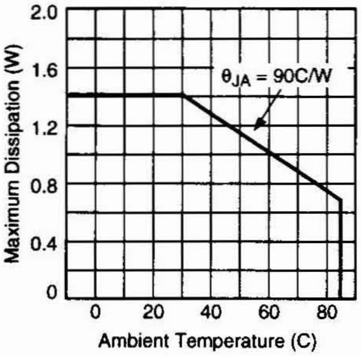
Typical Performance Curves — Contd.

Maximum Power Dissipation vs Ambient Temperature— 16-Pin PDIP

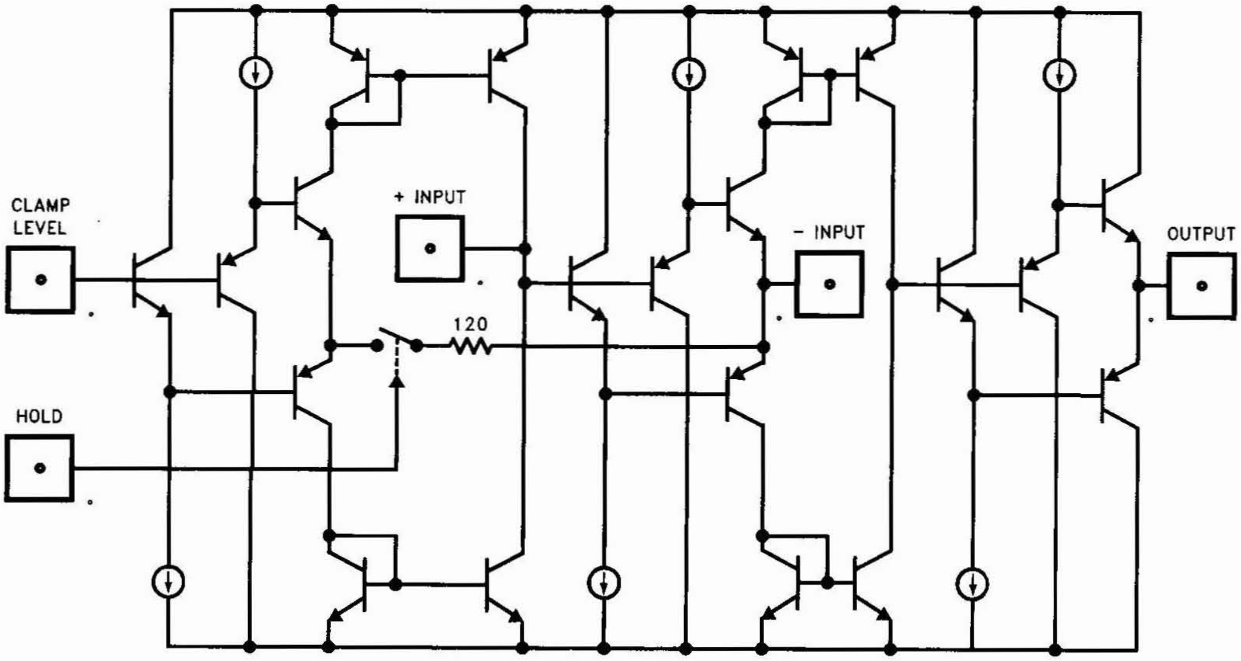


4390-29

Maximum Power Dissipation vs Ambient Temperature— 16-Pin SOL



4390-30


CLAMP LEVEL
HOLD
+ INPUT
120
− INPUT
OUTPUT

4390-31

Simplified Schematic of One Channel of EL4390

Applications Information

Circuit Operation

Each channel of the EL4390 contains a current feedback amplifier and a TTL/CMOS compatible clamp circuit. The current that the clamp can source or sink into the non-inverting input is approximately:

$$I = (V_{CLAMP} - V_{IN+}) / 120$$

So, when the non-inverting input is at the same voltage as the clamp reference, no current will flow, and hence no charge is added to the capacitor. When there is a difference in voltage, current will flow, in an attempt to cancel the error AT THE NON-INVERTING input. The amplifier's offset voltage and ($I_{B-} \times R_F$) DC errors are not cancelled with this loop. It is purely a method of adding a controlled DC offset to the signal.

As well as the offset voltage error, which goes up with gain, and the $I_{B-} \times R_F$ error which drops with gain, there is also the I_{B+} error term. Since the amplifier is capacitively coupled, this small current is slowly integrated and shows up as a very slow ramp voltage. Table below shows the output voltage drift in 60μS for various values of coupling capacitor, all assuming the very worst I_{B+} current.

Table 1. Charge Storage Capacitor Value vs. Droop and Charging Rates

Cap Value (nF)	Droop in 60μS (mV)	Charge in 2μS (mV)	Charge in 4μS (mV)
10	30	400	800
22	13.6	182	364
47	6.4	85	170
100	3.0	40	80
220	1.36	18	36

In normal circuit operation, the picture content will also cause a slow change in voltage across the capacitor, so at every back porch time period, these error terms can be corrected.

When a signal source is being switched, eg. from two different surveillance cameras, it is recommended to synchronize the switching with the vertical blanking period, and to drive the HOLD pin (pin 6) low, during these lines. This will ensure that the system has been completely restored, regardless of the average intensity of the two pictures.

Application Hints

Figures 1 & 2 shows a three channel DC-restoring system, suitable for R-G-B or Y-U-V component video, or three synchronous composite signals.

Figure 1 shows the amplifiers configured for non-inverting gain, and Figure 2 shows the amplifiers configured for inverting gains. Note that since the DC-restoring function is accomplished by clamping the amplifier's non-inverting input, during the back porch period, any signal on the non-inverting input will be distorted. For this reason, it is recommended to use the inverting configuration for composite video, since this avoids the color burst being altered during the clamp time period.

Since all three amplifiers are monolithic, they run at the same temperature, and will have very similar input bias currents. This can be used to advantage, in situations where the droop voltage needs to be compensated, since a single trim circuit can be used for all three channels. A 560KΩ or similar value resistor helps to isolate each signal. See Figure 2. The advantage of compensating for the droop voltage, is that a smaller capacitor can be used, which allows a larger level restoration within one line. See Table 1 for values of capacitor and charge/droop rates.

Applications Information — Contd.

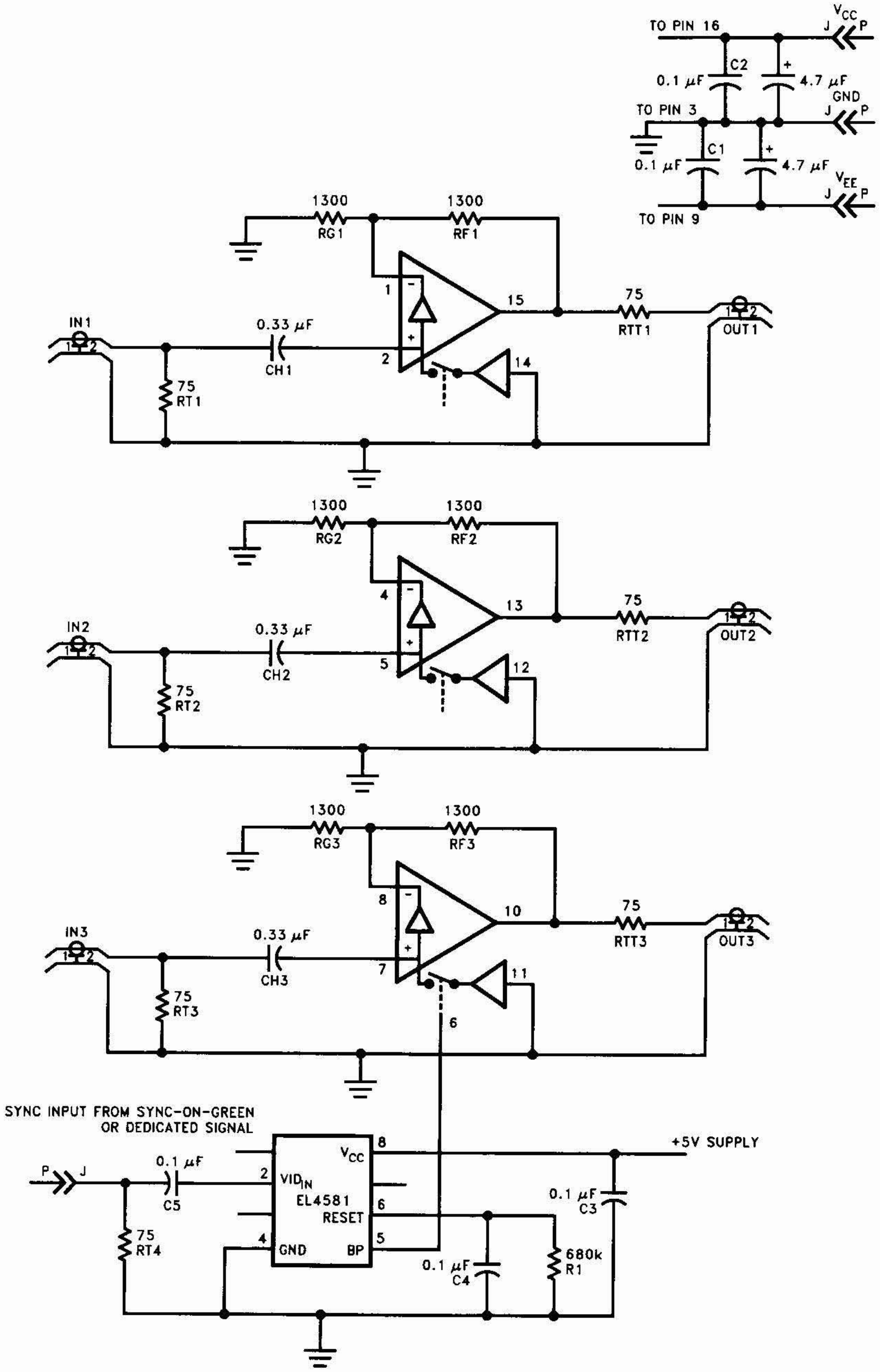

TO PIN 16
VCC
J P
0.1 µF
C2
4.7 µF
GND
TO PIN 3
C1
0.1 µF
4.7 µF
VEE
TO PIN 9
1300 RG1
1300 RF1
1 15 2 14
IN1
0.33 µF CH1
75 RT1
75 RTT1
OUT1
1300 RG2
1300 RF2
4 13 5 12
IN2
0.33 µF CH2
75 RT2
75 RTT2
OUT2
1300 RG3
1300 RF3
8 10 7 11 6
IN3
0.33 µF CH3
75 RT3
75 RTT3
OUT3
SYNC INPUT FROM SYNC-ON-GREEN OR DEDICATED SIGNAL
P J
0.1 µF C5
75 RT4
VCC 8
2 VIDIN
EL4581
RESET 6
4 GND
BP 5
+5V SUPPLY
0.1 µF C3
0.1 µF C4
680k R1
4390-32

Figure 1

Applications Information — Contd.

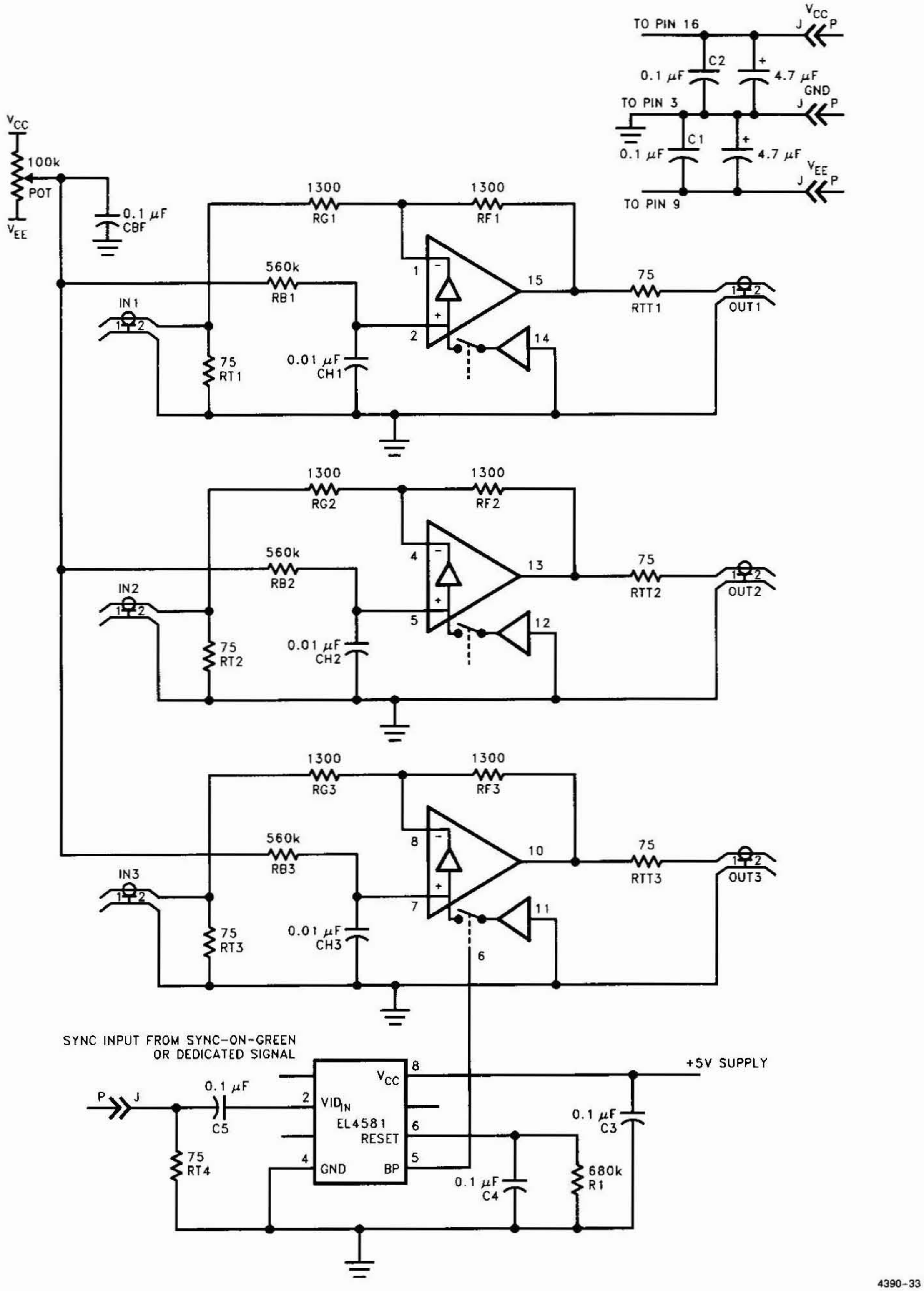

TO PIN 16
V_{CC}
J
P
C2
0.1 µF
+
4.7 µF
GND
TO PIN 3
C1
0.1 µF
+
4.7 µF
V_{EE}
TO PIN 9
V_{CC}
100k
POT
V_{EE}
0.1 µF
CBF
1300
RG1
1300
RF1
560k
RB1
IN1
1
2
75
RT1
0.01 µF
CH1
2
1
15
14
75
RTT1
OUT1
1300
RG2
1300
RF2
560k
RB2
IN2
75
RT2
0.01 µF
CH2
4
5
13
12
75
RTT2
OUT2
1300
RG3
1300
RF3
560k
RB3
IN3
75
RT3
0.01 µF
CH3
8
7
10
11
6
75
RTT3
OUT3
SYNC INPUT FROM SYNC-ON-GREEN
OR DEDICATED SIGNAL
P
J
0.1 µF
C5
75
RT4
2
VID_{IN}
EL4581
4
GND
V_{CC}
8
RESET
6
BP
5
+5V SUPPLY
0.1 µF
C3
0.1 µF
C4
680k
R1
4390-33

Figure 2

Applications Information — Contd.

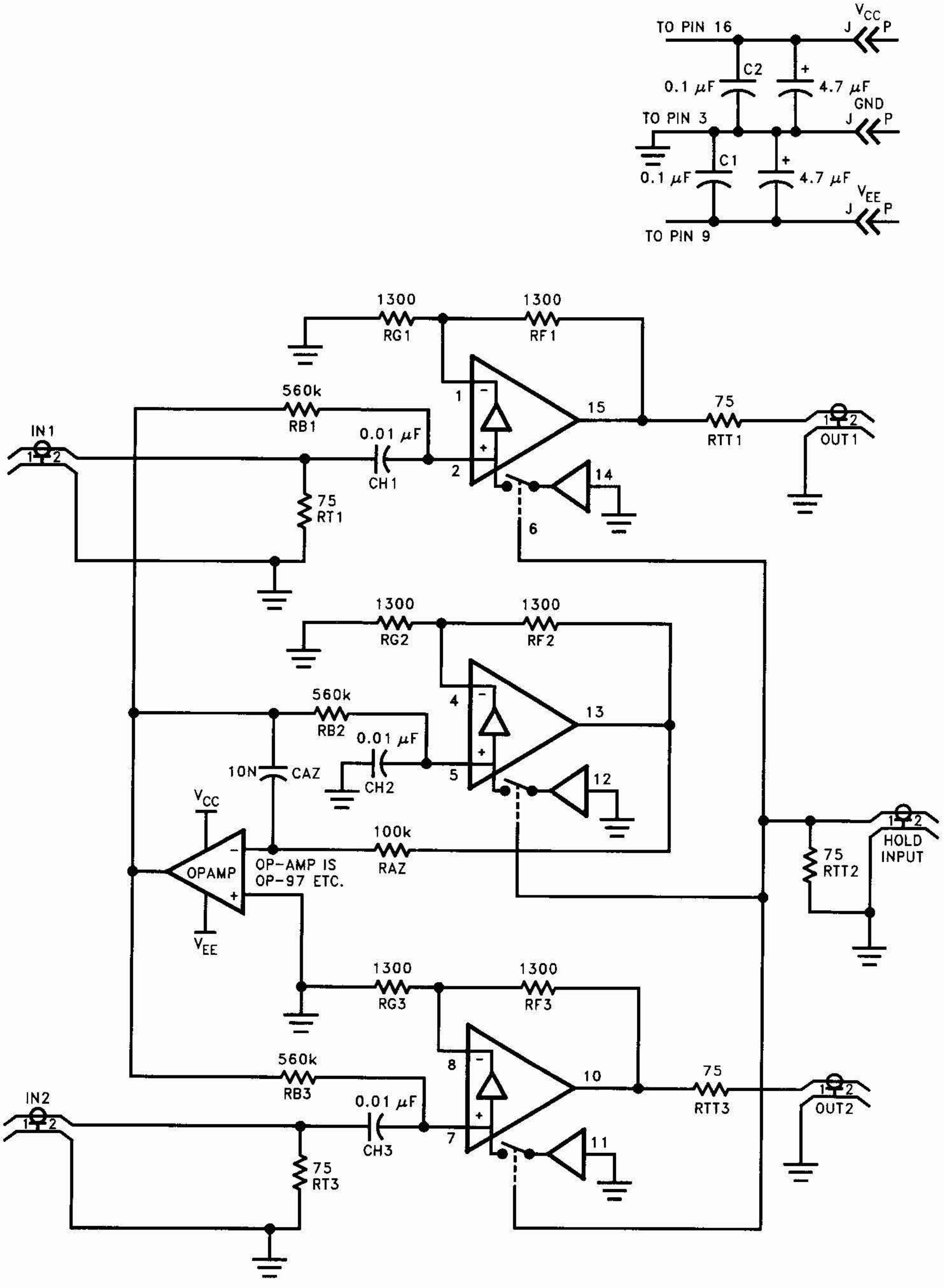

TO PIN 16
V_CC
J P
C2
0.1 µF
+
4.7 µF
GND
TO PIN 3
C1
0.1 µF
+
4.7 µF
V_EE
TO PIN 9
1300
RG1
1300
RF1
560k
RB1
IN1
0.01 µF
CH1
75
RT1
1
2
15
14
6
75
RTT1
OUT1
1300
RG2
1300
RF2
560k
RB2
0.01 µF
CH2
4
5
13
12
10N
CAZ
V_CC
OPAMP
V_EE
100k
RAZ
OP-AMP IS
OP-97 ETC.
75
RTT2
HOLD
INPUT
1300
RG3
1300
RF3
560k
RB3
IN2
0.01 µF
CH3
75
RT3
8
7
10
11
75
RTT3
OUT2
4390-34

Figure 3

Applications Information — Contd.

In Figure 3, one of the three channels is used, together with a low-offset op-amp, to automatically trim the bias current of the other two channels. The two remaining channels are shown in the non-inverting configuration, but could equally well be set to provide inverting gains. Two DC-restored channels are typically needed in fader applications. See the EL4094 and EL4095 for suitable, monolithic video faders.

Layout and Dissipation Considerations

As with all high frequency circuits, the supplies should be bypassed with a 0.1μF ceramic capacitor very close to the supply pins, and a 4.7μF tantalum capacitor fairly close, to handle the high current surges. While a ground plane is recommended, the amplifier will work well with a "star" grounding scheme. The pin 3 ground is only used for the internal bias generator and the reference for the TTL compatible "HOLD" input.

As with all current feedback capacitors, all stray capacitance to the inverting inputs should be kept as low as possible, to avoid unwanted peaking at the output. This is especially true if the value of Rf has already been reduced to raise the bandwidth of the part, while tolerating some peaking. In this situation, additional capacitance on the inverting input can lead to an unstable amplifier.

Since there are three amplifiers all in one package, and each amplifier can sink or source typically more than 70mA, some care is needed to avoid excessive die temperatures. Sustained, DC currents, of over 30mA, are not recommended, due to the limited current handling capability of the metal traces inside the IC. Also, the short circuit protection can be tripped with currents as low as 45mA, which is seen as excessive distortion in the output waveform. As a quick rule of thumb, both the SOL and DIP 16 pin packages can dissipate about 1.4 watts at 25°C, and with ±15V supplies and a worst case quiescent current of 32mA, yields 0.96 watts, before any load is driven.

Dissipation of the EL4390 can be reduced by lowering the supply voltage. Although some performance is degraded at lower supplies, as seen in the characteristic curves, it is often found to be a useful compromise. The bandwidth can be recovered, by reducing the value of R_F, and R_G as appropriate.

EL4421C/22C/41C/42C/43C/44C
Multiplexed-Input Video Amplifiers

Features

- Unity or + 2-gain bandwidth of 80 MHz
- 70 dB off-channel isolation at 4 MHz
- Directly drives high-impedance or 75Ω loads
- .02% and .02° differential gain and phase errors
- 8 ns switching time
- <100 mV switching glitch
- 0.2% loaded gain error
- Compatible with ±3V to ±15V supplies
- 160 mW maximum dissipation at ±5V supplies

Ordering Information

Part No.	Temp. Range	Package	Outline
EL4421CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL4421CS	−40°C to +85°C	8-Pin SO	MDP0027
EL4422CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL4422CS	−40°C to +85°C	8-Pin SO	MDP0027
EL4441CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4441CS	−40°C to +85°C	14-Pin SO	MDP0027
EL4442CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4442CS	−40°C to +85°C	14-Pin SO	MDP0027
EL4443CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4443CS	−40°C to +85°C	14-Pin SO	MDP0027
EL4444CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4444CS	−40°C to +85°C	14-Pin SO	MDP0027

General Description

The EL44XX family of video multiplexed-amplifiers offers a very quick 8 ns switching time and low glitch along with very low video distortion. The amplifiers have good gain accuracy even when driving low-impedance loads. To save power, the amplifiers do not require heavy loading to remain stable.

The EL4421 and EL4422 are two-input multiplexed amplifiers. The -inputs of the input stages are wired together and the device can be used as a pin-compatible upgrade from the MAX453.

The EL4441 and EL4442 have four inputs, also with common feedback. These may be used as upgrades of the MAX454.

The EL4443 and EL4444 are also 4-input multiplexed amplifiers, but both positive and negative inputs are wired separately. A wide variety of gain- and phase-switching circuits can be built using independent feedback paths for each channel.

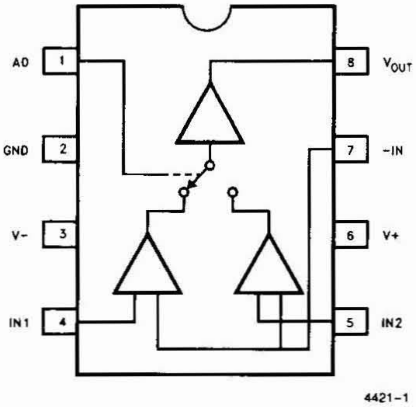
The EL4421, EL4441, and EL4443 are internally compensated for unity-gain operation. The EL4422, EL4442, and EL4444 are compensated for gains of +2 or more, especially useful for driving back-matched cables.

The amplifiers have an operational temperature of −40°C to +85°C and are packaged in plastic 8- and 14-pin DIP and 8- and 14-pin SO.

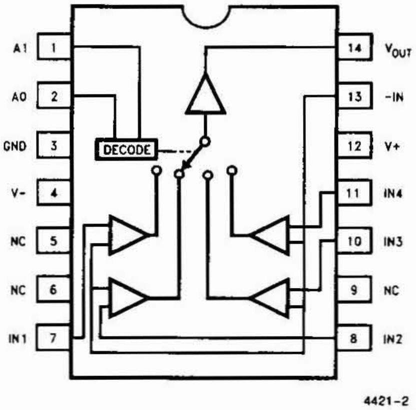
The EL44XX multiplexed-amplifier family is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is very rugged.

Connection Diagrams

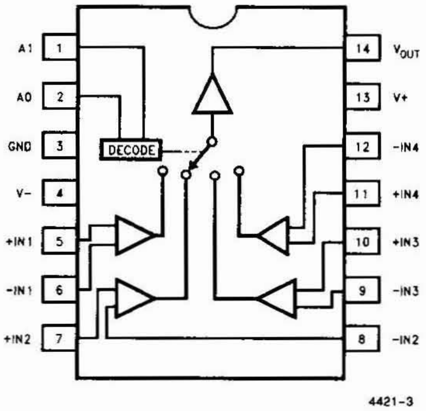
EL4421/EL4422



EL4441/EL4442



EL4443/EL4444



Manufactured under U.S. Patent No. 5,352,987

January 1996 Rev C

EL4421C/22C/41C/42C/43C/44C
Multiplexed-Input Video Amplifiers

Absolute Maximum Ratings

V+	Positive Supply Voltage	16.5V	V_{LOGIC}	Voltage at A0 or A1	−4V to 6V
V_S	V+ to V− Supply Voltage	33V	I_{IN}	Current into any Input, Feedback, or Logic Pin	4 mA
V_{IN}	Voltage at any Input or Feedback	V+ to V−	I_{OUT}	Output Current	30 mA
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V	P_D	Maximum Power Dissipation	See Curves

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics

Power supplies at ±5V, T_A = 25°C, R_L = 500Ω, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage '21, '41, and '43	−9	±3	9	I	mV
	'22, '42, and '44	−7	±2	7	I	
I_B	Input Bias Current, Positive Inputs Only of the '21, '22, '41, '42, and All Inputs of the '43 and '44	−12	−5	0	I	µA
I_{FB}	Input Bias Currents of Common Feedback					
	−'21 and '22	−24	−10	0	I	µA
	−'41 and '42	−48	−20	0	I	µA
I_{OS}	Input Offset Currents of the '43 and '44		60	350	I	nA
E_G	Gain Error of the '21 and '41 and '43		0.2	0.6	I	%
	(Note 1) '22, '42 and '44		0.1	0.6	I	V/V
A_{VOL}	Open-Loop Gain EL4443	350	500		I	V/V
	(Note 1) EL4444	500	750		I	V/V
V_{IN}	Input Signal Range, EL4421 and EL4441 (Note 2)	±2.5	±3		I	V
CMRR	Common-Mode Rejection Ratio, EL4443 and EL4444	70	90		I	dB
PSRR	Power Supply Rejection Ratio V_s from ±5V to ±15V	60	70		I	dB

Open-Loop DC Electrical Characteristics — Contd.

Power supplies at ±5V, $T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level	Units
CMIR	Common-Mode Input Range (Note 3) EL4443 and EL4444	±2.5	±3		I	V
V_{OUT}	Output Swing	±2.5	±3.5		I	V
I_{SC}	Output Short-Circuit Current	±40	±80		I	mA
F_T	Unselected Channel Feedthrough '21, '41, '43 Attenuation, (Note 1) '22, '42, '44	70 55	80 64		I I	dB dB
I_{LOGIC}	Input Current at A0 and A1 with Input = 0V and 5V	−16	−8	0	I	µA
V_{LOGIC}	Logic Valid High and Low Input Levels	0.8		2.0	I	V
I_S	Supply Current EL4421 and EL4422 EL4441, EL4442, EL4443, and EL4444		11 13	14 16	I	mA

Note 1: The '21, '41, and '43 devices are connected for unity-gain operation with 75Ω load and an input span of ±1V. The '22, '42, and '44 devices are connected for a gain of +2 with a 150Ω load and a ±1V input span with $R_F = R_G = 270Ω$.

Note 2: The '21 and '41 devices are connected for unity gain with a ±3V input span while the output swing is measured.

Note 3: CMIR is assured by passing the CMRR test at input voltage extremes.

Closed-Loop AC Electrical Characteristics

Power supplies at ±5V. $T_A = 25°C$, for EL4421, EL4441, and EL4443 $A_V = +1$ and $R_L = 500Ω$, for EL4422, EL4442, and EL4444 $A_V = +2$ and $R_L = 150Ω$ with $R_F = R_G = 270Ω$ and $C_F = 3$ pF; for all $C_L = 15$ pF

Parameter	Description	Min	Typ	Max	Test Level	Units
BW − 3 dB	−3 dB Small-Signal Bandwidth, EL4421, '41, '43 EL4422, '42, '44		80 65		V V	MHz MHz
BW ± 0.1 dB	0.1 dB Flatness Bandwidth		10		V	MHz
Peaking	Frequency Response Peaking		0.5		V	dB
SR	Slewrate, V_{OUT} between −2.5V and +2.5V, $V_S = ±12V$ EL4421, EL4441, EL4443 EL4422, EL4442, EL4444	 150 180	 200 240		 I I	 V/µsec V/µsec
V_n	Input-Referred Noise Voltage Density EL4421, EL4441, EL4443 EL4422, EL4442, EL4444		 18 14		 V V	 nV/rt-hz nV/rt-hz
d_G	Differential Gain Error, V_{OFFSET} between −0.7V and +0.7V EL4421, EL4441, EL4443 ($V_S = ±12V$) EL4421, EL4441, EL4443 ($V_S = ±5V$) EL4422, EL4442, EL4444 ($V_S = ±12V$) EL4422, EL4442, EL4444 ($V_S = ±5V$)		 0.01 0.10 0.02 0.11		 V V V V	 % % % %

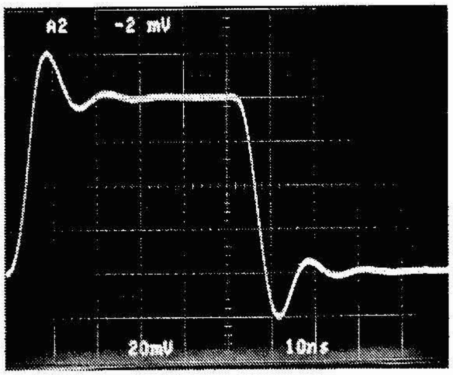
Closed-Loop AC Electrical Characteristics

Power supplies at ±5V. T_A = 25°C, for EL4421, EL4441, and EL4443 A_V = +1 and R_L = 500Ω, for EL4422, EL4442, and EL4444 A_V = +2 and R_L = 150Ω with R_F = R_G = 270Ω and C_F = 3 pF; for all C_L = 15 pF — Contd.

Parameter	Description	Min	Typ	Max	Test Level	Units
d∅	Differential Phase Error, V_{OFFSET} between −0.7V and +0.7V					
	EL4421, EL4441, EL4443 (V_S = ±12V)		0.01		V	°
	EL4421, EL4441, EL4443 (V_S = ±5V)		0.1		V	°
	EL4422, EL4442, EL4444 (V_S = ±12V)		0.02		V	°
	EL4422, EL4442, EL4444 (V_S = ±5V)		0.15		V	°
T_{MUX}	Multiplex Delay Time, Logic Threshold to 50% Signal Change					
	EL4421, '22		8		V	nsec
	EL4441, '42, '43, '44		12		V	nsec
V_{GLITCH}	Peak Multiplex Glitch					
	EL4421, '22		70		V	mV
	EL4441, '42, '43, '44		100		V	mV
ISO	Channel Off Isolation at 3.58 MHz (See Text)					
	EL4421, EL4441, EL4443		76		V	dB
	EL4422, EL4442, EL4444		63		V	dB

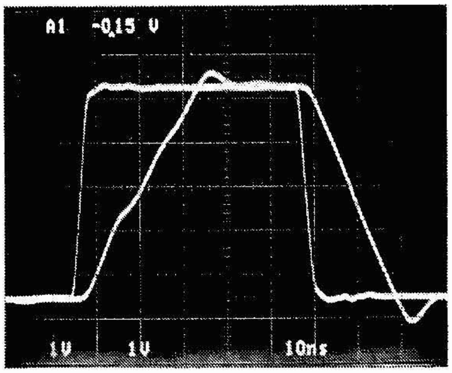
Typical Performance Curves

EL4421, EL4441, and EL4443
Small-Signal Transient Response
V_S = ±5V, R_L = 500Ω



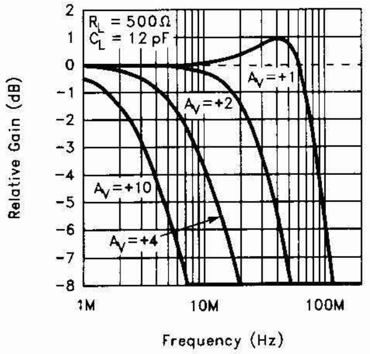
4421-5

EL4421, EL4441, and EL4443
Large-Signal Response
V_S = ±12V, R_L = 500Ω



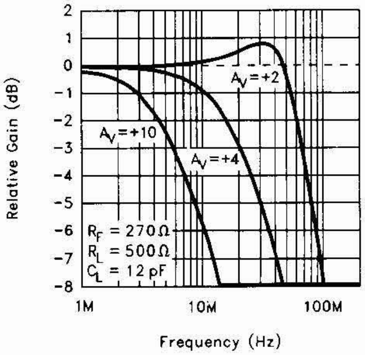
4421-6

EL4421, EL4441, and EL4443
Frequency Response for
Various Gains



4421-7

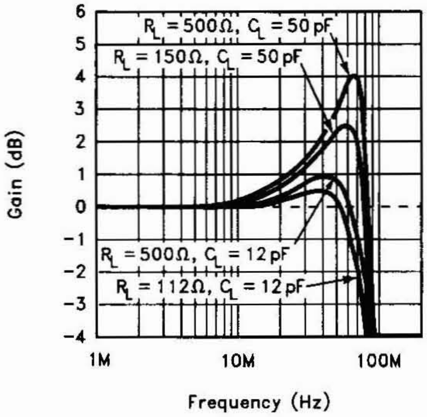
EL4422, EL4442, and EL4444
Frequency Response for
Various Gains



4421-8

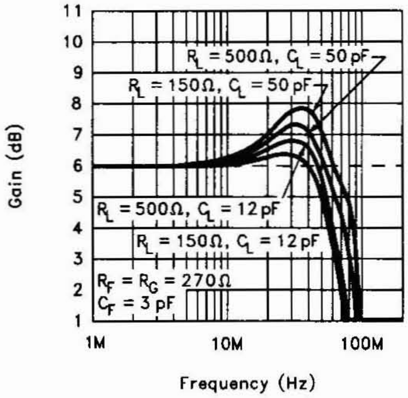
Typical Performance Curves — Contd.

EL4421, EL4441, and EL4443
Frequency Response for Various Loads
$V_S = \pm 5V$, $A_V = +1$



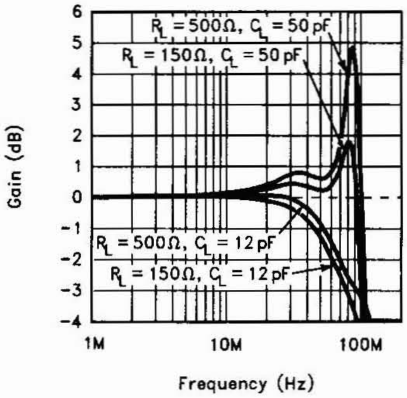
4421-9

EL4422, EL4442, and EL4444
Frequency Response for Various Loads
$V_S = \pm 5V$, $A_V = +2$



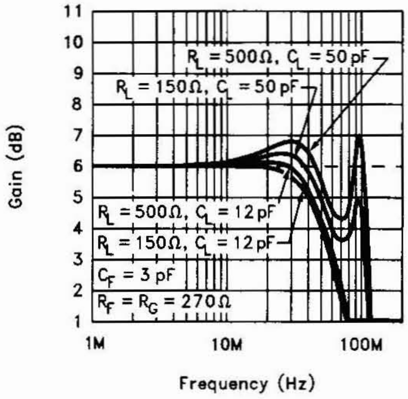
4421-10

Frequency Response
for Various Loads
$V_S = \pm 15V$, $A_V = +1$



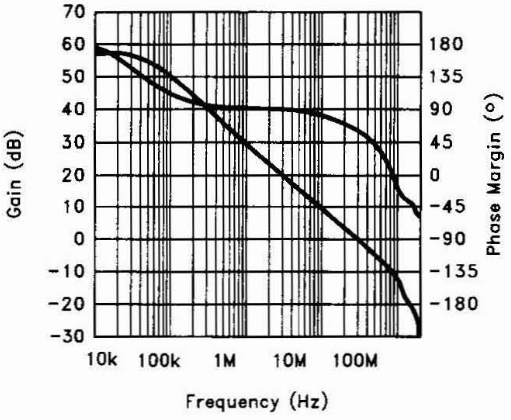
4421-11

EL4422, EL4442, and EL4444
Frequency Response for Various Loads
$V_S = \pm 15V$, $A_V = +2$



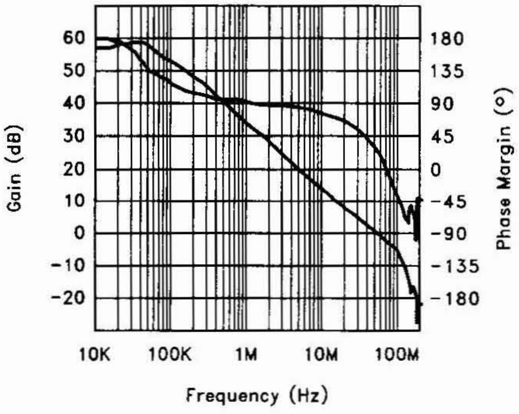
4421-12

EL4443 Open-Loop Gain and
Phase vs Frequency



4421-13

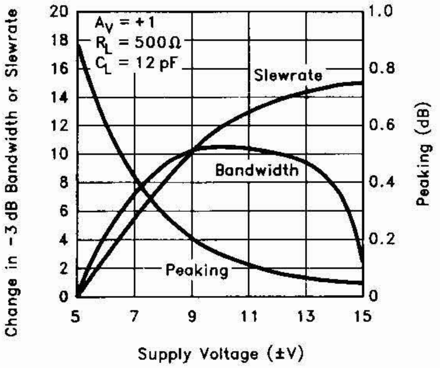
EL4444 Open-Loop Gain and
Phase vs Frequency



4421-37

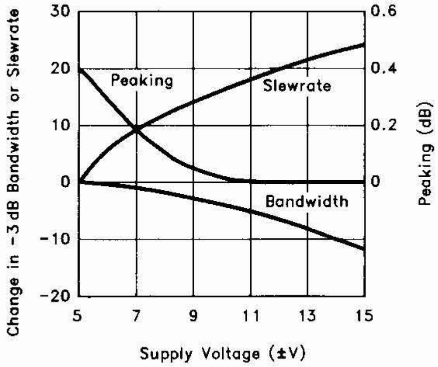
Typical Performance Curves — Contd.

EL4421, EL4441, and EL4443 −3 dB Bandwidth, Slewrate, and Peaking vs Supply Voltage



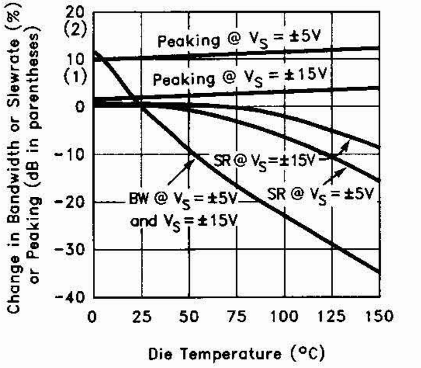
4421-14

EL4422, EL4442, and EL4444 −3 dB Bandwidth, Slewrate, and Peaking vs Supply Voltage



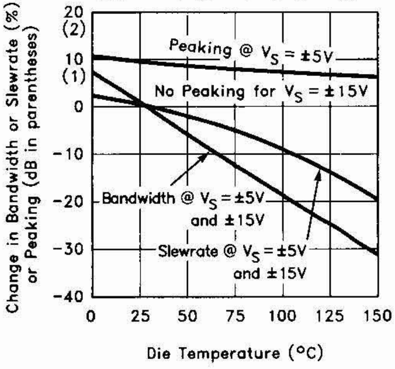
4421-15

EL4421, EL4441, and EL4443 Bandwidth, Slewrate, and Peaking vs Temperature, A_V = +1, R_L = 500Ω



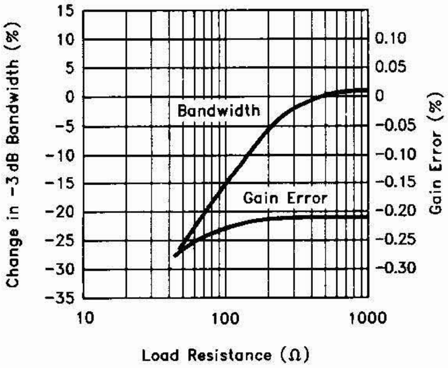
4421-16

EL4422, EL4442, and EL4444 Bandwidth, Slewrate, and Peaking vs Temperature, A_V = +2, R_L = 150Ω, R_I = R_G = 270Ω, C_F = 3 pF



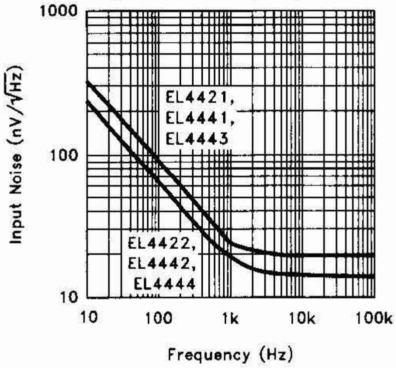
4421-17

EL4421, EL4441, and EL4443 −3 dB Bandwidth and Gain Error vs Load Resistance



4421-18

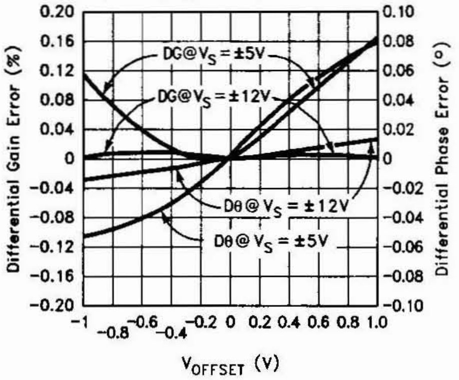
Input Noise vs Frequency



4421-19

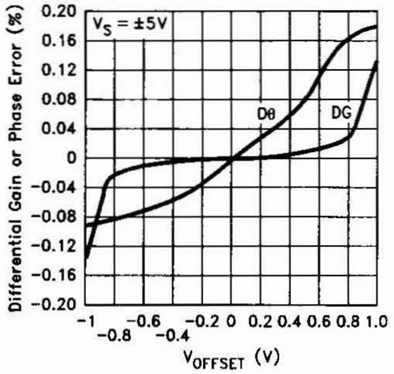
Typical Performance Curves — Contd.

EL4421, EL4441, and EL4443 Differential Gain and Phase Errors, vs Input Offset, $A_V = +1$, $R_L = 500\Omega$, F = 3.58 MHz



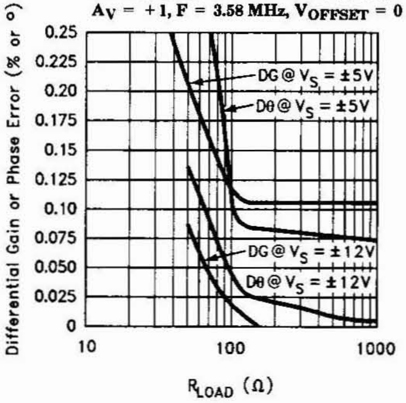
4421-20

EL4422, EL4442, and EL4444 Differential Gain and Phase Error vs Input Offset; $A_V = +2$, $R_L = 150\Omega$, F = 3.58 MHz



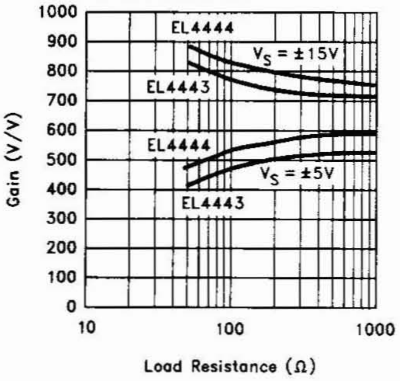
4421-21

EL4421, EL4441, and EL4443 Differential Gain and Phase Error vs Load Resistance; $A_V = +1$, F = 3.58 MHz, $V_{OFFSET} = 0 \rightarrow 0.714V$



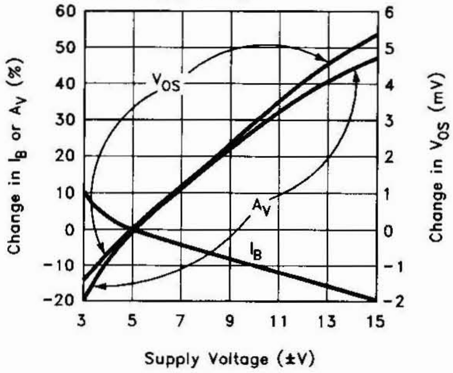
4421-22

EL4443 and EL4444 Open-Loop Gain vs Load Resistance



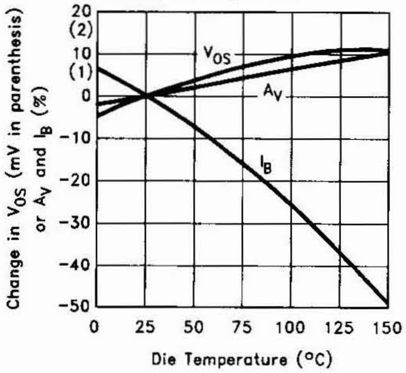
4421-23

Change in V_{OS}, A_V, and I_B with Supply Voltage



4421-24

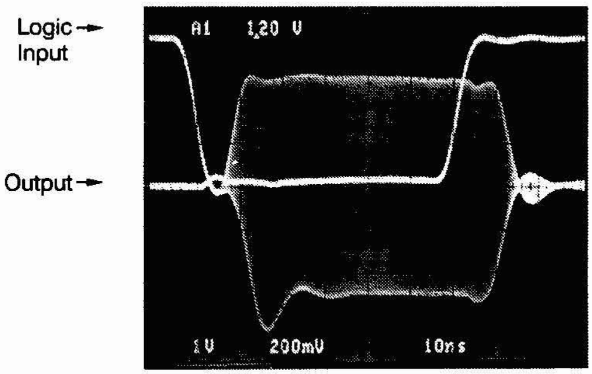
Change in V_{OS}, I_B, and A_V vs Temperature



4421-25

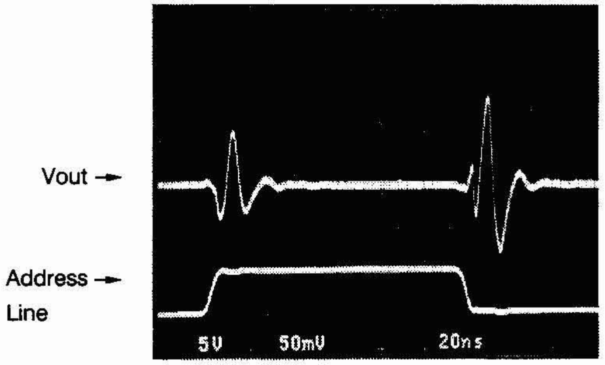
Typical Performance Curves — Contd.

Switching Waveforms
Switching from Grounded Input
to Uncorrelated Sinewave and Back



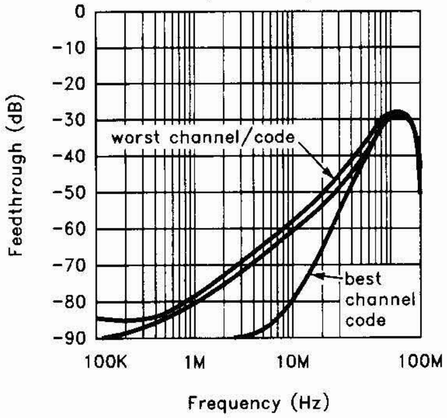
4421-26

Channel-to-Channel
Switching Glitch



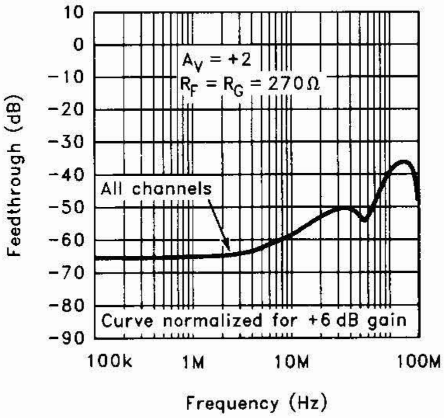
4421-27

EL4421, EL4441, and EL4443
Unselected Channel
Feedthrough vs Frequency



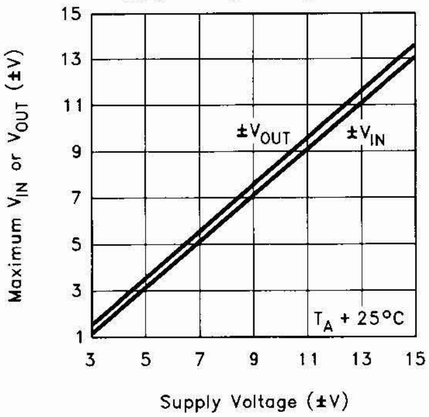
4421-28

EL4422, EL4442, and EL4444
Unselected Channel
Feedthrough vs Frequency



4421-29

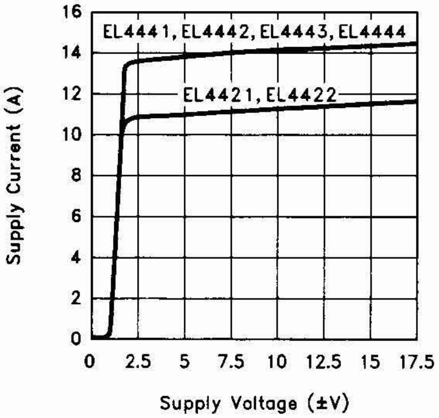
EL4443 and EL4444
Input and Output Range vs
Supply Voltage (Output Unloaded)



4421-30

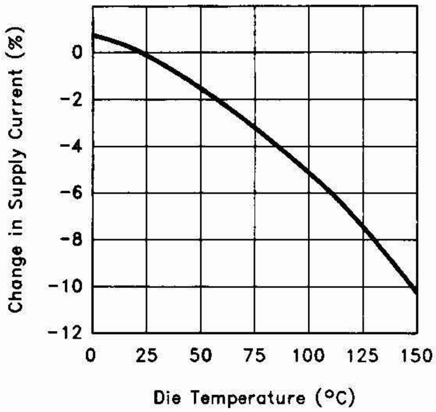
Typical Performance Curves — Contd.

Supply Current vs Supply Voltage



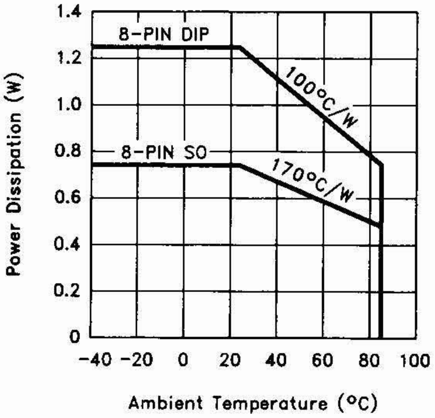
4421-31

Supply Current vs Temperature



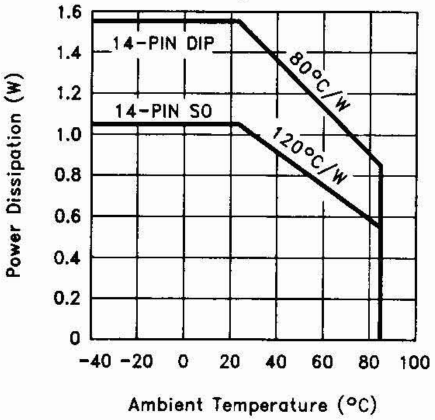
4421-32

8-Pin Package Power Dissipation vs Ambient Temperature



4421-33

14-Pin Package Power Dissipation vs Ambient Temperature



4421-34

Applications Information

General Description

The EL44XX family of video mux-amps are composed of two or four input stages whose inputs are selected and control an output stage. One of the inputs is active at a time and the circuit behaves as a traditional voltage-feedback op-amp for that input, rejecting signals present at the unselected inputs. Selection is controlled by one or two logic inputs.

The EL4421, EL4422, EL4441, and EL4442 have all −inputs wired in parallel, allowing a single feedback network to set the gain of all inputs. These devices are wired for positive gains. The EL4443 and EL4444, on the other hand, have all +inputs and −inputs brought out separately so that the input stage can be wired for independent gains and gain polarities with separate feedback networks.

The EL4421, EL4441, and EL4443 are compensated for unity-gain stability, while the EL4422, EL4442, and EL4444 are compensated for a fed-back gain of +2, ideal for driving back-terminated cables or maintaining bandwidth at higher fed-back gains.

Applications Information — Contd.

Switching Characteristics

The logic inputs work with standard TTL levels of 0.8V or less for a logic 0 and 2.0V or more for a logic 1, making them compatible for TTL and CMOS drivers. The ground pin is the logic threshold biasing reference. The simplified input circuitry is shown below:

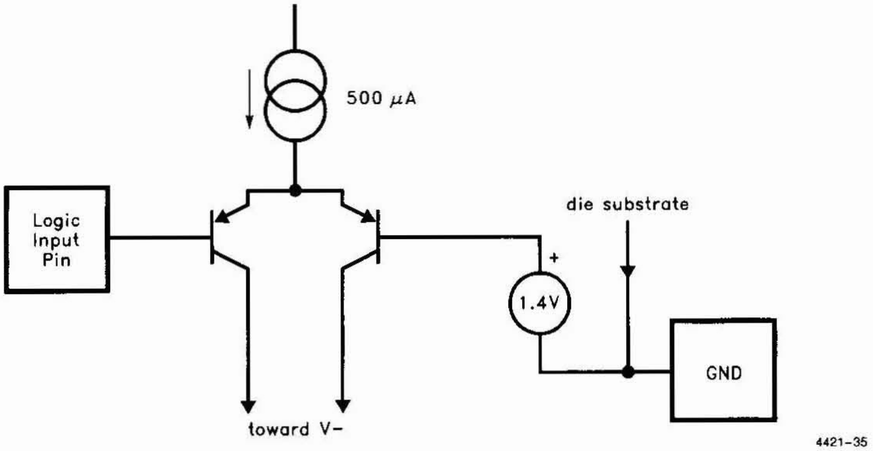

500 μA
Logic Input Pin
die substrate
+
1.4V
GND
toward V−
4421-35

Figure 1. Simplified Logic Input Circuitry

The ground pin draws a maximum DC current of 6 μA, and may be biased anywhere between (V−) + 2.5V and (V+) − 3.5V. The logic inputs may range from (V−) + 2.5V to V+, and are additionally required to be no more negative than V(Gnd pin) − 4V and no more positive than V(Gnd pin) + 6V.

For example, within these constraints, we can power the EL44XX's from + 5V and + 12V without a negative supply by using these connections:

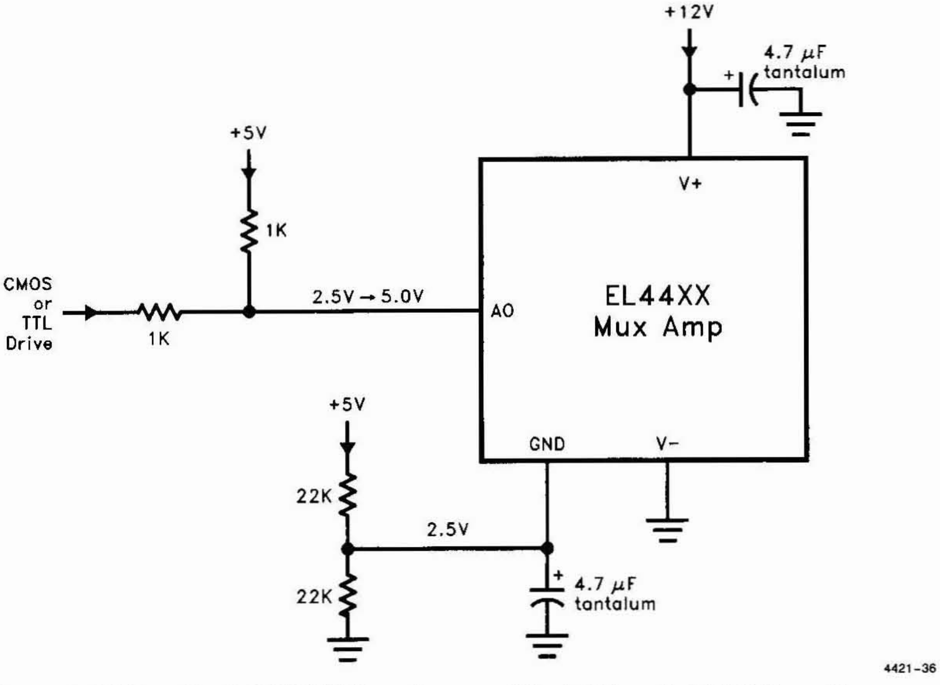

+12V
4.7 μF tantalum
+
+5V
1K
V+
CMOS or TTL Drive
1K
2.5V → 5.0V
A0
EL44XX Mux Amp
+5V
GND
V−
22K
2.5V
22K
+
4.7 μF tantalum
4421-36

Figure 2. Using the EL44XX Mux Amps with + 5V and + 12V Supplies

Applications Information — Contd.

The logic input(s) and ground pin are shifted 2.5V above system ground to correctly bias the mux-amp. Of course, all the signal inputs and output will have to be shifted 2.5V above system ground to ensure proper signal path biasing.

A final caution: the ground pin is also connected to the IC's substrate and frequency compensation components. The ground pin must be returned to system ground by a short wire or nearby bypass capacitor. In figure 2, the 22 KΩ resistors also serve to isolate the bypassed ground pin from the +5V supply noise.

Signal Amplitudes

Signal input and output voltages must be between (V−)+2.5V and (V+)−2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. In unity-gain connections, any input could have ±3V applied and the output would be at ±3V, putting us at our 6V differential limit. Higher-gain circuit applications divide the output voltage and allow for larger outputs. For instance, at a gain of +2 the maximum input is again ±3V and the output swing is ±6V. The EL4443 or EL4444 can be wired for inverting gain with even more amplitude possible.

The output and positive inputs respond to overloading amplitudes correctly; that is, they simply clamp and remain monotonic with increasing +input overdrive. A condition exists, however, where the −input of an active stage is overdriven by large outputs. This occurs mainly in unity-gain connections, and only happens for negative inputs. The overloaded input cannot control the feedback loop correctly and the output can become non-monotonic. A typical scenario has the circuit running on ±5V supplies, connected for unity gain, and the input is the maximum ±3V. Negative input extremes can cause the output to jump from −3V to around −2.3V. This will never happen if the input is restricted to ±2.5V, which is the guaranteed maximum input compliance with ±5V supplies, and is not a problem with greater supply voltages. Connecting the feedback network with a divider will prevent the overloaded output voltage from being large enough to overload the −input and monotonic

Applications Information — Contd.

behavior is assured. In any event, keeping signals within guaranteed compliance limits will assure freedom from overload problems.

The input and output ranges are substantially constant with temperature.

Power Supplies

The mux-amps work well on any supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the Gnd pin are observed (see the Switching Characteristics section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used as described in the Switching Characteristics section. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the mux-amps increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2V_S \times I_s,\text{max} + (V_S - V_O) \times V_O / R_{PAR}$$

Where I_s, max is the maximum supply current

V_S is the ± supply voltage (assumed equal)

V_O if the output voltage

R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4422 draws a maximum of 14 mA and we might require a 2V peak output into 150Ω and a 270Ω +270Ω feedback divider. The R_{PAR} is 117Ω. The dissipation with ±5V supplies is 191 mW. The maximum Supply voltage that the device can run on for a given P_D and the other parameter is

$$V_S,\text{max} = (P_D + V_O^2/R_{PAR})/2Is + V_O/R_{PAR})$$

The maximum dissipation a package support is

$$P_D,\text{max} = (T_D,\text{max} - T_A,\text{max})/R_{TH}$$

Where T_D, max is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performance

T_A, max is the ambient temperature, 70° for commercial and 85°C for industrial range

R_{TH} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The most difficult case is the SO-8 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 85°, the 65° temperature rise and package thermal resistance of 170°/W gives a maximum dissipation of 382 mW. This allows a maximum supply voltage of ±9.2V for the EL4422 operated in our example. If the EL4421 were driving a light load ($R_{PAR} \rightarrow \infty$), it could operate on ±15V supplies at a 70° maximum ambient.

The EL4441 through EL4444 can operate on ±12V supplies in the SO package, and all parts can be powered by ±15V supplies in DIP packages.

Output Loading

The output stage of the mux-amp is very powerful, and can source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain or gain accuracy degrades only 10% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion only a bit, becoming noticeably worse for loads < 100Ω.

Applications Information — Contd.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.

Input Connections

The input transistors can be driven from resistive and capacitive sources but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about 6″ of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz.

Often simply placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the mux-amp input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Feedback Connections

A feedback divider is used to increase circuit gain, and some precautions should be observed. The first is that parasitic capacitance at the −input will add phase lag to the feedback path and increase frequency response peaking or even cause oscillation. One solution is to choose feedback resistors whose parallel value is low. The pole frequency of the feedback network should be maintained above at least 200 MHz. For a 3 pF parasitic, this requires that the feedback divider have less than 265Ω impedance, equivalent to two 510Ω resistors when a gain of +2 is desired. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should match the parasitic capacitance at the −input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors will dominate parasitic effects and allow a higher divider resistance.

The other major concern about the divider concerns unselected-channel crosstalk. The differential input impedance of each input stage is around 200 KΩ. The unselected input's signal sources thus drive current through that input impedance into the feedback divider, inducing an unwanted output. The gain from unselected input to output, the crosstalk attenuation, if R_F/R_{IN}. In unity-gain connection the feedback resistor is 0Ω and very little crosstalk is induced. For a gain of +2, the crosstalk is about −60 dB.

Feedthrough Attenuation

The channels have different crosstalk levels with different inputs. Here is the typical attenuation for all combinations of inputs for the mux-amps at 3.58 MHz:

Feedthrough of EL4441 and EL4443 at 3.58 MHz

		In1	In2	In3	In4
Select Inputs, A1A0	00	Selected	−77 dB	−90 dB	−92 dB
	01	−80 dB	Selected	−77 dB	−90 dB
	10	−101 dB	−76 dB	Selected	−66 dB
	11	−96 dB	−84 dB	−66 dB	Selected

Feedthrough of EL4421 at 3.58 MHz

		In1	In2
Channel Select Input, A0	0	Selected	−88 dB
	1	−93 dB	Selected

Switching Glitches

The output of the mux-amps produces a small "glitch" voltage in response to a logic input change. A peak amplitude of only about 90 mV occurs, and the transient settles out in 20 ns. The glitch does not change amplitude with different gain settings.

With the four-input multiplexers, when two logic inputs are simultaneously changed, the glitch amplitude doubles. The increase can be a avoided by keeping transitions at least 6 ns apart. This can be accomplished by inserting one gate delay in one of the two logic inputs when they are truly synchronous.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4450C

Wideband Four-Quadrant Multiplier

Features

- Complete four-quandrant multiplier with output amp—requires no extra components
- Good linearity of 0.3%
- 90 MHz bandwidth for both X and Y inputs
- Operates on ±5V to ±15V supplies
- All inputs are differential
- 400V/µs slew rate

Applications

- Modulation/Demodulation
- RMS computation
- Real-time power computation
- Nonlinearity correction/generation

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4450CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL4450CM	−40°C to +85°C	14-Lead SO	MDP0027

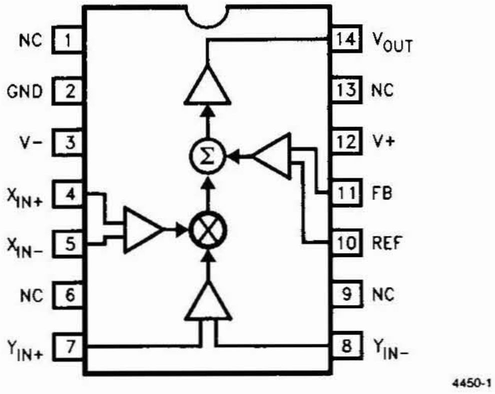
General Description

The EL4450C is a complete four-quadrant multiplier circuit. It offers wide bandwidth and good linearity while including a powerful output voltage amplifier, drawing modest supply current.

The EL4450C operates on ±5V supplies and has an analog input range of ±2V, making it ideal for video signal processing. AC characteristics do not vary over the ±5V to ±15V supply range.

The multiplier has an operational temperature range of −40°C to +85°C and are packaged in plastic 14-pin P-DIP and SO.

Connection Diagram



January 1996 Rev B

Absolute Maximum Ratings ($T_A = 25°C$)

V+	Positive Supply Voltage	16.5V
V_S	V+ to V− Supply Voltage	33V
V_{IN}	Voltage at any Input or Feedback	V+ to V−
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V
I_{IN}	Current into any Input or Feedback Pin	4 mA
I_{OUT}	Output Current	30 mA
P_D	Maximum Power Dissipation	See Curves
T_A	Operating Temperature Range	−40°C to +85°C
T_S	Storage Temperature Range	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

Open-Loop DC Electrical Characteristics Power Supplies at ±5V, $T_A = 25°C$, $V_{FB} = V_{OUT}$.

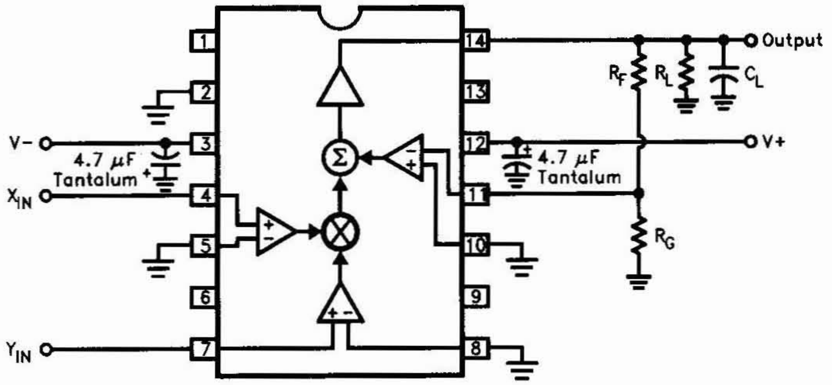
Parameter	Description	Min	Typ	Max	Test Level	Units
V_{DIFF}	Differential Input Voltage—Clipping	1.8	2.0		I	V
	0.2% nonlinearity		1.0		V	V
V_{CM}	Common-Mode Range of $V_{DIFF} = 0$, $V_S = \pm 5V$	±2.5	±2.8		I	V
	$V_S = \pm 15V$	±12.5	±12.8		I	V
V_{OS}	Input Offset Voltage		8	35	I	mV
I_B	Input Bias Current		9	20	I	μA
I_{OS}	Onput Offset Current between $X_{IN}+$ and $X_{IN}-$, $Y_{IN}+$ and $Y_{IN}-$, REF and FB		0.5	4	I	μA
Gain	Gain Factor of $V_{OUT} = \text{Gain} \times X_{IN}+ \times Y_{IN}$	0.45	0.5	0.55	I	V/V²
NLx	Nonlinearity of X Input; X_{IN} between −1V and +1V		0.3	0.7	I	%
NLy	Nonlinearity of Y Input; Y_{IN} between −1V and +1V		0.2	0.35	I	%
R_{IN}	Input resistance, X_{IN+} to X_{IN-}, Y_{IN+} to Y_{IN-},		230		V	kΩ
	REF to FB		90			
CMRR	Common-Mode Rejection Ratio, X_{IN} and Y_{IN}	70	90		I	dB
PSRR	Power-Supply Rejection Ratio, FB	60	72		I	dB
V_O	Output Voltage Swing $V_S = \pm 5V$	±2.5	±2.8		I	V
	($V_{IN} = 0$, V_{REF} Varied) $V_S = \pm 15V$	±12.5	±12.8			
I_{SC}	Output Short-Circuit Current	40	85		I	mA
I_S	Supply Current, $V_S = \pm 15V$		15.4	18	I	mA

Closed-Loop AC Electrical Characteristics

Power Supplies at ±12V, T_A = 25°C, R_L = 500Ω, C_L = 15pF

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, −3 dB	−3 dB Small-Signal Bandwidth, X or Y		90		V	MHz
BW, ±0.1 dB	0.1 dB Flatness Bandwidth		10		V	MHz
Peaking	Frequency Response Peaking		1.0		V	dB
SR	Slew Rate, V_{OUT} between −2V and +2V	300	400		I	V/μs
V_N	Input-Referred Noise Voltage Density		100		V	nV/$\sqrt{Hz}$

Test Circuit

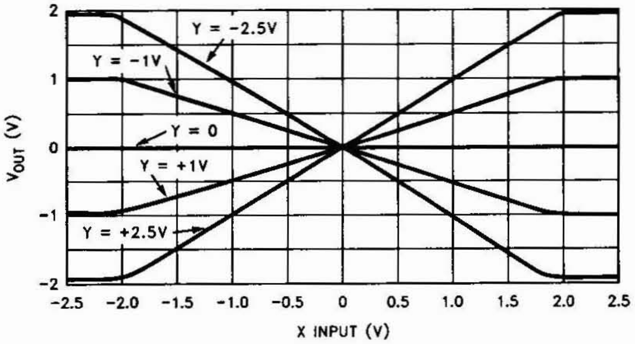

1
2
3
4
5
6
7
8
9
10
11
12
13
14
V−
X_{IN}
Y_{IN}
4.7 μF Tantalum
4.7 μF Tantalum
Output
V+
R_F
R_L
C_L
R_G
Σ

4450-2

Note: For typical performance curves, R_F = 0, R_G = ∞, V_S = ±5V, R_L = 500Ω, and C_L = 15 pF unless otherwise noted.

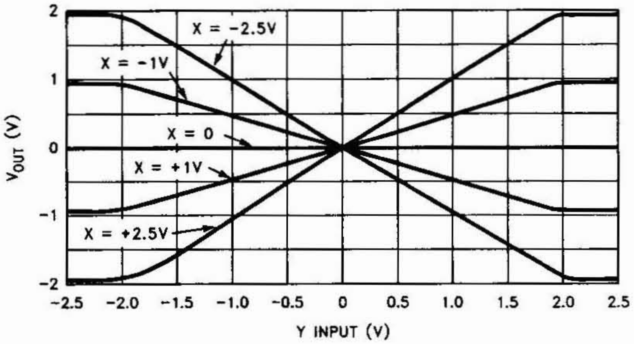
Typical Performance Curves

Transfer Function of X Input for Various Y Inputs



4450-3

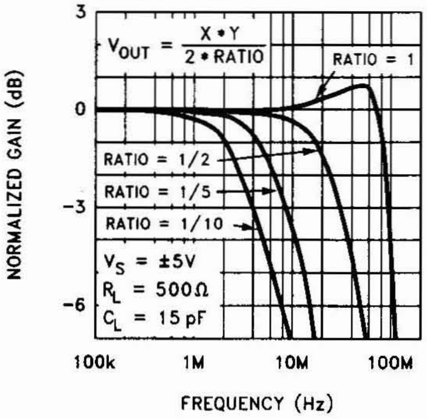
Transfer Function of Y Input for Various X Inputs



4450-4

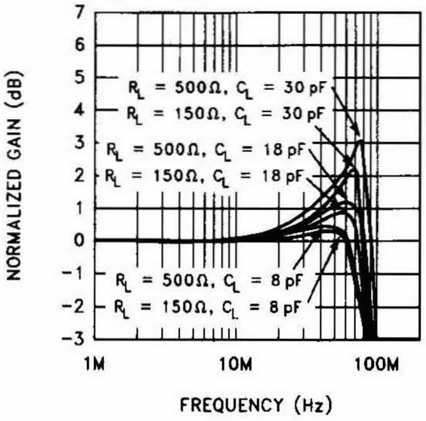
Typical Performance Curves — Contd.

Frequency Response for Various Feedback Divider Ratios



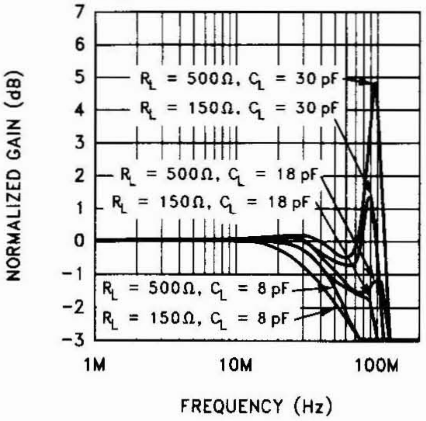
4450-5

Frequency Response for Various R_L, C_L V_S = ±5V



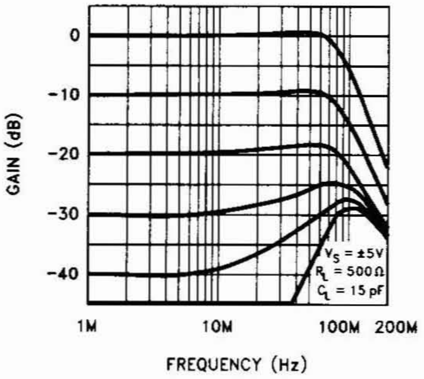
4450-6

Frequency Response for Various R_L, C_L V_S = ±15V



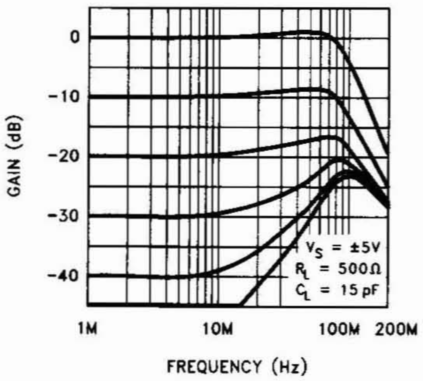
4450-7

X Input Frequency Response for Various Y DC Inputs



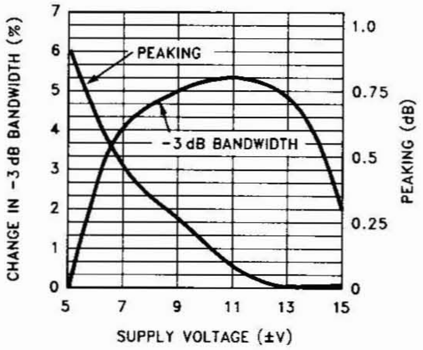
4450-8

Y Input Frequency Response for Various X DC Inputs



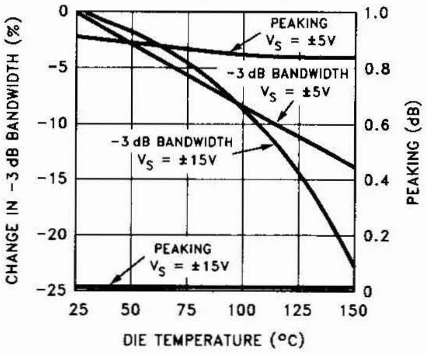
4450-9

−3 dB Bandwidth and Peaking vs Supply Voltage



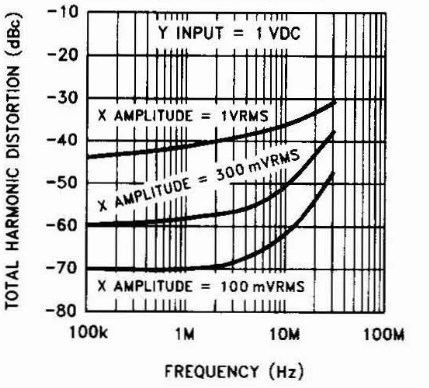
4450-10

Change in Bandwidth and Peaking vs Temperature



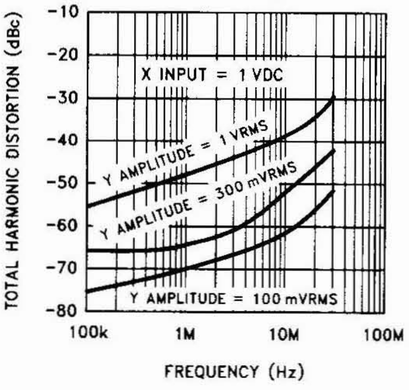
4450-11

Total Harmonic Distortion of X Input vs Frequency



4450-12

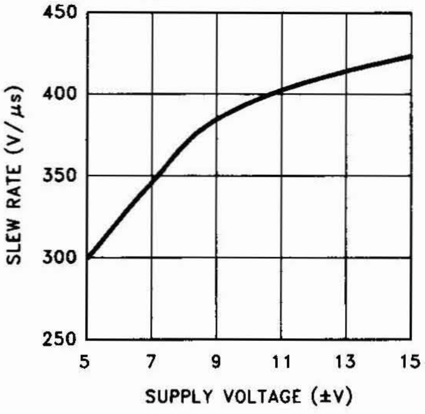
Total Harmonic Distortion of Y Input vs Frequency



4450-13

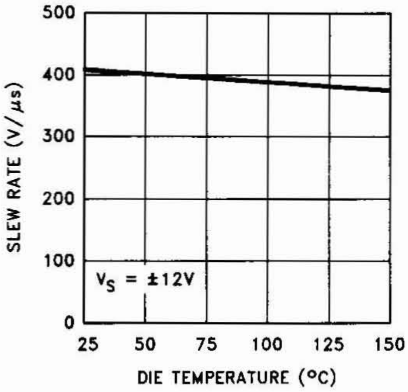
Typical Performance Curves — Contd.

Slew Rate vs Supply Voltage



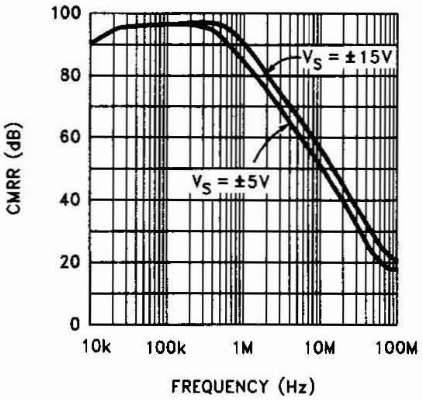
4450-14

Slew Rate vs Die Temperature



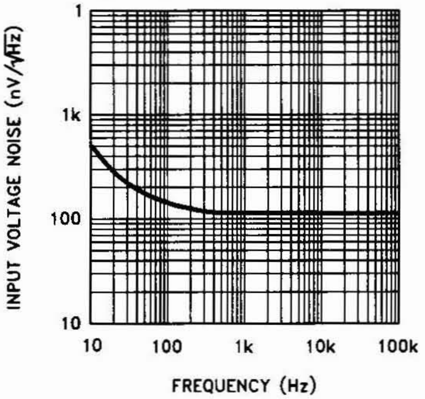
4450-15

CMRR vs Frequency



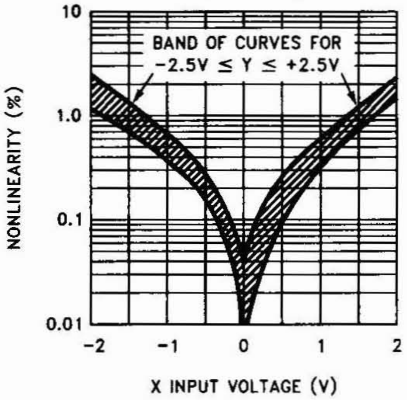
4450-16

Input Voltage Noise vs Frequency



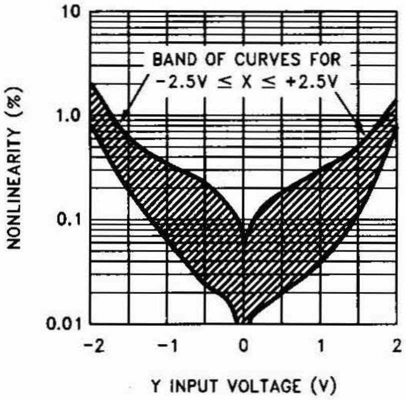
4450-17

Nonlinearity of X Input



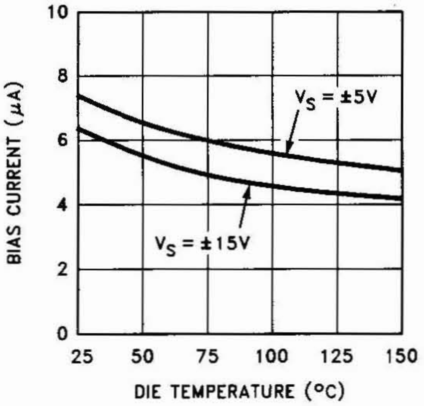
4450-18

Nonlinearity of Y Input



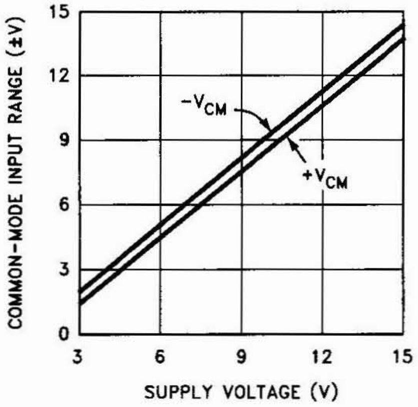
4450-19

Bias Current vs Die Temperature



4450-20

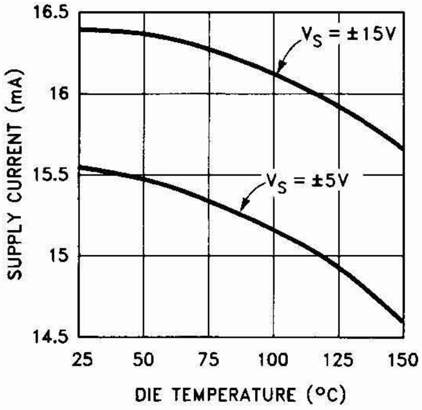
Common-Mode Input Range vs Supply Voltage



4450-21

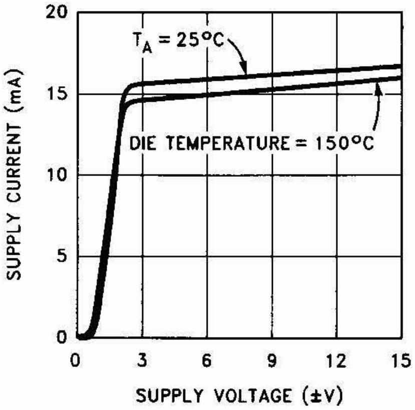
Typical Performance Curves — Contd.

Supply Current vs Die Temperature



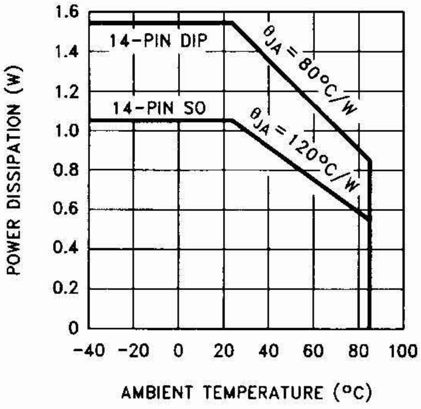
4450-22

Supply Current vs Supply Voltage



4450-23

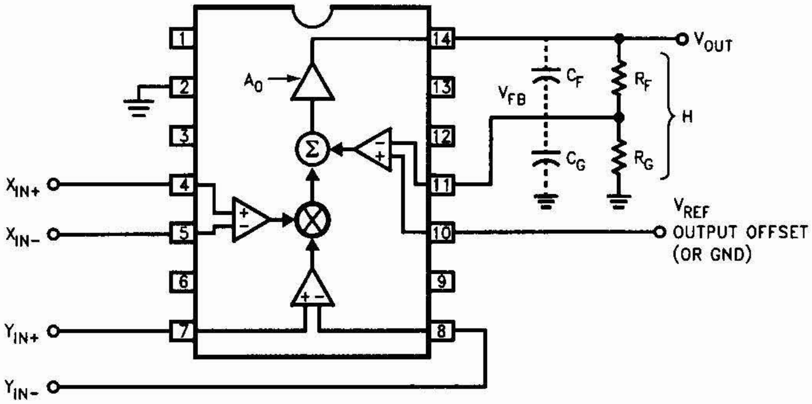
14-Pin Package Power Dissipation vs Ambient Temperature



4450-24

Applications Information

The EL4450 is a complete four-quadrant multiplier with 90 MHz bandwidth. It has three sets of inputs; a differential multiplying X-input, a differential multiplying Y-input, and another differential input which is used to complete a feedback loop with the output. Here is a typical connection:



The gain of the feedback divider is H, and $H = R_G/(R_G + R_F)$. The transfer function of the part is

$$V_{OUT} = A_O \times (½ \times ((V_{INX+} - V_{INX-})) \times ((V_{INY+} - V_{INY-})) + (V_{REF} - V_{FB})).$$

V_{FB} is connected to V_{OUT} through a feedback network, so $V_{FB} = H^*V_{OUT}$. A_O is the open-loop gain of the amplifier, and is about 600. The large value of A_O drives

$$(½ \times ((V_{INX+} - V_{INX-})) \times ((V_{INY+} - V_{INY-})) + (V_{REF} - V_{FB})) \rightarrow 0.$$

Rearranging and substituting for V_{REF}

$$V_{OUT} = (½ \times ((V_{INX+} - V_{INX-})) \times ((V_{INY+} - V_{INY-})) + V_{REF})/H, \text{ or}$$

$$V_{OUT} = (XY/2 + V_{REF})/H$$

Thus the output is equal to one-half the product of X and Y inputs and offset by V_{REF}, all gained up by the feedback divider ratio. The EL4450 is stable for a direct connection between V_{OUT} and FB, and the feedback divider may be used for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 150 MHz; typical strays of 3 pF thus require a feedback impedance of 360Ω or less, Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors for a maximum gain of 1 will dominate parasitic effects and allow a higher divider resistance.

The REF pin can be used as the output's ground reference, or for DC offsetting of the output, or it can be used to sum in another signal.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about 6″ of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is not possible, one can insert series resistors of around to 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between (V−) + 2.5V and (V+) −2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ± 6V to prevent damage. The differential signal range is ± 2V in the EL4450C. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 μA maximum DC current, and may be biased anywhere between (V−) +2.5V and (V+) −3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4450C works well on supplies from ± 3V to ± 15V. The supplies may be of different voltages as long as the requirements of the GND pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as low as 0.01 μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4450C increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2*I_{S,max}*V_S + (V_S - V_O)*V_O/R_{PAR}$$

where

$I_{S,max}$ is the maximum supply current
V_S is the ± supply voltage (assumed equal)
V_O is the output voltage
R_{PAR} is the parallel of all resistors loading the output

For instance, the EL4450C draws a maximum of 18 mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with ±5V supplies is 180 mW. The maximum supply voltage that the device can run on for a given P_D and the other parameters is

$$V_{S,max} = (P_D + V_O^2/R_{PAR})/(2I_S + V_O/R_{PAR})$$

The maximum dissipation a package can offer is

$$P_{D,max} = (T_{J,max} - T_{A,max})/\theta_{JA}$$

Where $T_{J,max}$ is the maximum junction temperature, 150°C for reliability, less to retain optimum electrical performance

$T_{A,max}$ is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum junction temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded significantly.

Output Loading

The output stage is very powerful. It typically can source 85 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain accuracy degrades only 0.2% from no-load-to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads < 100Ω.

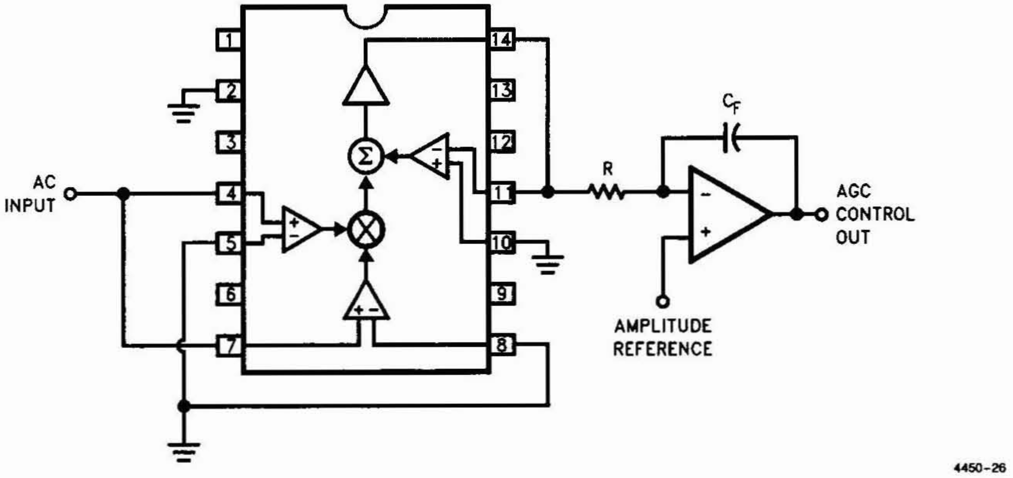
Capacitive loads will cause peaking in the frequency response. If a capacitive load must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.

Mixer Applications

Because of its lower distortion levels, the Y input is the better choice for a mixer's signal port. The X input would receive oscillator amplitudes of about 1V RMS maximum. Carrier suppression is initially limited by the offset voltage of the Y input, 20 mV maximum, and is about 37 dB worst-case. Better suppression can be obtained by nulling the offset of the X input. Similarly, nulling the offset of the Y input will improve signal-port suppression. Driving an input differentially will also maximize feedthrough suppression at frequencies beyond 10 MHz.

AC Level Detectors

Square-law converters are commonly used to convert AC signals to DC voltages corresponding to the original amplitude in subsystems like automatic gain controls (AGC's) and amplitude-stabilized oscillators. Due to the controlled AC amplitudes, the inputs of the multiplier will see a relatively constant signal level. Best performance will be obtained for inputs between 200 mVRMS and 1 VRMS. The traditional use of the EL4450C as an AGC detector and control loop would be:



Traditional AGC Detector/DC Feedback Circuit

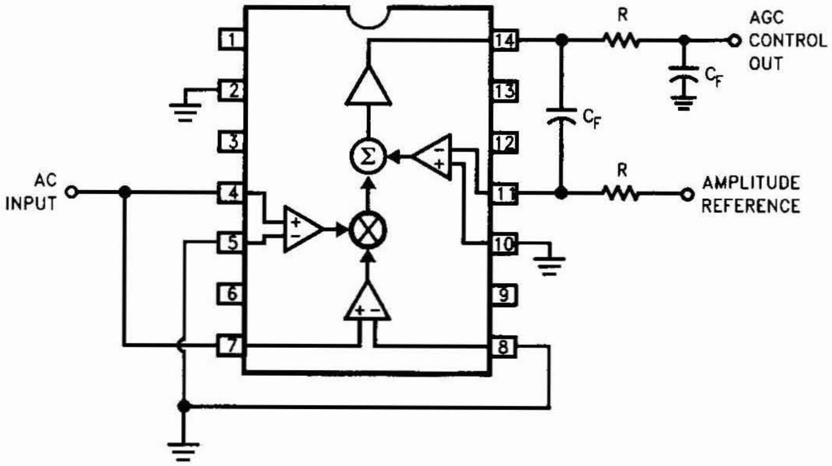
AC Level Detectors — Contd.

The EL4450C simply provides an output equal to the square of the input signal and an integrator filters out the AC component, while comparing the DC component to an amplitude reference. The integrator output is the DC control voltage to the variable-gain sections of the AGC (not shown). If a negative polarity of reference is required, one of the multiplier input terminal pairs is reversed, inverting the multiplier output. Input bias current will cause input voltage offsets due to source impedances; putting a compensating resistor in series with the grounded inputs of the EL4450C will reduce this offset greatly.

This control system will attempt to force

$V_{IN,RMS}{}^2/4 = V_{REF}$.

The extra op-amp can be eliminated by using this circuit:



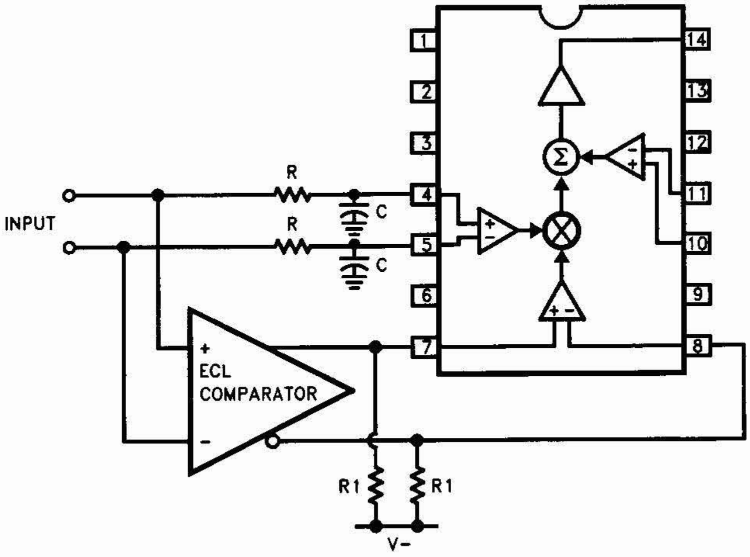
Simplified AGC Detector/DC Feedback Circuit

AC Level Detectors — Contd.

Here the internal op-amp of the EL4450C replaces the external amplifier. The feedback capacitor C_F does not provide a perfect integration action; a zero occurs at a frequency of $1/2\pi RC_F$. This is canceled by including another RC_F pair at the AGC control output. If the reference voltage must be negative, the resistor at pin 11 is connected to ground rather than the reference and pin 10 connected to the reference.

The amplitude reference will have to support some AC currents flowing through R. If this is a problem, several changes can be made to eliminate it. The reference is connected to pin 10 and the resistor R connected to pin 11 reconnected to ground, and one of the multiplier input connections are reversed.

Square-law detectors have a restricted input range, about 10:1, because the output rapidly disappears into the DC errors as signal amplitudes reduce. This circuit gives a multiplier output that is the absolute value of the input, thus increasing range to 100:1:



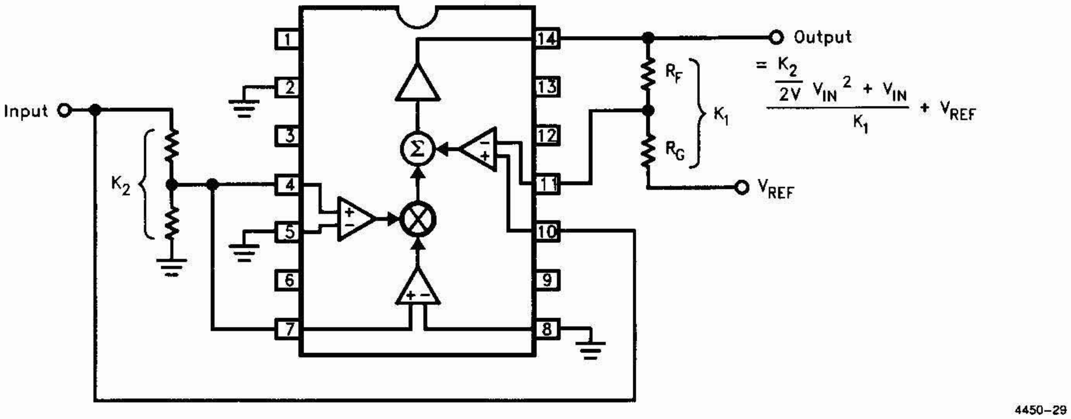
Absolute-Value Input Circuitry

AC Level Detectors — Contd.

An ECL comparator produces an output corresponding to the sign of the input, which when multiplied by the input produces an effective absolute-value function. The RC product connected to the X inputs simply emulates the time delay of the comparator to maintain circuit accuracy at higher frequencies.

Nonlinear Function Generation

The REF pin of the EL4450C can be used to sum in various quantities of polynominal function generators. For instance, this sum of REF allows a linear signal path which can have various amounts of squared signal added:

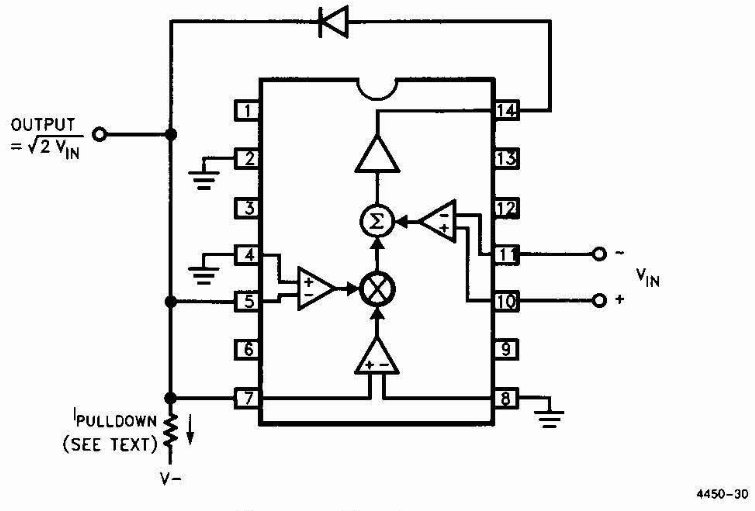

Input
K_2
Output
$= \frac{\frac{K_2}{2V} V_{IN}^2 + V_{IN}}{K_1} + V_{REF}$
R_F
R_G
K_1
V_{REF}
1
2
3
4
5
6
7
8
9
10
11
12
13
14
Σ
4450-29

Polynomial Function Generator

The polarity of the squared signal can be reversed by swapping one of the X or Y input pairs.

The REF and FB pins also simplify feedback schemes that allow square-rooting:

The diode and $I_{pulldown}$ assure that the output will always produce the positive square-root of the input signal. $I_{pulldown}$ should be large enough to assure that the diode be forward-biased for any load current. In this configuration, the bandwidth of the circuit will reduce for smaller input signals.

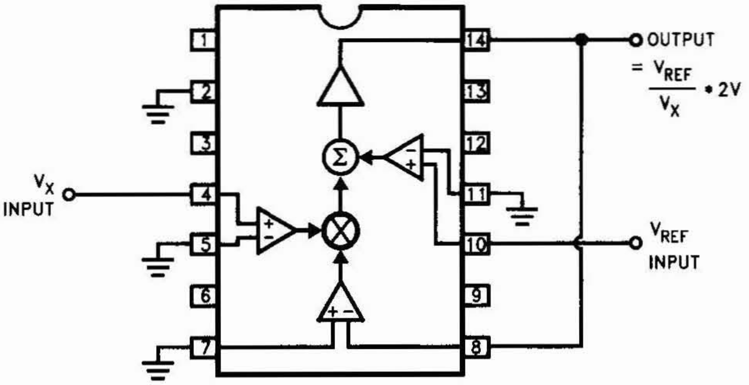

OUTPUT
$= \sqrt{2}\, V_{IN}$
$I_{PULLDOWN}$
(SEE TEXT)
V-
−
+
V_{IN}
1
2
3
4
5
6
7
8
9
10
11
12
13
14
Σ
4450-30

Square-Rooter

Nonlinear Function Generation — Contd.

The REF and FB terminals can also be used to implement division:

The output frequency response reduces for smaller values of V_X, but is not affected by V_{REF}.


1
2
3
4
5
6
7
8
9
10
11
12
13
14
V_X INPUT
OUTPUT
$= \frac{V_{REF}}{V_X} \cdot 2V$
V_{REF} INPUT
4450-31

Divider Connection

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4453C
Video Fader

Features

- Complete two-input fader with output amplifier—uses no extra components
- 80 MHz bandwidth
- Fast fade control speed
- Operates on ±5V to ±15V supplies
- >60 dB attenuation @ 5 MHz

Applications

- Mixing two inputs
- Picture-in-picture
- Text overlay onto video
- General gain control

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL4453CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL4453CS	−40°C to +85°C	14-Lead SOIC	MDP0027

General Description

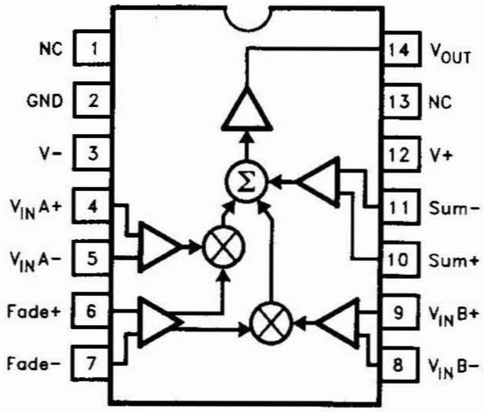
The EL4453C is a complete fader subsystem. It variably blends two inputs together for such applications as video picture-in-picture effects.

The EL4453C operates on ±5V to ±15V supplies and has an analog differential input range of ±2V. AC characteristics do not change appreciably over the supply range.

The circuit has an operational temperature of −40°C to +85°C and is packaged in 14-pin P-DIP and SO-14.

The EL4453C is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is free from latch up.

Connection Diagram



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January 1995 Rev A

Absolute Maximum Ratings $T_A = 25°C$

$V+$	Positive Supply Voltage	16.5V	I_{IN}	Current into any Input, or Feedback Pin	4 mA
V_S	$V+$ to $V-$ Supply Voltage	33V	I_{OUT}	Output Current	30 mA
V_{IN}	Voltage at any Input or Feedback	$V+$ to $V-$	P_D	Maximum Power Dissipation	See Curves
ΔV_{IN}	Difference between Pairs of Inputs or Feedback	6V	T_A	Operating Temperature Range	−40°C to +85°C
			T_S	Storage Temperature Range	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	**Test Procedure**
I	**100% production tested and QA sample tested per QA test plan QCX0002.**
II	**100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.**
III	**QA sample tested per QA test plan QCX0002.**
IV	**Parameter is guaranteed (but not tested) by Design and Characterization Data.**
V	**Parameter is typical value at $T_A = 25°C$ for information purposes only.**

Open-Loop DC Electrical Characteristics

Power Supplies at ±5V, Sum+ = Sum− = 0, $T_A = 25°C$

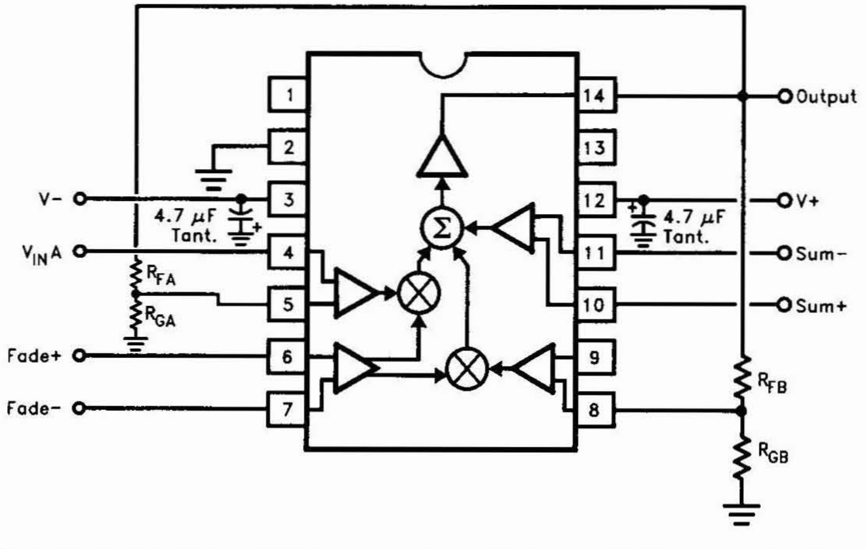
Parameter	Description		Min	Typ	Max	Test Level	Units
V_{DIFF}	$V_{IN}A$, $V_{IN}B$, or Sum Differential Input Voltage—	Clipping 0.2% Nonlinearity	1.8	2.0 0.7		I V	V V
V_{CM}	Common-Mode Range (All Inputs; $V_{DIFF} = 0$)	$V_S = \pm 5V$ $V_S = \pm 15V$	±2.5 ±12.5	±2.8 ±12.8		I I	V V
V_{OS}	A or B Input Offset Voltage				25	I	mV
V_{FADE}, 100%	Extrapolated Voltage for 100% Gain for $V_{IN}A$		0.9	1.05	1.2	I	V
V_{FADE}, 0%	Extrapolated Voltage for 0% Gain for $V_{IN}A$		−1.2	−1.15	−0.9	I	V
I_B	Input Bias Current (All Inputs) with all $V_{IN} = 0$			9	20	I	μA
I_{OS}	Input Offset Current between $V_{IN}A+$ and $V_{IN}A-$, $V_{IN}B+$ and $V_{IN}B-$, Fade+ and Fade−, and Sum+ and Sum−			0.2	4	I	μA
F_T	$V_{IN}A$ Signal Feedthrough, $V_{FADE} = -1.5V$			−100	−60	I	dB
NL	A or B Input Nonlinearity, V_{IN} between +1V and −1V,	$V_{IN}A$ or $V_{IN}B$ Sum Input		0.2 0.5	0.5	I V	% %
R_{IN}, Signal	Input Resistance, A, B, or Sum Input			230		V	kΩ
R_{IN}, Fade	Input Resistance, Fade Input			120		V	kΩ
CMRR	Common-Mode Rejection Ratio, $V_{IN}A$ or $V_{IN}B$		70	80		I	dB
PSRR	Power Supply Rejection Ratio		50	70		I	dB
E_G	Gain Error, $V_{FADE} = 1.5V$,	$V_{IN}A$ or $V_{IN}B$ Sum Input	−2 −4		+2 +4	I I	% %
V_O	Output Voltage Swing ($V_{IN} = 0$, V_{REF} Varied)	$V_S = \pm 5V$ $V_S = \pm 15V$	±2.5 ±12.5	±2.8 ±12.8		I I	V V
I_{SC}	Output Short-Circuit Current		40	85		I	mA
I_S	Supply Current, $V_S = \pm 15V$			17	21	I	mA

Closed-Loop AC Electrical Characteristics

Power supplies at ±12V, $T_A = 25°C$, $R_L = 500\Omega$, $C_L = 15$ pF, $V_{FADE} = 1.5V$, Sum+ = Sum− = 0

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, −3 dB	−3 dB Small-Signal Bandwidth, $V_{IN}A$ or $V_{IN}B$		80		V	MHz
BW, ±0.1 dB	0.1 dB Flatness Bandwidth, $V_{IN}A$ or $V_{IN}B$		9		V	MHz
Peaking	Frequency Response Peaking		1.0		V	dB
BW, Fade	−3 dB Small-Signal Bandwidth, Fade Input		80		V	MHz
SR	Slew Rate, V_{OUT} between −2V and +2V	TBD	380		I	V/µs
V_N	Input-Referred Noise Voltage Density		160		V	nV/Hz
F_T	Feedthrough of Faded-Out Channel, F = 3.58 MHz		−63		V	dB
dG	Differential Gain Error, V_{OFFSET} from 0 to ±0.714V, Fade at 100%					
	$V_{IN}A$ or $V_{IN}B$		0.05		V	%
	Sum Input		0.35		V	%
dθ	Differential Phase Error, V_{OFFSET} from 0 to ±0.71V, Fade at 100%					
	$V_{IN}A$ or $V_{IN}B$		0.05		V	(°)
	Sum Input		0.1		V	(°)

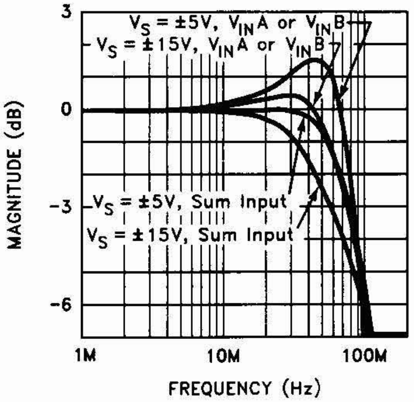
Test Circuit


1
2
3
4
5
6
7
8
9
10
11
12
13
14
Output
V−
$V_{IN}A$
4.7 µF Tant.
R_{FA}
R_{GA}
Fade+
Fade−
V+
4.7 µF Tant.
Sum−
Sum+
R_{FB}
R_{GB}
Σ
4453-2

Note: For typical performance curves Sum+ = Sum− = 0, $R_F = 0\Omega$, $R_G = \infty$, $V_{FADE} = +1.5V$, and $C_L = 15$ pF, unless otherwise noted.

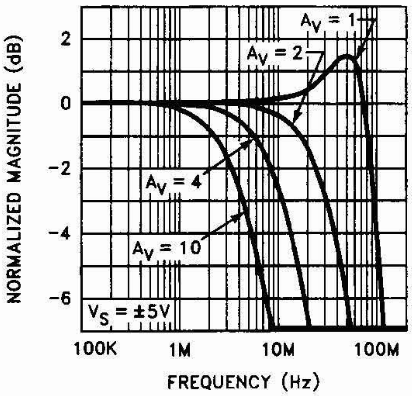
Typical Performance Curves

Frequency Response



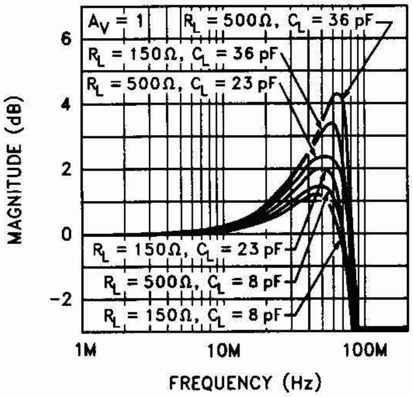
4453-3

Frequency Response vs Gain



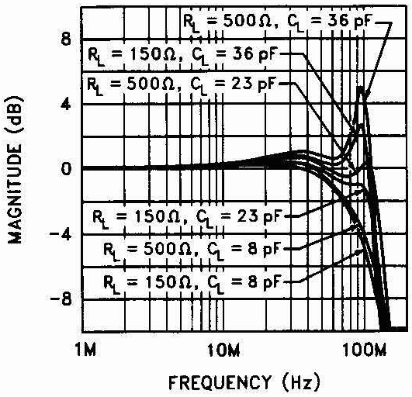
4453-4

Frequency Response for Various Loads, V_S = ±5V



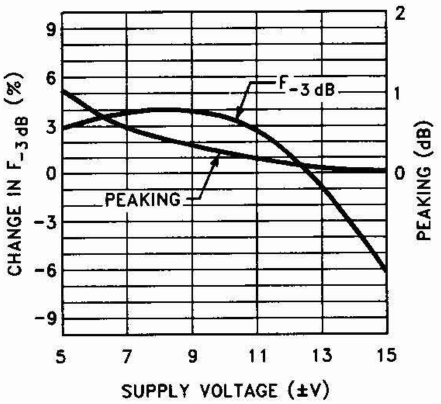
4453-6

Frequency Response for Various Loads, V_S = ±15V



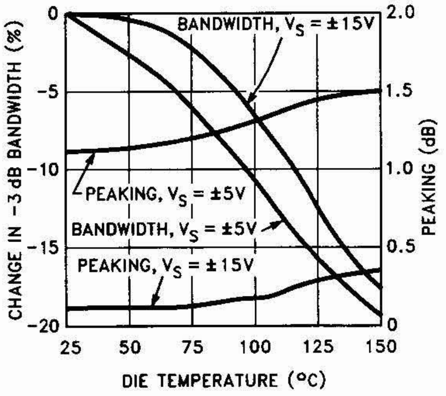
4453-7

−3 dB Bandwidth and Peaking vs Supply Voltage



4453-9

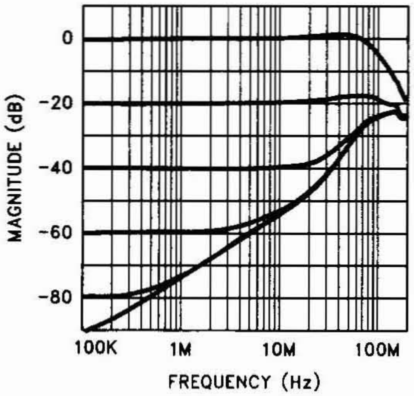
−3 dB Bandwidth and Peaking vs Die Temperature



4453-10

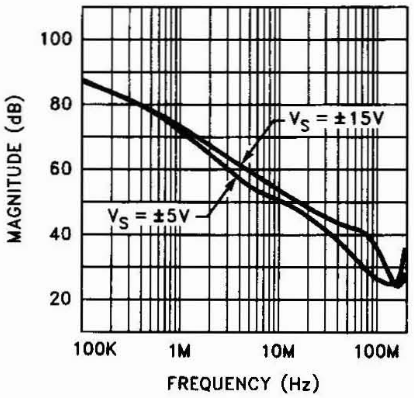
Typical Performance Curves — Contd.

Frequency Response for Different Gains, $V_S = \pm 5V$



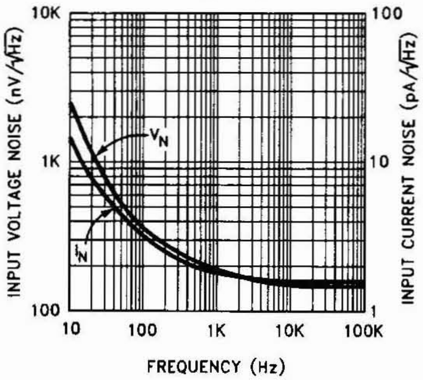
4453-5

Input Common-Mode Rejection Ratio vs Frequency



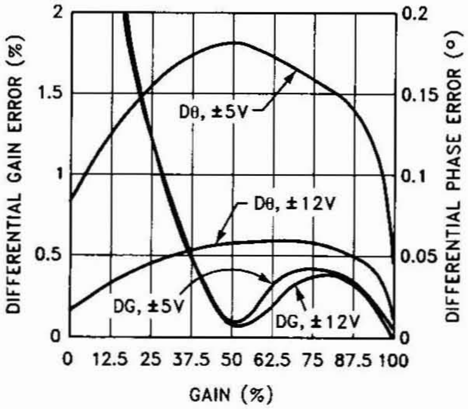
4453-8

Input Voltage and Current Noise vs Frequency



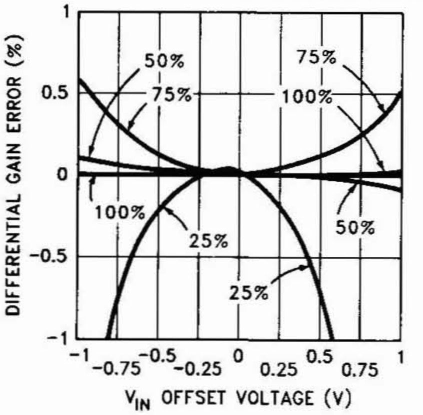
4453-11

V_{IN} Differential Gain and Phase Error vs Gain



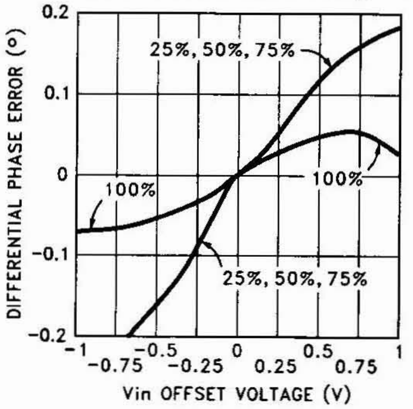
4453-14

V_{IN} Differential Gain Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%



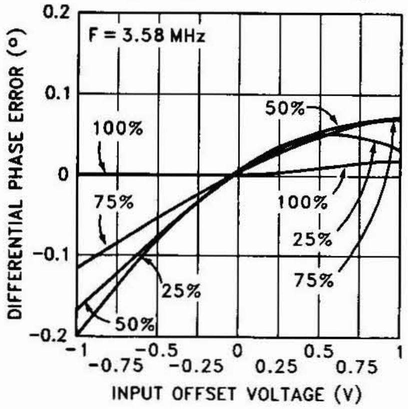
4453-15

V_{IN} Differential Phase Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%. $V_S = \pm 5V$



4453-16

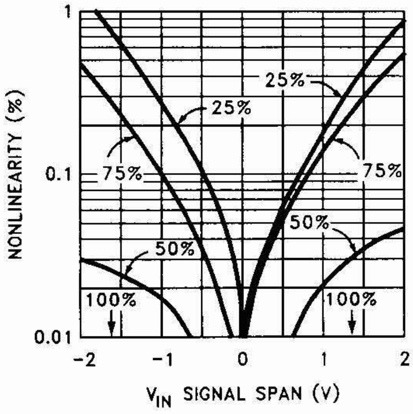
V_{IN} Differential Phase Error vs Input Offset Voltage for Gain = 100%, 75%, 50% and 25%. $V_S = \pm 12V$



4453-17

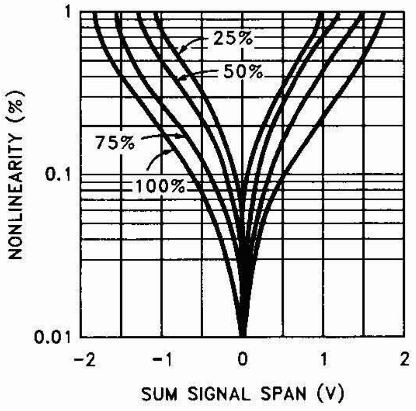
Typical Performance Curves — Contd.

Nonlinearity vs V_{IN} Signal Span



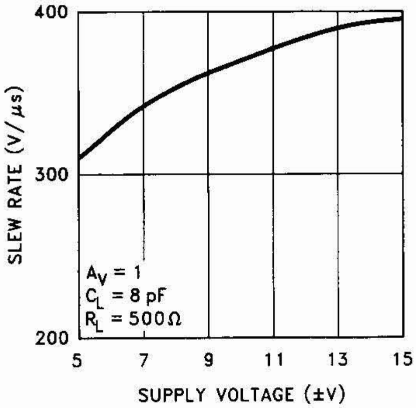
4453-12

Nonlinearity vs Sum Signal Span



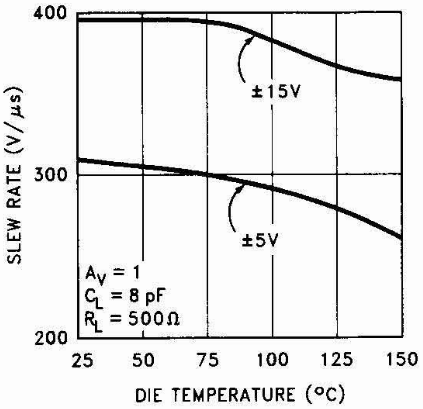
4453-13

Slew Rate vs Supply Voltage



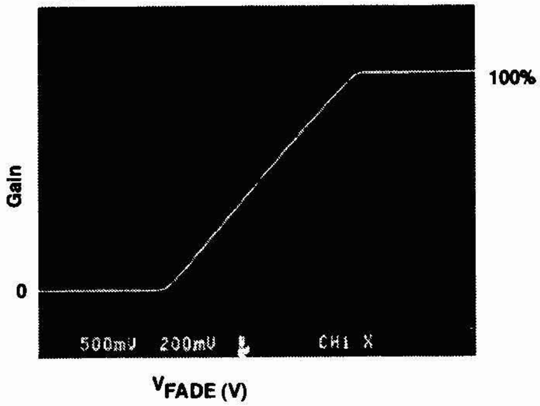
4453-18

Slew Rate vs Die Temperature



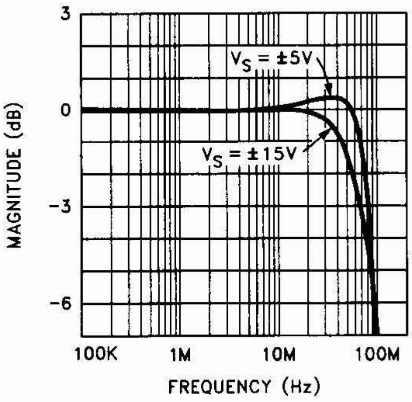
4453-19

V_{IN}A Gain vs V_{FADE}



4453-20

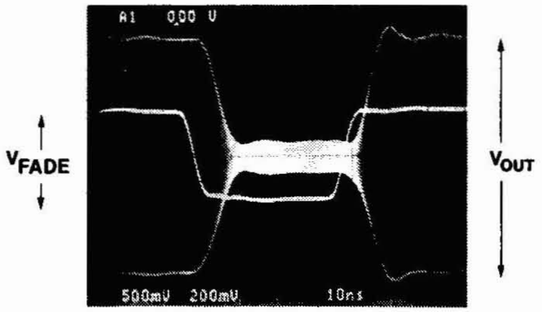
Frequency Response of Fade Input



4453-21

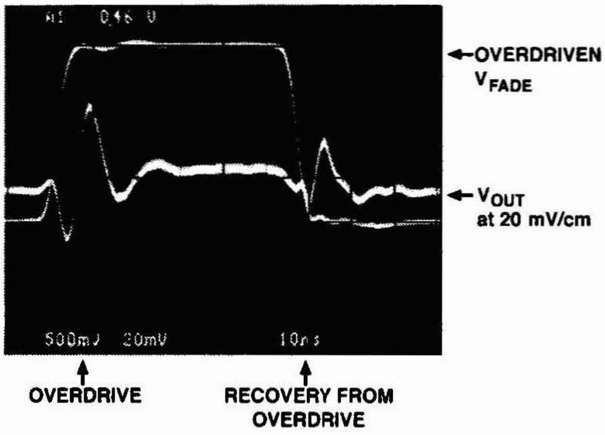
Typical Performance Curves — Contd.

Transient Response of Fade Input Constant Signal into $V_{IN}A$



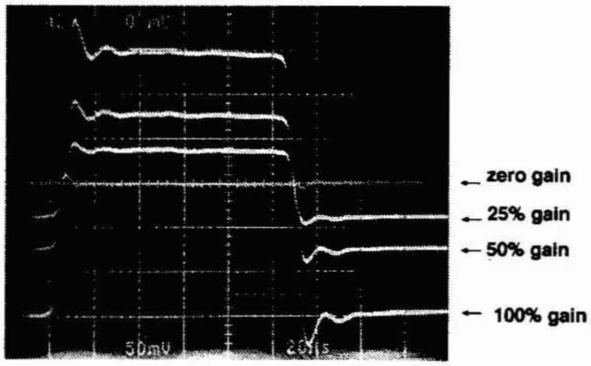
4453-22

Overdrive Recovery Glitch from V_{FADE}, No Input Signal



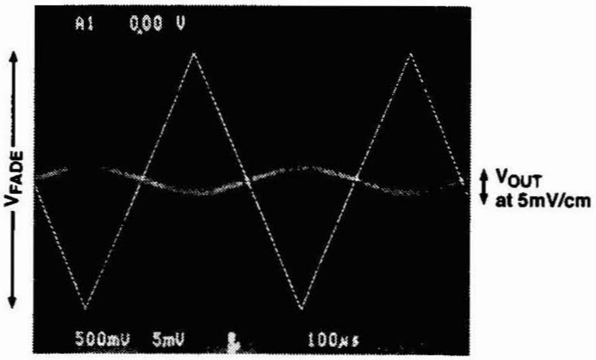
4453-23

$V_{IN}A$ Transient Response for Various Gains



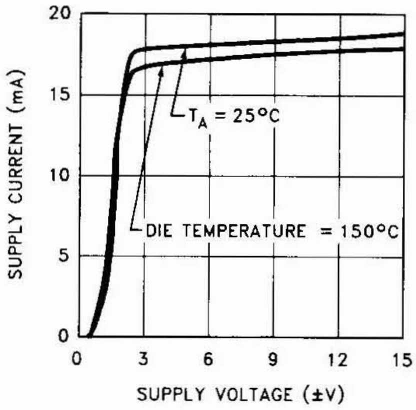
4453-24

Cross-Fade Balance with $V_{IN}A = V_{IN}B = 0$



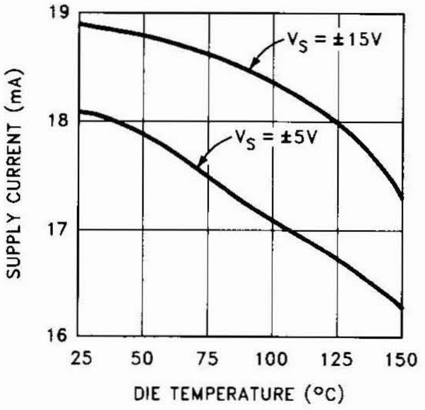
4453-25

Supply Current vs Supply Voltage



4453-26

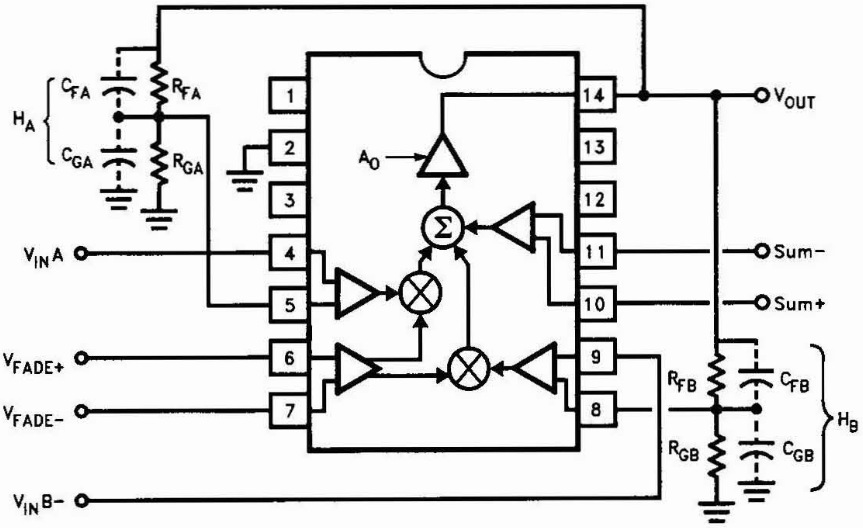
Supply Current vs Die Temperature



4453-27

Applications Information

The EL4453C is a complete two-quadrant fader/gain control with 80 MHz bandwidth. It has four sets of inputs; a differential signal input $V_{IN}A$, a differential signal input $V_{IN}B$, a differential fade-controlling input V_{FADE}, and another differential input Sum which can be used to add in a third input at full gain. This is the general connection of the EL4453C:


C_{FA}
R_{FA}
H_A
C_{GA}
R_{GA}
$V_{IN}A$
V_{FADE+}
V_{FADE-}
$V_{IN}B-$
1
2
3
4
5
6
7
8
9
10
11
12
13
14
A_0
Σ
V_{OUT}
Sum−
Sum+
R_{FB}
C_{FB}
R_{GB}
C_{GB}
H_B

4453-28

Applications Information — Contd.

The gain of the feedback dividers are H_A and H_B, and $0 \leq H \leq 1$. The transfer function of the part is

$$V_{OUT} = A_O \times [((V_{IN}A+) - H_A \times V_{OUT}) \times (1 + (V_{FADE}+) - (V_{FADE}-))/2 + ((V_{IN}B+) - H_B \times V_{OUT}) \times (1 - (V_{FADE}+) + (V_{FADE}-))/2 + (\mathrm{Sum}+) - (\mathrm{Sum}-))],$$

with $-1 \leq (V_{FADE}+) - (V_{FADE}-) \leq +1$ numerically.

A_O is the open-loop gain of the amplifier, and is about 600. The large value of A_O drives

$$((V_{IN}A+) - H_A \times V_{OUT}) \times (1 + (V_{FADE}+) - (V_{FADE}-))/2 + ((V_{IN}B+) - H_B \times V_{OUT}) \times (1 - (V_{FADE}+) + (V_{FADE}-))/2 + (\mathrm{Sum}+) - (\mathrm{Sum}-)) \longrightarrow 0.$$

Rearranging and substituting

$$V_{OUT} = \frac{F \times V_{IN}A + \overline{F} \times V_{IN}B + \mathrm{Sum}}{F \times H_A + \overline{F} \times H_B}$$

Where $F = (1 + (V_{FADE}+) - (V_{FADE}-))/2$,
$\overline{F} = (1 - (V_{FADE}+) + (V_{FADE}-))/2$, and
$\mathrm{Sum} = (\mathrm{Sum}+) - (\mathrm{Sum}-)$

In the above equations, F represents the fade amount, with $F = 1$ giving 100% gain on $V_{IN}A$ but 0% for $V_{IN}B$; $F = 0$ giving 0% gain for $V_{IN}A$ but 100% to $V_{IN}B$. $\overline{F}$ is $1 - F$, the complement of the fade gain. When $F = 1$,

$$V_{OUT} = \frac{V_{IN}A + \mathrm{Sum}}{H_A}$$

and the amplifier passes $V_{IN}A$ and Sum with a gain of $1/H_A$. Similarly, for $F = 0$

$$V_{OUT} = \frac{V_{IN}B + \mathrm{Sum}}{H_B}$$

and the gains vary linearly between fade extremes.

The EL4453C is stable for a direct connection between V_{OUT} and $V_{IN}A-$ or $V_{IN}B-$, yielding a gain of +1. The feedback divider may be used for higher output gain, although with the traditional loss of bandwidth. It is important to keep the feedback dividers' impedances low so that stray capacitance does not diminish the feedback loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 150 MHz; typical strays of 3 pF thus require a feedback impedance of 360Ω or less. Alternatively, a small capacitor across R_F can be used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors for a gain of two will dominate parasitic effects and allow a higher divider resistance. Either input channel can be set up for inverting gain using traditional feedback resistor connections.

At 100% gain, an input stage operates just like an op-amp's input, and the gain error is very low, around −0.2%. Furthermore, nonlinearities are vastly improved since the gain core sees only small error signals, not full inputs. Unfortunately, distortions increase at lower fade gains for a given input channel.

The Sum pins can be used to inject an additional input signal, but it is not as linear as the V_{IN} paths. The gain error is also not as good as the main inputs, being about 1%. Both sum pins should be grounded if they are not to be used.

Fade-Control Characteristics

The quantity V_{FADE} in the above equations is bounded as $-1 \leq V_{FADE} \leq 1$, even though the externally applied voltages often exceed this range. Actually, the gain transfer function around −1V and +1V is "soft", that is, the gain does not clip abruptly below the 0%-V_{FADE} voltage or above the 100%−V_{FADE} level. An overdrive of 0.3V must be applied to V_{FADE} to obtain truly 0% or 100%. Because the 0% = or 100%-V_{FADE} levels cannot be precisely determined, they are extrapolated from two points measured inside the slope of the gain transfer curve. Generally, an applied V_{FADE} range of −1.5V to +1.5V will assure the full span of numerical $-1 \leq V_{FADE} \leq 1$ and $0 \leq F \leq 1$.

The fade control has a small-signal bandwidth equal to the V_{IN} channel bandwidth, and overload recovery resolves in about 20 ns.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about six inches of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Often placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high frequency construction obviates any such problems, where the input source is reasonably close to the fader input. If this is not possible, one can insert series resistors of around 51Ω to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between (V−) + 2.5V and (V+) − 2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to ±6V to prevent damage. The differential signal range is ±2V in the EL4453C. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 μA maximum DC current, and may be biased anywhere between (V−) +2.5V and (V+) − 3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR and channel-to-channel isolation over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4453C works well on any supplies from ±3V to ±15V. The supplies may be of different voltages as long as the requirements of the GND pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as small as 0.01 μF can be used if small load currents flow.

Singe-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V− to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The dissipation of the fader increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \times V_S, \max \times V_S + (V_S - V_O) \times V_O / R_{PAR}$$

where I_S, max is the maximum supply current
V_S is the ± supply voltage (assumed equal)
V_O is the output voltage
R_{PAR} is the parallel of all resistors loading the output

Power Supplies — Contd.

For instance, the EL4453C draws a maximum of 21 mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with ±5V supplies is 210 mW. The maximum supply voltage that the device can run on for a given P_D and the other parameters is

$$V_S, \max = (P_D + V_O^2/R_{PAR})/(2I_S + V_O/R_{PAR})$$

The maximum dissipation a package can offer is

$$P_D, \max = (T_D, \max - T_A, \max)/\theta_{JA}$$

where T_D, max is the maximum die temperature, 150°C for reliability, less to retain optimum electrical performace

T_A, max is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from datasheet dissipation curves

The more difficult case is the SO-14 package. With a maximum die temperature of 150°C and a maximum ambient temperature of 70°C, the 80°C temperature rise and package thermal resistance of 110°/W gives a dissipation of 636 mW at 85 °C. This allows ±15V operation over the commercial temperature range, but higher ambient temperature or output loading may require lower supply voltages.

Output Loading

The output stage of the EL4453C is very powerful. It typically can source 80 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain changes only 0.2% from no load to 100Ω load. Heavy resistive loading will degrade frequency response and video distortion for loads < 100Ω.

Capacitive loads will cause peaking in the frequency response. If capacitive loads must be driven, a small-valued series resistor can be used to isolate it. 12Ω to 51Ω should suffice. A 22Ω series resistor will limit peaking to 2.5 dB with even a 220 pF load.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4581C
Sync Separator, 50% Slice, S-H, Filter

Features

- NTSC, PAL and SECAM sync separation
- Single supply, +5V
- Precision 50% slicing, internal caps
- Built-in color burst filter
- Decodes non-standard verticals
- Pin compatible with LM1881
- Low power
- Typically 1.5 mA supply current
- Resistor programmable scan rate
- Few external components
- Available in 8-pin DIP and SO-8 pkg.

Applications

- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL4581CN	−40°C to +85°C	8-Pin DIP	MDP0031
EL4581CS	−40°C to +85°C	8-Lead SO	MDP0027

Demo Board

A dedicated demo board is not available. However, this device can be placed on the EL4584/5 Demo Board.

General Description

The EL4581C extracts timing information from standard negative going video sync found in NTSC, PAL, and SECAM broadcast systems. It can also be used in non standard formats and with computer graphics systems at higher scan rates, by adjusting a single external resistor. When the input does not have correct serration pulses in the vertical interval, a default vertical output is produced.

Outputs are composite sync, vertical sync, burst/back porch output, and odd/even output. The later operates only in interlaced scan formats.

The EL4581C provides a reliable method of determining correct sync slide level by setting it to the mid-point between sync tip and blanking level at the back porch. This 50% level is determined by two internal self timing sample and hold circuits that track sync tip and back porch levels. This also provides a degree of hum and noise rejection to the input signal, and compensates for varying input levels of 0.5 p-p to 2.0 Vp-p.

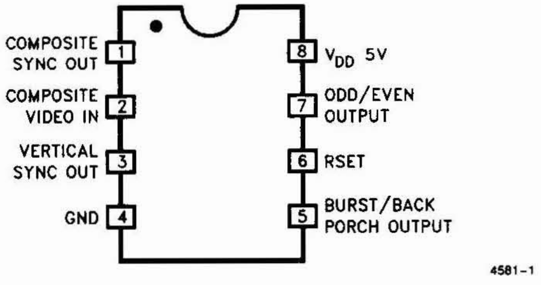
A built in linear phase, third order, low pass filter attenuates the chroma signal in color systems to prevent incorrectly set color burst from disturbing the 50% sync slide.

This device may be used to replace the industry standard LM1881, offering improved performance and reduced power consumption.

The EL4581C video sync separator is manufactured using Elantec's high performance analog CMOS process.

Connection Diagram

EL4581C SO, P-DIP Packages



Top View

Manufactured under U.S. Patent No. 5,528,303

January 1996 Rev B

EL4581C
Sync Separator, 50% Slice, S-H, Filter

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Pin Voltages	−0.5V to V_{CC} +0.5V
Storage Temperature	−65°C to +150°C	Operating Temperature Range	−40°C to +85°C
Lead Temperature	260°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics Unless otherwise state V_{DD} = 5V, T_A = 25°C, R_{set} = 680 kΩ.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C	0.75	1.7	3	I	mA
Clamp Voltage	Pin 2, Unloaded	25°C	1.3	1.5	1.9	I	V
Discharge Current	Pin 2 = 2V	25°C	6	10	20	I	μA
Clamp Charge Current	Pin 2, V_{IN} = 1V	25°C	2	3		I	mA
Ref Voltage	Pin 6, V_{DD} = 5V (Note 2)	25°C	1.5	1.8	2.1	I	V
V_{OL} Output Low Voltage	I_{OL} = 1.6 mA	25°C			800	I	mV
V_{OH} Output High Voltage	I_{OH} = −40 μA I_{OH} = −1.6 mA	25°C	4 2.4			IV I	V

Note 1: No video signal, outputs unloaded.
Note 2: Tested for V_{DD} 5V ±5% which guarantees timing of output pulses over this range.

EL4581C
Sync Separator, 50% Slice, S-H, Filter

Dynamic Characteristics

V_{DD} = 5V, I_V pk-pk video, T_A = 25°C, C_L = 15 pF, I_{OH} = −1.6 mA, I_{OL} = 1.6 mA. Signal voltages are peak to peak.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Vertical Sync Width, t_{VS}	(Note 3)	25°C	190	230	300	I	μs
Burst/Back Porch Width, t_B	(Note 3)	25°C	2.5	3.5	4.5	I	μs
Vertical Sync Default Delay t_{VSD}		25°C	40	55	70	I	μs
Filter Attenuation	F_{IN} = 3.4 MHz (Note 4)	25°C		24		V	dB
Composite Sync Prop Delay	V_{IN} − Composite Sync (Note 3)	25°C		260	400	I	ns
Input Dynamic Range	p-p NTSC Signal (Note 5)	25°C	0.5		2	I	V
Slice Level	Input Voltage = 1V_{P-P} (Note 6)	25°C Full	40% 40%	50% 50%	60% 60%	I IV	

Note 3: C/S, Vertical and Burst outputs are all active low − V_{OH} = 2.4V, V_{OL} = 0.8V.

Note 4: Attenuation is a function of Rset (PIN6).

Note 5: Typical min. is 0.3 V_{P-P}.

Note 6: Refers to threshold level of sync. tip to back porch amplitude.

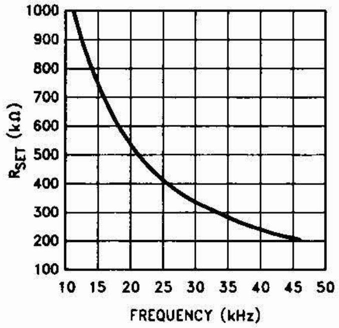
Pin Descriptions

Pin No.	Pin Name	Function
1	Composite Sync Out	Composite sync pulse output. Sync pulses start on a falling edge and end on a rising edge.
2	Composite Video in	AC coupled composite video input. Sync tip must be at the lowest potential (Positive picture phase).
3	Vertical Sync Out	Vertical sync pulse output. The falling edge of Vert Sync is the start of the vertical period.
4	GND	Supply ground.
5	Burst/Back Porch Output	Burst/Back porch output. Low during burst portion of composite video.
6	R_{SET}	An external resistor to ground sets all internal timing. 681k, 1% resistor will provide correct timing for NTSC signals.
7	Odd/Even Output	Odd/Even field output. Low during odd fields, high during even fields. Transitions occur at start of Vert Sync pulse.
8	V_{DD} 5V	Positive supply. (5V)

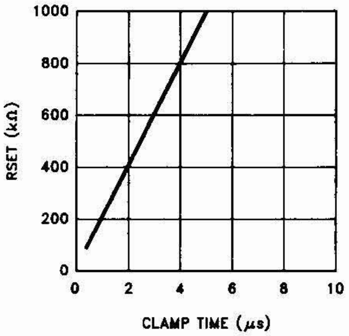
Note: R_{SET} must be a 1% resistor.

Typical Performance Characteristics

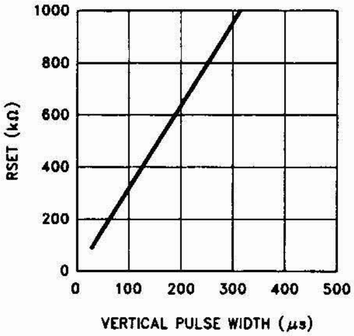
RSET vs Horizontal Frequency



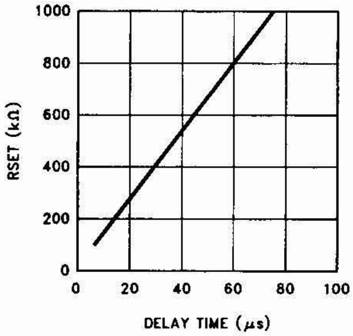
Back Porch Clamp On Time vs RSET



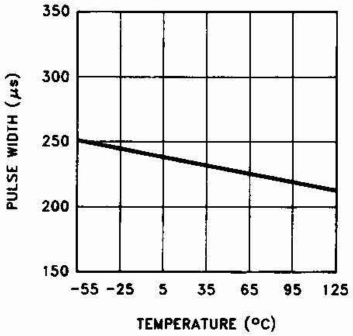
Vertical Pulse Width vs RSET



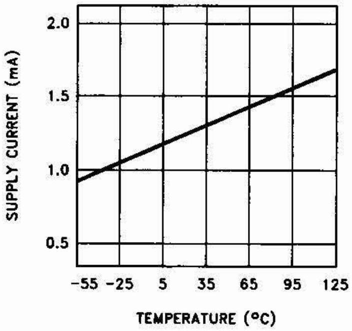
Vertical Default Delay Time vs RSET



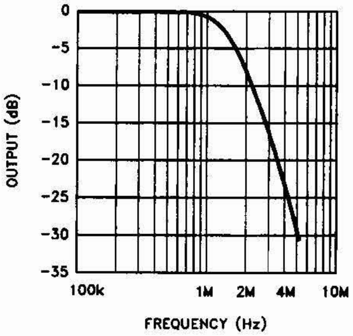
Vertical Pulse Width vs Temperature



Supply Current vs Temperature



Input Signal = 300 $mV_{P\text{-}P}$
EL4581 Filter Characteristic
Constant Delay 240 ns



4581-2

Timing Diagrams

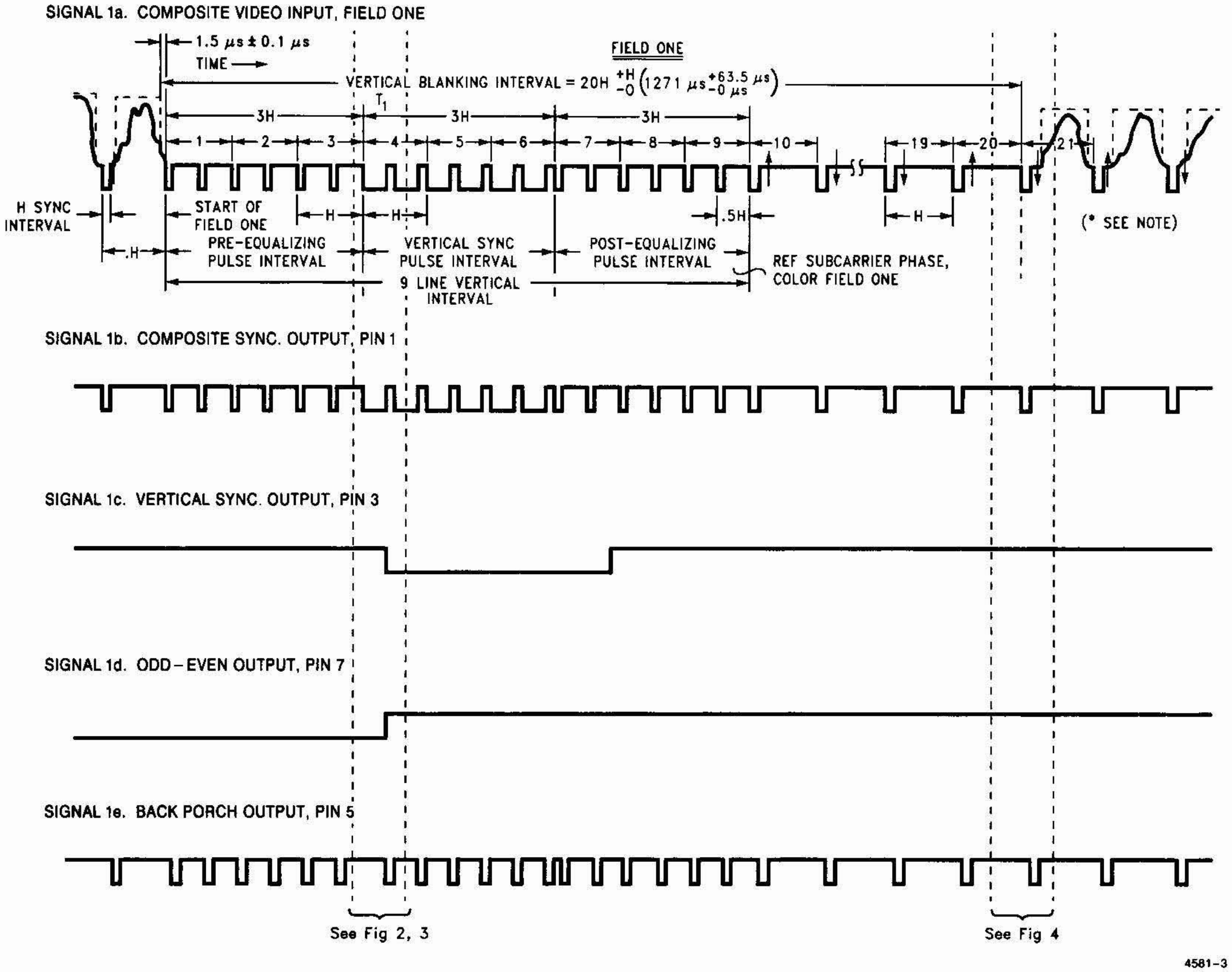

SIGNAL 1a. COMPOSITE VIDEO INPUT, FIELD ONE
1.5 μs ± 0.1 μs
TIME
FIELD ONE
VERTICAL BLANKING INTERVAL = 20H +H -0 (1271 μs +63.5 μs -0 μs)
T1
3H
3H
3H
1
2
3
4
5
6
7
8
9
10
19
20
21
H SYNC INTERVAL
.H
START OF FIELD ONE
H
H
.5H
H
(* SEE NOTE)
PRE-EQUALIZING PULSE INTERVAL
VERTICAL SYNC PULSE INTERVAL
POST-EQUALIZING PULSE INTERVAL
REF SUBCARRIER PHASE, COLOR FIELD ONE
9 LINE VERTICAL INTERVAL
SIGNAL 1b. COMPOSITE SYNC. OUTPUT, PIN 1
SIGNAL 1c. VERTICAL SYNC. OUTPUT, PIN 3
SIGNAL 1d. ODD-EVEN OUTPUT, PIN 7
SIGNAL 1e. BACK PORCH OUTPUT, PIN 5
See Fig 2, 3
See Fig 4
4581-3

Figure 1

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

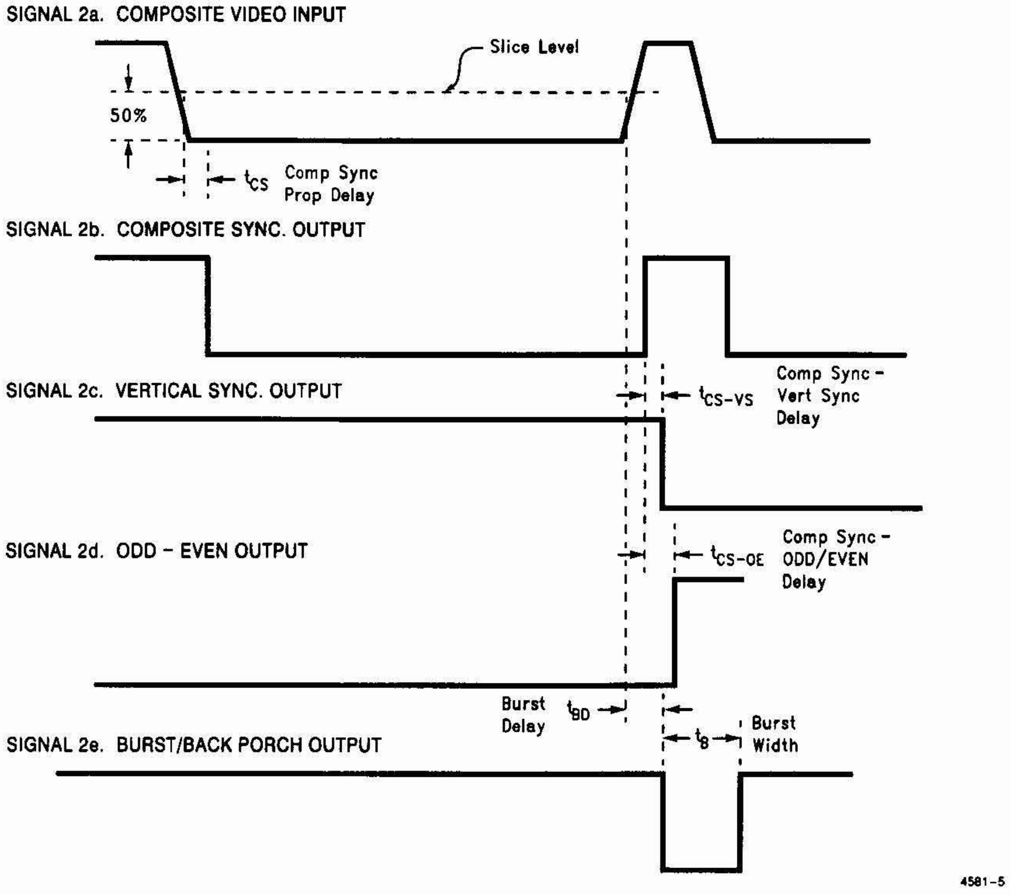

SIGNAL 2a. COMPOSITE VIDEO INPUT
Slice Level
50%
t_{CS}
Comp Sync Prop Delay
SIGNAL 2b. COMPOSITE SYNC. OUTPUT
SIGNAL 2c. VERTICAL SYNC. OUTPUT
t_{CS-VS}
Comp Sync - Vert Sync Delay
SIGNAL 2d. ODD - EVEN OUTPUT
t_{CS-OE}
Comp Sync - ODD/EVEN Delay
Burst Delay
t_{BD}
t_B
Burst Width
SIGNAL 2e. BURST/BACK PORCH OUTPUT
4581-5

Figure 2

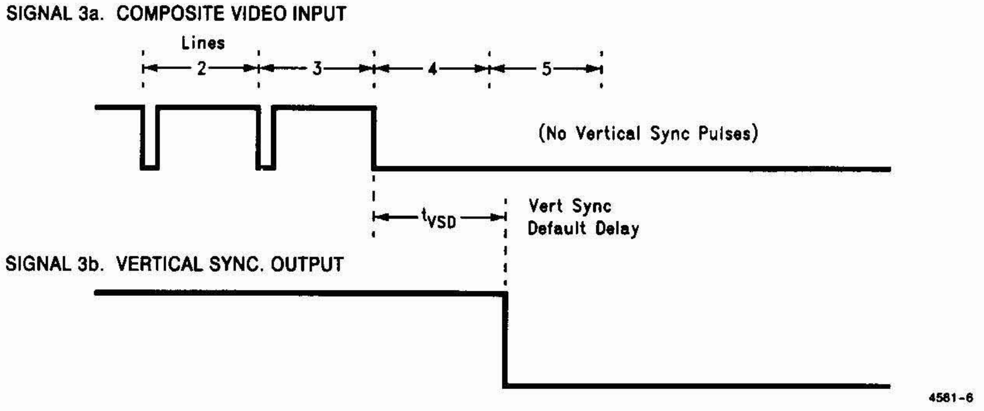

SIGNAL 3a. COMPOSITE VIDEO INPUT
Lines
2
3
4
5
(No Vertical Sync Pulses)
t_{VSD}
Vert Sync Default Delay
SIGNAL 3b. VERTICAL SYNC. OUTPUT
4581-6

Figure 3

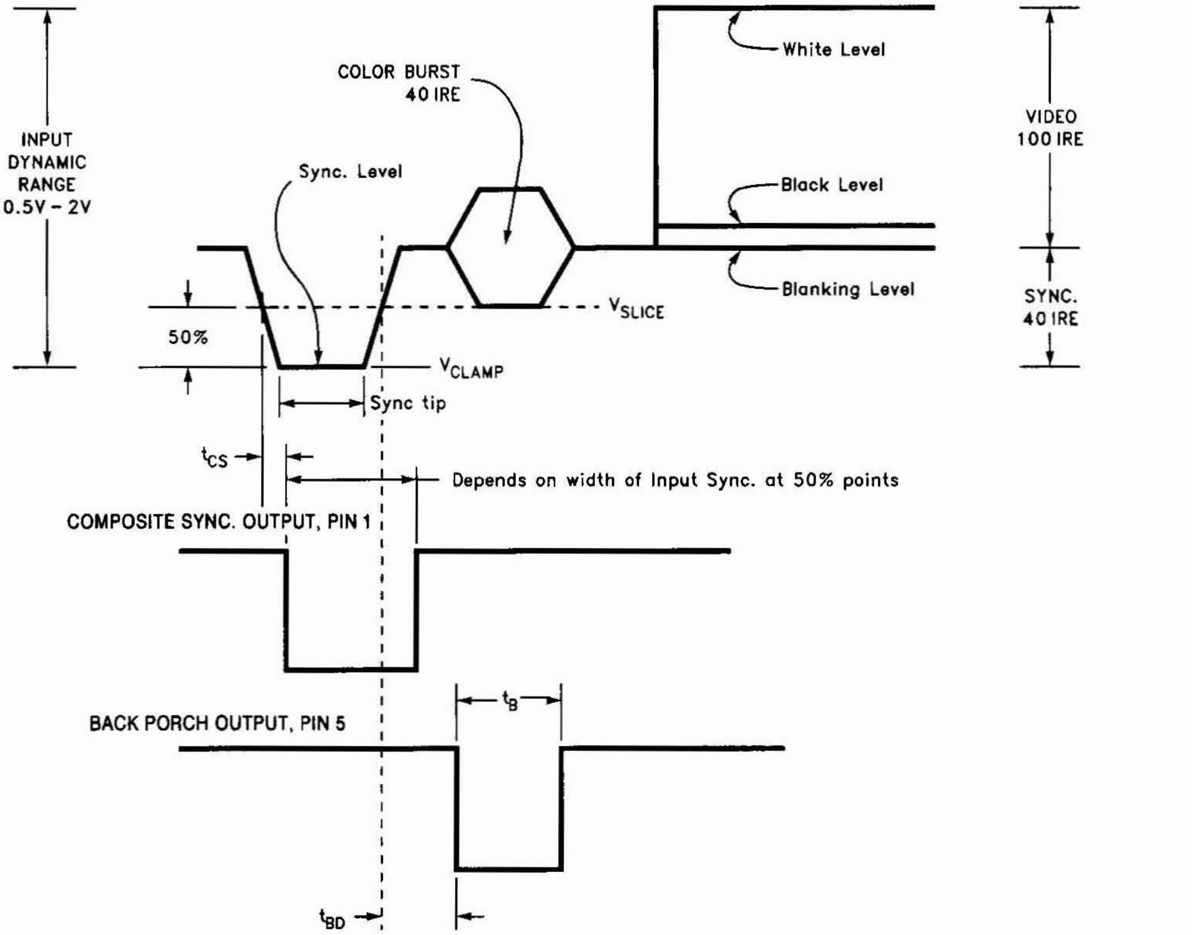

INPUT DYNAMIC RANGE 0.5V - 2V
COLOR BURST 40 IRE
Sync. Level
White Level
VIDEO 100 IRE
Black Level
Blanking Level
SYNC. 40 IRE
50%
V_{SLICE}
V_{CLAMP}
Sync tip
t_{CS}
Depends on width of Input Sync. at 50% points
COMPOSITE SYNC. OUTPUT, PIN 1
t_B
BACK PORCH OUTPUT, PIN 5
t_{BD}
4581-7

Figure 4. Standard (NTSC Input) H. Sync Detail

Description of Operation

A simplified block schematic is shown in Figure 2. The following description is intended to provide the user with sufficient information to be able to understand the effects that the external components and signal conditions have on the outputs of the integrated circuit.

The video signal is AC coupled to pin 2 via the capacitor C_1, nominally 0.1 μF. The clamp circuit A1 will prevent the input signal on pin 2 going any more negative than 1.5V, the value of reference voltage V_{R1}. Thus the sync tip, the most negative part of the video waveform, will be clamped at 1.5V. The current source I_1, nominally 10 μA, charges the coupling capacitor during the remaining portion of the H line, approximately 58 μs for a 15.75 kHz timebase. From $I \bullet t = C \bullet V$, the video time-constant can be calculated. It is important to note that the charge taken from the capacitor during video must be replaced during the sync tip time, which is much shorter, (ratio of x 12.5). The corresponding current to restore the charge during sync will therefore be an order of magnitude higher, and any resistance in series with C_I will cause sync tip crushing. For this reason, the internal series resistance has been minimized and external high resistance values in series with the input coupling capacitor should be avoided. The user can exercise some control over the value of the input time constant by introducing an external pull-up resistance from pin 2 to the 5V supply. The maximum voltage across the resistance will be V_{DD} less 1.5V, for black level. For a net discharge current greater than zero, the resistance should be greater than 450k. This will have the effect of increasing the time constant and reducing the degree of picture tilt. The current source I_1 directly tracks reference current I_{TR} and thus increases with scan rate adjustment, as explained later.

The signal is processed through an active 3 pole filter (F1) designed for minimum ripple with constant phase delay. The filter attenuates the color burst by 24 dB and eliminates fast transient spikes without sync crushing. An external filter is not necessary. The filter also amplifies the video signal by 6 dB to improve the detection accuracy. Note that the filter cut-off frequency is a function of RSET through I_{OT} and is proportional to I_{OT}.

Internal reference voltages (block V_{REF}) with high immunity to supply voltage variation are derived on the chip. Reference V_{R4} with op-amp A2 forces pin 6 to a reference voltage of 1.7V nominal. Consequently, it can be seen that the external resistance RSET will determine the value of the reference current I_{TR}. The internal resistance R3 is only about 6 kΩ, much less than RSET. All the internal timing functions on the chip are referenced to I_{TR} and have excellent supply voltage rejection.

Comparator C2 on the input to the sample and hold block (S/H) compares the leading and trailing edges of the sync. pulse with a threshold voltage V_{R2} which is referenced at a fixed level above the clamp voltage V_{R1}. The output of C2 initiates the timing one-shots for gating the sample and hold circuits. The sample of the sync tip is delayed by 0.8 μs to enable the actual sample of 2 μs to be taken on the optimum section of the sync. pulse tip. The acquisition time of the circuit is about three horizontal lines. The double poly CMOS technology enables long time constants to be achieved with small high quality on-chip capacitors. The back porch voltage is similarly derived from the trailing edge of sync, which also serves to cut off the tip sample if the gate time exceeds the tip period. Note that the sample and hold gating times will track RSET through I_{OT}.

The 50% level of the sync tip is derived, through the resistor divider R1 and R2, from the sample and held voltages V_{TIP} and V_{BP}, and applied to the plus input of comparator C1. This comparator has built in hysteresis to avoid false triggering. The output of C2 is a digital 5V signal which feeds the C/S ouput buffer B1 and the other internal circuit blocks, the vertical, back porch and odd/even functions.

The vertical circuit senses the C/S edges and initiates an integrator which is reset by the shorter horizontal sync pulses but times out the longer

Description of Operation — Contd.

vertical sync. pulse widths. The internal timing circuits are referenced to I_{OT} and V_{R3}, the time-out period being inversely proportional to the timing current. The vertical output pulse is started on the first serration pulse in the vertical interval and is then self-timed out. In the absense of a serration pulse, an internal timer will default the start of vertical.

The back porch is triggered from the sync tip trailing edge and initiates a one-shot pulse. The period of this pulse is again a function of I_{OT} and will therefore track the scan rate set by RSET.

The odd/even circuit (O/E) comprises of flip flops which track the relationship of the horizontal pulses to the leading edge of the vertical output, and will switch on every field at the start of vertical. Pin 7 is high during the odd field.

Loss of video signal can be detected by monitoring the C/S output. The 50% level of the previous video signal will remain held on the S/H capacitors after the input video signal has gone and the input on pin 2 has defaulted to the clamp voltage. Consequently the C/S output will remain low longer than the normal vertical pulse period. An external timing circuit could be used to detect this condition.

Block Diagram

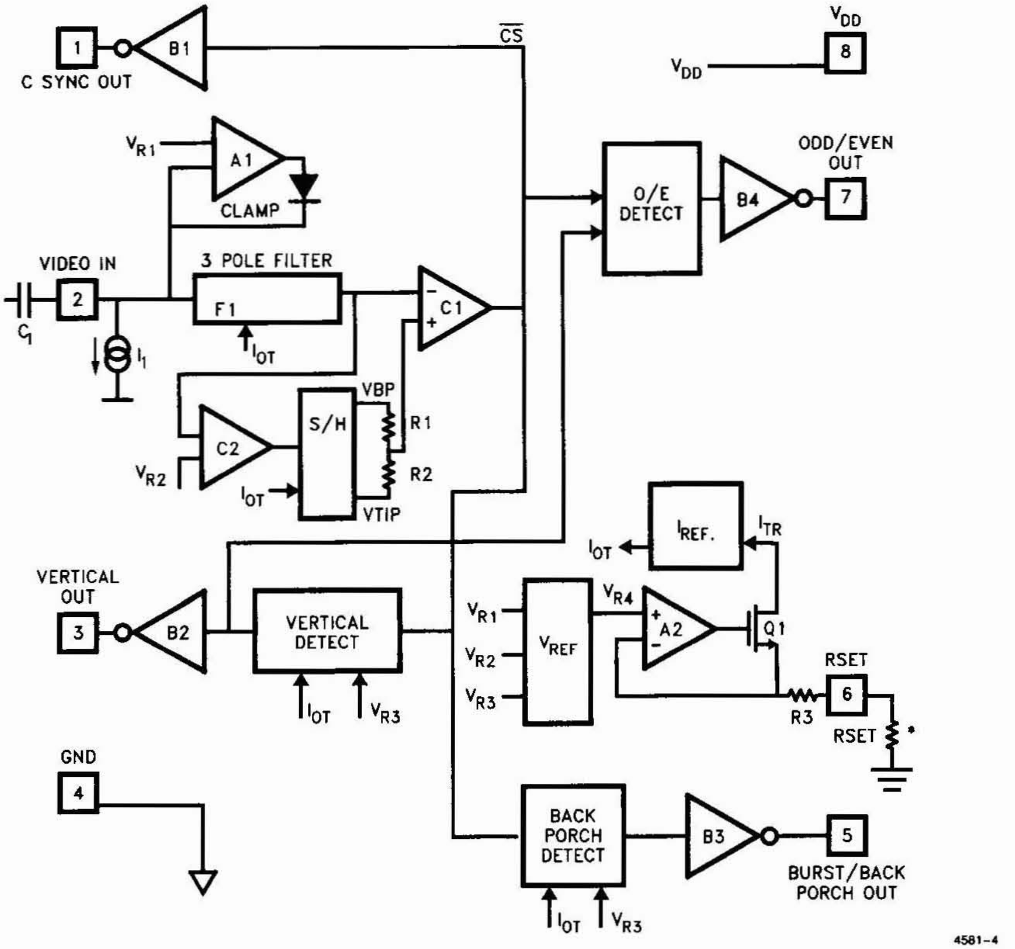

1
B1
C SYNC OUT
$\overline{CS}$
V_{DD}
V_{DD}
8
V_{R1}
A1
CLAMP
ODD/EVEN OUT
O/E DETECT
B4
7
VIDEO IN
3 POLE FILTER
2
C_1
F1
I_{OT}
I_1
C1
VBP
S/H
R1
C2
R2
V_{R2}
I_{OT}
VTIP
$I_{REF.}$
I_{TR}
I_{OT}
VERTICAL OUT
3
B2
VERTICAL DETECT
I_{OT}
V_{R3}
V_{R1}
V_{R2}
V_{R3}
V_{REF}
V_{R4}
A2
Q1
RSET
6
R3
RSET
GND
4
BACK PORCH DETECT
B3
5
BURST/BACK PORCH OUT
I_{OT}
V_{R3}
4581-4

Figure 5

*Note: RSET must be a 1% resistor.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4583C

Sync Separator, 50% Slice, S-H, Filter, H_{OUT}

Features

- NTSC, PAL and SECAM sync separation
- Single supply, + 5V operation
- Precision 50% slicing, internal caps
- Built in programmable color burst filter
- Decodes non-standard verticals
- Horizontal sync output
- Sync. pulse amplitude output
- Same socket can be used for 8-pin EL4581
- Low power CMOS
- Detects loss of signal
- Resistor programmable scan rate
- Few external components
- Available in 16-Pin DIP and SO-16 pkg.

Applications

- Video special effects
- Video test equipment
- Video distribution
- Multimedia
- Displays
- Imaging
- Video data capture
- Video triggers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4583CN	−40°C to +85°C	16-Pin DIP	MDP0031
EL4583CS	−40°C to +85°C	16-Lead SO	MDP0027

General Description

The EL4583C extracts timing from video sync in NTSC, PAL, and SECAM systems, and non standard formats, or from computer graphics operating at higher scan rates. Timing adjustment is via an external resistor. Input without valid vertical interval (no serration pulses) produces a default vertical output.

A larger package (16-pin) is used for greater flexibility. The "core" pins match the same pin functions of the 8-pin (EL4581C etc.) for substitution in applications not requiring these features.

Outputs are: **composite sync, vertical sync, filter, burst/ back porch, horizontal, no signal detect, level,** and **odd/ even output** (in interlaced scan formats only).

The EL4583C sync slice level is set to a mid-point halfway between sync tip and the blanking level. This 50% point is determined by two internal sample and hold circuits that track sync tip and back porch levels. It provides hum and noise rejection and compensates for input levels of 0.5V to $2.0V_{p\text{-}p}$.

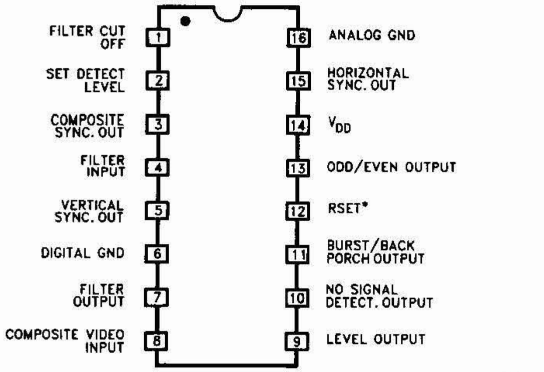
A built in filter attenuates the chroma signal to prevent color burst from disturbing the 50% sync slice. Cut off frequency is set by a resistor to ground from the **Filter Cut Off** pin. The filter can be by-passed, the video signal is fed to the **Video Input**.

A DC voltage, twice the sync amplitude, from the **Level Output** pin drives AGC circuits. A TTL/CMOS compatible **No Signal Detect Output** signals a loss or reduction in input signal level. A resistor sets the **Set Detect Level**.

The EL4583C is manufactured using Elantec's high performance analog CMOS process.

Connection Diagram

EL4583C SO, PDIP Packages


FILTER CUT OFF
1
SET DETECT LEVEL
2
COMPOSITE SYNC. OUT
3
FILTER INPUT
4
VERTICAL SYNC. OUT
5
DIGITAL GND
6
FILTER OUTPUT
7
COMPOSITE VIDEO INPUT
8
ANALOG GND
16
HORIZONTAL SYNC. OUT
15
V_{DD}
14
ODD/EVEN OUTPUT
13
RSET*
12
BURST/BACK PORCH OUTPUT
11
NO SIGNAL DETECT. OUTPUT
10
LEVEL OUTPUT
9
4583-1

Top View

*Note: RSET must be a 1% resistor.

January 1996, Rev. B

EL4583C

Sync Separator, 50% Slice, S-H, Filter, H_{OUT}

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Pin Voltages	−0.5V to V_{CC} +0.5V
Storage Temperature	−65°C to +150°C	Operating Temperature Range	−40°C to +85°C
Lead Temperature	260°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C, RSET = 681k, RF = 22k, RLV = 82k)

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C		2.5	4	I	mA
Clamp Voltage	Pins 4, 8, unloaded	25°C	1.3	1.55	1.8	I	V
Discharge Current	Pins 4, 8, with Signal (Note 2) No Signal	25°C	3	1 6	12	I I	µA
Clamp Charge Current	Pins 4, 8, V_{IN} = IV	25°C	2	3	4	I	mA
Ref. Voltage V_{REF}	Pin 12, V_{DD} = 5V (Note 3)	25°C	1.5	1.75	2	I	V
Filter Reference Voltage, VRF	Pin 1	25°C	0.35	0.5	0.65	I	V
Level Reference Current	Pin 2 (Note 4)	25°C	1.5	2.5	3.5	I	µA
V_{OL} Output Low Voltage	I_{OL} = 1.6 mA	25°C		350	800	I	mV
V_{OH} Output High Voltage	I_{OH} = −40 µA I_{OH} = −1.6 mA	25°C	4 2.4	 4		IV I	V

Note 1: No video signal, outputs unloaded.
Note 2: At loss of signal (pin 10 high) the pull down current source switches to a value of 10 µA.
Note 3: Tested for V_{DD} 5V ±5%.
Note 4: Current sourced from pin 2 is V_{REF}/RSET.

Dynamic Characteristics

RF = 22 kΩ, RSET = 681 kΩ, V_{DD} = 5V, 1 V_{p-p} VIDEO, T_A = 25°C, C_L = 15 pF, I_{OH} = −1.6 mA, I_{OL} = 1.6 mA

Parameter	Description	Min	Typ	Max	Test Level	Units
Horizontal Pulse Width, Pin 15, t_H	(Note 5)	3.8	5	6.2	I	µs
Vertical Sync Width, Pin 5, t_{VS}	(Note 6)		195		I	µs
Burst/Back Porch Width, Pin 11, t_B	(Note 5)	2.7	3.7	4.7	I	µs
Filter Attenuation	F_{IN} = 3.6 MHz (Note 7)		12		IV	dB
Comp. Sync Prop. Delay, t_{CS}	V_{IN} (Pin 4)—Comp Sync		250	400	I	ns
Input Dynamic Range	p-p NTSC Signal	0.4		2	I	V
Slice Level	Input Voltage = 1 V_{p-p} V_{SLICE}/V_{BLANK}	40% 40%	50% 50%	60% 60%	I IV	
Level Out, Pin 9	Input Voltage = 1 V_{p-p} Pin 4	555	620	685	I	mV
Vertical Sync Default Time, t_{VSD}	(Note 8)	27	36	45	I	µs
Loss of Signal Time-Out	Pin 10	400	600	800	I	µs
Burst/Back Porch Delay, t_{BD}	See Figure 4		250	400	V	µs

Note 5: Width is a function of RSET.
Note 6: c/s, Vertical, Back porch and H are all active low, V_{OH} = 0.8V. Vertical is 3H lines wide of NTSC signal.
Note 7: Attenuation is a function of RF. See filter typical characteristics.
Note 8: Vertical pulse width in absence of serrations on input signal.

Pin Description

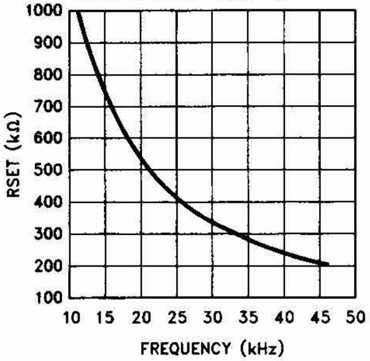
Pin No.	Pin Name	Function
1	Filter Cut-Off	A resistor RF connected between this input and ground determines the input filter characteristic. Increasing RF increases the filter 3.58 MHz color burst attenuation. See the graph showing filter characteristics.
2	Set Detect Level	A resistor RLV connected between pin 2 and ground determines the value of the minimum signal which will trigger the loss of signal output on pin 10. The relationship is V_PMIN = 0.75 RLV/RSET, where V_PMIN is the minimum detected sync pulse amplitude applied to pin 4. See characterization curve.
3	Composite Sync Output	This output replicates all the sync inputs on the input video.
4	Filter Input	The filter is a 3 pole active filter with a gain of 2, designed to produce a constant phase delay of nominally 260 ns with signal amplitude. Resistor RF on pin 1 controls the filter cut-off. An internal clamp sets the minimum voltage on pin 4 at 1.55V when the input becomes low impedance. Above the clamp voltage, an input current of 1 µA charges the input coupling capacitor. With loss of signal, the current source switches to a value of 10 µA, for faster signal recovery.
5	Vertical Sync Output	The vertical sync output is synchronous with the first serration pulse rising edge in the vertical interval of the input signal and ends on the trailing edge of the first equalizing Output pulse after the vertical interval. It will therefore be slightly more than 3H lines wide.

Pin Description — Contd.

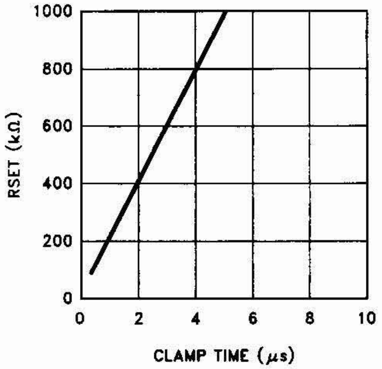
Pin No.	Pin Name	Function
6	Digital Ground	This is the ground return for digital buffer outputs.
7	Filter Output	Output of the active 3 pole filter which has its input on pin 4. It is recommended to ac couple the output to pin 8.
8	Video Input	This input can be directly driven by the signal if it is desired to bypass the filter, for example, in the case of strong clean signals. This input is 6 dB less sensitive than the filter input.
9	Level Output	This pin provides an analog voltage which is nominally equal to twice the sync pulse amplitude of the video input signal applied to pin 4. It therefore provides an indication of signal strength.
10	No Signal Detect Output	This is a digital output which goes high when either a) loss of input signal or b) the input signal level falls below a predetermined amplitude as set by RLV on pin 2. There will be several horizontal lines delay before the output is initiated.
11	Burst/Back Porch Output	The start of back porch output is triggered on the trailing edge of normal H sync, and on the rising edge of serration pulses in the vertical interval. The pulse is timed out internally to produce a one-shot output. The pulse width is a function of RSET. This output can be used for d.c. restore functions where the back porch level is a known reference.
12	RSET	The current through the resistor RSET determines the timing of the functions within the I.C. These functions include the sampling of the sync pulse 50% point, back porch output and the 2H eliminator. For faster scan rates, the resistor needs to be reduced inversely. For NTSC 15.7 kHz scan rate RSET is 681k 1%. RSET must be a 1% resistor.
13	Odd/Even Output	Odd-even output is low for even field and high for odd field. The operation of this circuit has been improved for rejecting spurious noise pulses such as those present in VCR signals.
14	V_{DD} 5V	The internal circuits are designed to have a high immunity to supply variations, although as with most I.C.s a 0.1 μF decoupling capacitor is advisable.
15	Horizontal Sync Output	This output produces only true H pulses of nominal width 5 μs. The leading edge is triggered from the leading edge of the input H sync, with the same prop. delay as the composite sync. The half line pulses present in the input signal during vertical blanking are eliminated with an internal 2H eliminator circuit.
16	Analog Ground	This is the ground return for the signal paths in the chips, RSET, RF and RLV.

Typical Performance Characteristics

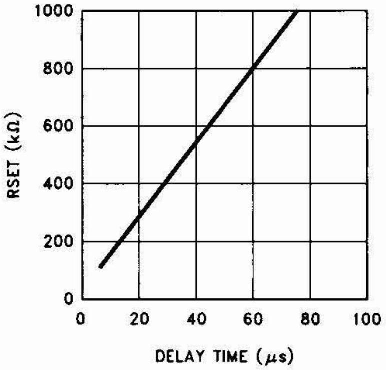
RSET vs Horizontal Frequency



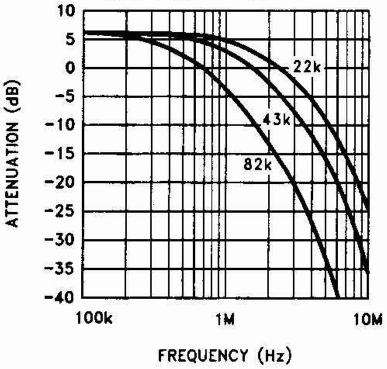
Back Porch Clamp On Time vs RSET



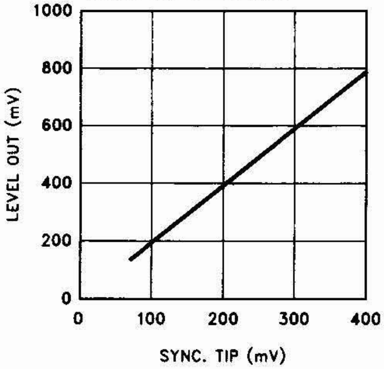
Vertical Default Delay Time vs RSET



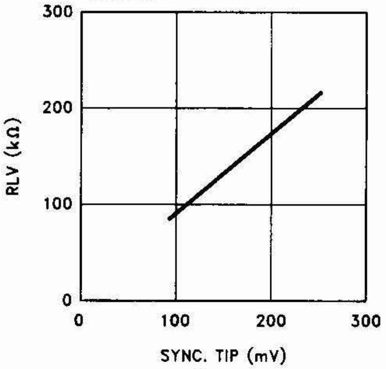
Filter 3 dB BW vs RF



Level Out (Pin 9) vs Sync. Tip Amplitude



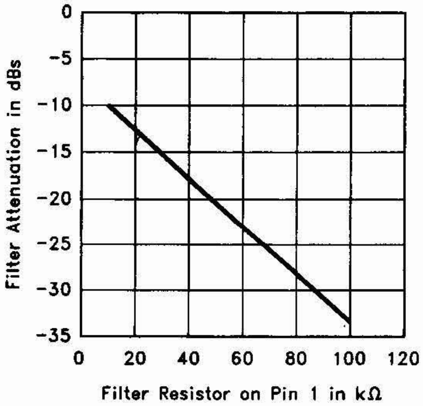
Minimum Signal Detect vs RLV



*Note 1

4583-3

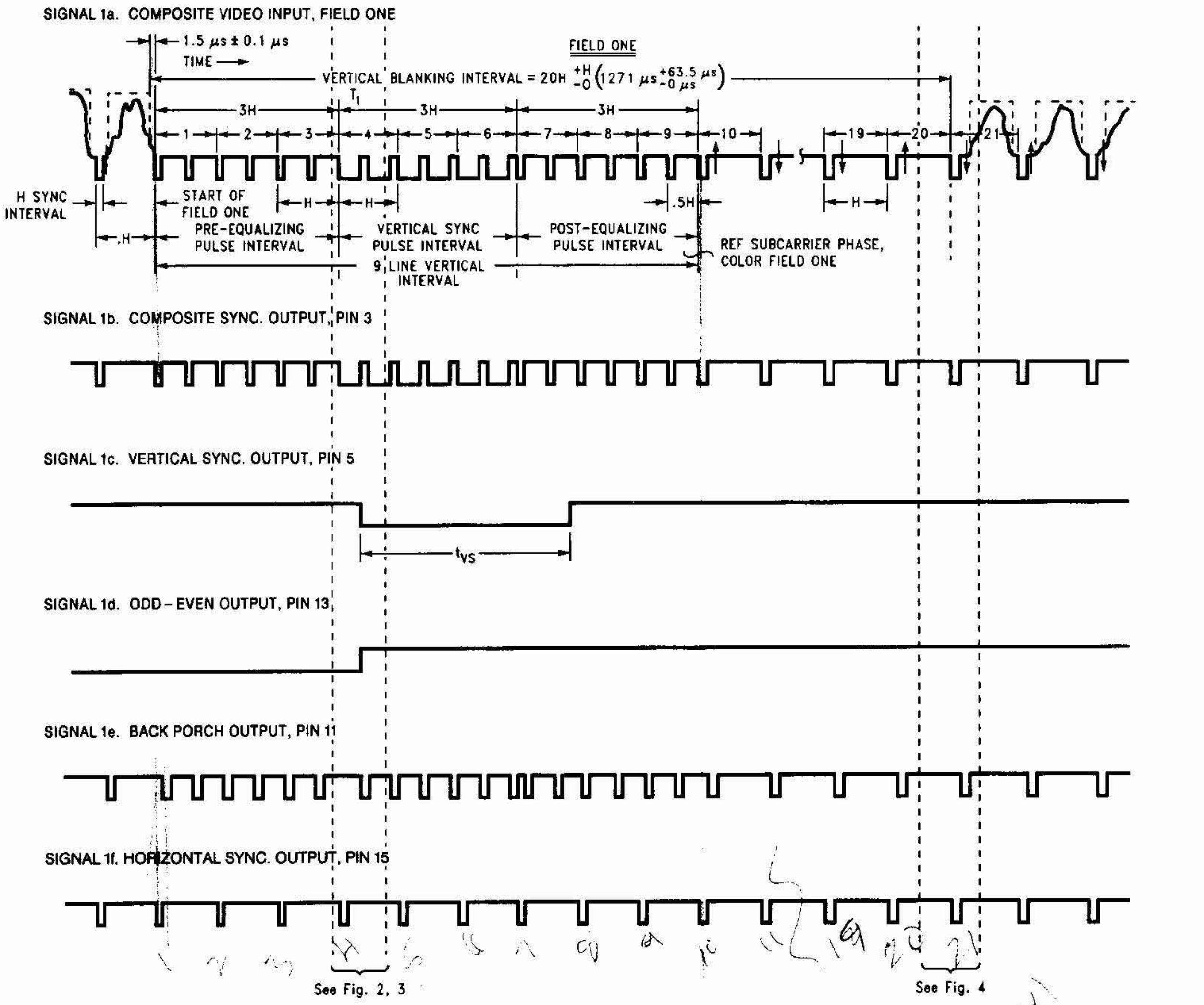
Filter Attenuation vs RF @ f = 3.58 MHz



4583-4

Note 1: For RLV < 100 kΩ, no signal detect output (pin 10) will default high at minimum signal sensitivity specification, or at complete loss of signal.

Timing Diagram


SIGNAL 1a. COMPOSITE VIDEO INPUT, FIELD ONE
1.5 µs ± 0.1 µs
TIME
FIELD ONE
VERTICAL BLANKING INTERVAL = 20H +H -0 (1271 µs +63.5 µs -0 µs)
T1
3H
3H
3H
1 2 3 4 5 6 7 8 9 10 19 20 21
H SYNC INTERVAL
START OF FIELD ONE
H
H
.5H
H
PRE-EQUALIZING PULSE INTERVAL
VERTICAL SYNC PULSE INTERVAL
POST-EQUALIZING PULSE INTERVAL
REF SUBCARRIER PHASE, COLOR FIELD ONE
9 LINE VERTICAL INTERVAL
SIGNAL 1b. COMPOSITE SYNC. OUTPUT, PIN 3
SIGNAL 1c. VERTICAL SYNC. OUTPUT, PIN 5
tVS
SIGNAL 1d. ODD - EVEN OUTPUT, PIN 13
SIGNAL 1e. BACK PORCH OUTPUT, PIN 11
SIGNAL 1f. HORIZONTAL SYNC. OUTPUT, PIN 15
1 2 3 4 5 6 7 8 9 10 11 19 20 21
See Fig. 2, 3
See Fig. 4
(284)

4583-5

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

f. Horizontal sync output produces the true "H" pulses of nominal width of 5µs. It has the same delay as the composite sync.

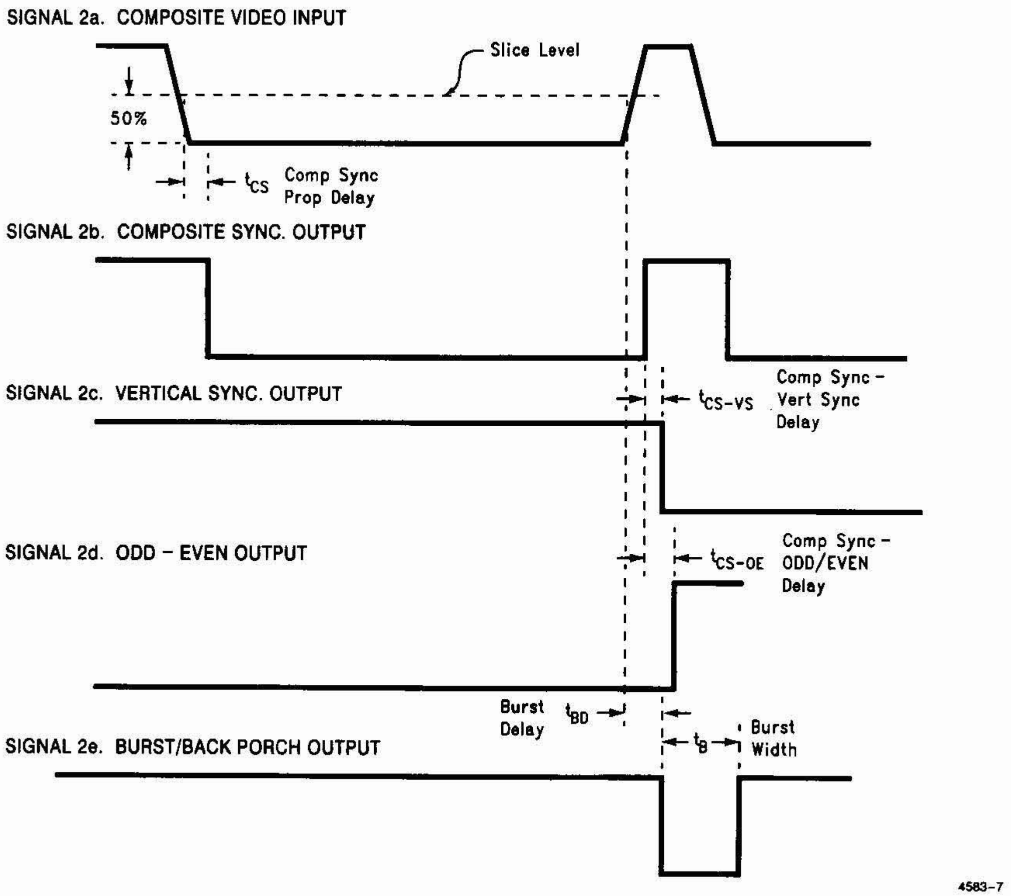

SIGNAL 2a. COMPOSITE VIDEO INPUT
Slice Level
50%
tCS Comp Sync Prop Delay
SIGNAL 2b. COMPOSITE SYNC. OUTPUT
SIGNAL 2c. VERTICAL SYNC. OUTPUT
tCS-VS Comp Sync - Vert Sync Delay
SIGNAL 2d. ODD - EVEN OUTPUT
tCS-OE Comp Sync - ODD/EVEN Delay
Burst Delay tBD
tB Burst Width
SIGNAL 2e. BURST/BACK PORCH OUTPUT
4583-7

Figure 2

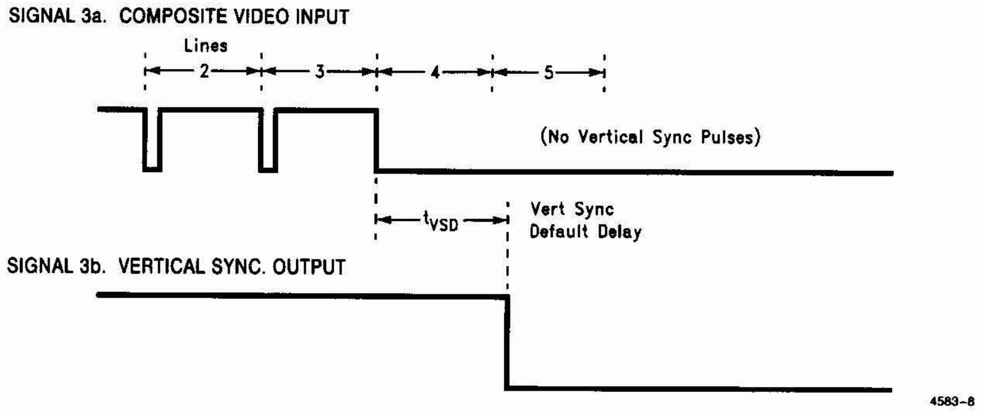

SIGNAL 3a. COMPOSITE VIDEO INPUT
Lines
2
3
4
5
(No Vertical Sync Pulses)
tVSD Vert Sync Default Delay
SIGNAL 3b. VERTICAL SYNC. OUTPUT
4583-8

Figure 3

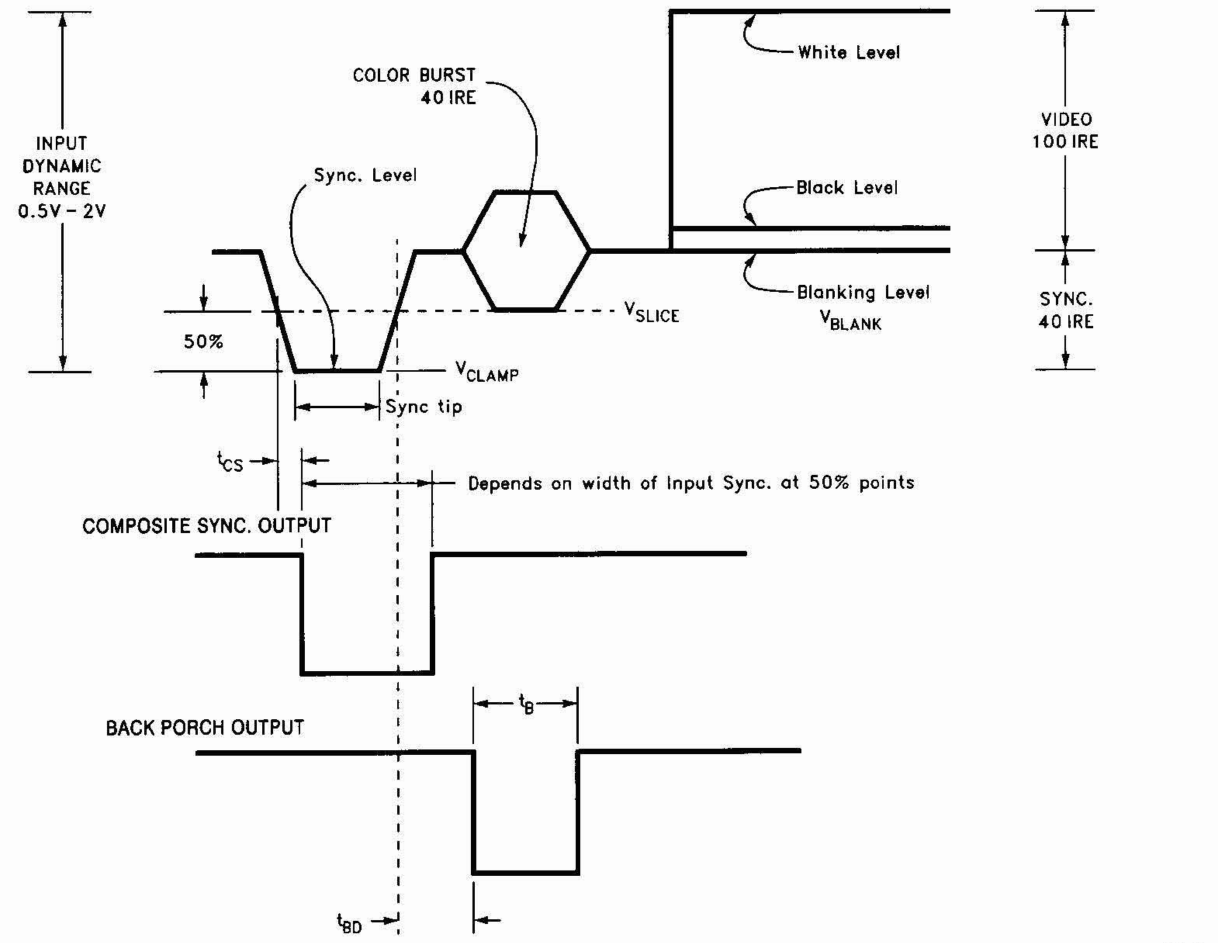

INPUT DYNAMIC RANGE 0.5V – 2V
COLOR BURST 40 IRE
Sync. Level
White Level
Black Level
Blanking Level V_{BLANK}
VIDEO 100 IRE
SYNC. 40 IRE
50%
V_{SLICE}
V_{CLAMP}
Sync tip
t_{CS}
Depends on width of Input Sync. at 50% points
COMPOSITE SYNC. OUTPUT
BACK PORCH OUTPUT
t_B
t_{BD}
4583-9

Figure 4. Standard (NTSC Input) H. Sync Detail

Description of Operation

A simplified block schematic is shown in Figure 1. The following description is intended to provide the user with sufficient information to be able to understand the effects that the external components and signal conditions have on the outputs of the integrated circuit.

The video signal is AC compuled to pin 4 via the capacitor C_1, nominally 0.1 μF. The clamp circcuit A1 will prevent the input signal on pin 4 going any more negative than 1.5V, the value of reference voltage V_{R1}. Thus the sync tip, the most negative part of the video waveform, will be clamped at 1.5V. The current source I_1, nominally 10 μA, charges the coupling capacitor during the remaining portion of the H line, approximately 58 μs for a 15.75 kHz timebase. From $I \bullet t = C \bullet V$, the video time-constant can be calculated. It is important to note that the charge taken from the capacitor during video must be replaced during the sync tip time, which is much shorter, (ratio of x 12.5). The corresponding current to restore the charge during sync will therefore be an order of magnitude higher, and any resistance in series with C_I will cause sync tip crushing. For this reason, the internal series resistance has been minimized and external high resistance values in series with the input coupling capacitor should be avoided. The user can exercise some control over the value of the input time constant by introducing an external pull-up resistance from pin 2 to the 5V supply. The maximum voltage across the resistance will be V_{DD} less 1.5V, for black level. For a net discharge current greater than zero, the resistance should be greater than 450k. This will have the effect of increasing the time constant and reducing the degree of picture tilt. The current source I_1 directly tracks reference current I_{TR} and thus increases with scan rate adjustment, as explained later.

The signal is processed through an active 3 pole filter (F1) designed for minimum ripple with constant phase delay. The filter attenuates the color burst by 24 dB and eliminates fast transient spikes without sync crushing. An external filter is not necessary. The filter also amplifies the video signal by 6 dB to improve the detection accuracy. The filter cut-off frequency is controlled by an external resistor from pin 1 to ground.

Internal reference voltages (block V_{REF}) with high immunity to supply voltage variation are derived on the chip. Reference V_{R4} with op-amp A2 forces pin 12 to a reference voltage of 1.7V nominal. Consequently, it can be seen that the external resistance RSET will determine the value of the reference current I_{TR}. The internal resistance R3 is only about 6 kΩ, much less than RSET. All the internal timing functions on the chip are referenced to I_{TR} and have excellent supply voltage rejection.

To improve noise immunity, the output of the 3 pole filter is brought out to pin 7. It is recommended to AC couple the output to pin 8, the video input pin. In case of strong clean video signal, the video input pin, pin 8, can be driven by the signal directly.

Comparator C2 on the input to the sample and hold block (S/H) compares the leading and trailing edges of the sync. pulse with a threshold voltage V_{R2} which is referenced at a fixed level above the clamp voltage V_{R1}. The output of C2 initiates the timing one-shots for gating the sample and hold circuits. The sample of the sync tip is delayed by 0.8 μs to enable the actual sample of 2 μs to be taken on the optimum section of the sync. pulse tip. The acquisition time of the circuit is about three horizontal lines. The double poly CMOS technology enables long time constants to be achieved with small high quality on-chip capacitors. The back porch voltage is similarly derived from the trailing edge of sync, which also serves to cut off the tip sample if the gate time exceeds the tip period. Note that the sample and hold gating times will track RSET through I_{OT}.

The 50% level of the sync tip is derived, through the resistor divided R1 and R2, from the sample and held voltages V_{TIP} and V_{BP}, and applied to the plus input of comparator C1. This comparator has built in hysteresis to avoid false triggering. The output of C2 is a digital 5V signal which feeds the C/S output buffer B1 and the other internal circuit blocks, the vertical, back porch and odd/even functions.

Description of Operation — Contd.

The vertical circuit senses the C/S edges and initiates an integrator which is reset by the shorter horizontal sync pulses but times out the longer vertical sync. pulse widths. The internal timing circuits are referenced to I_{OT} and V_{R3}, the timout period being inversely proportional to the timing current. The vertical output pulse is started on the first serration pulse in the vertical interval and is then self-timed out. In the absence of a serration pulse, an internal timer will default the start of vertical.

The Horizontal circuit senses the C/S edges and produces the true horizontal pulses of nominal width 5 μs. The leading edge is triggered from the leading edge of the input H sync, with the same prop. delay as the composite sync. The half line pulses present in the input signal during vertical blanking are eliminated with an internal 2 H eliminator circuit. The 2 H eliminator circuit initiates a time out period after a horizontal pulse if generated. The time out period is a function of I_{OT} which is set by RSET.

The back porch is triggered from the sync tip trailing edge and initiates a one-shot pulse. The period of this pulse is again a function of I_{OT} and will therefore track the scan rate set by RESET.

The odd/even circuit circuit (O/E) is comprised of flip flops which track the relationship of the horizontal pulses to the leading edge of the vertical output, and will switch on every field at the start of vertical. Pin 13 is high during the odd field.

Loss of video signal can be detected by monitoring the No Signal Detect Output pin 10. The VTIP voltage held by the sample and hold is compared with a voltage level set by RLV on pin 2. Pin 10 output goes high when the VTIP falls below RLV set value.

VTIP voltage is also passed through an amplifier with gain of 2 and buffed to pin 9. This is done to provide an indication of signal strength. The Level Output signal can be used for AGC applications.

Block Diagram

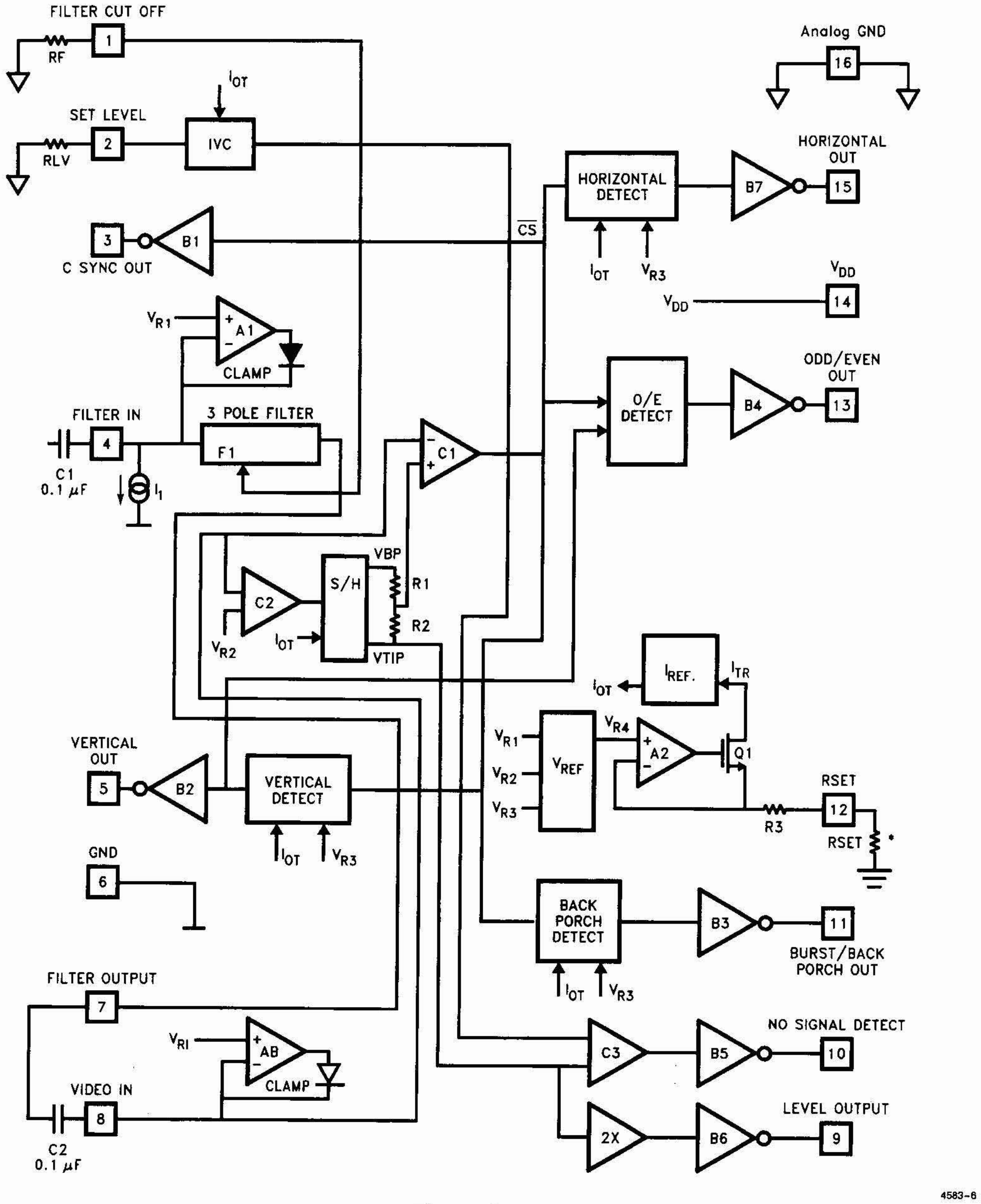

FILTER CUT OFF
RF
1
SET LEVEL
RLV
2
IOT
IVC
3
B1
C SYNC OUT
VR1
A1
CLAMP
FILTER IN
4
C1
0.1 μF
I1
3 POLE FILTER
F1
C1
VBP
S/H
R1
R2
C2
VR2
IOT
VTIP
VERTICAL OUT
5
B2
VERTICAL DETECT
IOT
VR3
GND
6
FILTER OUTPUT
7
VRI
AB
CLAMP
VIDEO IN
8
C2
0.1 μF
Analog GND
16
HORIZONTAL OUT
HORIZONTAL DETECT
B7
15
CS
IOT
VR3
VDD
VDD
14
ODD/EVEN OUT
O/E DETECT
B4
13
IREF.
ITR
IOT
VR4
VR1
VR2
VR3
VREF
A2
Q1
R3
RSET
12
RSET
*
BACK PORCH DETECT
B3
11
BURST/BACK PORCH OUT
IOT
VR3
C3
B5
NO SIGNAL DETECT
10
2X
B6
LEVEL OUTPUT
9
4583-6

Figure 5

* Note: RSET must be a 1% resistor

elantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4584C
Horizontal Genlock, 4 F_{SC}

Features

- 36 MHz, general purpose PLL
- 4 F_{SC} based timing (use the EL4585 for 8 F_{SC})
- Compatible w/EL4583 Sync Separator
- VCXO, Xtal, or LC tank oscillator
- <2 ns jitter (VCXO)
- User controlled PLL capture and lock
- Compatible with NTSC and PAL TV formats
- 8 pre-programmed TV scan rate clock divisors
- Selectable external divide for custom ratios
- Single 5V, low current operation

Applications

- Pixel Clock regeneration
- Video compression engine (MPEG) clock generator
- Video capture or digitization
- PIP (Picture in Picture) timing generator
- Text or graphics overlay timing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4584CN	-40°C to +85°C	16-Pin DIP	MDP0031
EL4584CS	-40°C to +85°C	16-Lead SO	MDP0027

For 6Fsc and 8Fsc clock frequencies, see EL4585 datasheet.

Demo Board

A demo PCB is available for this product. Request "EL4584/5 Demo Board".

General Description

The EL4584C is a PLL (Phase Lock Loop) sub system, designed for video applications but also suitable for general purpose use up to 36 MHz. In a video application this device generates a TTL/CMOS compatible Pixel Clock (Clk Out) which is a multiple of the TV Horizontal scan rate, and phase locked to it.

The reference signal is a horizontal sync signal, TTL/CMOS format, which can be easily derived from an analog composite video signal with the EL4583 Sync Separator. An input signal to "coast" is provided for applications were periodic disturbances are present in the reference video timing such as VTR head switching. The Lock detector output indicates correct lock.

The divider ratio is four ratios for NTSC and four similar ratios for the PAL video timing standards, by external selection of three control pins. These four ratios have been selected for common video applications including 4 F_{SC}, 3 F_{SC}, 13.5 MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate 8 F_{SC}, 6 F_{SC}, 27 MHz (CCIR 601 format) etc. use the EL4585, which includes an additional divide by 2 stage.

For applications where these frequencies are inappropriate or for general purpose PLL applications the internal divider can be bypassed and an external divider chain used.

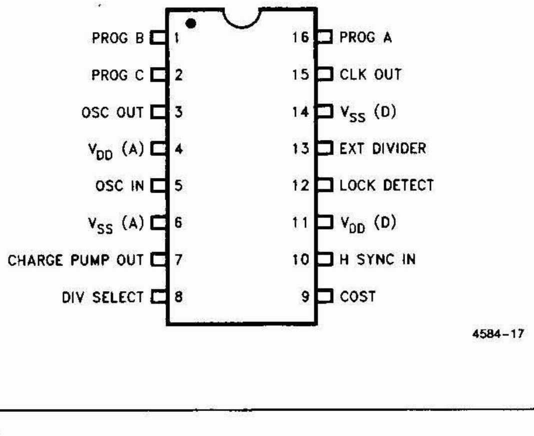
FREQUENCIES and DIVISORS

Function	3Fsc	CCIR 601	Square	4Fsc
Divisor	851	864	944	1135
PAL Fosc (MHz)	13.301	13.5	14.75	17.734
Divisor	682	858	780	910
NTSC Fosc (MHz)	10.738	13.5	12.273	14.318

CCIR 601 Divisors yield 720 pixels in the portion of each line for NTSC and PAL.
Square pixels format gives 640 pixels for NTSC and 768 pixels for PAL in the active portion.
3Fsc numbers do not yield integer divisors.

Connection Diagram

EL4584 SO, P-DIP Packages



EL4584C

Horizontal Genlock, 4 F_{SC}

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Operating Junction Temp	125°C
Storage Temperature	−65°C to +150°C	Power Dissipation	400 mW
Lead Temperature	260°C	Oscillator Frequency	36 MHz
Pin Voltages	−0.5V to V_{CC}+0.5V		
Operating Ambient Temperature Range	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Test Level	Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C		2	4	I	mA
V_{IL} Input Low Voltage		25°C			1.5	I	V
V_{IH} Input High Voltage		25°C	3.5			I	V
I_{IL} Input Low Current	All inputs except COAST, V_{IN} = 1.5V	25°C	−100			I	nA
I_{IH} Input High Current	All inputs except COAST, V_{IN} = 3.5V	25°C			100	I	nA
I_{IL} Input Low Current	COAST pin, V_{IN} = 1.5V	25°C	−100	−60		I	µA
I_{IH} Input High Current	COAST pin, V_{IN} = 3.5V	25°C		60	100	I	µA
V_{OL} Output Low Voltage	Lock Det, I_{OL} = 1.6mA	25°C			0.4	I	V
V_{OH} Output High Voltage	Lock Det, I_{OH} = −1.6mA	25°C	2.4			I	V
V_{OL} Output Low Voltage	CLK, I_{OL} = 3.2mA	25°C			0.4	I	V
V_{OH} Output High Voltage	CLK, I_{OH} = −3.2mA	25°C	2.4			I	V
V_{OL} Output Low Voltage	OSC Out, I_{OL} = 200µA	25°C			0.4	I	V
V_{OH} Output High Voltage	OSC Out, I_{OH} = −200µA	25°C	2.4			I	V
I_{OL} Output Low Current	Filter Out, V_{OUT} = 2.5V	25°C	200	300		I	µA
I_{OH} Output High Current	Filter Out, V_{OUT} = 2.5V	25°C		−300	−200	I	µA
I_{OL}/I_{OH} Current Ratio	Filter Out, V_{OUT} = 2.5V	25°C	1.05	1.0	0.95	I	
I_{LEAK} Filter Out	Coast Mode, $V_{DD} > V_{OUT} > 0V$	25°C	−100	±1	100	I	nA

Note 1: All inputs to 0V, COAST floating.

EL4584C

Horizontal Genlock, 4 F_{SC}

AC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Test Level	Units
VCO Gain @ 20 MHz	Test Circuit 1	25°C		15.5		V	dB
H-sync S/N Ratio	V_{DD} = 5V (Note 2)	25°C	35			V	dB
Jitter	VCXO Oscillator	25°C		1		V	ns
Jitter	LC Oscillator (Typ)	25°C		10		V	ns

Note 2: Noisy video signal input to EL4583C, H-sync input to EL4584C. Test for positive signal lock.

Pin Description

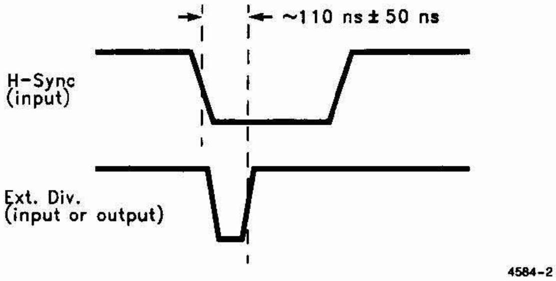
Pin No.	Pin Name	Function
16,1,2	Prog A,B,C	Digital inputs to select ÷ N value for internal counter. See table below for values.
3	Osc/VCO Out	Output of internal inverter/oscillator. Connect to external crystal or LC tank VCO circuit.
4	V_{DD} (A)	Analog positive supply for oscillator, PLL circuits.
5	Osc/VCO In	Input from external VCO.
6	V_{SS} (A)	Analog ground for oscillator, PLL circuits.
7	Charge Pump Out	Connect to loop filter. If the H-sync phase is leading or H-sync frequency > CLK ÷ N, current is pumped into the filter capacitor to increase VCO frequency. If H-sync phase is lagging or frequency < CLK ÷ N, current is pumped out of the filter capacitor to decrease VCO frequency. During coast mode or when locked, charge pump goes to a high impedance state.
8	Div Select	Divide select input. When high, the internal divider is enabled and EXT DIV becomes a test pin, outputting CLK ÷ N. When low, the internal divider is disabled and EXT DIV is an input from an external ÷ N.
9	Coast	Tri-state logic input. Low($<\frac{1}{3}*V_{CC}$) = normal mode, Hi Z(or ⅓ to ⅔$*V_{CC}$) = fast lock mode, High($>\frac{2}{3}*V_{CC}$) = coast mode.
10	H-sync In	Horizontal sync pulse (CMOS level) input.
11	V_{DD} (D)	Positive supply for digital, I/O circuits.
12	Lock Det	Lock Detect output. Low level when PLL is locked. Pulses high when out of lock.
13	Ext Div	External Divide input when DIV SEL is low, internal ÷ N output when DIV SEL is high.
14	V_{SS} (D)	Ground for digital, I/O circuits.
15	CLK Out	Buffered output of the VCO.

VCO Divisors Table 1

Prog A Pin 16	Prog B Pin 1	Prog C Pin 2	Div Value N
0	0	0	851
0	0	1	864
0	1	0	944
0	1	1	1135
1	0	0	682
1	0	1	858
1	1	0	780
1	1	1	910

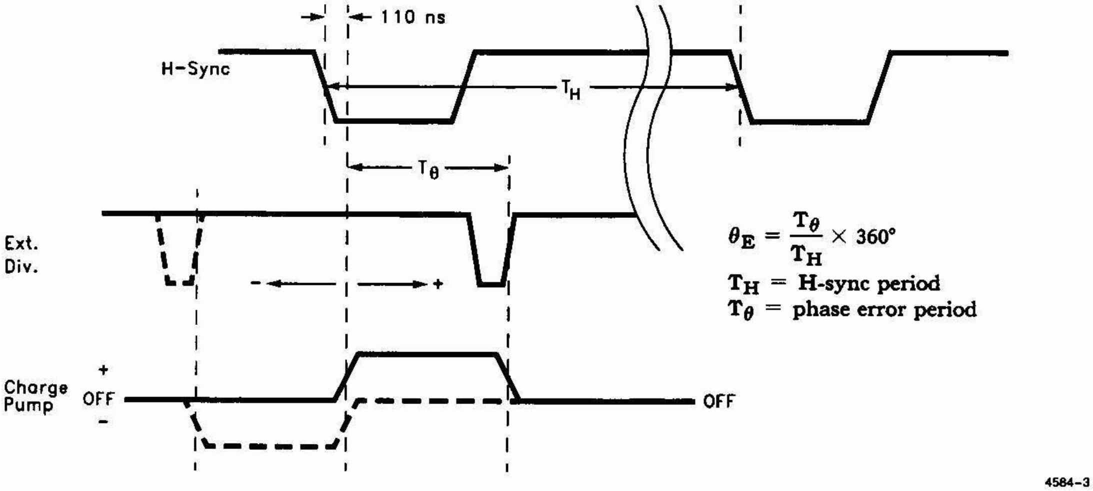
Timing Diagrams

PLL Locked Condition (Phase Error = 0)


~110 ns ± 50 ns
H-Sync (input)
Ext. Div. (input or output)
4584-2

Falling edge of H-sync + 110 ns locks to rising edge of Ext Div signal.

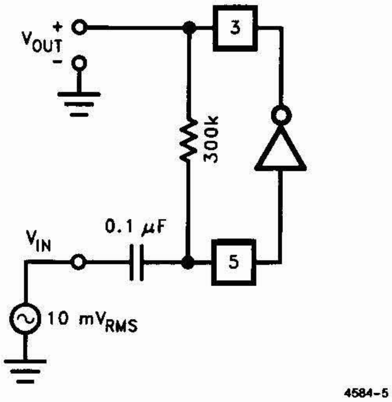
Out of Lock Condition


110 ns
H-Sync
T_H
T_θ
Ext. Div.
+
Charge Pump
+
OFF
-
OFF
4584-3

$$\theta_E = \frac{T_\theta}{T_H} \times 360°$$

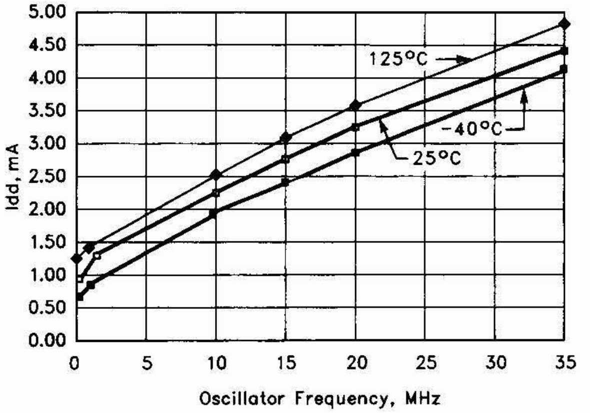
T_H = H-sync period
T_θ = phase error period

Test Circuit 1


V_{OUT}
+
-
3
300k
0.1 µF
V_{IN}
5
10 mV_{RMS}
4584-5

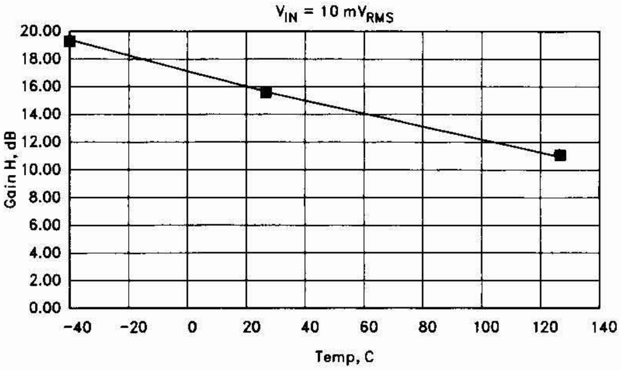
Typical Performance Curves

Idd vs Fosc



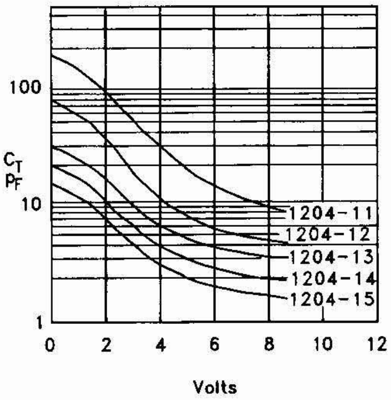
4584-4

4584 OSC Gain @ 20 MHz vs Temp



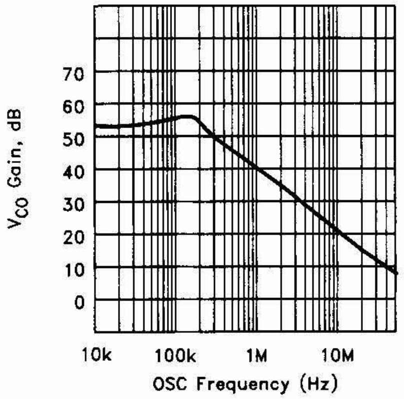
4584-6

Typical Varactor



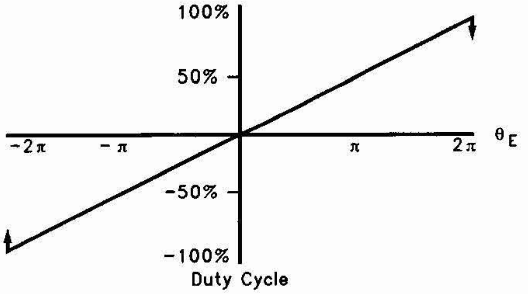
4584-7

OSC Gain vs Fosc



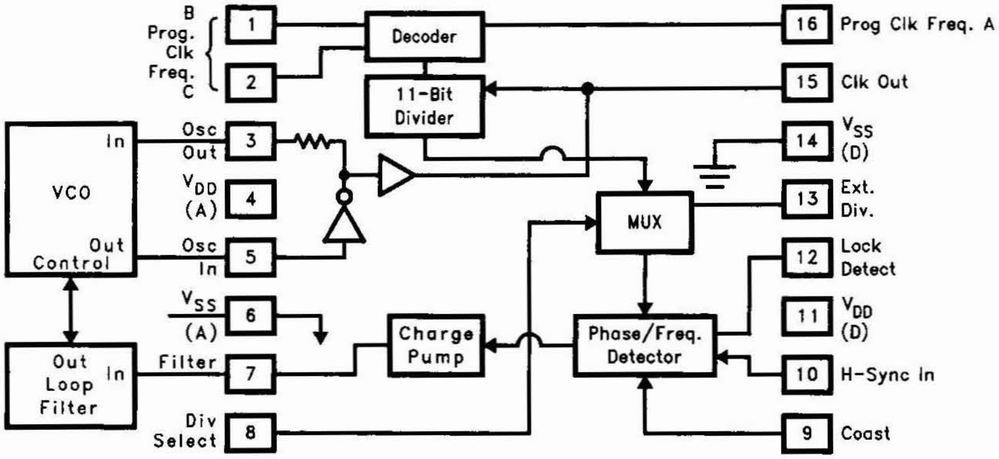
4584-8

Charge Pump Duty Cycle vs θ_E



4584-9

Block Diagram


B
Prog.
Clk
Freq.
C
1
2
Decoder
11-Bit
Divider
16
Prog Clk Freq. A
15
Clk Out
VCO
In
Out
Control
Osc
Out
3
V_{DD}
(A)
4
Osc
In
5
V_{SS}
(A)
6
14
V_{SS}
(D)
13
Ext.
Div.
MUX
12
Lock
Detect
11
V_{DD}
(D)
Charge
Pump
Phase/Freq.
Detector
Out
Loop
Filter
In
Filter
7
10
H-Sync In
Div
Select
8
9
Coast

4584-1

Description Of Operation

The horizontal sync signal (CMOS level, falling leading edge) is input to H-sync input (pin 10). This signal is delayed about 110 ns, the falling edge of which becomes the reference to which the clock output will be locked. (See timing diagrams.) The clock is generated by the signal on pin 5, OSC in. There are 2 general types of VCO that can be used with the EL4584C, LC and crystal controlled. Additionally, each type can be either built up using discrete components, including a varactor as the frequency controlling element, or complete, self contained modules can be purchased with everything inside a metal can. The modules are very forgiving of PCB layout, but cost more than discrete solutions. The VCO or VCXO is used to generate the clock. An LC tank resonator has greater "pull" than a crystal controlled circuit, but will also be more likely to drift over time, and thus will generate more jitter. The "pullability" of the circuit refers to the ability to "pull" the frequency of oscillation away from its center frequency by modulating the voltage on the control pin of a VCO module or varactor, and is a function of the slope and range of the capacitance-voltage curve of the varactor or VCO module used. The VCO signal is sent to a divide by N counter, and to the CLK out pin. The divisor N is determined by the state of pins 1,2, and 16 and is described in table 1 above. The divided signal is sent, along with the delayed H-sync input, to the phase/frequency detector, which compares the two signals for phase and frequency differences. Any phase difference is converted to a current at the charge pump output FILTER (pin 7). A VCO with positive frequency deviation with control voltage must be used. Varactors have negative capacitance slope with voltage, resulting in positive frequency deviation with control voltage for the oscillators in figures 10 and 11 below.

VCO

The VCO should be tuned so its frequency of oscillation is very close to the required clock output frequency when the voltage on the varactor is 2.5 volts. VCXO and VCO modules are already tuned to the desired frequency, so this step is not necessary if using one of these units. The range of the charge pump output (pin 7) is 0 to 5 volts and it can source or sink a maximum of about 300 μA, so all frequency control must be accomplished with variable capacitance from the varactor within this range. Crystal oscillators are more stable than LC oscillators, which translates into lower jitter, but LC oscillators can be pulled from their mid-point values further, resulting in a greater capture and locking range. If the incoming horizontal sync signal is known to be very stable, then a crystal oscillator circuit can be used. If the h-sync signal experiences frequency variations of greater than about 300 ppm, an LC oscillator should be considered, as crystal oscillators are very difficult to pull this far. When H-SYNC input frequency is greater than CLK frequency ÷ N, charge pump output (pin 7) sources current into the filter capacitor, increasing the voltage across the varactor, which lowers its capacitance, thus tending to increase VCO frequency. Conversely, filter output pulls current from the filter capacitor when H-SYNC frequency is less than CLK ÷ N, forcing the VCO frequency lower.

Loop Filter

The loop filter controls how fast the VCO will respond to a change in filter output stimulus. Its components should be chosen so that fast lock can be achieved, yet with a minimum of VCO "hunting", preferably in one to two oscillations of charge pump output, assuming the VCO frequency starts within capture range. If the filter is under-damped, the VCO will over and undershoot the desired operating point many times before a stable lock takes place. It is possible to under-damp the filter so much that the loop itself oscillates, and VCO lock is never achieved. If the filter is over-damped, the VCO response time will be excessive and many cycles will be required for a lock condition. Over-damping is also characterized by an easily unlocked system because the filter can't respond fast enough to perturbations in VCO frequency. A severely over damped system will seem to endlessly oscillate, like a very large mass at the end of a long pendulum. Due to parasitic effects of PCB traces and component variables, it will take some trial and error experimentation to determine the best values to use for any given situation. Use the component tables as a starting point, but be aware that deviation from these values is not out of the ordinary.

Description of Operation — Contd.

External Divide

DIV SEL (pin 8) controls the use of the internal divider. When high, the internal divider is enabled and EXT DIV (pin 13) outputs the CLK out divided by N. This is the signal to which the horizontal sync input will lock. When divide select is low, the internal divider output is disabled, and external divide becomes an input from an external divider, so that a divisor other than one of the 8 pre-programmed internal divisors can be used.

Normal Mode

Normal mode is enabled by pulling COAST (pin 9) low (below $\frac{1}{3}*V_{CC}$). If H-sync and CLK ÷ N have any phase or frequency difference, an error signal is generated and sent to the charge pump. The charge pump will either force current into or out of the filter capacitor in an attempt to modulate the VCO frequency. Modulation will continue until the phase and frequency of CLK ÷ N exactly match the H-sync input. When the phase and frequency match (with some offset in phase that is a function of the VCO characteristics), the error signal goes to zero, lock detect no longer pulses high, and the charge pump enters a high impedance state. The clock is now locked to the H-sync input. As long as phase and frequency differences remain small, the PLL can adjust the VCO to remain locked and lock detect remains low.

Fast Lock Mode

Fast Lock mode is enabled by either allowing coast to float, or pulling it to mid supply (between $\frac{1}{3}$ and $\frac{2}{3}*V_{CC}$). In this mode, lock is achieved much faster than in normal mode, but the clock divisor is modified on the fly to achieve this. If the phase detector detects an error of enough magnitude, the clock is either inhibited or reset to attempt a "fast" lock of the signals. Forcing the clock to be synchronized to the H-sync input this way allows a lock in approximately 2 H-cycles, but the clock spacing will not be regular during this time. Once the near lock condition is attained, charge pump output should be very close to its lock-on value and placing the device into normal mode should result in a normal lock very quickly. Fast Lock mode is intended to be used where H-sync becomes irregular, until a stable signal is again obtained.

Coast Mode

Coast mode is enabled by pulling COAST (pin 9) high (above $\frac{2}{3}*V_{CC}$). In coast mode the internal phase detector is disabled and filter out remains in high impedance mode to keep filter out voltage and VCO frequency as constant a possible. VCO frequency will drift as charge leaks from the filter capacitor, and the voltage changes the VCO operating point. Coast mode is intended to be used when noise or signal degradation result in loss of horizontal sync for many cycles. The phase detector will not attempt to adjust to the resultant loss of signal so that when horizontal sync returns, sync lock can be re-established quickly. However, if much VCO drift has occurred, it may take as long to re-lock as when restarting.

Lock Detect

Lock detect (pin 12) will go low when lock is established. Any DC current path from charge pump out will skew EXT DIV relative to H-SYNC in, tending to offset or add to the 110 ns internal delay, depending on which way the extra current is flowing. This offset is called static phase error, and is always present in any PLL system. If, when the part stabilizes in a locked mode, lock detect is not low, adding or subtracting from the loop filter series resistor R_2 will change this static phase error to allow LDET to go low while in lock. The goal is to put the rising edge of EXT DIV in sync with the falling edge of H-SYNC + 110 ns. (See timing diagrams.) Increasing R_2 decreases phase error, while decreasing R_2 increases phase error. (Phase error is positive when EXT DIV lags H-SYNC.) The resistance needed will depend on VCO design or VCXO module selection.

Applications Information

Choosing External Components

1. To choose LC VCO components, first pick the desired operating frequency. For our example we will use 14.31818 MHz, with an H-sync frequency of 15.734 kHz.
2. Choose a reasonable inductor value (10–20μH works well). We choose 15 μH.
3. Calculate C_T needed to produce F_{OSC}.

$$F_{OSC} = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{1}{4\pi^2 F^2 L} = \frac{1}{4\pi^2(14.318e6)^2(15e-6)} = 8.2\text{ pF}$$

4. From the varactor data sheet find C_V @ 2.5V, the desired lock voltage. $C_V = 23$ pF for our SMV1204-12, for example.
5. C_2 should be about $10C_V$, so we choose $C_2 = 220$ pF for our example.
6. Calculate C_1. Since

$$C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)},$$

then

$$C_1 = \frac{C_2C_TC_V}{(C_2C_V) - (C_2C_T) - (C_TC_V)}.$$

For our example, $C_1 = 14$ pF. (A trim cap may be used for fine tuning.) Examples for each frequency using the internal divider follow.

Typical LC VCO

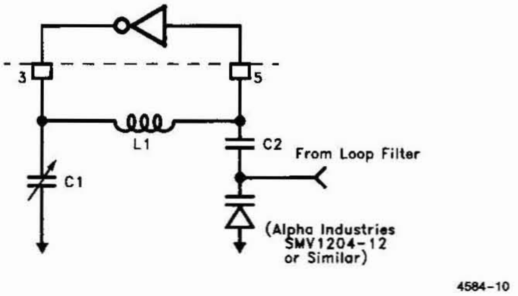

3
5
L1
C2
From Loop Filter
C1
(Alpha Industries SMV1204-12 or Similar)
4584-10

Figure 10

LC VCO Component Values (Approximate)

Frequency (MHz)	L1 (μH)	C1 (pF)	C2 (pF)
13.301	15	18	220
13.5	15	17	220
14.75	12	18	220
17.734	12	10	220
10.738	22	20	220
12.273	18	17	220
14.318	15	14	220

Note: Use shielded inductors for optimum performance.

Typical Xtal VCO

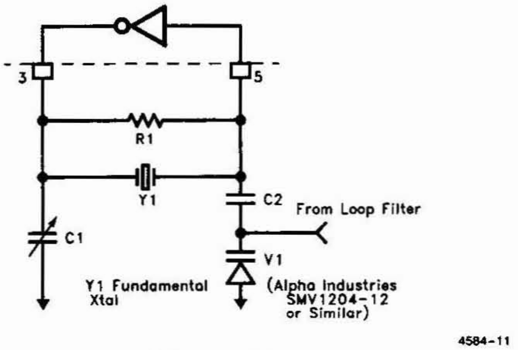
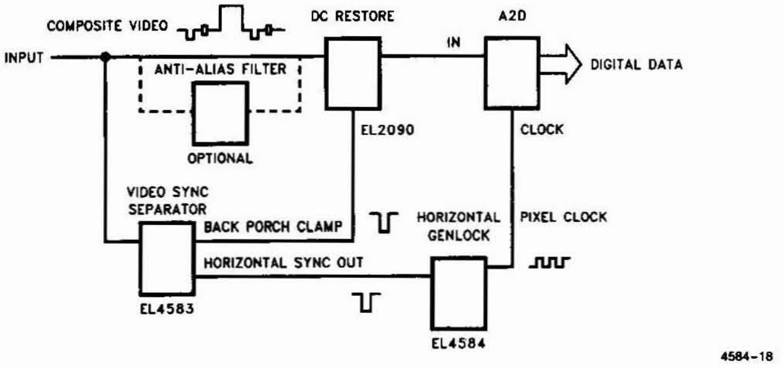

3
5
R1
Y1
C2
From Loop Filter
C1
V1
Y1 Fundamental Xtal
(Alpha Industries SMV1204-12 or Similar)
4584-11

Figure 11

Typical Application

Horizontal genlock provides clock for an analog to digital converter, digitizing analog video.

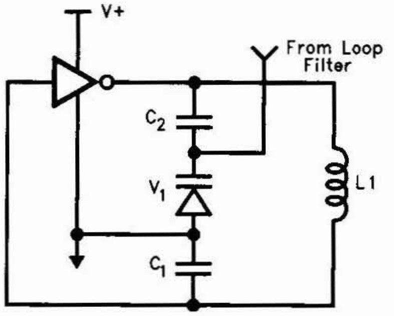

COMPOSITE VIDEO
INPUT
DC RESTORE
A2D
IN
DIGITAL DATA
ANTI-ALIAS FILTER
OPTIONAL
EL2090
CLOCK
VIDEO SYNC SEPARATOR
BACK PORCH CLAMP
HORIZONTAL GENLOCK
PIXEL CLOCK
HORIZONTAL SYNC OUT
EL4583
EL4584
4584-18

Xtal VCO Component Values (Approximate)

Frequency (MHz)	R1 (kΩ)	C1 (pF)	C2 (uF)
13.301	300	15	.001
13.5	300	15	.001
14.75	300	15	.001
17.734	300	15	.001
10.738	300	15	.001
12.273	300	15	.001
14.318	300	15	.001

The above oscillators are arranged as Colpitts oscillators, and the structure is redrawn here to emphasize the split capacitance used in a Colpitts oscillator. It should be noted that this oscillator configuration is just one of literally hundreds possible, and the configuration shown here does not necessarily represent the best solution for all applications. Crystal manufacturers are very informative sources on the design and use of oscillators in a wide variety of applications, and the reader is encouraged to become familiar with them.

Colpitts Oscillator



4584-12

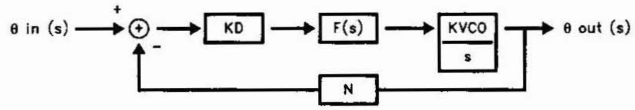
C_1 is to adjust the center frequency, C_2 DC isolates the control from the oscillator, and V1 is the primary control device. C_2 should be much larger than C_V so that V_1 has maximum modulation capability. The frequency of oscillation is given by:

$$F = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)}$$

Choosing Loop Filter Components

The PLL, VCO, and loop filter can be described as:



4584-13

Where:

K_d = phase detector gain in A/rad

F(s) = loop filter impedance in V/A

K_{VCO} = VCO gain in rad/s/V

N = internal or external divisor

It can be shown that for the loop filter shown below:

$$C_3 = \frac{K_dK_{VCO}}{N\omega_n^2}, C_4 = \frac{C_3}{10}, R_3 = \frac{2N\zeta\omega_n}{K_dK_{VCO}}$$

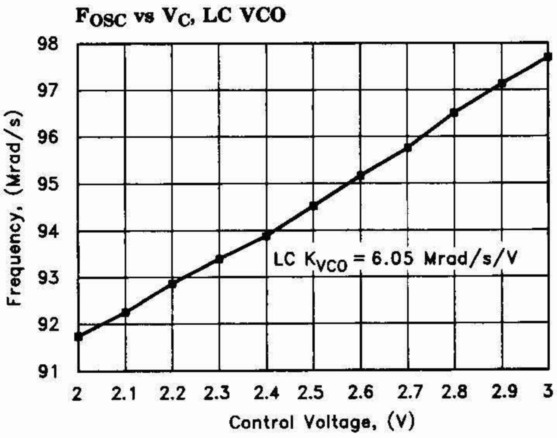
Where ω_n = loop filter bandwidth, and ζ = loop filter damping factor.

1. $K_d = 300\ \mu A/2\pi rad = 4.77e\text{-}5 A/rad$ for the EL4584C.
2. The loop bandwidth should be about H-sync frequency/20, and the damping ratio should be 1 for optimum performance. For our example, $\omega_n = 15.734\ kHz/20 = 787\ Hz \approx 5000\ rad/S$.
3. N = 910 from table 1.

$$N = \frac{\text{VCOfrequency}}{\text{H-SYNCfrequency}} = \frac{14.31818M}{15.73426k} = 910$$

4. K_{VCO} represents how much the VCO frequency changes for each volt applied at the control pin. It is assumed (but probably isn't) linear about the lock point (2.5V). Its value depends on the VCO configuration and the varactor

transfer function $C_V = F(V_C)$, where V_C is the reverse bias control voltage, and C_V is varactor capacitance. Since $F(V_C)$ is nonlinear, it is probably best to build the VCO and measure K_{VCO} about 2.5V. The results of one such measurement are shown below. The slope of the curve is determined by linear regression techniques and equals K_{VCO}. For our example, K_{VCO} = 6.05 Mrad/S/V.



4584-14

5. Now we can solve for C_3, C_4, and R_3.

$$C_3 = \frac{K_d K_{VCO}}{N\omega^2{}_n} = \frac{(4.77e-5)(6.05e6)}{(910)(5000)^2} = 0.01\ \mu F$$

$$C_4 = \frac{C_3}{10} = 0.001\ \mu F$$

$$R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}} = \frac{(2)(910)(1)(5000)}{(4.77e-5)(6.05e6)} = 31.5\ k\Omega$$

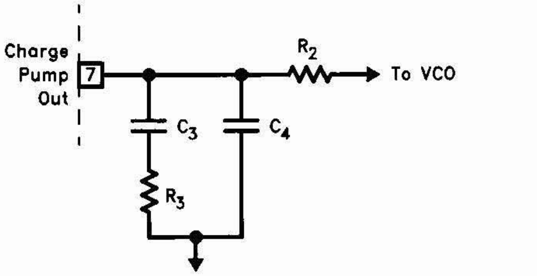
We choose $R_3 = 30\ k\Omega$ for convenience.

6. Notice R_2 has little effect on the loop filter design. R_2 should be large, around 100k, and can be adjusted to compensate for any static phase error T_θ at lock, but if made too large, will slow loop response. If R_2 is made smaller, T_θ (see timing diagrams) increases, and if R_2 increases, T_θ decreases. For LDET to be low at lock, $|T_\theta| < 50$ ns. C_4 is used mainly to attenuate high frequency noise from the charge pump.

Lock Time

Let $T = R_3C_3$. As T increases, damping increases, but so does lock time. Decreasing T decreases damping and speeds up loop response, but increases overshoot and thus increases the number of hunting oscillations before lock. Critical damping ($\zeta = 1$) occurs at minimum lock time. Because decreased damping also decreases loop stability, it is sometimes desirable to design slightly overdamped ($\zeta > 1$), trading lock time for increased stability.

Typical Loop Filter



4584-16

LC Loop Filter Components (Approximate)

Frequency (MHz)	R2 (kΩ)	R3 (kΩ)	C3 (μF)	C4 (μF)
13.301	100	30	0.01	0.001
13.5	100	30	0.01	0.001
14.75	100	33	0.01	0.001
17.734	100	39	0.01	0.001
10.738	100	22	0.01	0.001
12.273	100	27	0.01	0.001
14.318	100	30	0.01	0.001

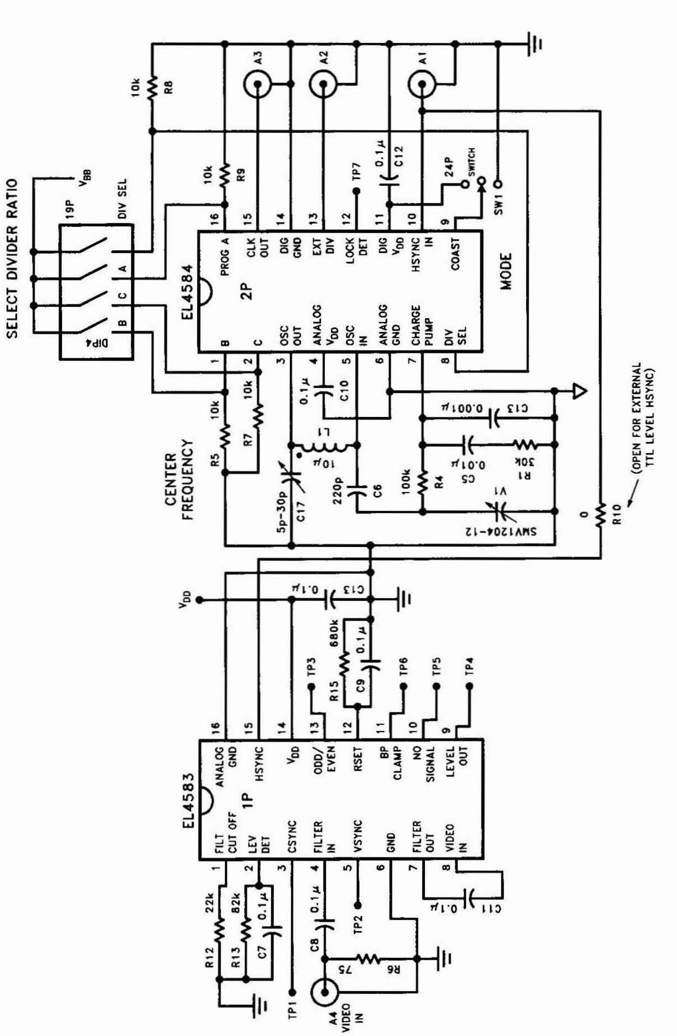
Xtal Loop Filter Components (Approximate)

Frequency (MHz)	R2 (kΩ)	R3 (MΩ)	C3 (pF)	C4 (pF)
13.301	100	4.3	68	6.8
13.5	100	4.3	68	6.8
14.75	100	4.3	68	6.8
17.734	100	4.3	68	6.8
10.738	100	4.3	68	6.8
12.273	100	4.3	68	6.8
14.318	100	4.3	68	6.8

PCB Layout Considerations

It is highly recommended that power and ground planes be used in layout. The oscillator and filter sections constitute a feedback loop and thus care must be taken to avoid any feedback signal influencing the oscillator except at the control input. The entire oscillator/filter section should be surrounded by copper ground to prevent unwanted influences from nearby signals. Use separate paths for analog and digital supplies, keeping the analog (oscillator section) as short and free from spurious signals as possible. Careful attention must be paid to correct bypassing. Keep lead lengths short and place bypass caps as close to the supply pins as possible. If laying out a PCB to use discrete components for the VCO section, care must be taken to avoid parasitic capacitance at the OSC pins 3 and 5, and FILTER out (pin 7). Remove ground and power plane copper above and below these traces to avoid making a capacitive connection to them. It is also recommended to enclose the oscillator section within a shielded cage to reduce external influences on the VCO, as they tend to be very sensitive to "hand-waving" influences, the LC variety being more sensitive than crystal controlled oscillators. In general, the higher the operating frequency, the more important these considerations are. Self contained VCXO or VCO modules are already mounted in a shielding cage and therefore do not require as much consideration in layout. Many crystal manufacturers publish informative literature regarding use and layout of oscillators which should be helpful.

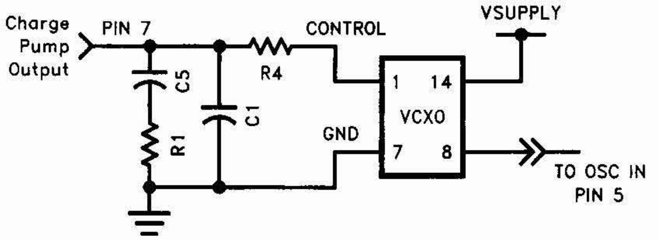
Demo Board


SELECT DIVIDER RATIO
DIP4
19P
V_{BB}
DIV SEL
B
C
A
CENTER FREQUENCY
R5
10k
R7
10k
EL4584
2P
B
C
OSC OUT
ANALOG V_{DD}
OSC IN
ANALOG GND
CHARGE PUMP
DIV SEL
PROG A
CLK OUT
DIG GND
EXT DIV
LOCK DET
DIG V_{DD}
HSYNC IN
COAST
MODE
R9
10k
R8
10k
A3
A2
A1
TP7
C12
0.1µ
24P
SWITCH
SW1
5p–30p
C17
10µ
L1
0.1µ
C10
220p
C6
100k
R4
C5
0.01µ
R1
30k
C13
0.001µ
V1
SMV1204–12
R10
0
(OPEN FOR EXTERNAL TTL LEVEL HSYNC)
V_{DD}
C13
0.1µ
R15
680k
C9
0.1µ
TP3
TP6
TP5
TP4
EL4583
1P
FILT CUT OFF
LEV DET
CSYNC
FILTER IN
VSYNC
GND
FILTER OUT
VIDEO IN
ANALOG GND
HSYNC
V_{DD}
ODD/ EVEN
RSET
BP CLAMP
NO SIGNAL
LEVEL OUT
R12
22k
R13
82k
C7
0.1µ
TP1
C8
0.1µ
TP2
75
R6
A4 VIDEO IN
C11
0.1µ

4584-19

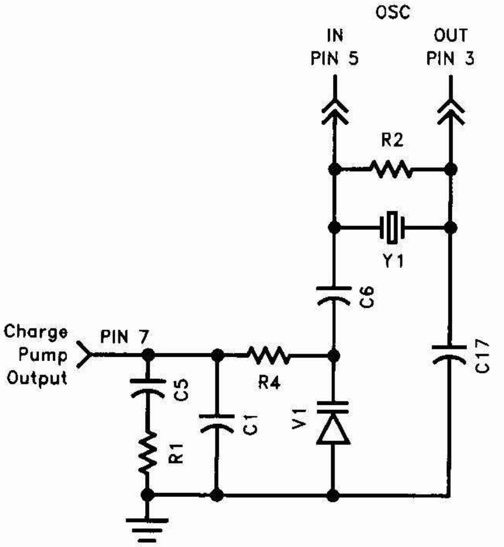
The VCO and loop filter section of the EL4583/4/5 demo board can be implemented in the following configurations:

(1) VCXO


Charge Pump Output
PIN 7
C5
R1
C1
R4
CONTROL
GND
VSUPPLY
1
14
VCXO
7
8
TO OSC IN PIN 5

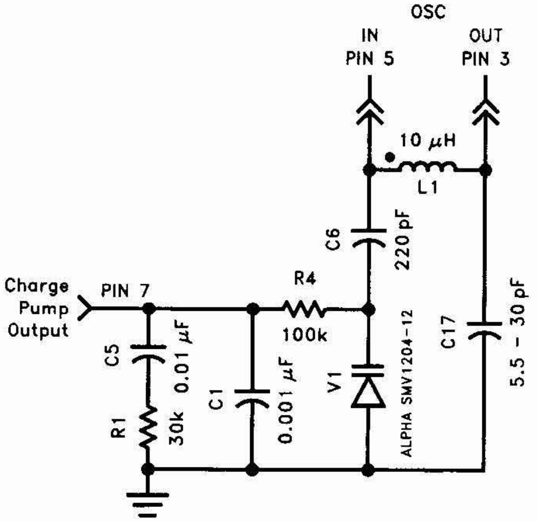
4584-20

(2) XTAL


OSC
IN PIN 5
OUT PIN 3
R2
Y1
C6
C17
Charge Pump Output
PIN 7
C5
R1
C1
R4
V1

4584-21

(3) LC Tank


OSC
IN PIN 5
OUT PIN 3
10 μH
L1
C6
220 pF
C17
5.5 - 30 pF
Charge Pump Output
PIN 7
R4
100k
C5
0.01 μF
R1
30k
C1
0.001 μF
V1
ALPHA SMV1204-12

4584-22

Component Sources

Inductors

- Dale Electronics
  E. Highway 50
  PO Box 180
  Yankton, SD 57078-0180
  (605) 665-9301

Crystals, VCXO, VCO Modules

- Connor-Winfield
  2111 Comprehensive Drive
  Aurora, IL 60606
  (708) 851-4722

- Piezo Systems
  100 K Street
  PO Box 619
  Carlisle, PA 17013
  (717) 249-2151

- Reeves-Hoffman
  400 West North Street
  Carlisle, PA 17013
  (717) 243-5929

- SaRonix
  151 Laura Lane
  Palo Alto, CA 94043
  (415) 856-6900

- Standard Crystal
  9940 Baldwin Place
  El Monte, CA 91731
  (818) 443-2121

Varactors

- Alpha Industries
  20 Sylvan Road
  Woburn, MA 01801
  (617) 935-5150

- Motorola Semiconductor Products
  2100 E. Elliot
  Tempe, AZ 85284
  (602) 244-6900

Note: These sources are provided for information purposes only. No endorsement of these companies is implied by this listing.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4585C
Horizontal Genlock, 8 F_{SC}

Features

- 36 MHz, general purpose PLL
- 8 F_{SC} timing. (Use the EL4584 for 4 F_{SC})
- Compatible with EL4583C Sync Separator
- VCXO, Xtal, or LC tank oscillator
- <2nS jitter (VCXO)
- User-controlled PLL capture and lock
- Compatible with NTSC and PAL TV formats
- 8 pre-programmed popular TV scan rate clock divisors
- Single 5V, low current operation

Applications

- Pixel Clock regeneration
- Video compression engine (MPEG) clock generator
- Video Capture or digitization
- PIP (Picture In Picture) timing generator
- Text or Graphics overlay timing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4585CN	−40°C to +85°C	16-Pin DIP	MDP0031
EL4585CS	−40°C to +85°C	16-Lead SO	MDP0027

For 3Fsc and 4Fsc clock frequency operation, see EL4584 datasheet.

Demo Board

A demo PCB is available for this product. Request "EL4584/5 Demo Board".

General Description

The EL4585C is a PLL (Phase Lock Loop) sub system, designed for video applications, but also suitable for general purpose use up to 36 MHz. In a video application this device generates a TTL/CMOS compatible Pixel Clock (Clk Out) which is a multiple of the TV Horizontal scan rate, and phase locked to it.

The reference signal is a horizontal sync signal, TTL/CMOS format, which can be easily derived from an analog composite video signal with the EL4583 Sync Separator. An input signal to "coast" is provided for applications where periodic disturbances are present in the reference video timing such as VTR head switching. The Lock detector output indicates correct lock.

The divider ratio is four ratios for NTSC and four similar ratios for the PAL video timing standards, by external selection of three control pins. These four ratios have been selected for common video applications including 8 F_{SC}, 6 F_{SC}, 27 MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate 4 F_{SC}, 3 F_{SC}, 13.5 MHz (CCIR 601 format) etc., use the EL4584, which does not have the additional divide by 2 stage of the EL4585.

For applications where these frequencies are inappropriate or for general purpose PLL applications the internal divider can be by passed and an external divider chain used.

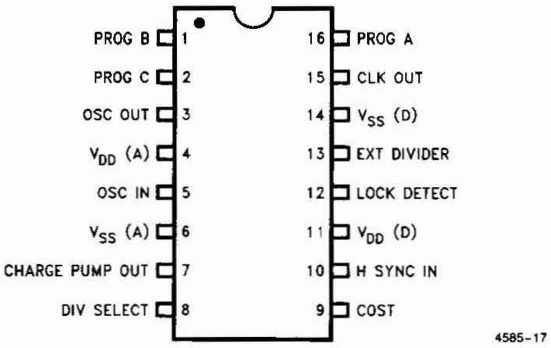
FREQUENCIES and DIVISORS

Function	6Fsc	CCIR 601	Square	8Fsc
Divisor*	1702	1728	1888	2270
PAL Fosc (MHz)	26.602	27.0	29.5	35.468
Divisor*	1364	1716	1560	1820
NTSC Fosc (MHz)	21.476	27.0	24.546	28.636

CCIR 601 divisors yield 1440 pixels in the active portion of each line for NTSC and PAL.
Square pixels format gives 640 pixels for NTSC and 768 pixels for PAL.
6Fsc frequencies do not yield integer divisors.
*Divisor does not include ÷ 2 block.

Connection Diagram

EL4585 SO, P-DIP Packages



March 1996 Rev C

EL4585C

Horizontal Genlock, 8 F_{SC}

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Operating Junction Temp	125°C
Storage Temperature	−65°C to +150°C	Power Dissipation	400mW
Lead Temperature	260°C	Oscillator Frequency	36MHz
Pin Voltages	−0.5V to V_{CC} + 0.5V		
Operating Ambient Temperature Range	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Test Level	Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C		2	4	I	mA
V_{IL} Input Low Voltage		25°C			1.5	I	V
V_{IH} Input High Voltage		25°C	3.5			I	V
I_{IL} Input Low Current	All inputs except COAST, V_{in} = 1.5V	25°C	−100			I	nA
I_{IH} Input High Current	All inputs except COAST, V_{in} = 3.5V	25°C			100	I	nA
I_{IL} Input Low Current	COAST pin, V_{in} = 1.5V	25°C	−100	−60		I	µA
I_{IH} Input High Current	COAST pin, V_{in} = 3.5V	25°C		60	100	I	µA
V_{OL} Output Low Voltage	Lock Det, I_{OL} = 1.6mA	25°C			0.4	I	V
V_{OH} Output High Voltage	Lock Det, I_{OH} = −1.6mA	25°C	2.4			I	V
V_{OL} Output Low Voltage	CLK, I_{OL} = 3.2mA	25°C			0.4	I	V
V_{OH} Output High Voltage	CLK, I_{OH} = −3.2mA	25°C	2.4			I	V
V_{OL} Output Low Voltage	OSC Out, I_{OL} = 200µA	25°C			0.4	I	V
V_{OH} Output High Voltage	OSC Out, I_{OH} = −200µA	25°C	2.4			I	V
I_{OL} Output Low Current	Filter Out, V_{OUT} = 2.5V	25°C	200	300		I	µA
I_{OH} Output High Current	Filter Out, V_{OUT} = 2.5V	25°C		−300	−200	I	µA
I_{OL}/I_{OH} Current Ratio	Filter Out, V_{OUT} = 2.5V	25°C	1.05	1.0	0.95	I	
I_{LEAK} Filter Out	Coast Mode, $V_{DD} > V_{OUT} > 0V$	25°C	−100	±1	100	I	nA

Note 1: All inputs to 0V, COAST floating.

AC Electrical Characteristics ($V_{DD} = 5V$, $T_A = 25°C$ unless otherwise noted)

Parameter	Conditions	Temp	Min	Typ	Max	Test Level	Units
VCO Gain @ 20 MHz	Test circuit 1	25°C		15.5		V	dB
H-sync S/N Ratio	$V_{DD} = 5V$ (Note 2)	25°C	35			V	dB
Jitter	VCXO Oscillator	25°C		1		V	ns
Jitter	LC Oscillator (Typ)	25°C		10		V	ns

Note 2: Noisy video signal input to EL4583C, H-sync input to EL4585C. Test for positive signal lock.

Pin Description

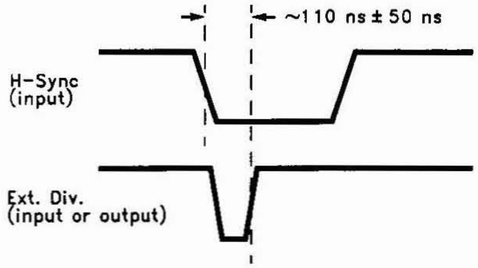
Pin No.	Pin Name	Function
16, 1, 2	Prog A,B,C	Digital inputs to select ÷ N value for internal counter. See table below for values.
3	Osc/VCO Out	Output of internal inverter/oscillator. Connect to external crystal or LC tank VCO circuit.
4	V_{DD} (A)	Analog positive supply for oscillator, PLL circuits.
5	Osc/VCO In	Input from external VCO.
6	V_{SS} (A)	Analog ground for oscillator, PLL circuits.
7	Charge Pump Out	Connect to loop filter. If the H-sync phase is leading or H-sync frequency > CLK ÷ 2N, current is pumped into the filter capacitor to increase VCO frequency. If H-sync phase is lagging or frequency < CLK ÷ 2N, current is pumped out of the filter capacitor to decrease VCO frequency. During coast mode or when locked, charge pump goes to a high impedance state.
8	Div Select	Divide select input. When high, the internal divider is enabled and EXT DIV becomes a test pin, outputting CLK ÷ 2N. When low, the internal divider is disabled and EXT DIV is an input from an external ÷ N.
9	Coast	Tri-state logic input. Low($< \frac{1}{3} * V_{CC}$) = normal mode, Hi Z(or $\frac{1}{3}$ to $\frac{2}{3} * V_{CC}$) = fast lock mode, High($> \frac{2}{3} * V_{CC}$) = coast mode.
10	H-sync In	Horizontal sync pulse (CMOS level) input.
11	V_{DD} (D)	Positive supply for digital, I/O circuits.
12	Lock Det	Lock Detect output. Low level when PLL is locked. Pulses high when out of lock.
13	Ext Div	External Divide input when DIV SEL is low, internal ÷ 2N output when DIV SEL is high.
14	V_{SS} (D)	Ground for digital, I/O circuits.
15	CLK Out	Buffered output of the VCO.

Table 5. VCO Divisors

Prog A Pin 16	Prog B Pin 1	Prog C Pin 2	Div Value N
0	0	0	1702
0	0	1	1728
0	1	0	1888
0	1	1	2270
1	0	0	1364
1	0	1	1716
1	1	0	1560
1	1	1	1820

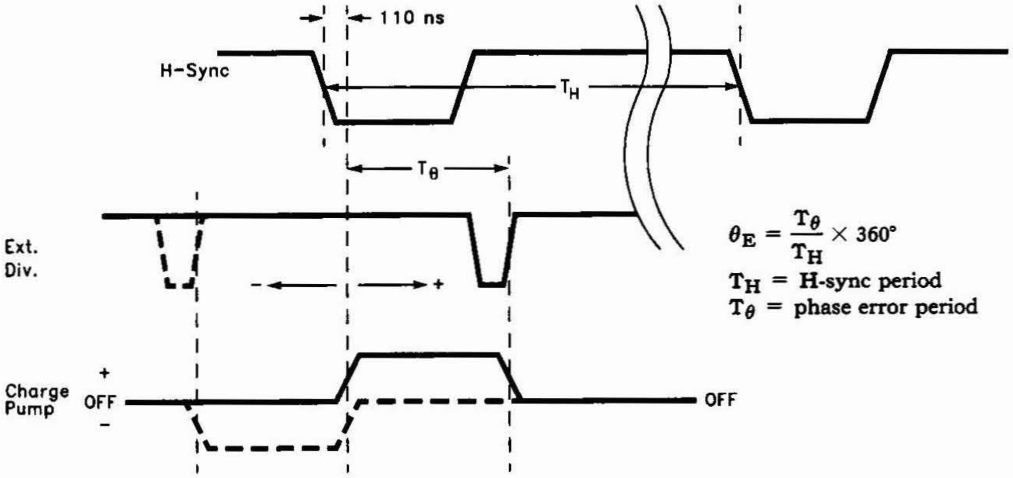
Timing Diagrams

PLL Locked Condition (Phase Error = 0)


~110 ns ± 50 ns
H-Sync (input)
Ext. Div. (input or output)

4585-2

Out of Lock Condition


110 ns
H-Sync
T_H
T_θ
Ext. Div.
−
+
Charge Pump
+
OFF
−
OFF

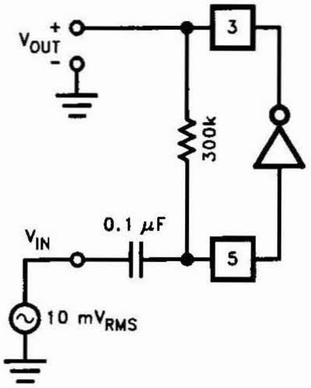
$$\theta_E = \frac{T_\theta}{T_H} \times 360^\circ$$

T_H = H-sync period
T_θ = phase error period

4585-3

Typical Performance Curves

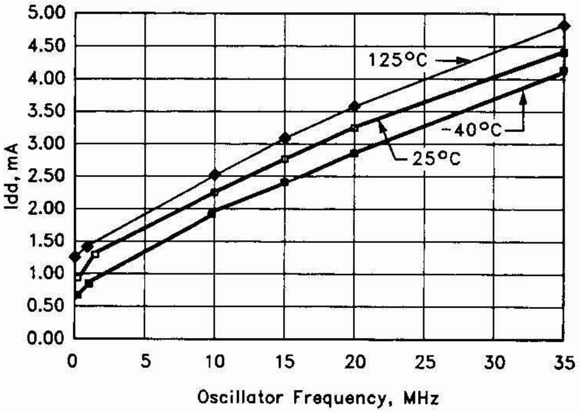
Test Circuit 1


V_{OUT}
+
−
3
300k
V_{IN}
0.1 μF
5
10 mV_{RMS}

4585-5

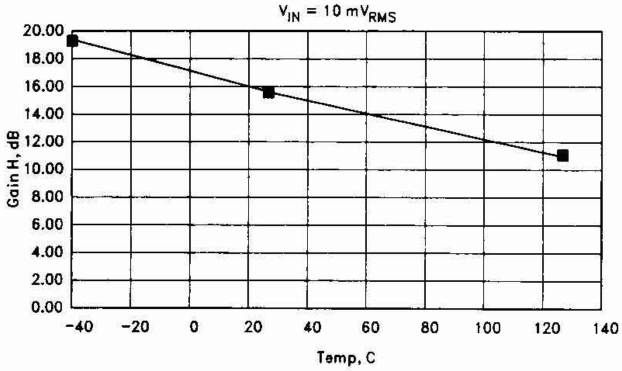
Typical Performance Curves — Contd.

Idd vs Fosc



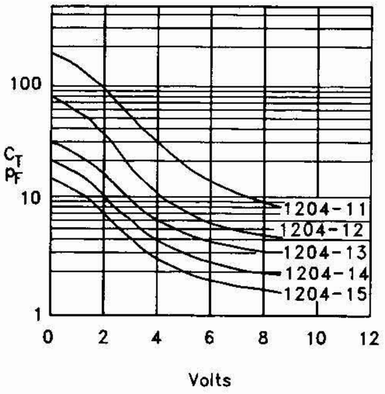
4585-4

OSC Gain @ 20 MHz vs Temp



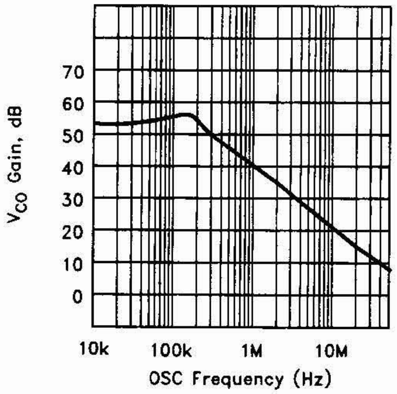
4585-6

Typical Varactor



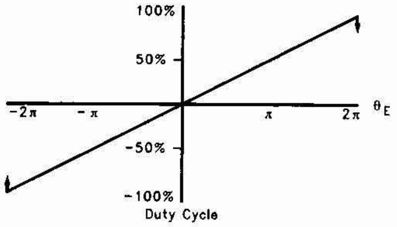
4585-7

OSC Gain vs Fosc



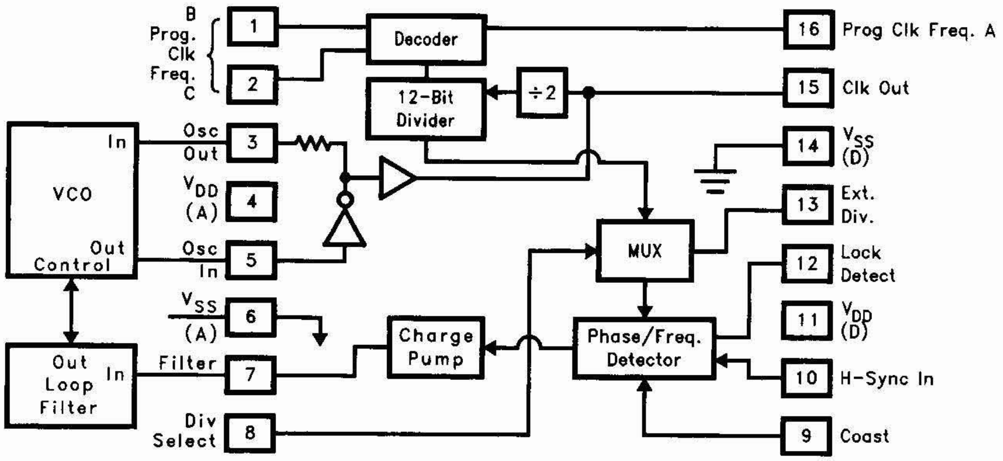
4585-8

Charge Pump Duty Cycle Vs θ_E



4585-9

EL4585 Block Diagram


B
Prog.
Clk
Freq.
C
1
2
3
4
5
6
7
8
Decoder
12-Bit
Divider
÷2
VCO
In
Out
Control
Osc
Out
V_{DD}
(A)
Osc
In
V_{SS}
(A)
Filter
Div
Select
Out
Loop
Filter
In
Charge
Pump
MUX
Phase/Freq.
Detector
16
15
14
13
12
11
10
9
Prog Clk Freq. A
Clk Out
V_{SS}
(D)
Ext.
Div.
Lock
Detect
V_{DD}
(D)
H-Sync In
Coast

4585-1

Description Of Operation

The horizontal sync signal (CMOS level, falling leading edge) is input to H-SYNC input (pin 10). This signal is delayed about 110nS, the falling edge of which becomes the reference to which the clock output will be locked. (See timing diagrams.) The clock is generated by the signal on pin 5, OSC in. There are 2 general types of VCO that can be used with the EL4585C, LC and crystal controlled. Additionally, each type can be either built up using discrete components, including a varactor as the frequency controlling element, or complete, self contained modules can be purchased with everything inside a metal can. These modules are very forgiving of PCB layout, but cost more than discrete solutions. The VCO or VCXO is used to regulate the clock. An LC tank resonator has greater "pull" than a crystal controlled circuit, but will also be more likely to drift over time, and thus will generate more jitter. The "pullability" of the circuit refers to the ability to pull the frequency of oscillation away from its center frequency by modulating the voltage on the control pin of the VCO module or varactor, and is a function of the slope and range of the capacitance-voltage curve of the varactor or VCO module used. The VCO signal is sent to the CLK out pin, divided by two, then sent to the divide by N counter. The divisor N is determined by the state of pins 1, 2, and 16 and is described in table 5 above. The divided signal is sent, along with the delayed H-sync input, to the phase/frequency detector, which compares the two signals for phase and frequency differences. Any phase difference is converted to a current at the charge pump output, (pin 7). A VCO with a positive frequency deviation with control voltage must be used. Varactors have negative capacitance slope with voltage, resulting in positive frequency deviation with increasing control voltage for the oscillators in figures 10 and 11 below.

VCO

The VCO should be tuned so that its frequency of oscillation is very close to the required clock output frequency when the voltage on the varactor is 2.5 volts. VCXO and VCO modules are already tuned to the desired frequency, so this step is not necessary if using one of these units. The output range of the charge pump output (pin 7) is 0 to 5 volts, and it can source or sink a maximum of about 300μA, so all frequency control must be accomplished with variable capacitance from the varactor within this range. Crystal oscillators are more stable than LC oscillators, which translates into lower jitter, but LC oscillators can be pulled from their mid-point values further, resulting in a greater capture and locking range. If the incoming horizontal sync signal is known to be very stable, then a crystal oscillator circuit can be used. If the H-sync signal experiences frequency variations of greater than about 300ppm, an LC oscillator should be considered, as crystal oscillators are very difficult to pull this far. When H-sync input frequency is greater than CLK frequency ÷ 2N, charge pump output (pin 7) sources current into the filter capacitor, increasing the voltage across the varactor, thus tending to increase VCO frequency. Conversely, charge pump output pulls current from the filter capacitor when H-sync frequency is less than CLK ÷ 2N, forcing the VCO frequency lower.

Loop Filter

The loop filter controls how fast the VCO will respond to a change in phase comparator output stimulus. Its components should be chosen so that fast lock can be achieved, yet with a minimum of VCO "hunting", preferably in one to two oscillations of charge pump output, assuming the VCO frequency starts within capture range. If the filter is under-damped, the VCO will over and under-shoot the desired operating point many times before a stable lock takes place. It is possible to under-damp the filter so much that the loop itself oscillates, and VCO lock is never achieved. If the filter is over-damped, the VCO response time will be excessive and many cycles will be required for a lock condition. Over-damping is also characterized by an easily unlocked system because the filter can't respond fast enough to perturbations in VCO frequency. A severely over damped system will seem to endlessly oscillate, like a very large mass at the end of a long pendulum. Due to parasitic effects of PCB traces and component variables, it will take some trial and error experimentation to determine the best values to use for any given situation. Use the component tables as a starting point, but be aware that deviations from these values are not out of the ordinary.

Description Of Operation — Contd.

External Divide

DIV SEL (pin 8) controls the use of the internal divider. When high, the internal divider is enabled and EXT DIV (pin 13) outputs the CLK out divided by 2N. This is the signal to which the horizontal sync input will lock. When divide select is low, the internal divider output is disabled, and external divide becomes an input from an external divider, so that a divisor other than one of the 8 pre-programmed internal divisors can be used.

Normal Mode

Normal mode is enabled by pulling COAST (pin 9) low (below ⅓*Vcc). If H-SYNC and CLK ÷ 2N have any phase or frequency difference, an error signal is generated and sent to the charge pump. The charge pump will either force current into or out of the filter capacitor in an attempt to modulate the VCO frequency. Modulation will continue until the phase and frequency of CLK ÷ 2N exactly match the H-sync input. When the phase and frequency match (with some offset in phase that is a function of the VCO characteristics), the error signal goes to zero, lock detect no longer pulses high, and the charge pump enters a high impedance state. The clock is now locked to the H-sync input. As long as phase and frequency differences remain small, the PLL can adjust the VCO to remain locked and lock detect remains low.

Fast Lock Mode

Fast Lock mode is enabled by either allowing coast to float, or pulling it to mid supply (between ⅓ and ⅔*Vcc). In this mode, lock is achieved much faster than in normal mode, but the clock divisor is modified on the fly to achieve this. If the phase detector detects an error of enough magnitude, the clock is either inhibited or reset to attempt a "fast lock" of the signals. Forcing the clock to be synchronized to the H-sync input this way allows a lock in approximately 2 H-cycles, but the clock spacing will not be regular during this time. Once the near lock condition is attained, charge pump output should be very close to its lock-on value, and placing the device into normal mode should result in a normal lock very quickly. Fast lock mode is intended to be used where H-sync becomes irregular, until a stable signal is again obtained.

Coast Mode

Coast mode is enabled by pulling COAST (pin 9) high (above ⅔*Vcc). In coast mode the internal phase detector is disabled and filter out remains in high impedance mode to keep filter out voltage and VCO frequency as constant a possible. VCO frequency will drift as charge leaks from the filter capacitor, and the voltage changes the VCO operating point. Coast mode is intended to be used when noise or signal degradation result in loss of horizontal sync for many cycles. The phase detector will not attempt to adjust to the resultant loss of signal so that when horizontal sync returns, sync lock can be re-established quickly. However, if much VCO drift has occurred, it may take as long to re-lock as when restarting.

Lock Detect

Lock detect (pin 12) will go low when lock is established. Any DC current path from charge pump out will skew EXT DIV relative to H-SYNC in, tending to offset or add to the 110nS internal delay, depending on which way the extra current is flowing. This offset is called static phase error, and is always present in any PLL system. If, when the part stabilizes in a locked mode, lock detect is not low, adding or subtracting from the loop filter series resistor R_2 will change this static phase error to allow LDET to go low while in lock. The goal is to put the rising edge of EXT DIV in sync with the falling edge of H-SYNC + 110nS. (See timing diagrams.) Increasing R_2 decreases phase error, while decreasing R_2 increases phase error. (Phase error is positive when EXT DIV lags H-SYNC.) The resistance needed will depend on VCO design or VCXO module selection.

Applications Information

Choosing External Components

1. To choose LC VCO components, first pick the desired operating frequency. For our example we will use 28.636MHz, with an H-sync frequency of 15.734kHz.
2. Choose a reasonable inductor value (1-5μH works well). We choose 3.3μH.
3. Calculate C_T needed to produce F_{OSC}.

$$F_{OSC} = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{1}{4\pi^2F^2L} = \frac{1}{4\pi^2(28.636e6)^2(3.3e-6)} = 9.4pF$$

4. From the varactor data sheet find C_V @ 2.5V, the desired lock voltage. $C_V = 23pF$ for our SMV1204-12 for example.
5. C_2 should be about $10C_V$, so we choose $C_2 = 220pF$ for our example.
6. Calculate C_1. Since

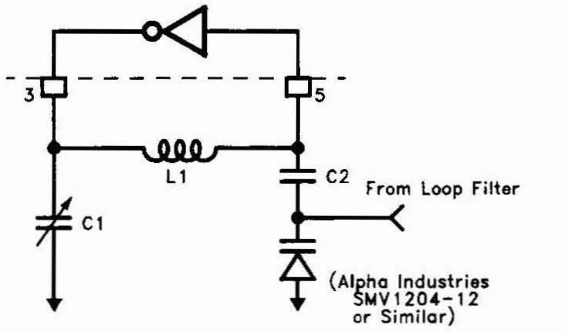
$$C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)},$$

then

$$C_1 = \frac{C_2C_TC_V}{(C_2C_v) - (C_2C_T) - (C_TC_V)}.$$

For our example, $C_1 = 17pF$. (A trim cap may be used for fine tuning.) Examples for each frequency using the internal divider follow.

Typical LC VCO


3
5
L1
C2
From Loop Filter
C1
(Alpha Industries
SMV1204-12
or Similar)

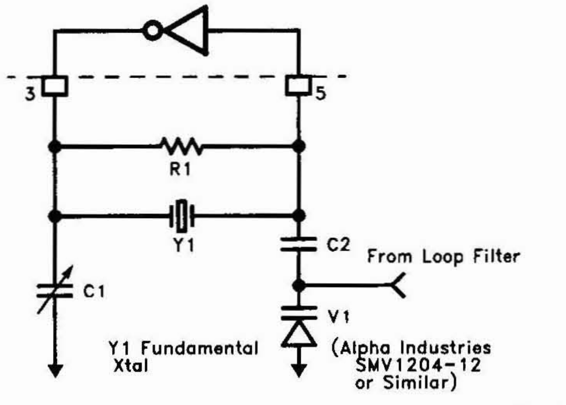
4585-10

LC VCO Component Values (Approximate)

Frequency (MHz)	L1 (μH)	C1 (pF)	C2 (pF)
26.602	3.3	22	220
27.0	3.3	21	220
29.5	2.7	22	220
35.468	2.2	16	220
21.476	4.7	26	220
24.546	3.9	22	220
28.636	3.3	17	220

Note: Use shielded inductors for optimum performance.

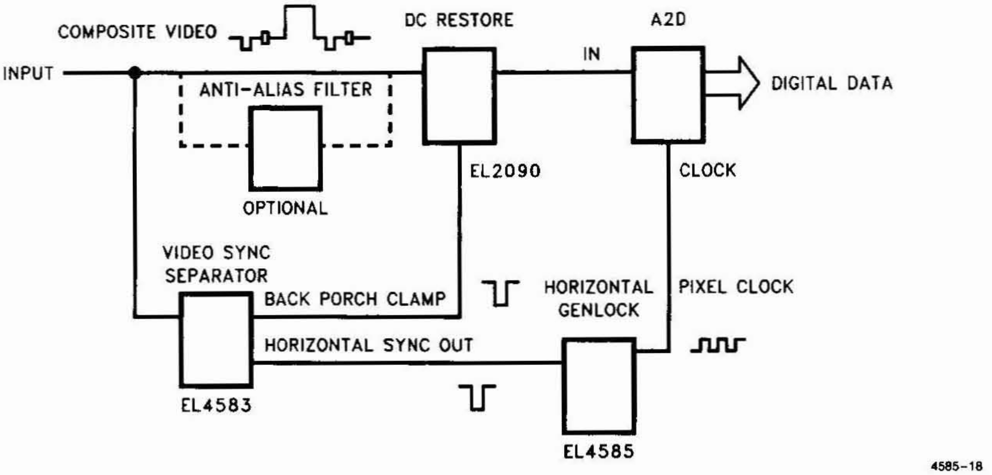
Typical Xtal VCO


3
5
R1
Y1
C2
From Loop Filter
C1
V1
Y1 Fundamental
Xtal
(Alpha Industries
SMV1204-12
or Similar)

4585-11

Typical Application

Horizontal genlock provides clock for an analog to digital converter, digitizing analog video.

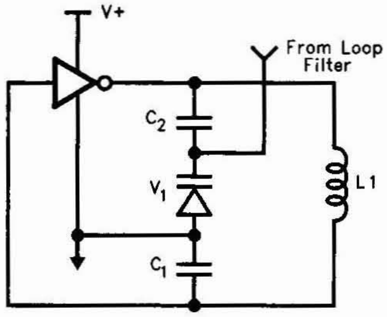

COMPOSITE VIDEO
INPUT
ANTI-ALIAS FILTER
OPTIONAL
DC RESTORE
EL2090
A2D
IN
DIGITAL DATA
CLOCK
VIDEO SYNC
SEPARATOR
BACK PORCH CLAMP
HORIZONTAL SYNC OUT
EL4583
HORIZONTAL
GENLOCK
PIXEL CLOCK
EL4585
4585-18

Xtal VCO Component Values (Approximate)

Frequency (MHz)	R1 (kΩ)	C1 (pF)	C2 (μF)
26.602	300	15	.001
27.0	300	15	.001
29.5	300	15	.001
35.468	300	15	.001
21.476	300	15	.001
24.546	300	15	.001
28.636	300	15	.001

The above oscillators are arranged as Colpitts oscillators, and the structure is redrawn here to emphasize the split capacitance used in a Colpitts oscillator. It should be noted that this oscillator configuration is just one of literally hundreds possible, and the configuration shown here does not necessarily represent the best solution for all applications. Crystal manufacturers are very informative sources on the design and use of oscillators in a wide variety of applications, and the reader is encouraged to become familiar with them.

Colpitts Oscillator


V+
From Loop Filter
C_2
V_1
C_1
L1
4585-12

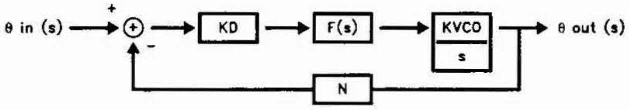
C_1 is to adjust the center frequency, C_2 DC isolates the control from the oscillator, and V1 is the primary control device. C_2 should be much larger than C_V so that V_1 has maximum modulation capability. The frequency of oscillation is given by:

$$F = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{C_1C_2C_V}{(C_1C_2) + (C_1C_V) + (C_2C_V)}$$

Choosing Loop Filter Components

The PLL, VCO, and loop filter can be described as:



4585-13

Where:

K_d = phase detector gain in A/rad

F(s) = loop filter impedance in V/A

K_{VCO} = VCO gain in rad/s/V

N = Total internal or external divisor (see 3 below)

It can be shown that for the loop filter shown below:

$$C_3 = \frac{K_d K_{VCO}}{N\omega_n^2}, C_4 = \frac{C_3}{10}, R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}}$$

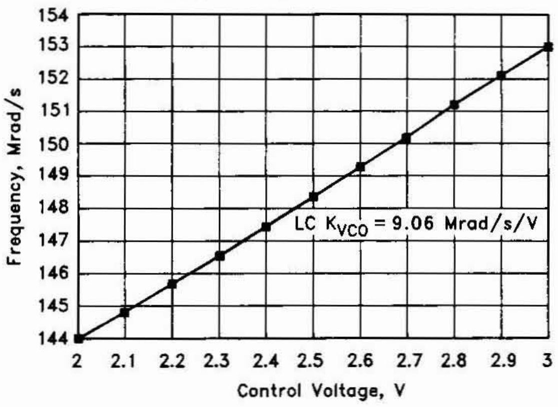
Where ω_n = loop filter bandwidth, and ζ = loop filter damping factor.

1. $K_d = 300\mu A/2\pi rad = 4.77e\text{-}5 A/rad$ for the EL4585C.
2. The loop bandwidth should be about H-sync frequency/20, and the damping ratio should be 1 for optimum performance. For our example, $\omega_n = 15.734kHz/20 = 787\ Hz \approx 5000\ rad/S$.
3. N = 910x2 = 1820 from table 1.

$$N = \frac{F_{VCO}}{F_{Hsync}} = \frac{28.636M}{15.73426k} = 1820 = 910x2$$

4. K_{VCO} represents how much the VCO frequency changes for each volt applied at the control pin. It is assumed (but probably isn't) linear about the lock point (2.5V). Its value depends on the VCO configuration and the varactor transfer function $C_v = F(V_C)$, where V_C is the reverse bias control voltage, and C_V is varactor capacitance. Since $F(V_C)$ is nonlinear, it is probably best to build the VCO and measure K_{VCO} about 2.5V. The results of one such measurement are shown below. The slope of the curve is determined by linear regression techniques and equals K_{VCO}. For our example, K_{VCO} = 9.06 Mrad/s/V.

F_{OSC} vs V_C, LC VCO



4585-14

5. Now we can solve for C_3, C_4, and R_3.

$$C_3 = \frac{K_d K_{VCO}}{N\omega_n^2} = \frac{(4.77e-5)(9.06e6)}{(1820)(5000)^2} = 0.01\mu F$$

$$C_4 = \frac{C_3}{10} = 0.001\mu F$$

$$R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}} = \frac{(2)(1820)(1)(5000)}{(4.77e-5)(9.06e6)} = 42.1k\Omega$$

We choose $R_3 = 43k\Omega$ for convenience.

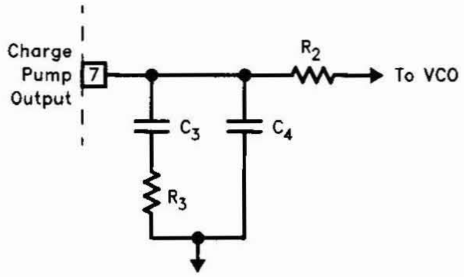
6. Notice R_2 has little effect on the loop filter design. R_2 should be large, around 100k, and can be adjusted to compensate for any static phase error T_θ at lock, but if made too large, will slow loop response. If R_2 is made smaller, T_θ (see timing diagrams) increases, and if R_2 in-

creases, T_θ decreases. For LDET to be low at lock, $|T_\theta| < 50nS$. C_4 is used mainly to attenuate high frequency noise from the charge pump. The effect these components have on time to lock is illustrated below.

Lock Time

Let $T = R_3C_3$. As T increases, damping increases, but so does lock time. Decreasing T decreases damping and speeds up loop response, but increases overshoot and thus increases the number of hunting oscillations before lock. Critical damping ($\zeta = 1$) occurs at minimum lock time. Because decreased damping also decreases loop stability, it is sometimes desirable to design slightly overdamped ($\zeta > 1$), trading lock time for increased stability.

Typical Loop Filter



4585-16

LC Loop Filter Components (Approximate)

Frequency (MHz)	R2 (kΩ)	R3 (kΩ)	C3 (μF)	C4 (μF)
26.602	100	39	0.01	0.001
27.0	100	39	0.01	0.001
29.5	100	43	0.01	0.001
35.468	100	51	0.01	0.001
21.476	100	30	0.01	0.001
24.546	100	36	0.01	0.001
28.636	100	43	0.01	0.001

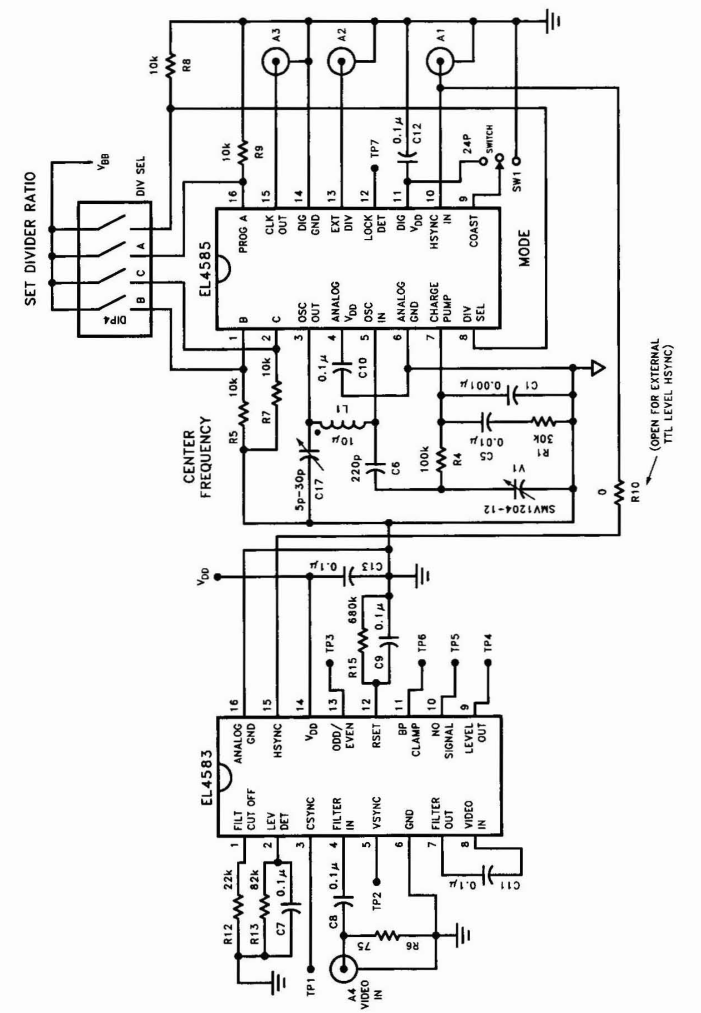
Xtal Loop Filter Components (Approximate)

Frequency (MHz)	R2 (kΩ)	R3 (MΩ)	C3 (pF)	C4 (pF)
26.602	100	4.3	68	6.8
27.0	100	4.3	68	6.8
29.5	100	4.3	68	6.8
35.468	100	4.3	68	6.8
21.476	100	4.3	68	6.8
24.546	100	4.3	68	6.8
28.636	100	4.3	68	6.8

PCB Layout Considerations

It is highly recommended that power and ground planes be used in layout. The oscillator and filter sections constitute a feedback loop and thus care must be taken to avoid any feedback signal influencing the oscillator except at the control input. The entire oscillator/filter section should be surrounded by copper ground to prevent unwanted influences from nearby signals. Use separate paths for analog and digital supplies, keeping the analog (oscillator section) as short and free from spurious signals as possible. Careful attention must be paid to correct bypassing. Keep lead lengths short and place bypass caps as close to the supply pins as possible. If laying out a PCB to use discrete components for the VCO section, care must be taken to avoid parasitic capacitance at the OSC pins 3 and 5, and FILTER out (pin 7). Remove ground and power plane copper above and below these traces to avoid making a capacitive connection to them. It is also recommended to enclose the oscillator section within a shielded cage to reduce external influences on the VCO, as they tend to be very sensitive to "hand waving" influences, the LC variety being more sensitive than crystal controlled oscillators. In general, the higher the operating frequency, the more important these considerations are. Self contained VCXO or VCO modules are already mounted in a shielding cage and therefore do not require as much consideration in layout. Many crystal manufacturers publish informative literature regarding use and layout of oscillators which should be helpful.

EL4585/4 Demo Board

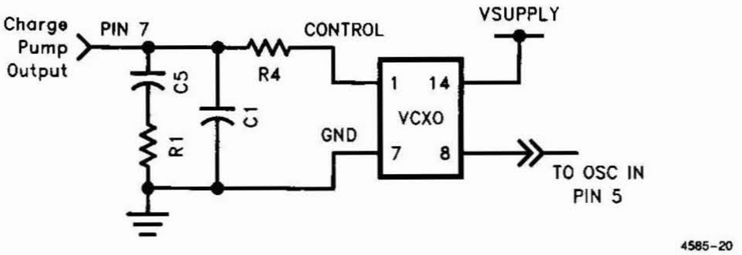

SET DIVIDER RATIO
V_{BB}
DIP4
B
C
A
DIV SEL
10k
R8
CENTER FREQUENCY
R5
10k
R7
10k
EL4585
B
C
OSC OUT
ANALOG V_{DD}
OSC IN
ANALOG GND
CHARGE PUMP
DIV SEL
PROG A
CLK OUT
DIG GND
EXT DIV
LOCK DET
DIG V_{DD}
HSYNC IN
COAST
10k
R9
A3
A2
A1
TP7
0.1µ
C12
24P
SWITCH
SW1
MODE
5p-30p
C17
10µ
L1
0.1µ
C10
220p
C6
100k
R4
C5
0.01µ
R1
30k
C1
0.001µ
SMV1204-12
V1
0
R10
(OPEN FOR EXTERNAL TTL LEVEL HSYNC)
V_{DD}
0.1µ
C13
EL4583
FILT CUT OFF
LEV DET
CSYNC
FILTER IN
VSYNC
GND
FILTER OUT
VIDEO IN
ANALOG GND
HSYNC
V_{DD}
ODD/ EVEN
RSET
BP CLAMP
NO SIGNAL
LEVEL OUT
TP3
R15
680k
C9
0.1µ
TP6
TP5
TP4
R12
22k
R13
82k
C7
0.1µ
TP1
C8
0.1µ
A4 VIDEO IN
75
R6
TP2
0.1µ
C11

4585-19

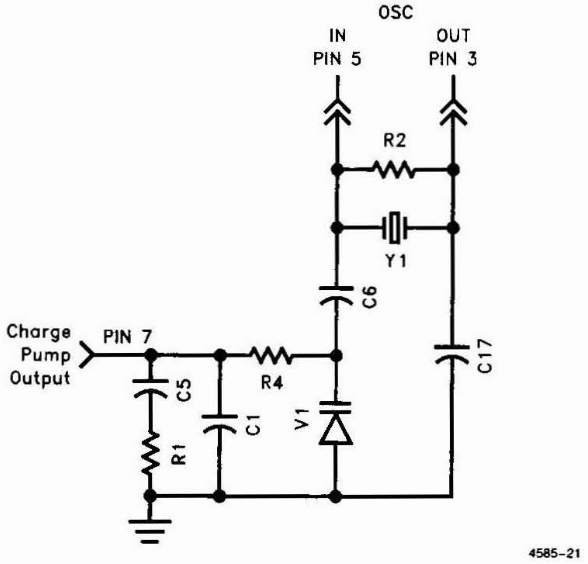
EL4585/4 Demo Board — Contd.

The VCO and loop filter section of the EL4583/4/5 Demo Board can be implemented in the following configurations:

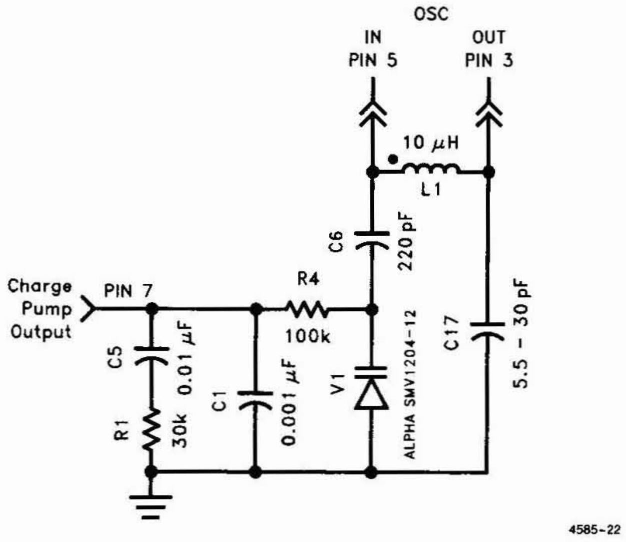
(1) VCXO


Charge Pump Output
PIN 7
CONTROL
VSUPPLY
R4
C5
C1
R1
GND
1
14
VCXO
7
8
TO OSC IN PIN 5
4585-20

(2) XTAL


OSC
IN PIN 5
OUT PIN 3
R2
Y1
C6
C17
Charge Pump Output
PIN 7
R4
C5
C1
V1
R1
4585-21

(3) LC Tank


OSC
IN PIN 5
OUT PIN 3
10 µH
L1
C6
220 pF
R4
100k
C17
5.5 - 30 pF
Charge Pump Output
PIN 7
C5
0.01 µF
C1
0.001 µF
V1
ALPHA SMV1204-12
R1
30k
4585-22

Component Sources

Inductors

- Dale Electronics
  E. Highway 50
  PO Box 180
  Yankton, SD 57078-0180
  (605) 665-9301

Crystals, VCXO, VCO Modules

- Connor-Winfield
  2111 Comprehensive Drive
  Aurora, IL 60606
  (708) 851-4722

- Piezo Systems
  100 K Street
  PO Box 619
  Carlisle, PA 17013
  (717) 249-2151

- Reeves-Hoffman
  400 West North Street
  Carlisle, PA 17013
  (717) 243-5929

- SaRonix
  151 Laura Lane
  Palo Alto, CA 94043
  (415) 856-6900

- Standard Crystal
  9940 Baldwin Place
  El Monte, CA 91731
  (818) 443-2121

Varactors

- Alpha Industries
  20 Sylvan Road
  Woburn, MA 01801
  (617) 935-5150

- Motorola Semiconductor Products
  2100 E. Elliot
  Tempe, AZ 85284
  (602) 244-6900

Note: These sources are provided for information purposes only. No endorsement of these companies is implied by this listing.

Communications

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Differential Line Driver/Receiver Amplifiers at ±5Vs and ±15Vs

- EL1501C Differential Line Driver/Receiver SLIDE* - ADSL Twisted Pair Line Interface.
- EL4430/31C Differential Line Receiver Video on Twisted Pair - ADSL/HDSL Twisted Pair Receiver.
- EL2140/41C Differential Line Driver Video or High Speed Data on Twisted Pair - HDSL/ADSL Twisted Pair Driver.
- EL2142C Differential Line Receiver Video or High Speed Data on Twisted Pair - HDSL/ADSL Twisted Pair Receiver.

Part #	Function	Comments	V_{OUT} diff pk-pk	I_{OUT} pk	THD at V_{OUT}, I_{OUT}	Band-width −3 dB at Gain	Test Gain	Slew Rate	Diff Gain	Diff Phase	Is at ±15V	Supply Voltage Range		Package P = Pins N = PDIP S = SOIC
			Min	pk	Typ	Typ		Typ	Typ	Typ	Typ	Min	Max	
Up to ±15Vs														
EL1501C	Driver	for ADSL	45 V_{P-P}	150 mA	−60 dBc	63 MHz	+10 A_V	1000V/µs	0.17%	0.06°	36 mA	±4.5V	±16V	20P-S
	Receiver	Implements Hybrid	22.5 V_{P-P}	31 mA	−72 dBc	80 MHz	−1 A_V	600V/µs						
**EL4430C	Receiver	Good CMRR				82 MHz	+1 A_V	380V/µs	0.02%	0.02°	16 mA	±4.5V	±16V	8P-N-S
**EL4431C	Receiver	Good CMRR				80 MHz	+2 A_V	380V/µs	0.04%	0.08°	16 mA	±4.5V	±16V	8P-N-S
Up to ±5Vs														
EL2140C	Driver	Fixed Gain	12 V_{P-P}	50 mA	−75 dBc	150 MHz	+2 A_V	800V/µs	0.24%	0.16°	11 mA	±3V	±6V	8P-N-S
EL2141C	Driver	Adjustable Gain	12 V_{P-P}	50 mA	−75 dBc	150 MHz	+2 A_V	800V/µs	0.24%	0.16°	11 mA	±3V	±6V	8P-N-S
EL2142C	Receiver	Match for EL2140/41				150 MHz	+1 A_V	400V/µs	0.2%	0.2°	11 mA	±3V	±6V	8P-N-S

*Subscriber Line Interface DEvice™
**See Amplifier/Buffer Section for datasheet

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1501C—SLIDE*

Differential Line Driver/Receiver

Features

- Complete ADSL differential driver and receiver
- 45 $V_{p\text{-}p}$ differential output drive into 200Ω
- −60 dB typical output distortion at full output at 2 MHz
- −73 dB typical receive distortion at 15 $V_{p\text{-}p}$ levels at 2 MHz
- Drives 8 single-ended video loads, or 4 S-VHS loads, or 4 differential video loads
- Power surface-mount package

Applications

- ADSL line interface
- HDSL line driver
- Video distribution amplifier
- Video twisted-pair line driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1501CM	−40°C to +85°C	20-Lead SO	MDP0027

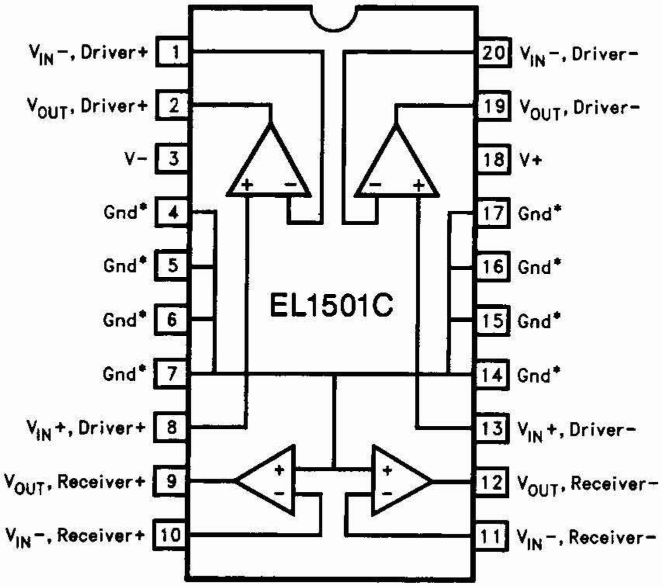
General Description

The EL1501C contains two wideband high-voltage drivers and two receive amplifiers. It is designed to drive 45 $V_{p\text{-}p}$ signals at 2 MHz into a 200Ω load differentially with very low distortion. The receive amplifiers also provide very low distortion and noise, and with external resistors can be wired as a hybrid coupler.

All amplifiers are of the current-feedback type, giving high slewrates while consuming moderate power. They retain frequency response over a wide range of externally set gains.

The EL1501C operates on ±5V to ±15V supplies, and retains its bandwidths and linearities over the supply range.

Eight center package pins are used as ground connections and heat spreaders, allowing a dissipation of 2W at the maximum ambient temperature of 85°C.



V_{IN}−, Driver+ 1
V_{OUT}, Driver+ 2
V− 3
Gnd* 4
Gnd* 5
Gnd* 6
Gnd* 7
V_{IN}+, Driver+ 8
V_{OUT}, Receiver+ 9
V_{IN}−, Receiver+ 10
20 V_{IN}−, Driver−
19 V_{OUT}, Driver−
18 V+
17 Gnd*
16 Gnd*
15 Gnd*
14 Gnd*
13 V_{IN}+, Driver−
12 V_{OUT}, Receiver−
11 V_{IN}−, Receiver−
EL1501C
+
−

1501-1

*Subscriber Line Interface Device

March 1995 Rev. A

*EL1501C—SLIDE**

Differential Line Driver/Receiver

Absolute Maximum Ratings (T_A = 25°C)

V_S	V+ to V− Supply Voltage	33V
V+	V+ Voltage to Ground	−0.3V to +33V
V−	V− Voltage to Ground	−33V to 0.3V
V_{IN}+	Driver V_{IN}+ Voltage	V− to V+
I_{IN}	Current into any Input	8 mA
I_{OUT}, driver	Output Current from Driver (Static)	75 mA
I_{OUT}, rec	Output Current from Receiver (Static)	15 mA
P_D	Maximum Power Dissipation	See Curves
T_A	Operating Temperature Range	−40°C to +85°C
T_S	Storage Temperature Range	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics

Power supplies at ±15V, R_F for both drivers and receivers is 1 kΩ, R_L for driver is 75Ω, R_L for receiver is 200Ω. T_A = 25°C. Amplifiers tested separately.

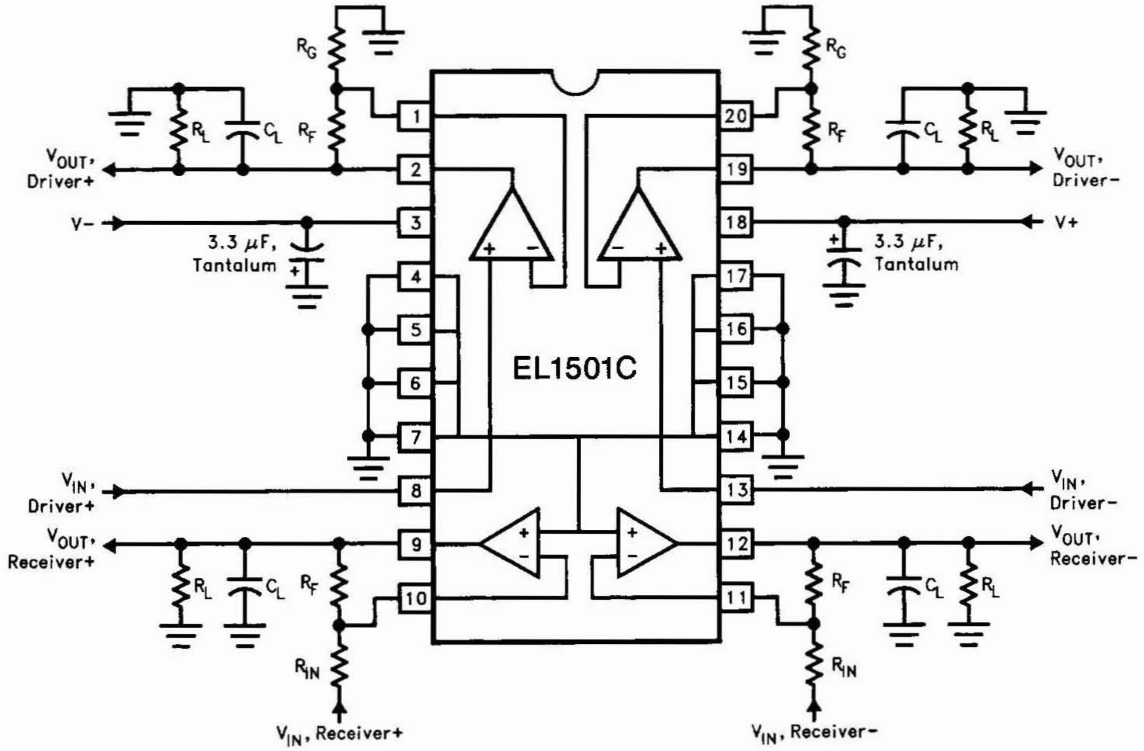
Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}, driver	Driver Input Offset Voltage	−30		30	I	mV
ΔV_{OS}, drivers	Driver-to-Driver V_{OS} Mismatch	−10		10	I	mV
I_B+, driver	Non-Inverting Driver Input Bias Current	−10		10	I	μA
I_B−, driver	Inverting Driver Input Bias Current	−40		40	I	μA
ΔI_B−, drivers	Driver-to-Driver I_B− Mismatch	−36		36	I	μA
R_{OL}, drivers	Driver Transimpedance, V_{OUT} from −12V to +12V	0.4	1.6		I	MΩ
V_{OUT}, driver	Driver Loaded Output Swing	±12.0	±13		I	V
V_{OS}, receiver	Receiver Input Offset Voltage	−30		30	I	mV
ΔV_{OS}, receivers	Receiver-to-Receiver V_{OS} Mismatch	−10		10	I	mV
I_B−, receiver	Receiver Inverting Input Bias Current	−15		15	I	μA
ΔI_B−, receiver	Receiver-to-Receiver I_B− Mismatch	−16		16	I	μA
R_{OL}, receiver	Receiver Transimpedance, V_{OUT} from −4V to +4V	2	6		I	MΩ
V_{OUT}, receiver	Receiver Loaded Output Swing	±6.25	±10		I	V
I_S	All Outputs at 0V	30	36	45	I	mA

Closed-Loop AC Electrical Characteristics

Power supplies at ±15V, R_F for both drivers and receivers is 510Ω, R_L for drivers is 75Ω, R_L for receivers is 200Ω. C_L = 15 pF. Driver gain is +10 and receiver gain is −1. T_A = 25°C. Amplifiers tested separately.

Parameter	Description	Min	Typ	Max	Test Level	Units
BW, driver	−3 dB Bandwidth of Driver Amplifiers		63		V	MHz
HD, driver	Total Harmonic Distortion of Driver					
	f = 2 MHz, Supplies at ±15V, 22.5 $V_{p\text{-}p}$ Output		−60		V	dBc
	f = 2 MHz, Supplies at ±9V, 10.5 $V_{p\text{-}p}$ Output		−66		V	dBc
	f = 300 kHz, Supplies at ±5V, 6 $V_{p\text{-}p}$ Output		−71		V	dBc
dG, driver	Driver Differential Gain Error, Standard NTSC Test A_V = +2, V_S = ±12V, R_L = 37.5Ω		0.17		V	%
dθ, driver	Driver Differential Phase Error, Standard NTSC Test A_V = +2, V_S = ±12V, R_L = 37.5Ω		0.06		V	°
SR, driver	Driver Slewrate, V_{OUT} from −10V to +10V Measured at ±5V	TBD	1000		I	V/µsec
e_N, driver	Driver Input Noise Voltage		3.3		V	nV/$\sqrt{Hz}$
i_N, driver	Driver −Input Noise Current		18		V	pA/$\sqrt{Hz}$
BW, receiver	−3 dB Bandwidth of Receive Amplifiers		80		V	MHz
HD, receiver	Total Harmonic Distortion of Receive Amplifiers					
	f = 2 MHz, Supplies at ±15V, 11.25 $V_{p\text{-}p}$ Output		−72		V	dBc
	f = 2 MHz, Supplies at ±9V, 5.25 $V_{p\text{-}p}$ Output		−71		V	dBc
	f = 300 kHz, Supplies at ±5V, 3 $V_{p\text{-}p}$ Output		−73		V	dBc
SR, receiver	Receiver Slewrate, V_{OUT} from −4V to +4V Measured at ±2.5V	TBD	600		I	V/µsec
e_N, receiver	Receiver Input Noise Voltage		3		V	nV/$\sqrt{Hz}$
i_N, receiver	Receiver −Input Noise Current		12		V	pA/$\sqrt{Hz}$

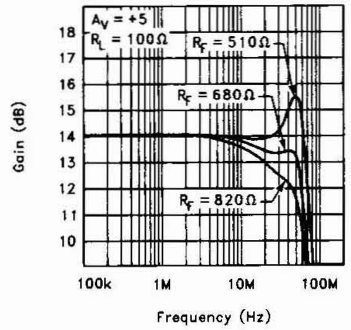
Test Circuit


R_G
R_F
R_L
C_L
V_OUT, Driver+
V_OUT, Driver−
V−
V+
3.3 µF, Tantalum
3.3 µF, Tantalum
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
EL1501C
V_IN, Driver+
V_IN, Driver−
V_OUT, Receiver+
V_OUT, Receiver−
R_IN
V_IN, Receiver+
V_IN, Receiver−

1501-2

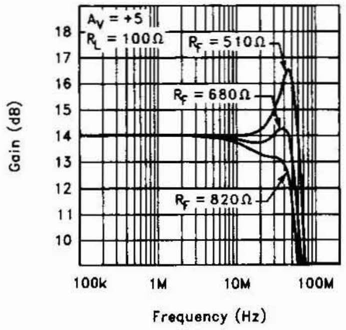
Typical Performance Curves

Driver Frequency Response vs R_F at ±15V Supplies



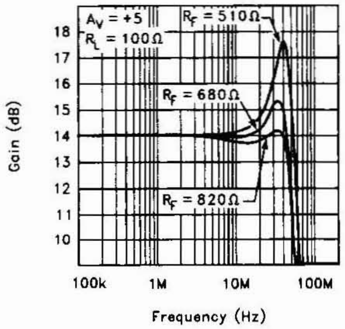
1501-3

Driver Frequency Response vs R_F at ±9V Supplies



1501-4

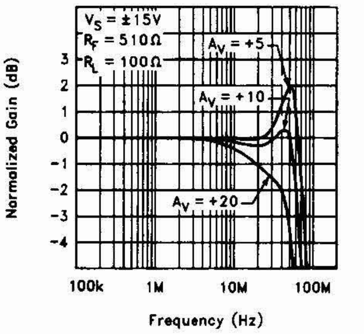
Driver Frequency Response vs R_F at ±5V Supplies



1501-5

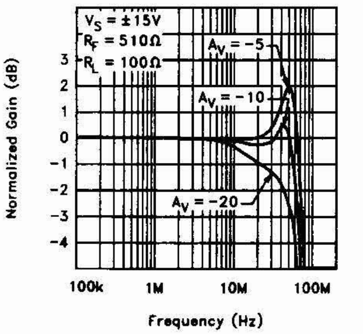
Typical Performance Curves — Contd.

Driver Frequency Response vs Gain (Non-Inverting)



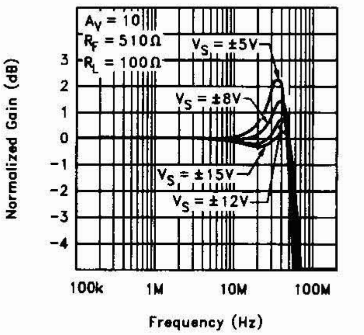
1501-6

Driver Frequency Response vs Gain (Inverting)



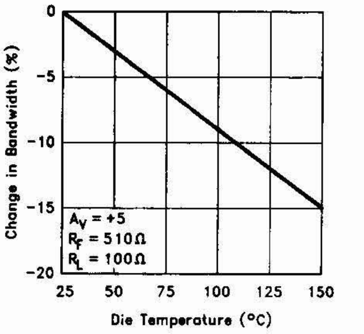
1501-7

Driver Frequency Response vs ± Supply Voltage



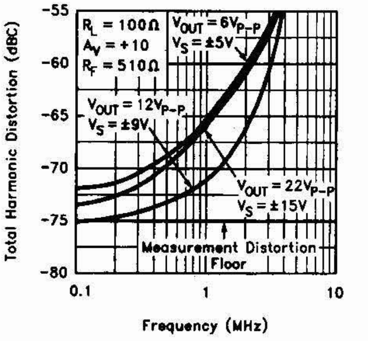
1501-8

Driver Bandwidth vs Temperature



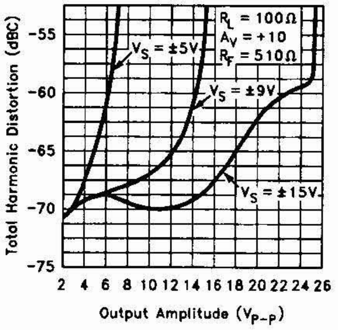
1501-9

Driver Harmonic Distortion vs Frequency (Single Amplifier)



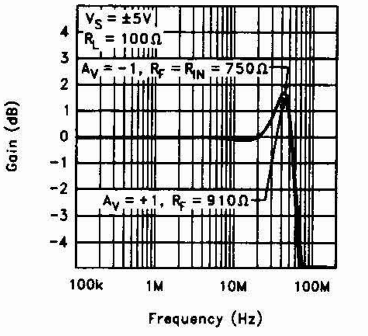
1501-10

Driver Harmonic Distortion vs Output Amplitude at 2 MHz (Single Amplifier)



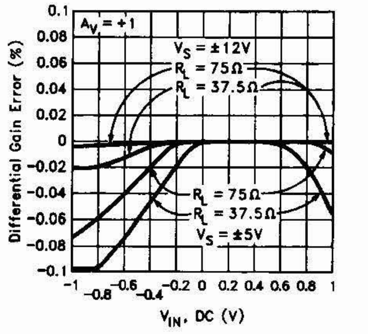
1501-11

Driver Frequency Responses Equalized for Gains of +1 and −1



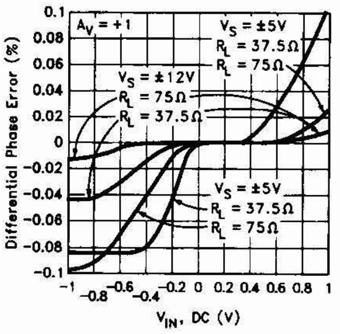
1501-12

Driver Differential Gain Error vs DC Input Offset Gain = +1



1501-13

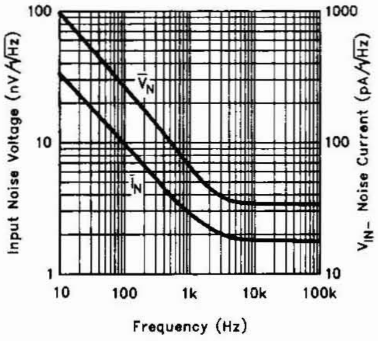
Driver Differential Phase Error vs DC Input Offset Gain = +1



1501-14

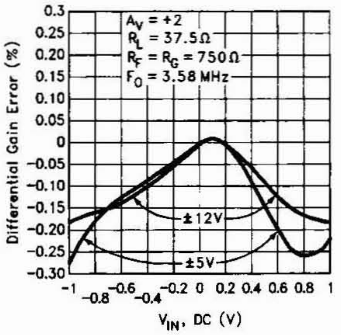
Typical Performance Curves — Contd.

Driver Input Noise Voltage and Current over Frequency



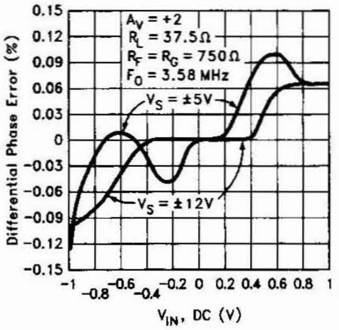
1501-15

Driver Differential Gain Error vs DC Input Voltage—Driving Four Video Loads; Gain = +2



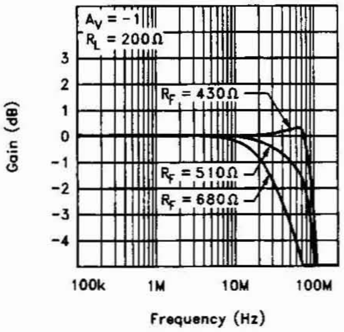
1501-16

Driver Differential Phase Error vs DC Input Voltage—Driving Four Video Loads; Gain = +2



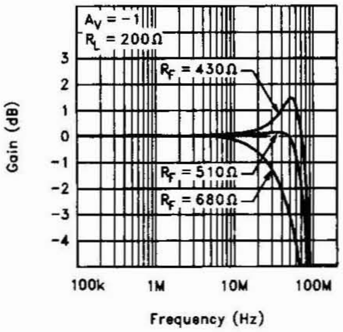
1501-17

Receive Amplifier Frequency Response at $V_S = \pm 15V$



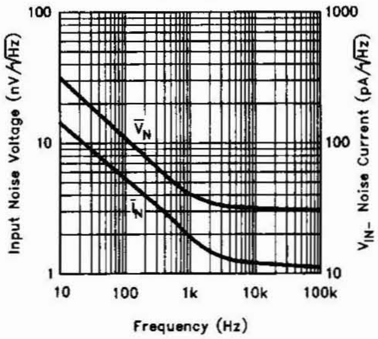
1501-18

Receive Amplifier Frequency Response at $V_S = \pm 5V$



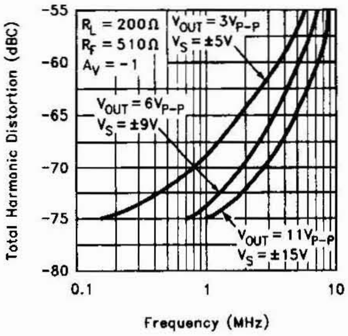
1501-19

Receive Amplifier Input Voltage and Current Noise over Frequency



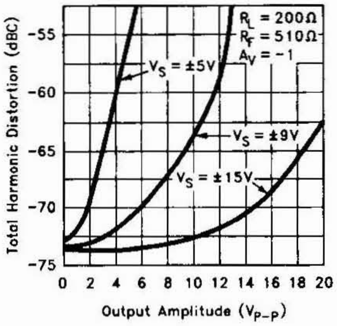
1501-20

Receive Amplifier Harmonic Distortion vs Frequency (Single Amplifier)



1501-21

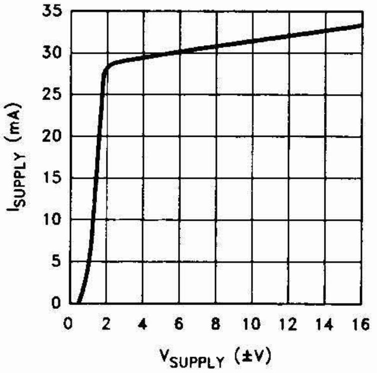
Receive Amplifier Harmonic Distortion vs Output Amplitude at 2 MHz (Single Amplifier)



1501-22

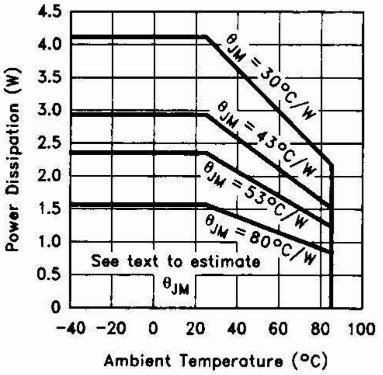
Typical Performance Curves — Contd.

Total Supply Current vs Supply Voltage (All Amplifiers)



1501-23

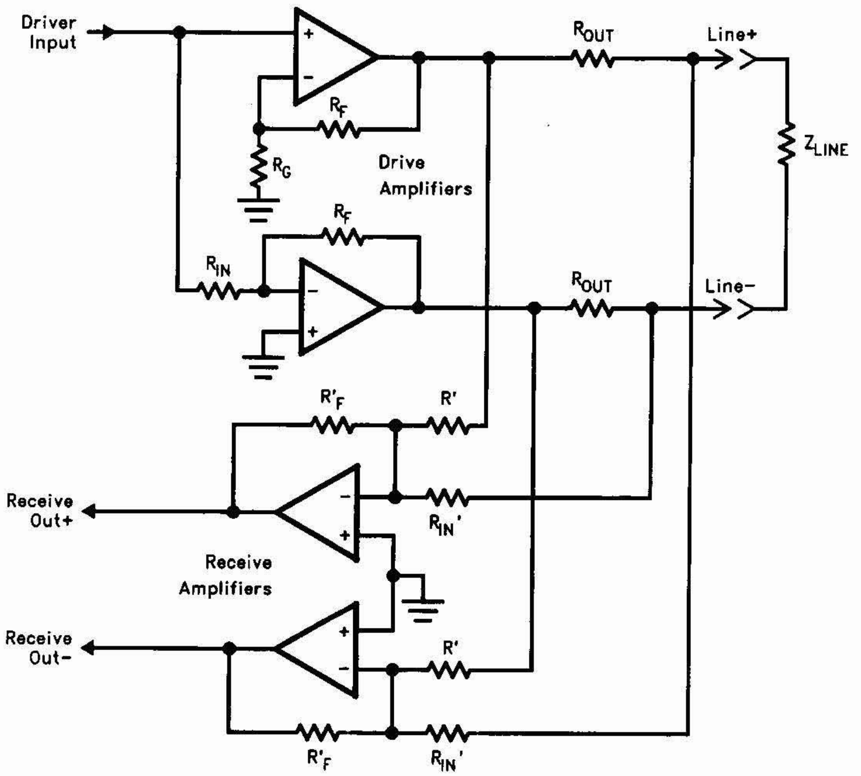
Power Dissipation vs Ambient Temperature for Various Mounted θ_{JM}'s



1501-24

Applications Information

The EL1501C consists of two power line drivers and two receiver amplifiers that can be connected for full duplex differential line transmission and reception. The amplifiers are designed to be used with signals up to 4 MHz and produce low distortion levels. Here is a typical interface circuit:


Driver Input
+
−
R_F
R_G
Drive Amplifiers
R_F
R_{IN}
−
+
R_{OUT}
Line+
Z_{LINE}
R_{OUT}
Line−
R'_F
R'
Receive Out+
−
+
R_{IN}'
Receive Amplifiers
Receive Out−
+
−
R'
R'_F
R_{IN}'

1501-25

Typical Line Interface Connections

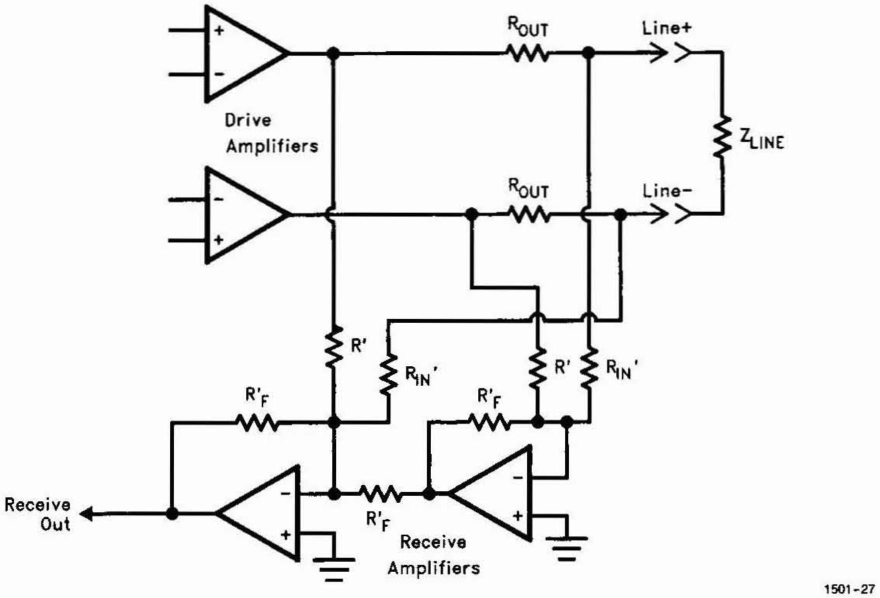
Applications Information — Contd.

The drive amplifiers are wired one in positive gain and the other in negative gain configurations to generate a differential output for a single-ended input. The drivers will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers R_F's need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver. The Typical Performance Curves section of this data sheet has a plot of driver responses matched at gains of +1 and −1 using feedback resistors of 910Ω and 750Ω, respectively.

The receiver amplifiers are wired as a hybrid coupler in the circuit. They reject the drivers' output signal (to the matching accuracy of the line impedance and resistors) while passing the signal coming from the line. Their outputs are still differential signals and can be converted to single-ended form by using a wideband instrumentation amplifier such as the EL4430. In a simplistic analysis we set $R_{OUT} = Z_{LINE}/2$ and $R' = 2^*R_{IN}'$. Signals coming in from the line convert to currents through the R_{IN}'s and pass through the receive amplifiers. Driver outputs pass through the R′ resistors and produce signal currents, but they are cancelled by opposite-polarity currents through the R_{IN}' resistors.

The actual value of R_{OUT} is increased from $Z_{LINE}/2$ to make its value in parallel R_{IN}' equal $Z_{LINE}/2$ and better match the line. For proper hybrid balance, R′ is increased to compensate for R_{OUT}'s adjustment. For $Z_{LINE} = 130\Omega$ and $R_{IN}' = 510\Omega$, we set $R_{OUT} = 74.5\Omega$ and $R' = 1.17\ k\Omega$.

For operating frequencies below 1 MHz, or in cases where the hybrid rejection of the drive signal is not very critical, the receive amplifiers can be wired to provide a single-ended hybrid coupler output:



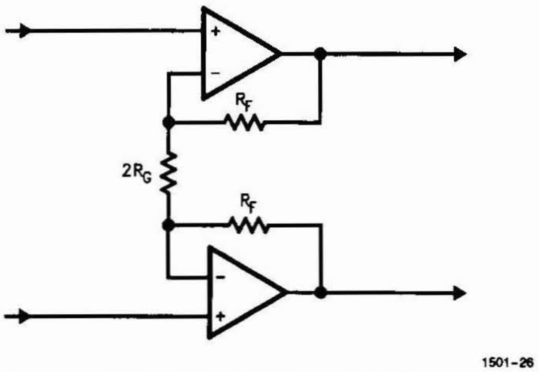
Receive Amplifiers Providing Hybrid and Differential Conversion

Applications Information — Contd.

Common-mode rejection is as good as resistor and line impedance match, as before, but there is a 4 ns time mismatch due to cascading the receive amplifiers. Thus, rejection of common-mode interference will degrade above 1 MHz.

If the receiver amplifiers are not used, their −inputs and outputs may simply be left open. This will reduce power consumption by 2 mA per amplifier.

If a differential signal is available to the drive amplifiers, they may be wired so:



Drivers Wired for Differential Input

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

Input Connections

The receiver amplifiers are not sensitive to source impedances, since they are wired for inverting gain. The drivers are somewhat sensitive to source impedance, however. In particular, they do not like being driven by inductive sources. More than 100 nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4″ of unshielded wiring, or 6″ of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Resistive sources greater than 2 kΩ will cause the driver to exhibit increased harmonic distortion. Most amplifier output stages are much lower in impedance and give no problem.

Power Supplies

The EL1501C works well over the ±5V to ±15V supply range. Frequency response varies only slightly, and output drive capability is constant. The major supply voltage issue is power dissipation. The internal dissipation P_D for an EL1501C running on supply voltages of $\pm V_S$ and delivering a DC output voltage V_O into a load of R_L is

$$P_D = 2 \times V_S \times I_S + \Sigma (V_S - V_O) \times V_O / R_L,$$

where the Σ indicates that all four amplifiers can produce dissipation by each driving a load. If outputs are sinusoidal signals of V_O volts per amplifier peak-to-peak rather than DC the dissipation is

$$P_D = 2 \times V_S \times I_S + \sum \frac{\sqrt{\frac{V_S^2 \times V_O^2}{8} - \frac{V_S \times V_O^3}{3\pi} + \frac{3 \times V_O^4}{128}}}{R_L}$$

Formula 1

As a worst-case example, assume the drivers are running on ±15.75V supplies, each delivering 19.4 $V_{p\text{-}p}$ outputs into 119Ω (the parallel of resistors the driver in the first schematic would see), and quiescent supply current I_S is the maximum 43 mA, and is substantially constant over temperature. The quiescent dissipation (the first term of the equation) is 1.42W, and each driver adds 0.44W, for a total of 2.24W dissipation. The 19.4 $V_{p\text{-}p}$ output level was chosen to produce the maximum internal dissipation: that is, $V_O = 1.234 \times V_S$ is the most dissipative output level.

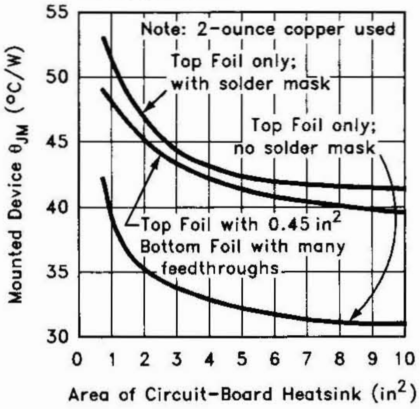
The power supplies should be well bypassed close to the EL1501C. 3.3 µF tantalum capacitors work well. Since the load currents are differential, they need not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no ground loops will occur. This scheme is employed in the layout of the EL1501C demonstration board, and documentation can be obtained from the factory.

Heat-Sinking

To disperse this heat, the center four leads on either side of the package are internally fused to the mounting platform of the die. Heat flows through the leads into the circuit board copper, then spreading and convecting to air. Thus, the ground plane on the component side of the board becomes the heatsink for the EL1501C. This has proven to be a very effective technique, but several aspects of board layout should be noted. First, the heat should not be shunted to internal copper layers of the board nor backside foil, since the feedthroughs and fiberglass of the board are not very thermally conductive. To obtain the best thermal resistance of the mounted part, θ_{JM}, the topside copper ground plane should have as much area as possible and be as thick as practical. If possible, the solder mask can be cut away from the EL1501C to improve thermal resistance. Finally, metal heatsinks can be placed against the board close to the part to draw heat toward the chassis.

The package will exhibit a θ_{JM} of 80°C/W with no assistance from circuit board heatsinks. This will suffice for the lowest supply voltages and output levels. The best θ_{JM} that can be obtained is about 30°C/W, and a practical layout would produce 43°C/W. More detail is available from the Elantec application note *Measuring the Thermal Resistance of Power Surface-Mount Packages*. This plot summarizes the note's results:

Thermal Resistance of EL1501C vs Copper Area



1501-28

For a given θ_{JM}, the maximum P_D is

$$P_D = (T_{MAX} - T_A)\theta_{JM},$$

where T_{MAX} = 150°C, the maximum die temperature in a plastic package, and T_A is the ambient air temperature.

Output Loading

While the drive amplifiers can output in excess of 250 mA, the internal metallization is not designed to carry more than 75 mA of steady DC current and there is no current-limit mechanism. This allows safely driving peak sinusoidal currents of $\pi \times 75$ mA, or 236 mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25 pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The receive amplifiers are connected in inverting mode and will produce a narrow range of characteristics, but the drives can be used for a wide range of gains. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency response (1 dB peaking) for different supply voltages and gains:

Optimum Driver Feedback Resistor for Various Gains and Supply Voltages

Supply Voltage	Driver Voltage Gain				
	−1	+1	2.5	5	10
±5V	750Ω	910Ω	750Ω	680Ω	620Ω
±9V	680Ω	820Ω	680Ω	620Ω	510Ω
±15V	620Ω	750Ω	620Ω	510Ω	470Ω

Driving Video Loads

Each driver amplifier can drive four doubly-terminated video loads while operating on ±5V supplies. Larger supply voltages slightly improve differential gain and phase distortions, which are around 0.2% and 0.1° for single-ended outputs with the standard NTSC test. Differential-output distortion drops to 0.09% and 0.08°.

EL1501 Macromodel

```
****************************************************************
Applications Hint. Pins 4, 5, 6, 7, 14, 15, 16 & 17 must be connected to
ground (node 0) for proper operation. Use resistors whose value is 1e-6 ohms.
****************************************************************
* Connections:
* VIN-, DR+
* |            VOUT, DR+
* |            |      V-
* |            |      |      GND
* |            |      |      |         GND
* |            |      |      |         |         GND
* |            |      |      |         |         |       GND
* |            |      |      |         |         |       |       VIN+, DR+
* |            |      |      |         |         |       |       |       VOUT, Rcvr+
* |            |      |      |         |         |       |       |       |         VIN-, Rcvr+
* |            |      |      |         |         |       |       |       |         |
* 1            2      3      4         5         6       7       8       9         10
*
*VIN-, Rcvr-
* |            VOUT, Rcvr-
* |            |      VIN+, DR-
* |            |      |      GND
* |            |      |      |         GND
* |            |      |      |         |         GND
* |            |      |      |         |         |       GND
* |            |      |      |         |         |       |       V+
* |            |      |      |         |         |       |       |       VOUT, DR-
* |            |      |      |         |         |       |       |       |         VIN-, DR-
* |            |      |      |         |         |       |       |       |         |
* 11           12     13     14        15        16      17      18      19        20
.subckt EL1501/EL 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
*
***************************
*Driver+ (Amplifier A)
*
e1a 30 0 8 0 1.0
visa 30 43 0V
h2a 43 44 v1a 1.0
r1a 1 45 25
l1a 45 44 2.5nH
i1a 8 0 1µA
i2a 1 0 5µA
h1a 46 0 visa 600
r2a 46 31 1K
d1a 31 0 dclamp
d2a 0 31 dclamp
e2a 32 0 31 0 0.0016666
```

EL1501 Macromodel — Contd.

```
l3a 32 33 0.5μH
c1a 33 0 1pF
r5a 33 0 200
g1a 0 34 33 0 1.0
rola 34 0 2Meg
c2a 34 0 3pF
q1a 3 34 35 qp
q2a 18 34 36 qn
q3a 18 35 37 qn
q4a 3 36 38 qp
r7a 37 2 2
r8a 38 2 2
i3a 18 35 3.3mA
i4a 36 3 3.3mA
ivosa 0 42 2mA
v1a 42 0 0V
*************************************
*Driver — (Amplifier B)
*
e1b 50 0 13 0 1.0
visb 50 63 0V
h2b 63 64 v1b 1.0
r1b 20 65 25
l1b 65 64 2.5nH
i1b 13 0 1μA
i2b 20 0 5μa
h1b 66 0 visb 600
r2b 66 51 1K
d1b 51 0 dclamp
d2b 0 51 dclamp
e2b 52 0 51 0 0.0016666
l3b 52 53 0.5μH
c1b 53 0 1pF
r5b 53 0 200
g1b 0 54 53 0 1.0
rolb 54 0 2Meg
c2b 54 0 3pF
g1b 3 54 55 qp
q2b 18 54 56 qn
q3b 18 55 57 qn
q4b 3 56 58 qp
r7b 57 19 2
r8b 58 19 2
i3b 18 55 3.3mA
i4b 56 3 3.3mA
ivosb 0 62 2mA
v1b 62 0 0V
```

EL1501 Macromodel — Contd.

```
*************************************
*Receiver+ (Amplifier C)
*
rpin1 4 5 1e-6
rpin2 5 6 1e-6
rpin3 6 7 1e-6
rpin4 7 14 1e-6
elc 70 0 7 0 1.0
visc 70 83 0V
h2c 83 84 v1b 1.0
rlc 10 85 25
l1c 85 84 2.5nH
i1c 7 0 1µA
i2c 10 0 5µA
h1c 86 0 visc 600
r2c 86 71 1K
d1c 71 0 dclamp
d2c 0 71 dclamp
e2c 72 0 71 0 0.0016666
l3c 72 73 0.5µH
c1c 73 0 1pF
r5c 73 0 200
g1c 0 74 73 0 1.0
rolc 74 0 2Meg
c2c 74 0 4.1pF
q1c 3 74 75 qp
q2c 18 74 76 qn
q3c 18 75 77 qn
q4c 3 76 78 qp
r7c 77 9 2
r8c 78 9 2
i3c 18 75 3.3mA
14c 76 3 3.3mA
ivosc 0 82 2mA
v1c 82 0 0V
**************************************
*Receiver− (Amplifier D)
*
rpin5 17 16 le-6
rpin6 16 15 le-6
rpin7 15 14 le-6
eld 90 0 14 0 1.0
visd 90 103 0v
h2d 103 104 vld 1.0
rld 11 105 25
l1d 105 104 2.5nH
i1d 7 0 1µA
i2d 11 0 5µA
hld 106 0 visd 600
r2d 106 91 1K
```

EL1501 Macromodel — Contd.

```
d1d 91 0 dclamp
d2d 0 91 dclamp
e2d 92 0 91 0 0.0016666
l3d 92 93 0.5μH
cld 93 0 1pF
r5d 93 0 200
gld 0 94 93 0 1.0
rold 94 0 2Meg
c2d 94 0 4.1pF
qld 3 94 95 qp
q2d 18 94 96 qn
q3d 18 95 97 qn
q4d 3 96 98 qp
r7d 97 12 2
r8d 98 12 2
i3d 18 95 3.3mA
i4d 96 3 3.3mA
ivosd 0 102 2mA
vld 102 0 0V
*
* Model
*
.model qn npn(is=5e-15 bf=350 tf=0.1nS)
.model qp pnp(is=5e-15 bf=350 tf=0.1nS)
.model dclamp d(is=le-30 ibv=0.266 bv=1.9 n=4)
.ends
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2140C/2141C

150 MHz Differential Twisted Pair Driver

Features

- Fully differential inputs, outputs, and feedback
- Differential input range ±2.3V
- 150 MHz 3 dB bandwidth
- 800 V/μs slew rate
- −55 dB distortion at 3 MHz
- −75 dB distortion at 100 kHz
- ±5V supplies or +6V single supply
- 50 mA minimum output current
- Output swing (200Ω load) to within 1.5V of supplies (14V pk-pk differential)
- Low power-11 mA typical supply current

Applications

- Twisted pair driver
- Differential line driver
- VGA over twisted pair
- ADSL/HDSL driver
- Single ended to differential amplification
- Transmission of analog signals in a noisy environment

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2140CN	−40°C to +85°C	8-pin PDIP	MDP0031
EL2140CS	−40°C to +85°C	8-pin SOIC	MDP0027
EL2141CN	−40°C to +85°C	8-pin PDIP	MDP0031
EL2141CS	−40°C to +85°C	8-pin SOIC	MDP0027

General Description

The EL2140C/2141C is a very high bandwidth amplifier whose output is in differential form, and is thus primarily targeted for applications such as driving twisted pair lines, or any application where common mode injection is likely to occur. The input signal can be in either single-ended or differential form, but the output is always in differential form.

On the EL2141C, two feedback inputs provide the user with the ability to set the device gain, (stable at minimum gain of two), whereas the EL2140C comes with a fixed gain of two.

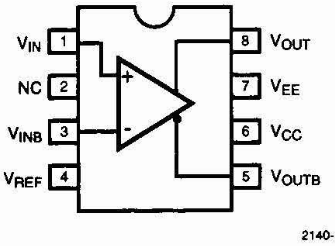
The output common mode level is set by the reference pin (V_{REF}), which has a −3 dB bandwidth of over 100 MHz. Generally, this pin is grounded, but it can be tied to any voltage reference.

The transmission of ADSL/HDSL signals requires very low distortion amplification, so this amplifier was designed with this as a primary goal. The actual signal distortion levels depend upon input and output signal amplitude, as well as the output load impedance. (See distortion data inside.)

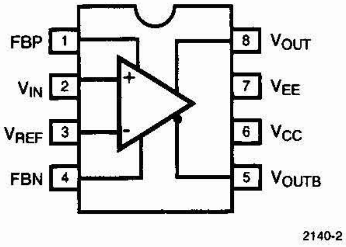
Both outputs (V_{OUT}, V_{OUTB}) are short circuit protected to withstand temporary overload condition.

Connection Diagrams

EL2140C



EL2141C



October 1995, Rev A

Absolute Maximum Ratings

Supply Voltage ($V_{CC}-V_{EE}$)	0V–12.6V
Maximum Output Current	±60 mA
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperaure	+150°C
Recommended Operating Temperature	−40°C to 85°C
V_{IN}, V_{INB}, V_{REF}	V_{EE}+0.8V (MIN) to V_{CC}−0.8V (MAX)
$V_{IN}-V_{INB}$	±5V

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_{CC} = +5V, V_{EE} = −5V, T_A = 25°C, V_{IN} = 0V, R_L = 200, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{supply}	Supply Operating Range ($V_{CC}-V_{EE}$)	±3.0	±5.0	±6.3	I	V
I_S	Power Supply Current (No Load)		11	14	I	mA
V_{OS}	Input Referred Offset Voltage	−25	10	40	I	mV
I_{IN}	Input Bias Current (V_{IN}, V_{INB}, V_{REF})	−20	6	20	I	μA
Z_{IN}	Differential Input Impedance		400		V	kΩ
V_{DIFF}	Differential Input Range	±2.0	±2.3		I	V
A_V	Voltage Gain (EL2140C) V_{IN} = 2V $_{pk\text{-}pk}$	1.95	1.985	2.02	I	V/V
A_{VOL}	Open Loop Voltage Gain (EL2141C)		75		V	dB
V_{CM}	Input Common Mode Voltage Range (EL2140C)	−2.6		+4.0	I	V
V_{OUT}(200)	Output Voltage Swing (200Ω load, V_{OUT} to V_{OUTB}) (EL2141C)	±3.4	±3.6		I	V
V_{OUT}(100)	Output Voltage Swing (100Ω Load, V_{OUT} to V_{OUTB}) (EL2141C)	±2.9	±3.1		I	V
V_N	Input Referred Voltage Noise		36		V	nV/√Hz
V_{REF}	Output Voltage Control Range (EL2140C)	−2.5		+3.3	I	V
V_{REFOS}	Output Offset Relative to V_{REF}	−60	−25	+60	I	mV
PSRR	Power Supply Rejection Ratio	60	70		I	dB
I_{OUT}(min)	Minimum Output Current	50	60		I	mA
CMRR	Input Common Mode Rejection Ratio (EL2140C) V_{CM} = ± 2V	60	70		I	dB
R_{OUT}	(V_{OUT} = V_{OUTB} = 0V) Output Impedence		0.1		V	Ω

AC Electrical Characteristics

V_{CC} = +5V, V_{EE} = −5V, T_A = 25°C, V_{IN} = 0V, R_{LOAD} = 200, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
BW(−3 dB)	−3 dB Bandwidth (EL2140C and EL2141C @ gain of 2)		150		V	MHz
SR	Differential Slewrate		800		V	V/μs
Tstl	Settling Time to 1%		15		V	ns
GBW	Gain Bandwidth Product		400		V	MHz
V_{REFBW}(−3 dB)	V_{REF} −3 dB Bandwidth		130		V	MHz
V_{REFSR}	V_{REF} Slewrate		100		V	V/μs
THDf1	Distortion at 100 kHz (Note 1)		−75		V	dB
dP	Differential Phase @ 3.58 MHz		0.16		V	°
dG	Differential Gain @ 3.58 MHz		0.24		V	%

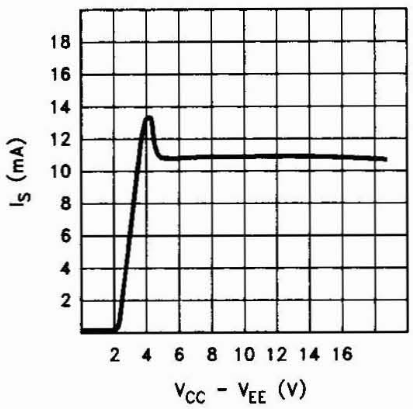
Note 1: Distortion measurement quoted for V_{OUT}−V_{OUTB} = 12V pk-pk, R_{LOAD} = 200Ω, Vgain = 8.

Pin Description

Pin No. EL2140C	Pin No. EL2141C	Pin Name	Function
1	2	V_{IN}	Non-inverting Input
3		V_{INB}	Inverting Input (EL2140C only)
	1	FBP	Non-inverting Feedback Input. Resistor R1 must be Connected from this Pin to V_{OUT}. (EL2141C only)
	4	FBN	Inverting Feedback Input. Resistor R3 must be Connected from this pin to V_{OUTB}. (EL2141C only)
4	3	V_{REF}	Output Common-mode Control. The Common-mode Voltage of V_{OUT} and V_{OUTB} will Follow the Voltage on this Pin. Note that on the EL2141, this pin is also the V_{INB} pin.
5	5	V_{OUTB}	Inverting Output
6	6	V_{CC}	Positive Supply
7	7	V_{EE}	Negative Supply
8	8	V_{OUT}	Non-inverting Output

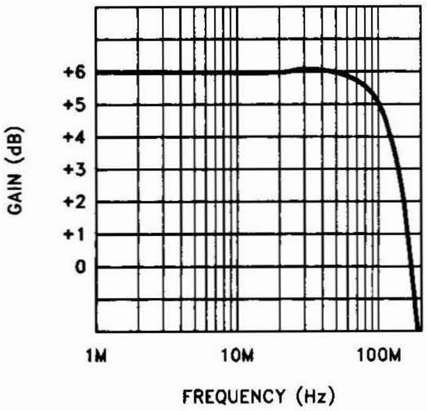
Typical Performance Curves

I_S vs Supply Voltage



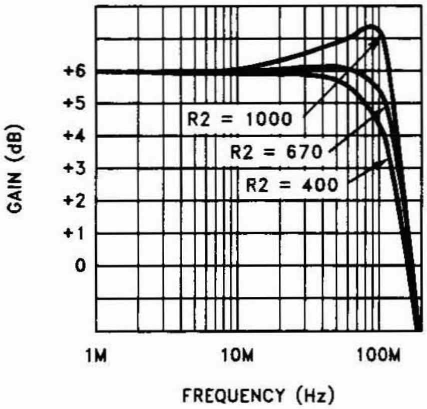
2140-3

EL2140 Frequency Response



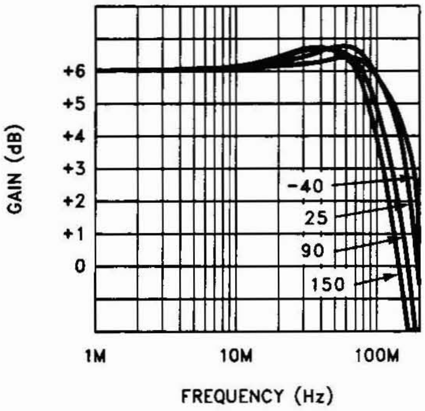
2140-4

EL2141 Frequency Response vs Resistor R2 (GAIN = 2)



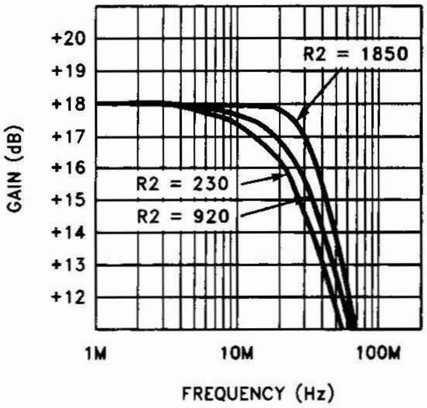
2140-5

Frequency Response vs Temperature



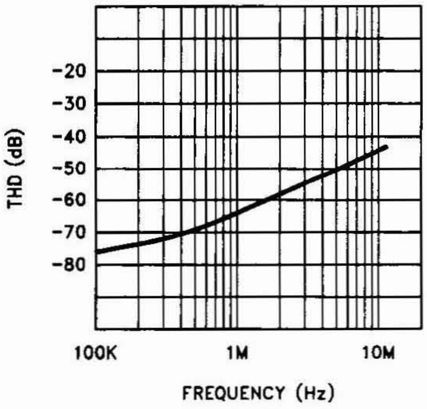
2140-6

EL2141 Frequency Response vs Resistor R2 (GAIN = 8)



2140-7

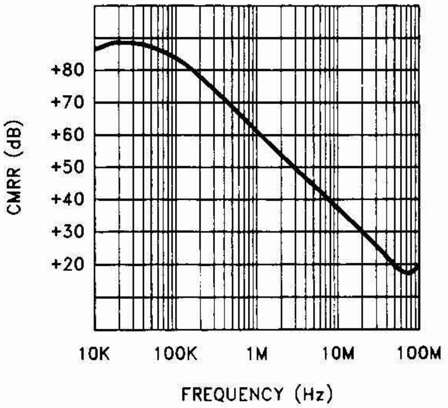
EL2141 Distortion vs Frequency (GAIN = 6, R_{LOAD} = 200Ω) V_{IN} = 2V pk/pk



2140-8

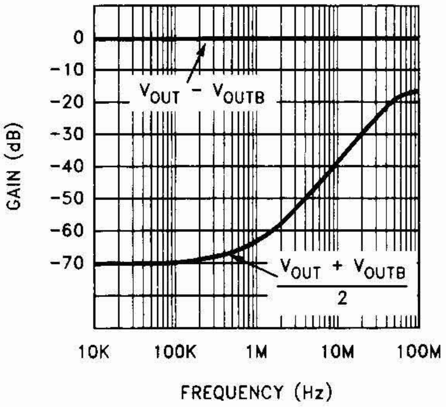
Typical Performance Curves — Contd.

EL2140 CMRR vs Frequency



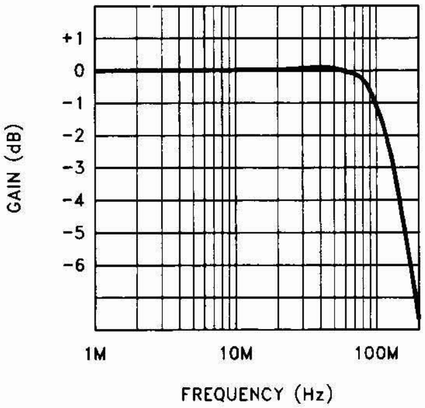
2140-9

EL2141 Output Signal and Common Mode Signal vs Frequency

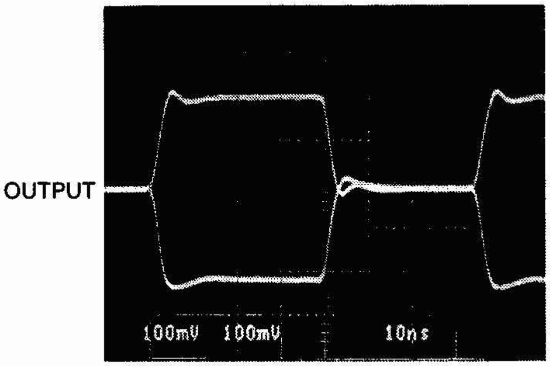


2140-10

EL2140 V_{REF} Frequency Response



2140-11



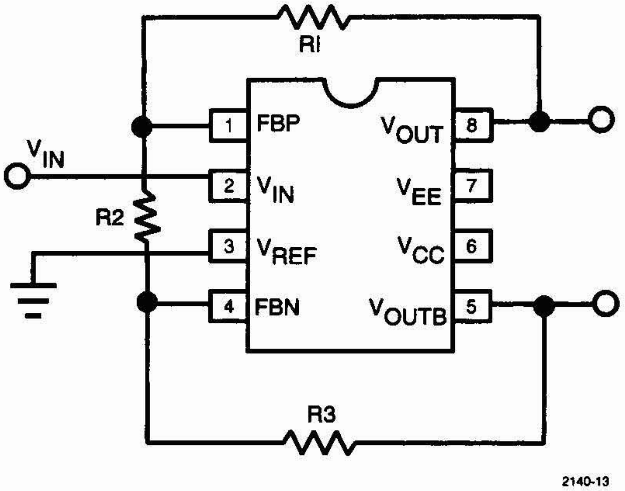
2140-12

EL2140 Small Signal Response (Note 1)

Note 1: Photo shows voltages on a 100Ω transmission line terminated at both ends, so voltages at V_{OUT}, V_{OUTB} are twice the values shown.

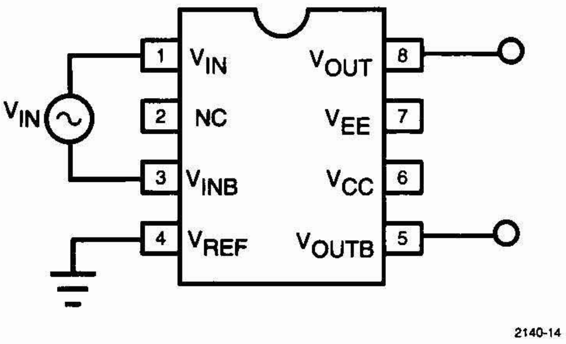
Applications Information

EL2141C



$$\text{GAIN} = \frac{R1 + R2 + R3}{R2}$$

EL2140C



GAIN = 2

$$\frac{V_{OUT} + V_{OUTB}}{2} = V_{REF}$$

(common mode)

Choice of feedback resistor

There is little to be gained from choosing resistor R2 values below 400Ω and, in fact, it would only result in increased power dissipation and signal distortion. Above 400Ω, the bandwidth response will develop some peaking (for a gain of two), but substantially higher resistor R2 values may be used for higher voltage gains, such as up to 2 kΩ at a gain of eight before peaking will develop. R1 and R3 are selected as needed to set the voltage gain, and while R1 = R3 is suggested, the gain equation above holds for any values (see distortion for further suggestions).

Capacitance considerations

As with many high bandwidth amplifiers, the EL2140C/2141C prefer not to drive highly capacitive loads. It is best if the capacitance on V_{OUT} and V_{OUTB} is kept below 10 pF if the user does not want gain peaking to develop.

In addition, on the EL2141C, the two feedback nodes FBP and FBN should be laid out so as to minimize stray capacitance, else an additional pole will potentially develop in the response with possible gain peaking.

The amount of capacitance tolerated on any of these nodes in an actual application will also be dependent on the gain setting and the resistor values in the feedback network.

Distortion considerations

The harmonics that these amplifiers will potentially produce are the 2nd, 3rd, 5th, and 6th. Their amplitude is application dependent. All other harmonics should be negligible by comparison. Each should be considered separately:

H2 The second harmonic arises from the input stage, and the lower the applied differential signal amplitude, the lower the magnitude of the second harmonic. For practical considerations of required output signal and input noise levels, the user will end up choosing a circuit gain. Referring to Figure 1, it is best if the voltage at the negative feedback node tracks the V_{REF} node, and the voltage at the positive feedback node tracks the V_{IN} node respectively. This would theoretically require that R1 + R2 = R3, although the lowest distortion is found at about R3 = R1 + (0.7*R2). With this arrangement, the second harmonic should be suppressed well below the value of the third harmonic.

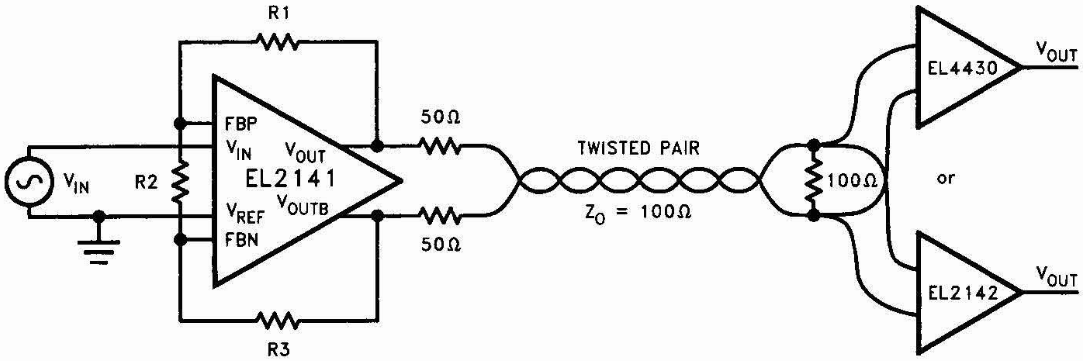
Applications Information — Contd.

H3 The third harmonic should be the dominant harmonic and is primarily affected by output load current which, of course, is unavoidable. However, this should encourage the user not to waste current in the gain setting resistors, and to use values that consume only a small proportion of the load current, so long as peaking does not occur. The more load current, the worse the distortion, but depending on the frequency, it may be possible to reduce the amplifier gain so that there is more internal gain left to cancel out any distortion.

H5 The fifth harmonic should always be below the third, and will not become significant until heavy load currents are drawn. Generally, it should respond to the same efforts applied to reducing the third harmonic.

H6 The sixth harmonic should not be a problem and is the result of poor power supply decoupling. While 100 nF chip capacitors may be sufficient for some applications, it would be insufficient for driving full signal swings into a twisted pair line at 100 kHz. Under these conditions, the addition of 4.7 μF tantalum capacitors would cure the problem.

Typical Applications Circuits



2140-15

Figure 1. Typical Twisted Pair Application

Typical Applications Circuits — Contd.

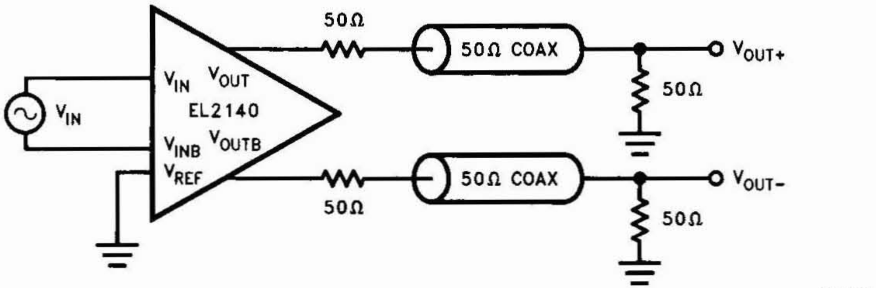

50Ω
50Ω COAX
V_{OUT+}
50Ω
V_{IN}
V_{OUT}
EL2140
V_{IN}
V_{INB}
V_{OUTB}
V_{REF}
50Ω COAX
V_{OUT-}
50Ω
50Ω
2140-16

Figure 2. Dual Coaxial Cable Driver

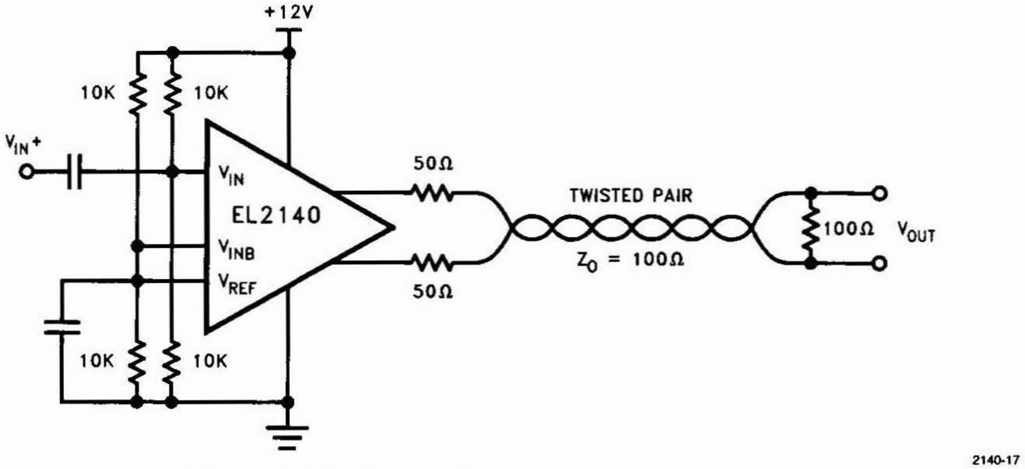

+12V
10K
10K
V_{IN}+
V_{IN}
EL2140
V_{INB}
V_{REF}
50Ω
TWISTED PAIR
100Ω
V_{OUT}
Z_0 = 100Ω
50Ω
10K
10K
2140-17

Figure 3. Single Supply Twisted Pair Driver

Typical Applications Circuits — Contd.

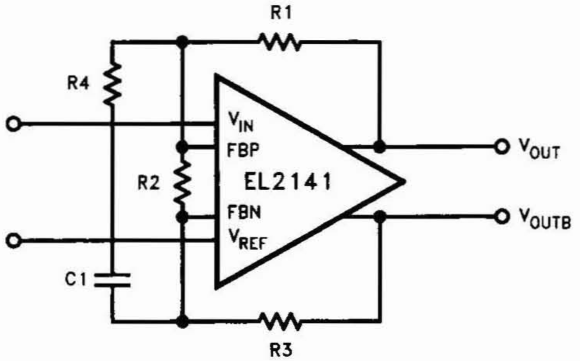

R1
R4
R2
C1
R3
V_IN
FBP
EL2141
FBN
V_REF
V_OUT
V_OUTB
2140-18

Figure 4. Differential Line Driver with Equalization

$$\text{DC Gain} = \frac{R1 + R2 + R3}{R2} \text{ (See Figure 5)}$$

$$\text{HF Gain} = \frac{R1 + (R2//R4) + R3}{(R2//R4)} \text{ (See Figure 5)}$$

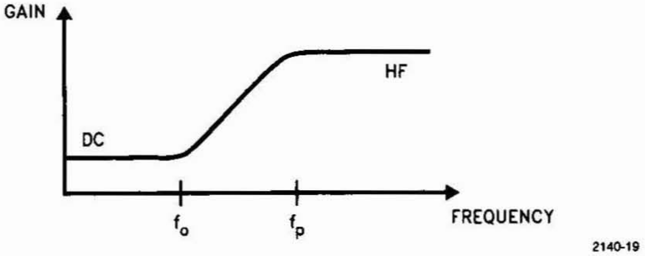
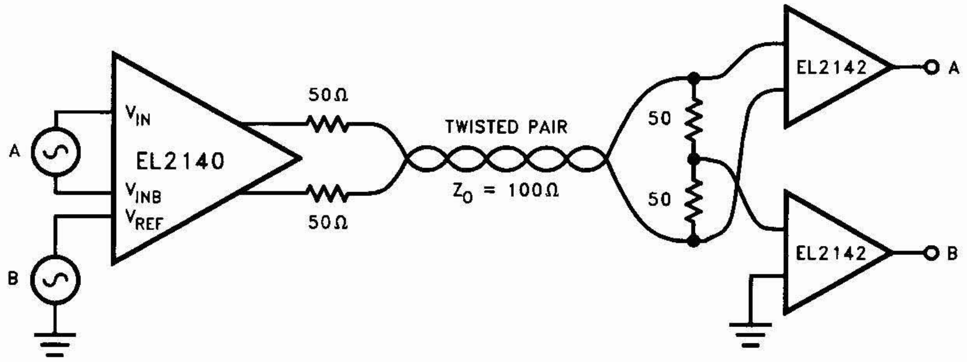


Figure 5

$$\text{where } f_o = \frac{1}{2\,\pi\, C_1\, R_2}$$

$$\text{and } f_p = \frac{1}{2\,\pi\, C_1\, R_4}$$

Typical Applications Circuits — Contd.


A
B
V_{IN}
EL2140
V_{INB}
V_{REF}
50Ω
50Ω
TWISTED PAIR
Z_0 = 100Ω
50
50
EL2142
EL2142
A
B

2140-20

Figure 6. Dual Signal Transmission Circuit

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EL2142C
Differential Line Receiver

Features

- Differential input range ±2.3V
- 150 MHz 3 dB bandwidth
- 400 V/µs slewrate
- ±5V supplies or single supply
- 50 mA minimum output current
- Output swing (100Ω load) to within 1.5V of supplies
- Low power −11 mA typical

Applications

- Twisted pair receiver
- Differential line receiver
- VGA over twisted pair
- ADSL/HDSL receiver
- Differential to single ended amplification.
- Reception of analog signals in a noisy environment.

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2142CN	−40°C to +85°C	8-pin DIP	MDP0031
EL2142CS	−40°C to +85°C	8-pin SOIC	MDP0027

General Description

The EL2142C is a very high bandwidth amplifier designed to extract the difference signal from noisy environments, and is thus primarily targeted for applications such as receiving signals from twisted pair lines, or any application where common mode noise injection is likely to occur.

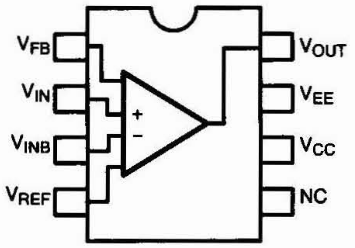
The EL2142C is stable for a gain of one, and requires two external resistors to set the voltage gain.

The output common mode level is set by the reference pin (V_{REF}), which has a −3 dB bandwidth of over 100 MHz. Generally, this pin is grounded, but it can be tied to any voltage reference.

The output can deliver a minimum of ±50 mA and is short circuit protected to withstand a temporary overload condition.

Connection Diagrams

EL2142C SO, P-DIP



2142-1

January 1996 Rev A

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage ($V_{CC}-V_{EE}$)	0V to 12.6V	Operating Junction Temperature	+150°C
Maximum Output Current	±60 mA	Lead Temperature (<5 sec)	+300°C
Storage Temperature Range	−65°C to +150°C	Recommended Operating Temperature	−40°C to +85°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

(V_{CC} = +5V, V_{EE} = −5V, T_A = 25C, V_{IN} = 0V, R_L = 100, unless otherwise specified)

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{supply}	Supply Operating Range ($V_{CC}-V_{EE}$)	±3.0	±5.0	±6.3	I	V
I_S	Power Supply Current (no load)		11	14	I	mA
V_{OS}	Input Referred Offset Voltage	−25	10	40	I	mV
I_{IN}	Input Bias Current (V_{IN}, V_{INB}, V_{REF})	−20	6	20	I	μA
Z_{IN}	Differential Input Resistance		400		V	KΩ
C_{IN}	Differential Input Capacitance		1		V	pF
V_{DIFF}	Differential Input Range	±2.0	±2.3		I	V
A_{VOL}	Open Loop Voltage Gain		75		V	dB
V_{IN}	Input Common Mode Voltage Range	−2.6		+4.0	I	V
V_{OUT}	Output Voltage Swing (50Ω load to GND)	±2.9	±3.1		I	V
I_{OUT}(min)	Minimum Output Current	50	60		I	mA
V_N	Input Referred Voltage Noise		36		V	nV/√Hz
V_{REF}	Output Voltage Control Range	−2.5		+3.3	I	V
PSRR	Power Supply Rejection Ratio	60	70		I	dB
CMRR2	Input Common Mode Rejection Ratio (V_{IN} = ±2V)	60	70		I	dB
CMRR1	Input Common Mode Rejection Ratio (full V_{IN} range)	50	60		I	dB

AC Electrical Characteristics

($V_{CC} = +5V$, $V_{EE} = -5V$, $T_A = 25C$, $V_{IN} = 0V$, $R_{LOAD} = 100$, unless otherwise specified)

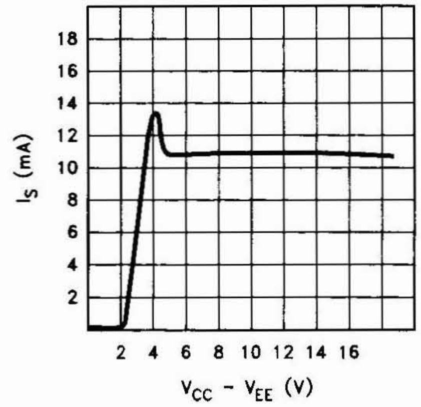
Parameter	Description	Min	Typ	Max	Test Level	Units
BW(−3dB)	−3 dB Bandwidth (Gain = 1)		150		V	MHz
SR	Slewrate		400		V	V/μs
T_{stl}	Settling time to 1%		15		V	ns
GBWP	Gain bandwidth product		200		V	MHz
V_{REF}BW(−3 dB)	V_{REF} −3dB Bandwidth		130		V	MHz
V_{REF}SR	V_{REF} Slewrate		100		V	V/μsec
dG	Differential gain at 3.58 MHz.		0.2		V	%
dθ	Differential phase at 3.58 MHz.		0.2		V	

Pin Description

Pin Number	Pin Name	Function
1	V_{FB}	Feedback input
2	V_{IN}	Non-inverting input
3	V_{INB}	Inverting input
4	V_{REF}	Sets output voltage level to V_{REF} when $V_{IN} = V_{INB}$
5	NC	
6	V_{CC}	Positive supply voltage
7	V_{EE}	Negative supply voltage
8	V_{OUT}	Output voltage

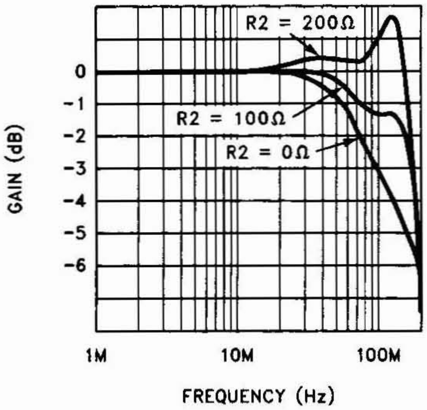
Typical Performance Curves

I_S vs Supply Voltage



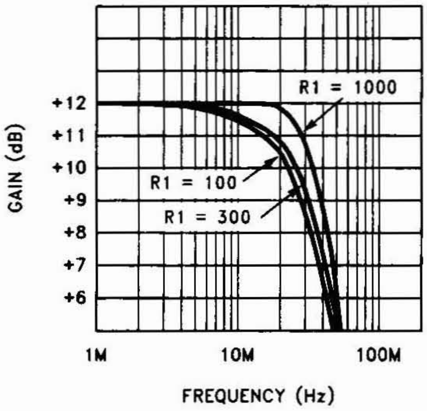
2142-2

Frequency Response
(Gain = 1)



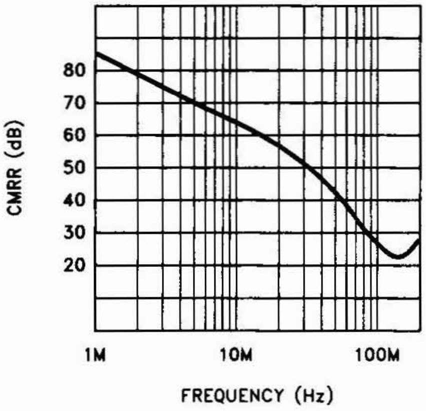
2142-3

Frequency Response
vs Resistor R1 (Gain = 4)



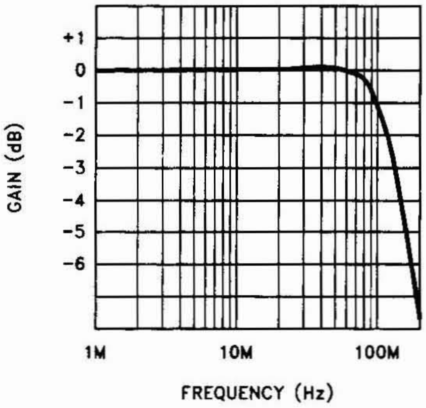
2142-4

CMRR vs Frequency



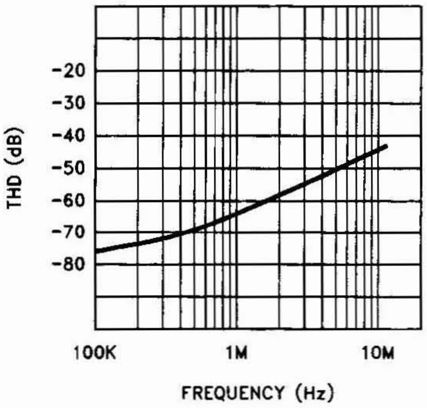
2142-5

V_{REF} Frequency Response



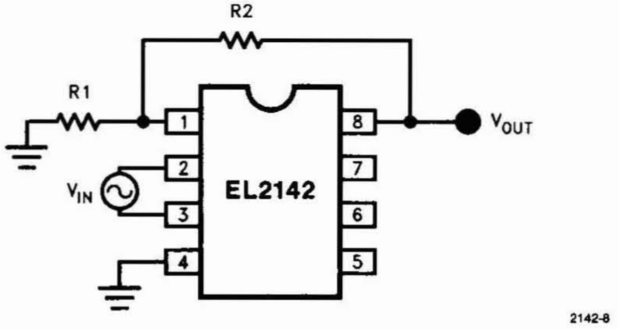
2142-6

Distortion vs Frequency
(GAIN = 3, R_{LOAD} = 100Ω)
V_{IN} = 2V pk/pk



2142-7

Applications Information



Gain Equation

V_{OUT} = ((R2+R1)/R1) × (V_{IN}-V_{INB}+V_{REF}) when R1 tied to GND
V_{OUT} = ((R2+R1)/R1) × (V_{IN}-V_{INB}) when R1 tied to V_{REF}

Choice of Feedback Resistor

For a gain of one, V_{OUT} may be shorted back to V_{FB}, but 100Ω–200Ω improves the bandwidth. For gains greater than one, there is little to be gained from choosing resistor R1 value below 200Ω, for it would only result in increased power dissipation and potential signal distortion. Above 200Ω, the bandwidth response will develop some peaking (for a gain of one), but substantially higher R1 values may be used for higher voltage gains, such as up to 1 kΩ at a gain of four before peaking will develop.

Capacitance Considerations

As with many high bandwidth amplifiers, the EL2142C prefers not to drive highly capacitive loads. It is best if the capacitance on V_{OUT} is kept below 10 pF if the user does not want gain peaking to develop. The V_{FB} node forms a potential pole in the feedback loop, so capacitance should be minimized on this node for maximum bandwidth.

The amount of capacitance tolerated on any of these nodes in an actual application will also be dependent on the gain setting and the resistor values in the feedback network.

Typical Applications

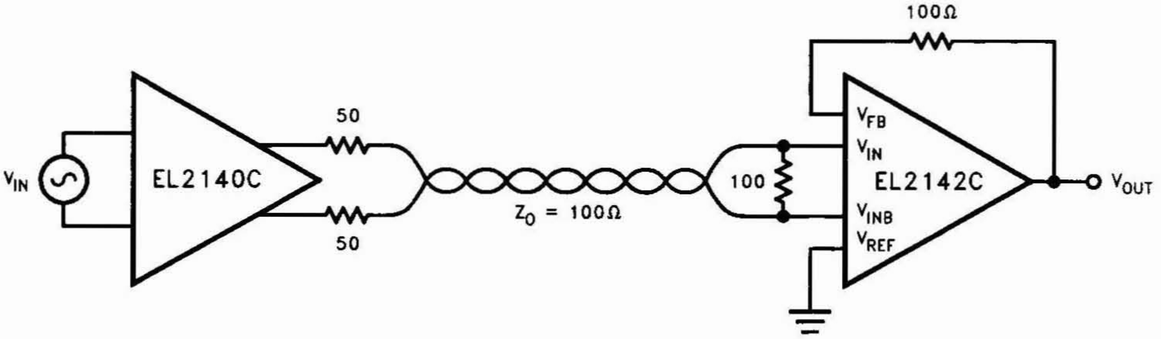

100Ω
50
50
V_IN
EL2140C
Z_0 = 100Ω
100
V_FB
V_IN
EL2142C
V_INB
V_REF
V_OUT
2142-9

Figure 1. Typical Twisted Pair Application

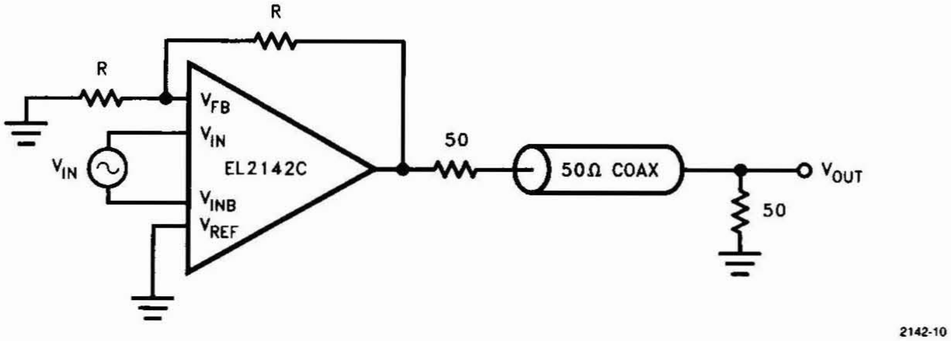

R
R
V_FB
V_IN
V_IN
EL2142C
V_INB
V_REF
50
50Ω COAX
V_OUT
50
2142-10

Figure 2. Coaxial Cable Driver

Typical Applications — Contd.

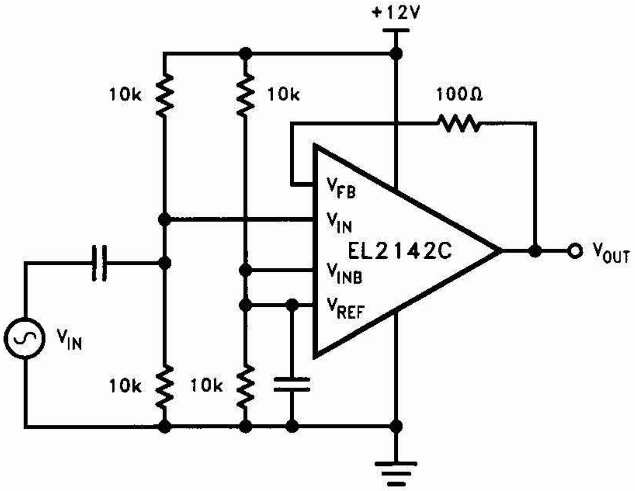

+12V
10k
10k
100Ω
VFB
VIN
EL2142C
VINB
VREF
VOUT
VIN
10k
10k
2142-11

Figure 3. Single Supply Receiver

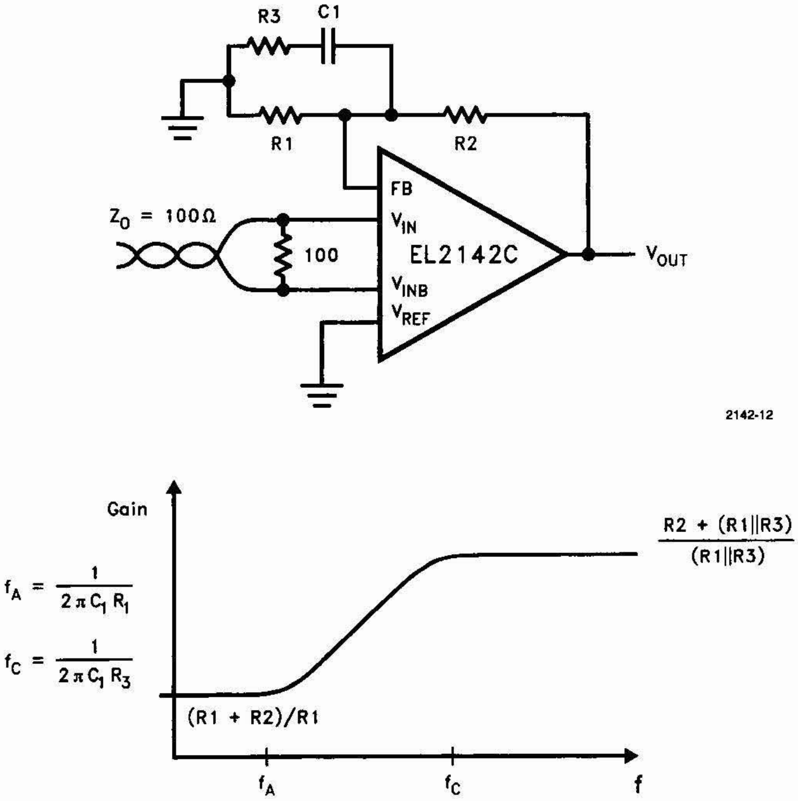

R3
C1
R1
R2
FB
VIN
Z0 = 100Ω
100
EL2142C
VOUT
VINB
VREF
2142-12
Gain
fA = 1 / 2πC1R1
fC = 1 / 2πC1R3
R2 + (R1||R3) / (R1||R3)
(R1 + R2)/R1
fA
fC
f
2142-13

Figure 4. Compensated Line Receiver

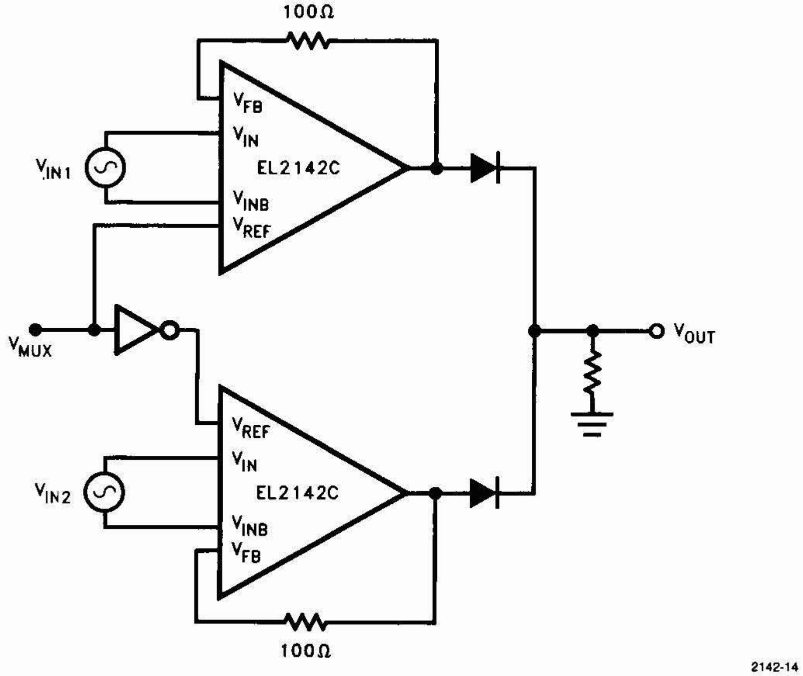

100Ω
V_{FB}
V_{IN}
EL2142C
V_{INB}
V_{REF}
V_{IN1}
V_{MUX}
V_{OUT}
V_{REF}
V_{IN}
EL2142C
V_{INB}
V_{FB}
V_{IN2}
100Ω
2142-14

Figure 5. Two Channel Multiplexer

Power
MOSFET
Drivers

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Power MOSFET Driver

Single	Dual	Features	Ipeak	R_{ON}	Tr/Tf	V_{SUPPLY}	Package P = Pins N = PDIP S = SOIC M = SOL
EL7104C		Non-Inverting	4A	3Ω	20 ns/20 ns	16.5V	8P-N-S
EL7114C		Inverting/Iso-Drains	4A	3Ω	20 ns/20 ns	16.5V	8P-N-S
*EL7134C		3-State	4A	3Ω	20 ns/20 ns	16.5V	8P-N-S
EL7144C		2-Input Logic AND	4A	3Ω	20 ns/20 ns	16.5V	8P-N-S
	EL7202C	Non-Inverting	2A	6Ω	20 ns/20 ns	16.5V	8P-N-S
	EL7212C	Inverting	2A	6Ω	20 ns/20 ns	16.5V	8P-N-S
	EL7222C	Complimentary Output	2A	6Ω	20 ns/20 ns	16.5V	8P-N-S
	*EL7232C	3-State	2A	6Ω	20 ns/20 ns	16.5V	8P-N-S
	EL7242C	2-Input Logic AND	2A	6Ω	20 ns/20 ns	16.5V	8P-N-S
	EL7243C	Logic AND/OR Output	2A	6Ω	20 ns/20 ns	16.5V	20P-M
	EL7252C	2-Input Logic NAND	2A	6Ω	20 ns/20 ns	16.5V	8P-N-S
	EL7262C	Inverting/Iso-Drains	2A	6Ω	20 ns/20 ns	16.5V	8P-N-S
	EL7272C	Non-Inverting/Iso-Drains	2A	6Ω	20 ns/20 ns	16.5V	8P-N-S

Programmable Delay Driver

Single	Dual	Features	Ipeak	R_{ON}	Tr/Tf	V_{SUPPLY}	Package P = Pins N = PDIP S = SOIC
EL7861C		User-Defined Polarity	1A	10Ω	40 ns	16.5V	8P-N-S
	EL7961C	Non-Inverting w/Enable	1A	10Ω	40 ns	16.5V	8P-N-S
	EL7971C	Inverting w/Enable	1A	10Ω	40 ns	16.5V	8P-N-S
	EL7981C	Complimentary w/Enable	1A	10Ω	40 ns	16.5V	8P-N-S
	EL7962C	Non-Invert w/Independent Delay	1A	10Ω	40 ns	16.5V	8P-N-S
	EL7972C	Inverting w/Independent Delay	1A	10Ω	40 ns	16.5V	8P-N-S
	EL7982C	Comp Outputs w/Independent Delay	1A	10Ω	40 ns	16.5V	8P-N-S

*For these datasheets see: Application Specific—A.T.E.

Power Supply Bridge Drivers

Single	Dual	Features	Ipeak	R_{ON}	Tr/Tf	V_{SUPPLY}	Package P = Pins N = PDIP S = SOIC
EL7501C		High-Side Driver	1A	10Ω	100 ns	16.5V	8P-N-S
	EL7661C	Full Bridge Driver	1A	10Ω	100 ns	16.5V	18P-N
	EL7761C	Half Bridge Driver	1A	10Ω	100 ns	16.5V	16P-N-S

Special Function Drivers

Dual	Quad	Features	Ipeak	R_{ON}	Tr/Tf	V_{SUPPLY}	Package P = Pins N = PDIP S = SOIC M = SOL
	EL7412C	Integrated 4-Channel Driver	2A	6Ω	20 ns/20 ns	16.5V	20P-M
EL7182C		2 Phase CCD Driver	2A	6Ω	20 ns/20 ns	16.5V	8P-N-S
EL7240C		Non-Inverting/ −V Outputs	2A	3Ω	20 ns/20 ns	16.5V	8P-N-S
EL7241C		Inverting/ − Outputs	2A	3Ω	20 ns/20 ns	16.5V	8P-N-S
*EL7154C		ATE/ + 15V ro −5V Outputs Level Shifter/3-State	2A	2.5Ω	20 ns/20 ns	16.5V	8P-N-S

Application Specific - DC:DC Converters - For Datasheets, see Power Product Section

Single		Features	Ipeak	V_{OUT}	Accuracy	V_{SUPPLY}	Package P = Pins M = SOL
**EL7560C	Ext Ref	Integrated PWM + FETs IC	12.4A	2.1V−3.5V	1%	6V	28P-M †
**EL7561C	Int Ref	Integrated PWM + FETs IC	12.4A	2.1V−3.5V	1%	6V	28P-M †
**EL7556C	Int Ref	Integrated PWM + FETs IC	6A	Variable	1%	6V	28P-M †
**EL7571C	Int Ref	PWM Controller IC	Variable	1.3V−3.5V	1%	4.5V−13.2V	20P-M †

*For these datasheets see: Application Specific—A.T.E.

**For datasheets see: Application Specific—Data Processing

†See Ordering Information section in this databook.

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7104C/EL7114C

High Speed, Single Channel, Power MOSFET Drivers

Features

- Industry standard driver replacement
- Improved response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating range
- Separate drain connections

Applications

- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Resonant charging
- Cascoded drivers

Ordering Information

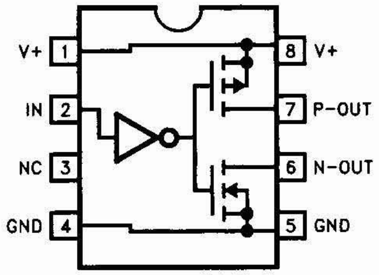
Part No.	Temp. Range	Pkg.	Outline #
EL7104CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7104CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL7114CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7114CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL7104C/EL7114C ICs are matched driver ICs that improve the operation of the industry standard TC-4420/29 clock drivers. The Elantec versions are very high speed drivers capable of delivering peak currents of 4A into highly capacitive loads. The high speed performance is achieved by means of a proprietary "Turbo-Driver" circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices.

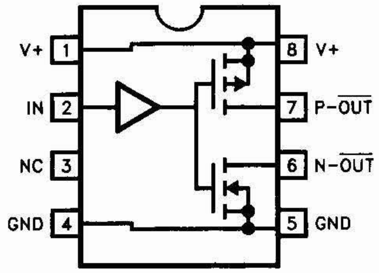
Connection Diagrams

EL7104C
Non-Inverting Driver



7104-1

EL7114C
Inverting Driver



7104-2

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V
Input Pins	−0.3V to +0.3V above V+
Peak Output Current	4A
Storage Temperature Range	−65°C to +150°C
Ambient Operating Temperature	−40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	
SOIC	570 mW
PDIP	1050 mW

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

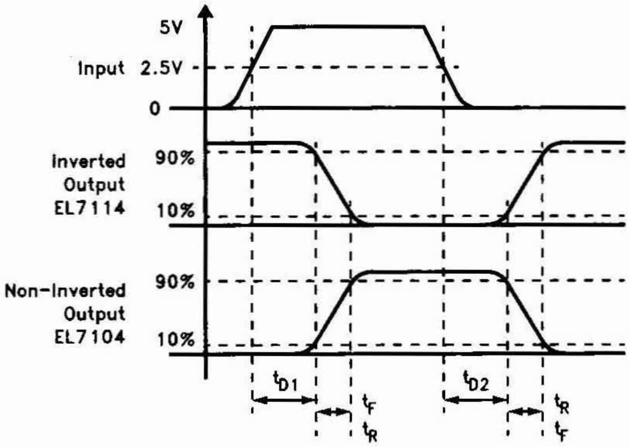
DC Electrical Characteristics $T_A = 25°C$, V+ = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	μA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	μA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		1.5	4	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		2	4	I	Ω
I_{OUT}	Output Current	V+/GND		0.2	10	I	μA
I_{PK}	Peak Output Current	Source Sink		4 4		IV	A
I_{DC}	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I_S	Power Supply Current	Input = V+ EL7104 EL7114		4.5 1	7.5 2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

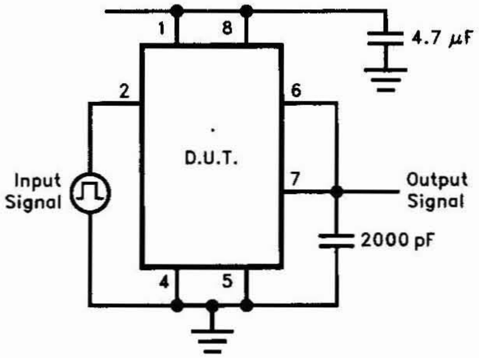
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 1000 pF C_L = 2000 pF		7.5 10	 20	IV	ns
t_F	Fall Time	C_L = 1000 pF C_L = 2000 pF		10 15	 20	IV	ns
$t_{D\text{-}ON}$	Turn-On Delay Time	See Timing Table		18	25	IV	ns
$t_{D\text{-}OFF}$	Turn-Off Delay Time	See Timing Table		18	25	IV	ns

Timing Table


5V
Input 2.5V
0
Inverted Output EL7114
90%
10%
Non-Inverted Output EL7104
90%
10%
t_{D1}
t_F
t_R
t_{D2}
t_R
t_F

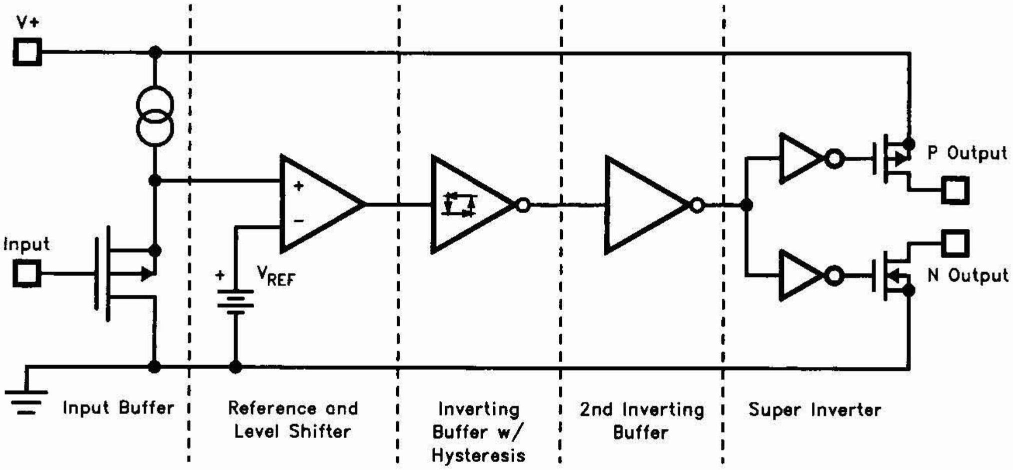
7104-3

Standard Test Configuration


1
8
4.7 μF
2
6
D.U.T.
Input Signal
7
Output Signal
2000 pF
4
5

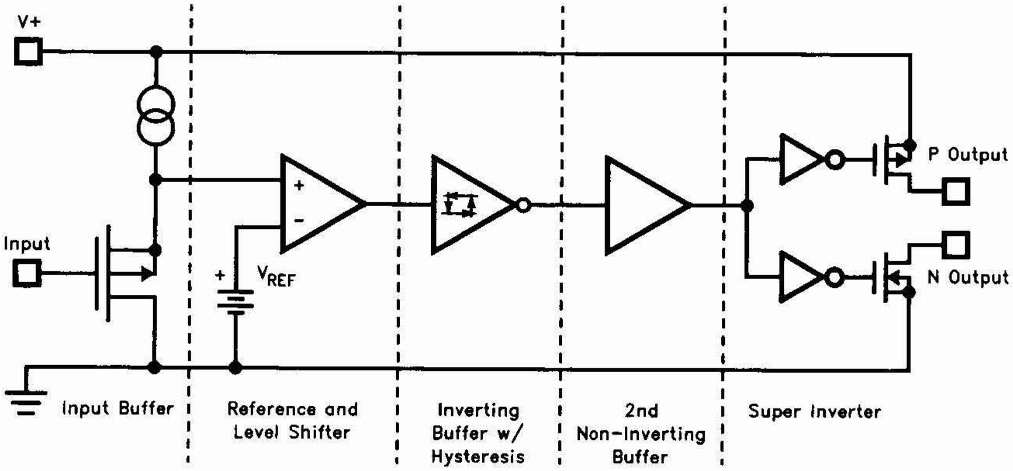
7104-4

7104C Simplified Schematic


V+
Input
+
-
+
V_{REF}
P Output
N Output
Input Buffer
Reference and
Level Shifter
Inverting
Buffer w/
Hysteresis
2nd Inverting
Buffer
Super Inverter

7104-5

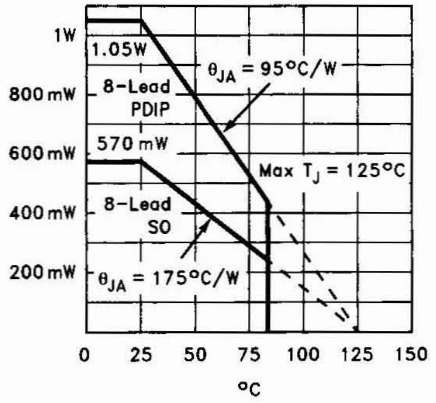
7114C Simplified Schematic


V+
Input
+
-
+
V_{REF}
P Output
N Output
Input Buffer
Reference and
Level Shifter
Inverting
Buffer w/
Hysteresis
2nd
Non-Inverting
Buffer
Super Inverter

7104-6

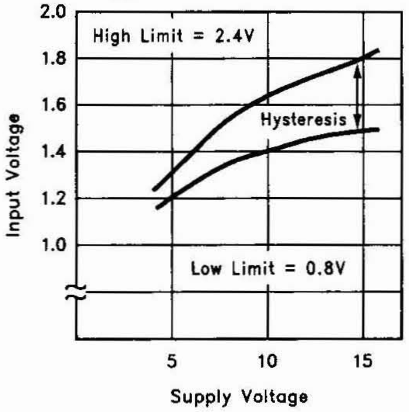
Typical Performance Curve

Max Power/Derating Curves



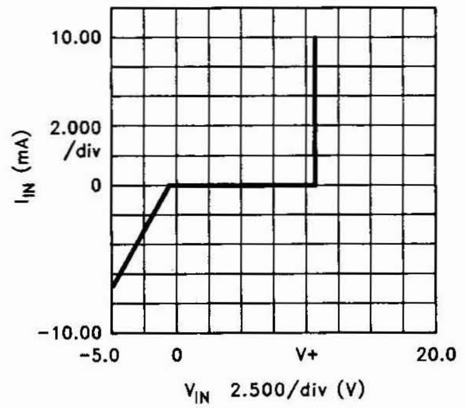
7104-7

Switch Threshold vs Supply Voltage



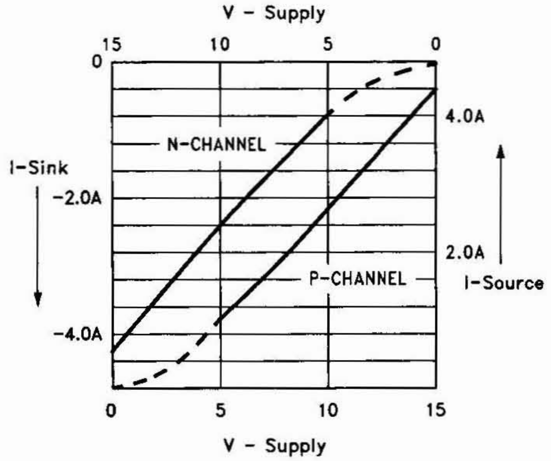
7104-8

Input Current vs Voltage



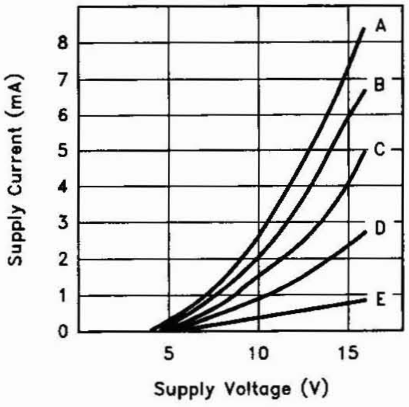
7104-9

Peak Drive vs Supply Voltage



7104-10

Quiescent Supply Current

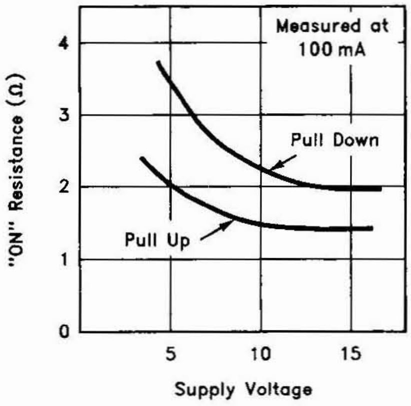


CASE:

Device	Input Level	Curve
EL7104	GND	A
EL7104	V+	C
EL7114	GND	C
EL7114	V+	E

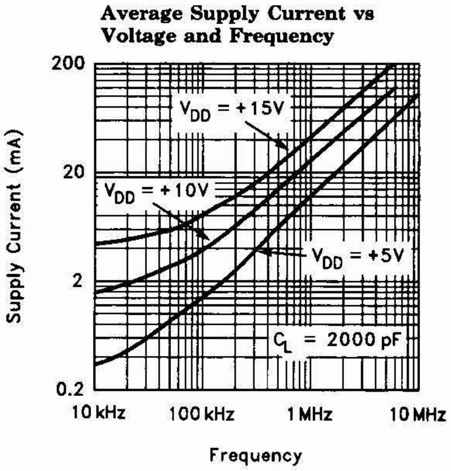
7104-11

"ON" Resistance vs Supply Voltage

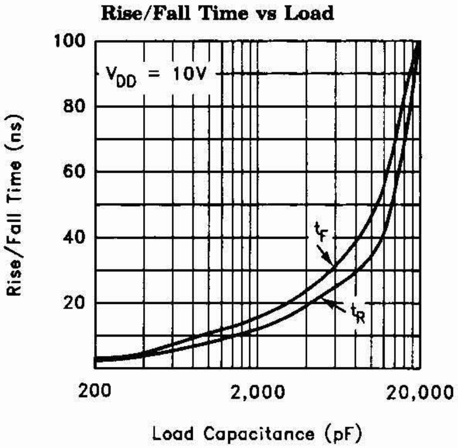


7104-12

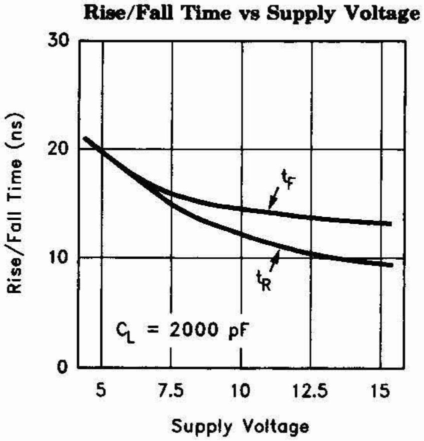
Typical Performance Curve — Contd.



7104-13

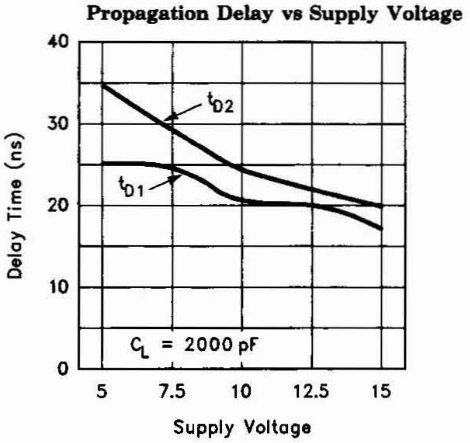


7104-15

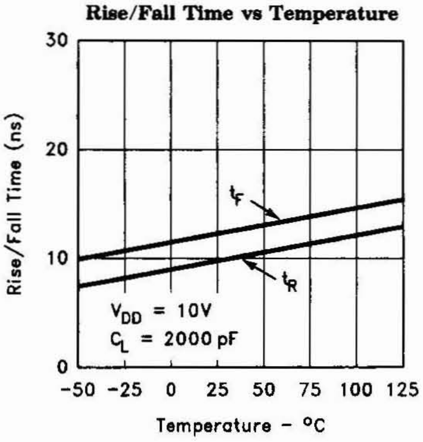


7104-16

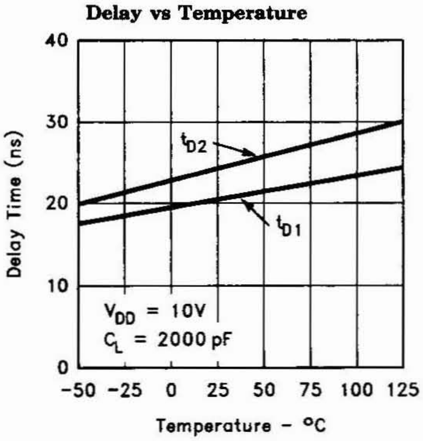
Typical Performance Curve — Contd.



7104-17



7104-18



7104-19

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7144C

Dual Input, High Speed, High Current Power MOSFET Driver

Features

- Logic and input
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 4A Peak drive
- Isolated drains
- Low output impedance—2.5Ω
- Low quiescent current—5 mA
- Wide operating voltage—4.5V–16V

Applications

- Short circuit protected switching
- Under-voltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Asymmetrical switching
- Resonant charging
- Cascoded switching

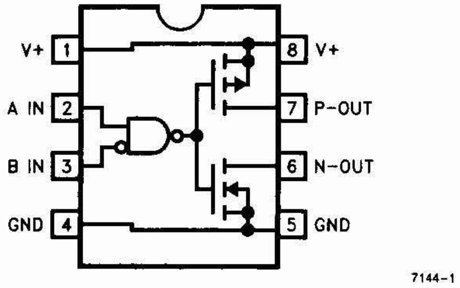
Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL7144CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7144CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL7144C dual input, driver achieves excellent switching while providing added flexibility. The 2-input logic and configuration coupled with the "isolated drains" makes this part well suited for various driver applications requiring an asymmetrical drive, resonant charging, and gated control. Providing twice as much drive as the EL7242 family, the EL7144C is excellent for driving large power MOSFET's and other capacitive loads.

Connection Diagram



Top View

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

January 1996 Rev. B

EL7144C

Dual Input, High Speed, High Current Power MOSFET Driver

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Peak Output Current	4A	SOIC	570 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

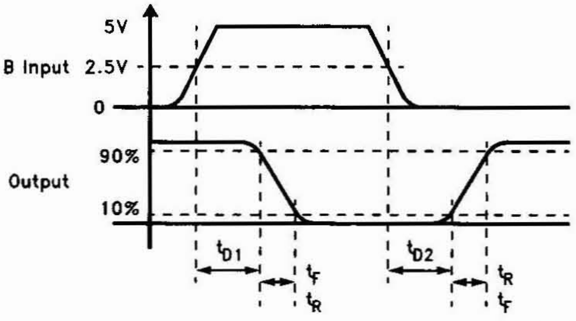
DC Electrical Characteristics $T_A = 25°C$, V+ = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	V_{IH} = V+		0.1	10	I	μA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	V_{IL} = GND		0.1	10	I	μA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		1.5	4	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		2	4	I	Ω
I_{OUT}	Output Leakage Current	V+/GND		0.2	10	I	μA
I_{PK}	Peak Output Current	Source Sink		4 4		V	A
I_{DC}	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I_S	Power Supply Current	Inputs V+		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

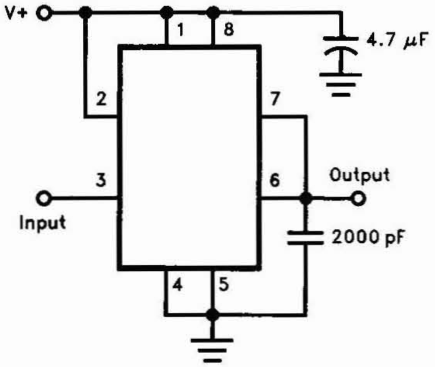
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 1000 pF C_L = 2000 pF		7.5 10	 20	IV	ns
t_F	Fall Time	C_L = 1000 pF C_L = 2000 pF		10 13	 20	IV	ns
$t_{D\text{-}ON}$	Turn-On Delay Time	See Timing Table		18	25	IV	ns
$t_{D\text{-}OFF}$	Turn-Off Delay Time	See Timing Table		20	25	IV	ns

Timing Table



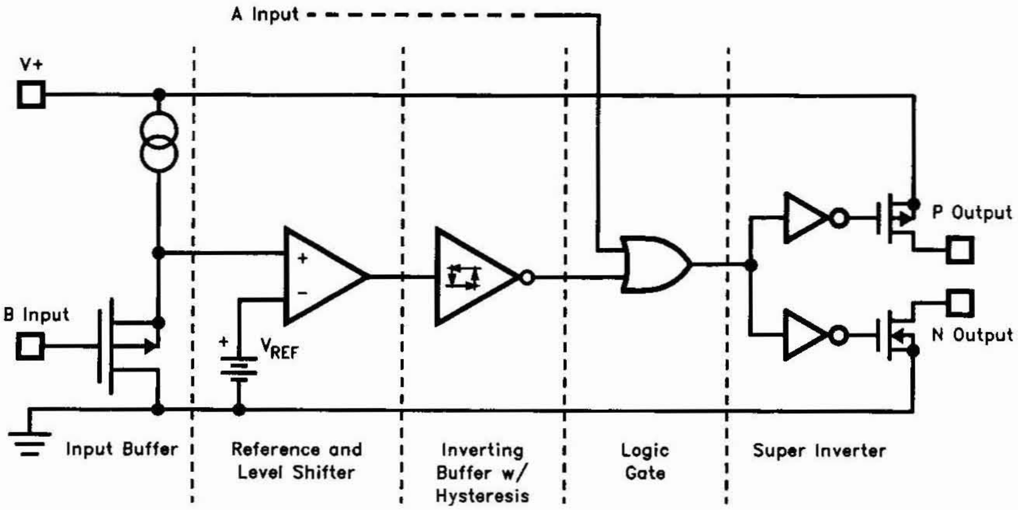
7144-2

Standard Test Configuration


V+
1
8
4.7 μF
2
7
3
6
Output
Input
2000 pF
4
5

7144-3

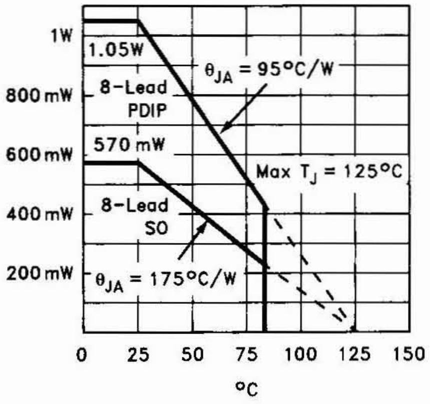
Simplified Schematic


A Input
V+
P Output
B Input
V_{REF}
N Output
Input Buffer
Reference and Level Shifter
Inverting Buffer w/ Hysteresis
Logic Gate
Super Inverter

7144-4

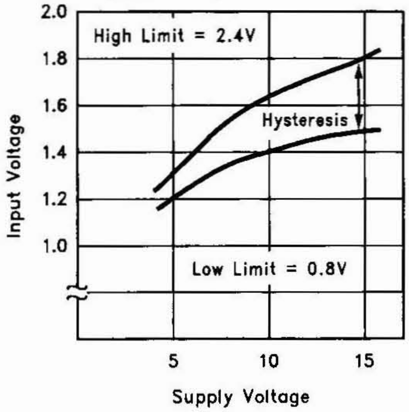
Typical Performance Curve

Max Power/Derating Curves



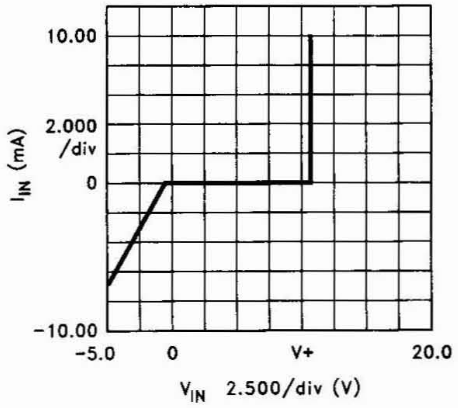
7144-5

Switch Threshold vs Supply Voltage



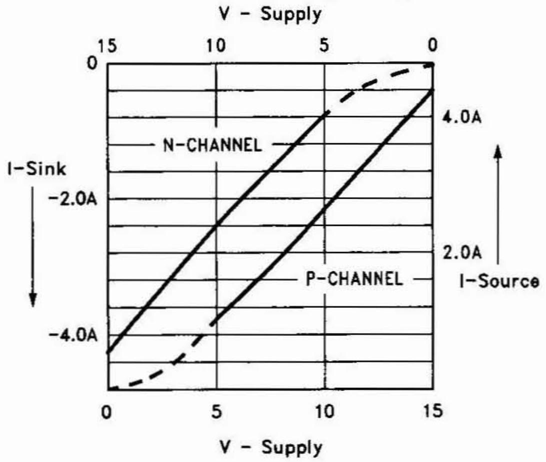
7144-6

Input Current vs Voltage



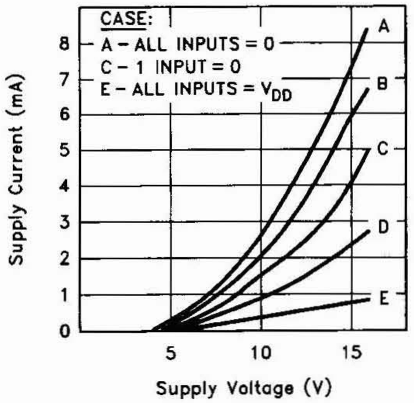
7144-7

Peak Drive vs Supply Voltage



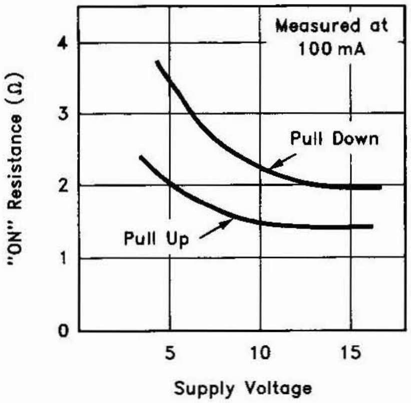
7144-8

Quiescent Supply Current



7144-9

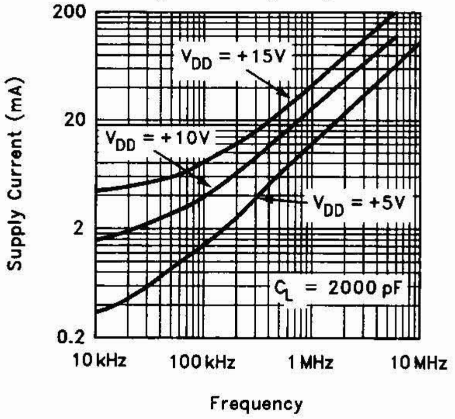
"ON" Resistance vs Supply Voltage



7144-10

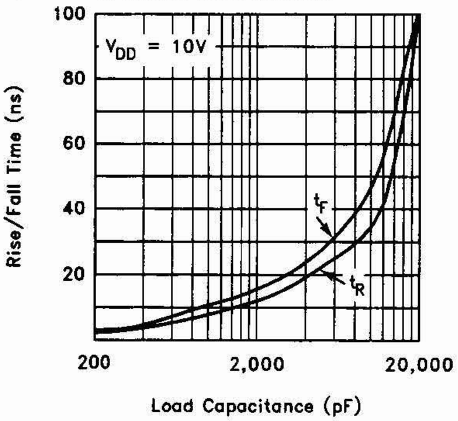
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



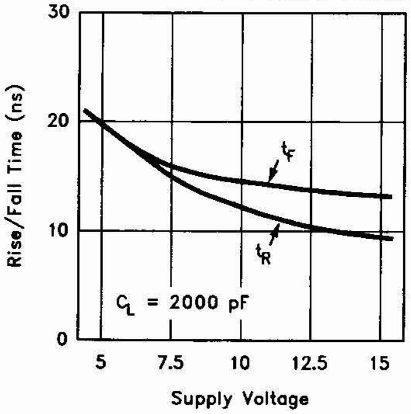
7144-11

Rise/Fall Time vs Load



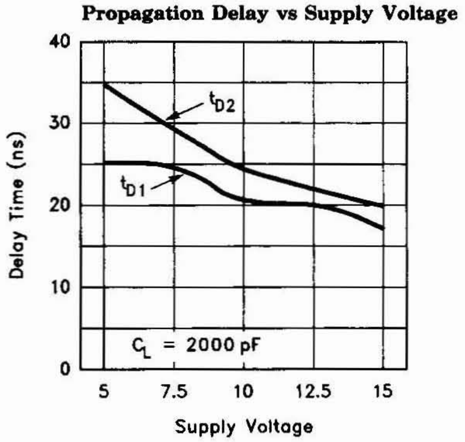
7144-13

Rise/Fall Time vs Supply Voltage

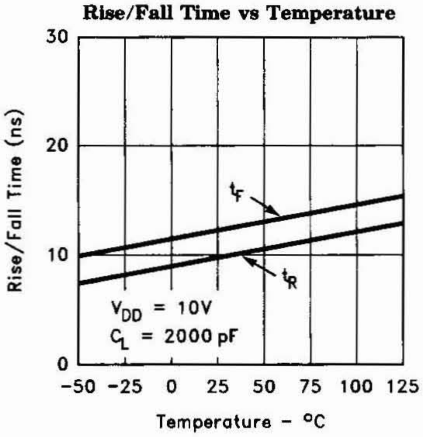


7144-14

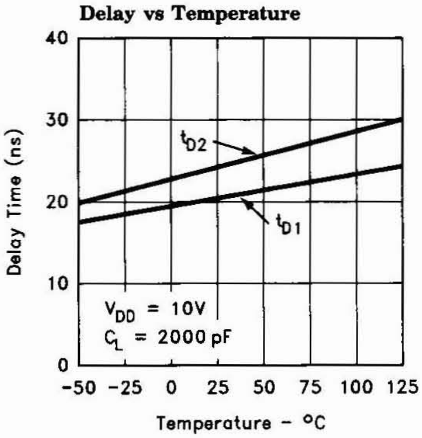
Typical Performance Curve — Contd.



7144-15



7144-16



7144-17

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7182C
2-Phase, High Speed CCD Driver

Features

- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- Reduced clock skew
- 20 ns Switching/delay time
- 2A Peak drive
- Low quiescent current
- Wide operating voltage—4.5V–16V

Applications

- CCD Drivers requiring high-contrast imaging
- Differential line drivers
- Push-pull circuits

Ordering Information

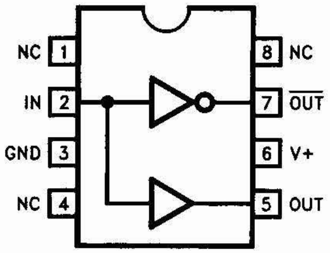
Part No.	Temp. Range	Pkg.	Outline #
EL7182CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7182CS	−40°C to +85°C	8-Pin SO	MDP0027

General Description

The EL7182C is extremely well suited for driving CCD's, especially where high contrast imaging is desirable. The 16V supply rating is attractive for higher voltage CCD applications, as in color fax machines. The input is TTL and 3V compatible. The low quiescent current requirement is advantageous in portable/battery powered systems. The EL7182 is available in 8-pin P-DIP and 8-lead SO packages.

Connection Diagram

EL7182C



7182-1

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

January 1996 Rev. B

EL7182C

2-Phase, High Speed CCD Driver

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V
Input Pins	−0.3V to +0.3V above V+
Combined Peak Output Current	4A
Storage Temperature Range	−65°C to +150°C
Ambient Operating Temperature	−40°C to +85°C

Operating Junction Temperature	125°C
Power Dissipation	
SOIC	570 mW
PDIP	1050 mW

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

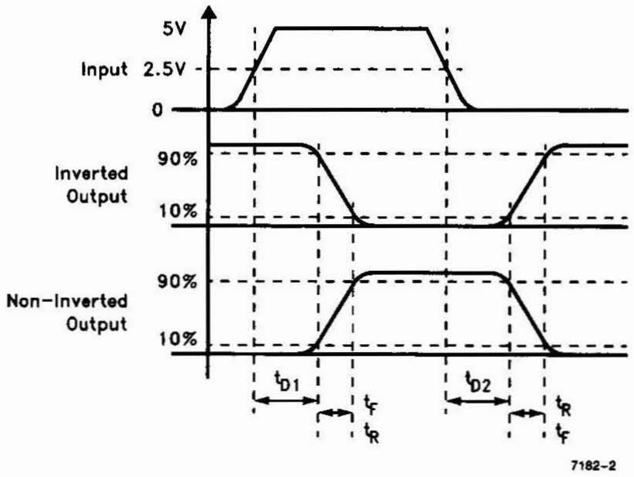
DC Electrical Characteristics $T_A = 25°C$, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	μA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	μA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	$I_{OUT} = -100$ mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	$I_{OUT} = +100$ mA		4	6	I	Ω
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Input High		2.5	5	I	mA
V_S	Operating Voltage		4.5		16	I	V

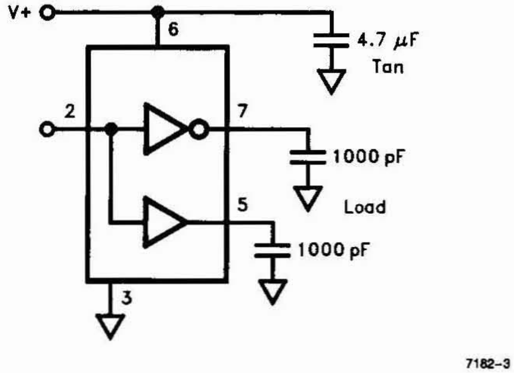
AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		7.5 10	 20	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		10 13	 20	IV	ns
$t_{D\text{-}ON}$	Turn-On Delay Time			18	25	IV	ns
$t_{D\text{-}OFF}$	Turn-Off Delay Time			20	25	IV	ns

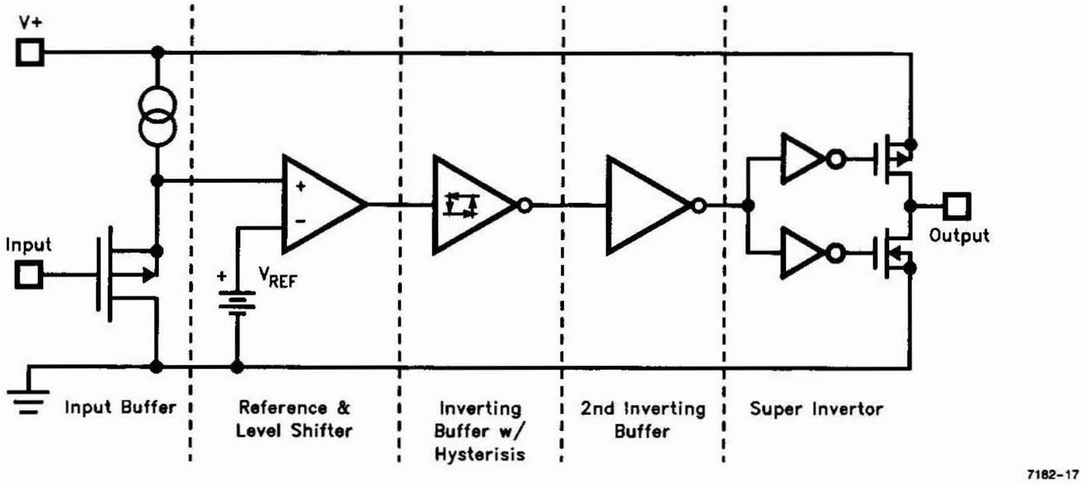
Timing Table


5V
Input 2.5V
0
90%
Inverted Output
10%
90%
Non-Inverted Output
10%
tD1
tF
tR
tD2
tR
tF
7182-2

Standard Test Configuration

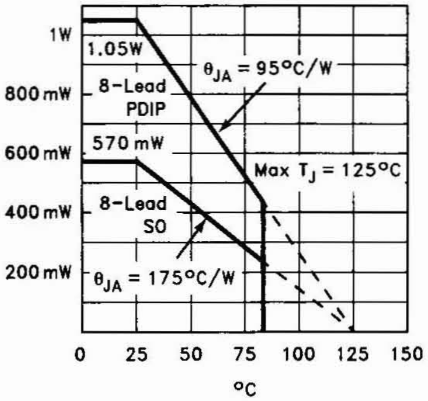

V+
6
4.7 μF
Tan
2
7
1000 pF
5
Load
1000 pF
3
7182-3

Simplified Schematic


V+
Input
+
-
+
VREF
Output
Input Buffer
Reference & Level Shifter
Inverting Buffer w/ Hysterisis
2nd Inverting Buffer
Super Invertor
7182-17

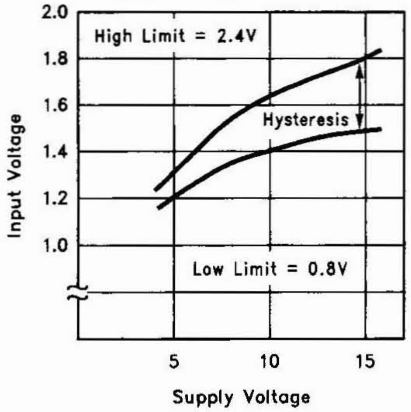
Typical Performance Curve

Max Power/Derating Curves



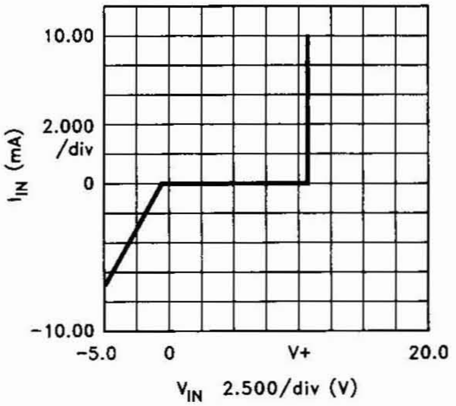
7182-15

Switch Threshold vs Supply Voltage



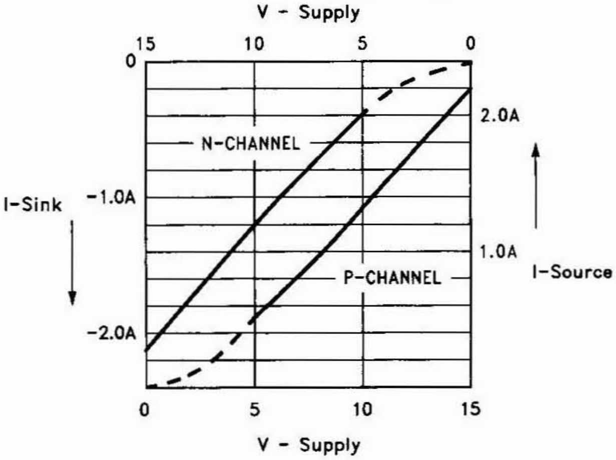
7182-4

Input Current vs Voltage



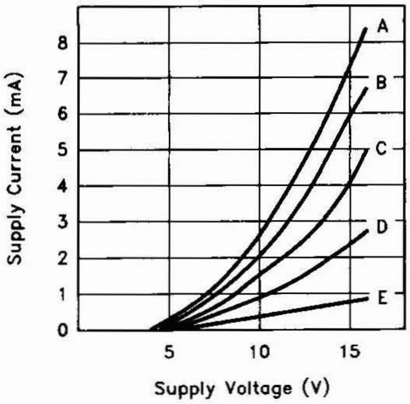
7182-5

Peak Drive vs Supply Voltage



7182-6

Quiescent Supply Current

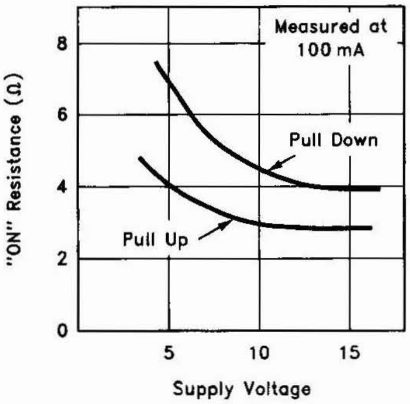


CASE:

Input Level	Curve
GND	B
V+	D

7182-7

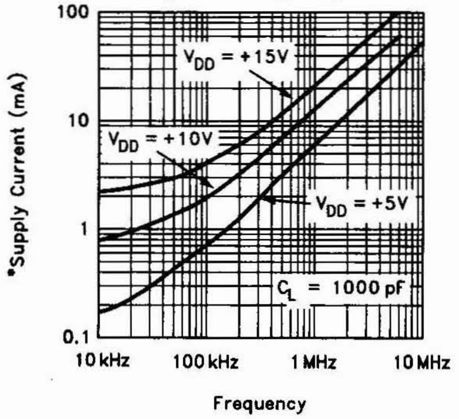
"ON" Resistance vs Supply Voltage



7182-16

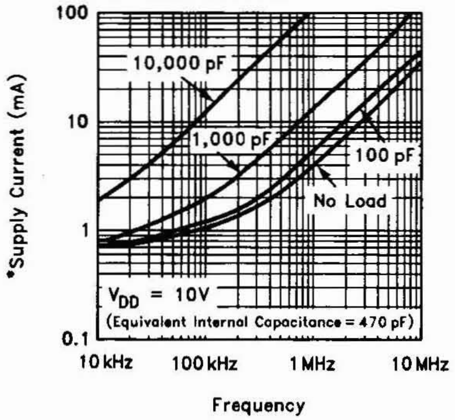
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



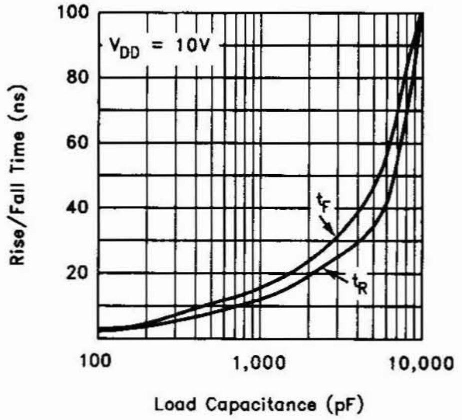
7182-8

Average Supply Current vs Capacitive Load



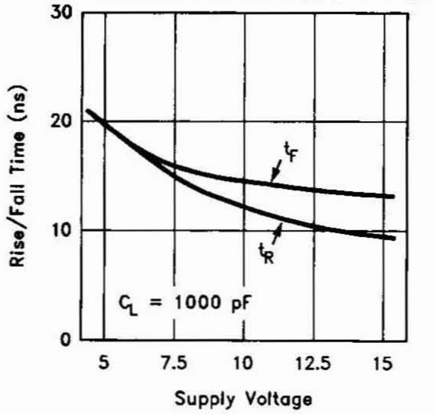
7182-9

Rise/Fall Time vs Load



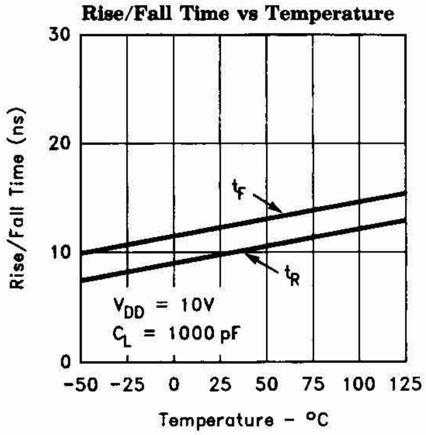
7182-14

Rise/Fall Time vs Supply Voltage

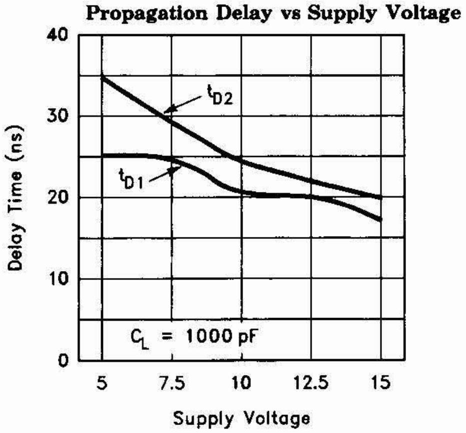


7182-10

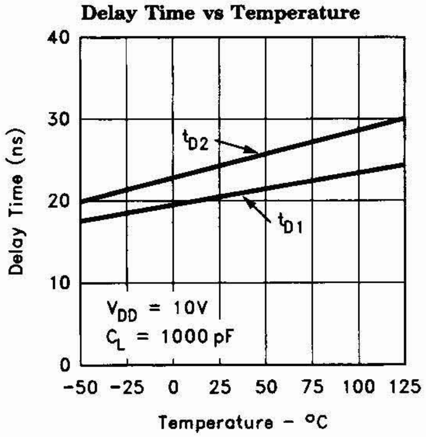
Typical Performance Curve — Contd.



7182-12



7182-11



7182-13

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7202C/7212C/7222C

High Speed, Dual Channel Power MOSFET Drivers

Features

- Industry standard driver replacement
- Improved response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating voltage range

Applications

- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Class D switching amplifiers
- Ultrasonic and RF generators
- Pulsed circuits

Ordering Information

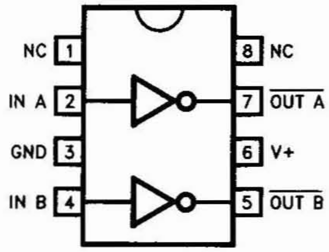
Part No.	Temp. Range	Pkg.	Outline #
EL7202CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7202CS	−40°C to +85°C	8-Pin SO	MDP0027
EL7212CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7212CS	−40°C to +85°C	8-Pin SO	MDP0027
EL7222CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7222CS	−40°C to +85°C	8-Pin SO	MDP0027

General Description

The EL7202C/EL7212C/EL7222C ICs are matched dual-drivers ICs that improve the operation of the industry standard DS0026 clock drivers. The Elantec Versions are very high speed drivers capable of delivering peak currents of 2.0 amps into highly capacitive loads. The high speed performance is achieved by means of a proprietary "Turbo-Driver" circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices. Dynamic switching losses are minimized with non-overlapped drive techniques.

Connection Diagrams

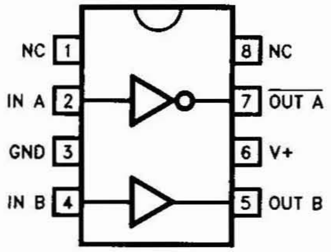
EL7212C



Inverting Drivers

7202-1

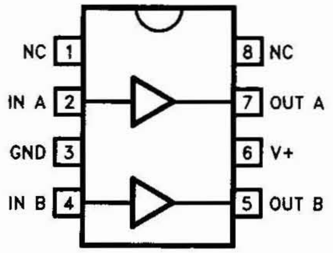
EL7222C



7202-2

Complementary Drivers

EL7202C



7202-3

Non-Inverting Drivers

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

January 1996 Rev. B

EL7202C/EL7212C/EL7222C

High Speed, Dual Channel Power MOSFET Drivers

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V
Input Pins	−0.3V to +0.3V above V+
Combined Peak Output Current	4A
Storage Temperature Range	−65°C to +150°C
Ambient Operating Temperature	−40°C to +85°C

Operating Junction Temperature	125°C
Power Dissipation	
SOIC	570 mW
PDIP	1050 mW

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

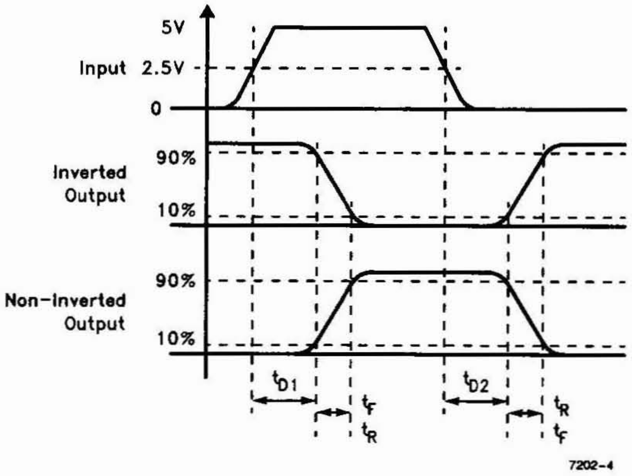
DC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	μA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	μA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		4	6	I	Ω
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Inputs High/7202 Inputs High/7212 Inputs High/7222		4.5 1 2.5	7.5 2.5 5.0	I I I	mA
V_S	Operating Voltage		4.5		15	I	V

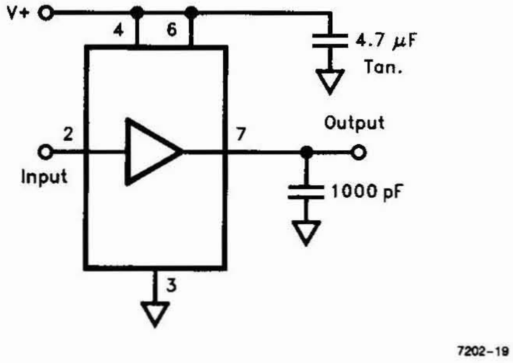
AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		7.5 10	 20	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		10 13	 20	IV	ns
t_{D1}	Turn-On Delay Time	See Timing Table		18	25	IV	ns
t_{D2}	Turn-Off Delay Time	See Timing Table		20	25	IV	ns

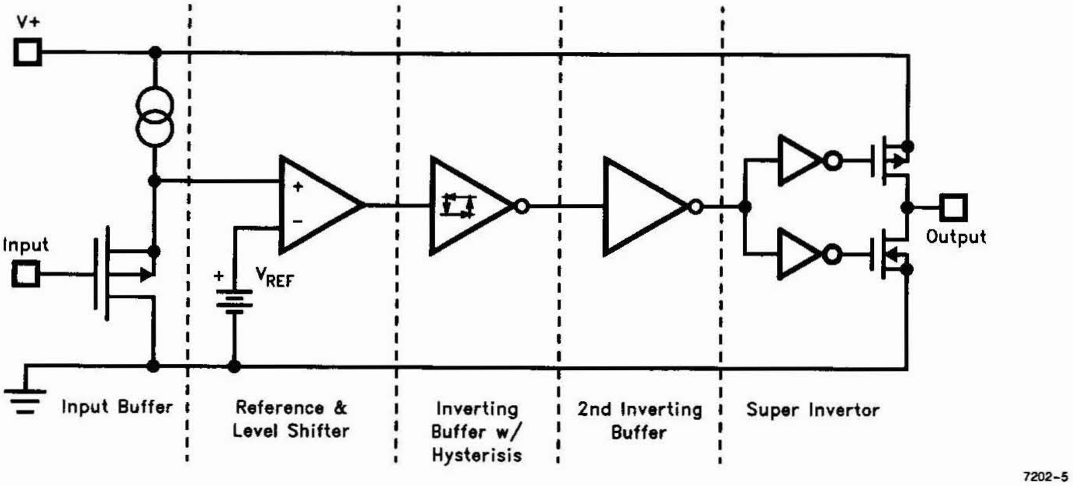
Timing Table



Standard Test Configuration

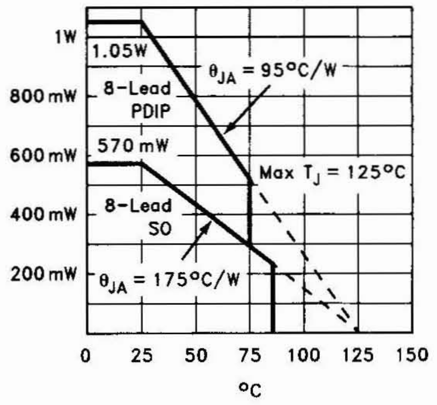

V+
4
6
4.7 μF Tan.
2
7
Output
Input
1000 pF
3
7202-19

Simplified Schematic


V+
Input
V_{REF}
Output
Input Buffer
Reference & Level Shifter
Inverting Buffer w/ Hysterisis
2nd Inverting Buffer
Super Invertor
7202-5

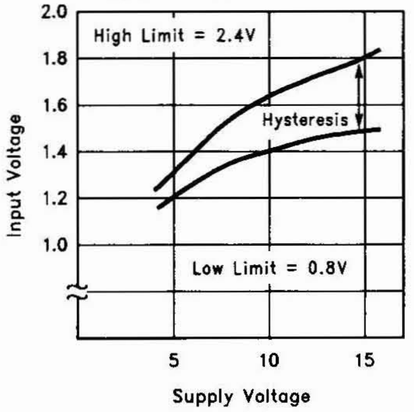
Typical Performance Curve

Max Power/Derating Curves



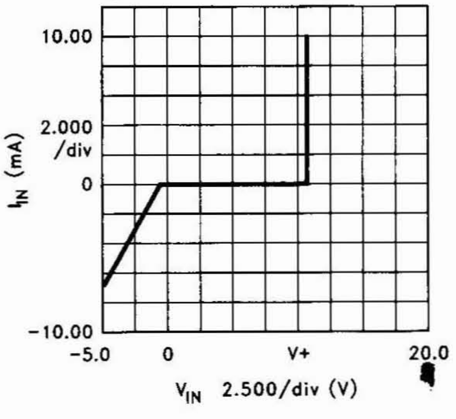
7202-6

Switch Threshold vs Supply Voltage



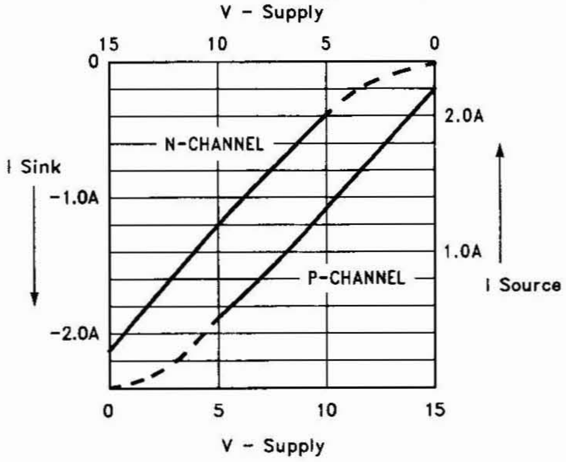
7202-7

Input Current vs Voltage



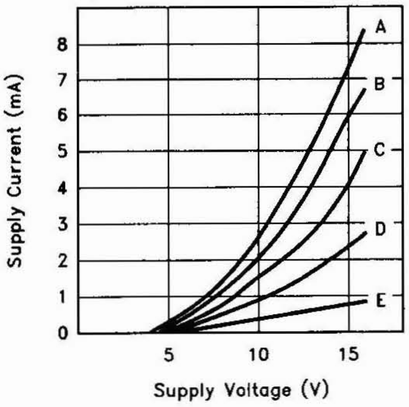
7202-8

Peak Drive vs Supply Voltage



7202-9

Quiescent Supply Current

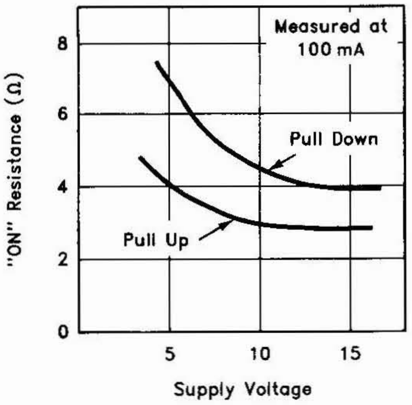


CASE:

Device	Input Level	Curve
EL7202	GND	A
EL7202	GND, V+	B
EL7202	V+	C
EL7212	GND	C
EL7212	GND, V+	D
EL7212	V+	E
EL7222	GND	B
EL7222	GND, V+	C
EL7222	V+	D

7202-10

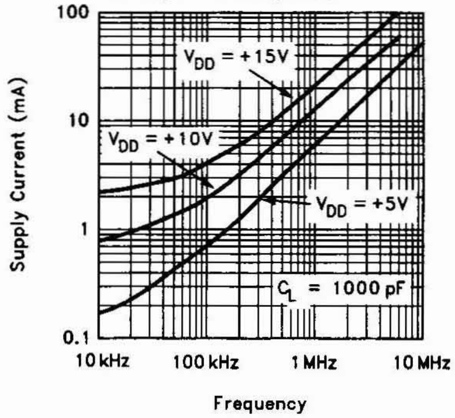
"ON" Resistance vs Supply Voltage



7202-11

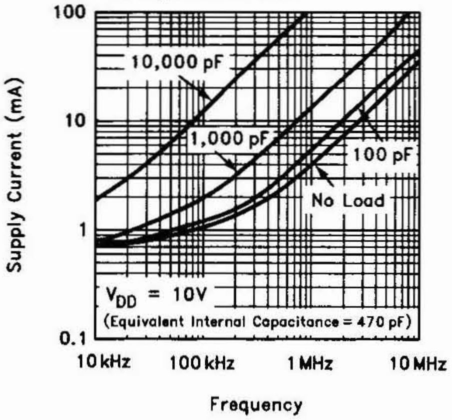
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



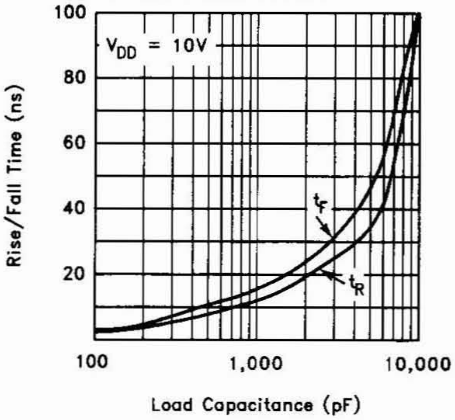
7202-12

Average Supply Current vs Capacitive Load



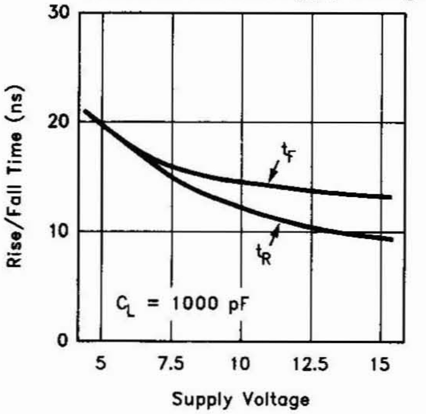
7202-13

Rise/Fall Time vs Load



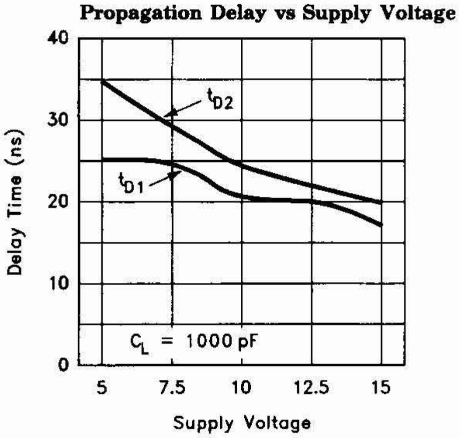
7202-14

Rise/Fall Time vs Supply Voltage

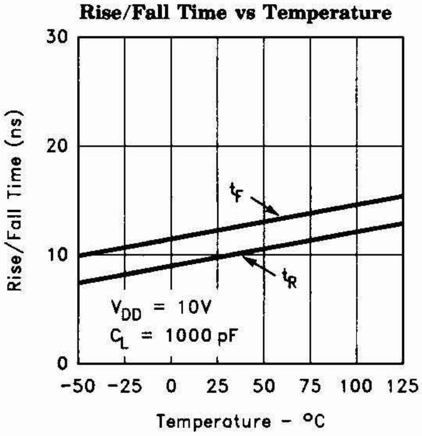


7202-15

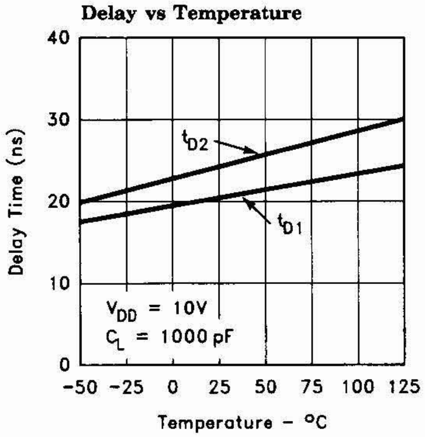
Typical Performance Curve — Contd.



7202-16

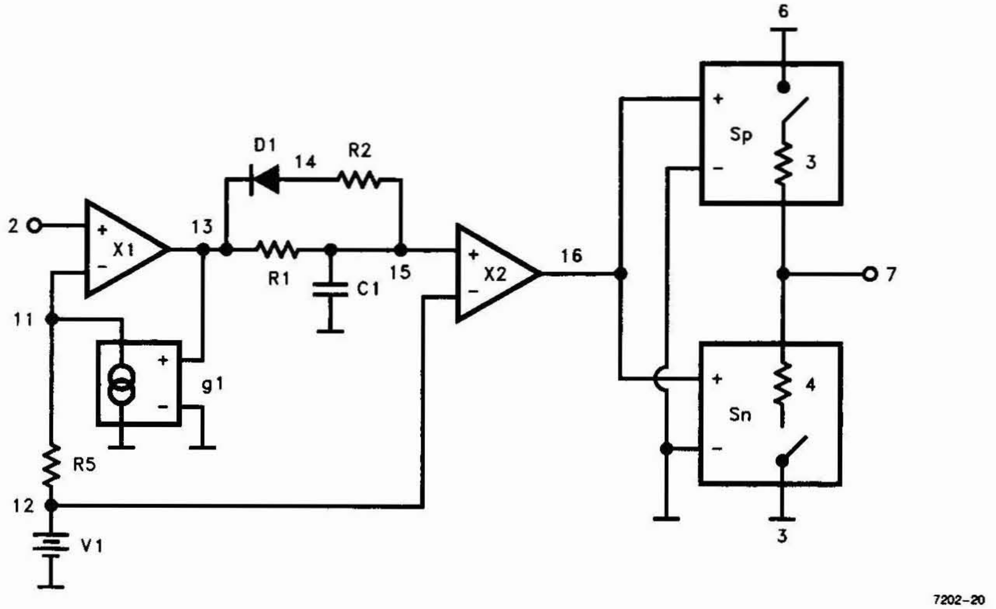


7202-17



7202-18

EL7212 Macro Model



```
**** EL7212 model ****
*               input
*               |        gnd
*               |        |        Vsupply
*               |        |        |        Vout
.subckt M7212   2        3        6        7
V1 12 3 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 3 43.3 pF
D1 14 13 dmod
X1 13 11 2 3 comp1
X2 16 12 15 3 comp1
sp 6 7 16 3 spmod
sn 7 3 16 3 snmod
g1 11 0 13 0 938μ
.model dmod d
.model spmod vswitch ron=3 roff=2meg von=1 voff=1.5
.model snmod vswitch ron=4 roff=2meg von=3 voff=2
.ends M7212
.subckt comp1 out inp inm vss
e1 out vss table { (v(inp) –v(inm))* 5000} = (0,0) (3.2,3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
.ends comp1
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7240C/EL7241C
High Speed Coil Drivers

Features

- 20 ns Propagation delay
- Clock to 10 MHz
- 2 Amp peak output drive
- 3Ω output impedance
- 3V/5V Logic input compatible
- Outputs "OK" below ground
- Operating voltage 4.5V to 16V

Applications

- Tape drive-write head driver
- Current switching
- Center-Tapped transformer driver
- ATE-pin drivers
- Analog switching
- AC switching
- T - switch

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7240CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7240CS	−40°C to +85°C	8-Pin P-SOIC	MDP0027
EL7241CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7241CS	−40°C to +85°C	8-Pin P-SOIC	MDP0027

Operating Voltage Range

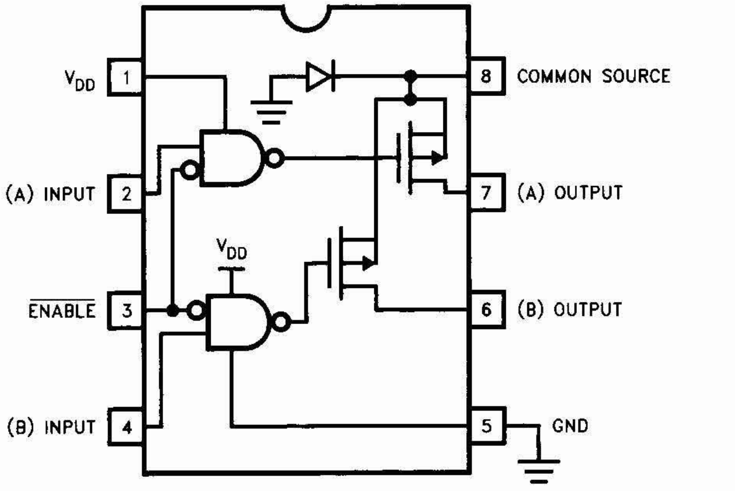
Pins	Min/Max (Volts)
V_{DD}/GND	4.5/16
V_{DD}/Output	0/−20
Source/Output	0/−16
Output/GND	16/−10

General Description

The EL7240C/EL7241C high speed coil drivers accept logic inputs which independently control a pair of 3Ω PMOS FET's. The output transistors share a common source, making these devices well suited for "current steering" and analog switching applications. The typical clamping diodes to ground are removed, thus allowing pins (6) and (7) to swing negative. This feature is desirable when driving "center-tapped" coils referenced to ground. The logic "NAND" input configuration can be used to "enable" the outputs. The EL7240C and EL7241C differ only by their logic polarity.

Connection Diagrams

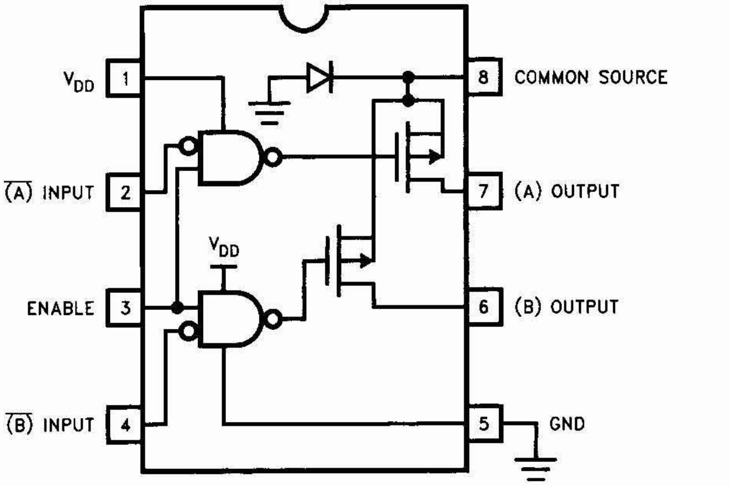
EL7240C



V_{DD}
1
8
COMMON SOURCE
(A) INPUT
2
7
(A) OUTPUT
V_{DD}
$\overline{\text{ENABLE}}$
3
6
(B) OUTPUT
(B) INPUT
4
5
GND

7240-1

EL7241C



V_{DD}
1
8
COMMON SOURCE
$\overline{\text{(A)}}$ INPUT
2
7
(A) OUTPUT
V_{DD}
ENABLE
3
6
(B) OUTPUT
$\overline{\text{(B)}}$ INPUT
4
5
GND

7240-2

Absolute Maximum Ratings

Supply (V+ to GND)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current	4A	SOIC	570 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

DC Electrical Characteristics $T_A = 25°C$, $V = 15V$ unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	µA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{ON}	Pull-Up Resistance	$I_{OUT} = -100$ mA		3	6	I	Ω
I_{OFF}	Off Leakage	$V_{OUT} = 0V$	0.2		10	I	µA
I_{PK}	Peak Output Current	Source		2.0		IV	A
I_{DC}	Continuous Output Current	Channel	100			I	mA
V_S	Source Potential with Grounded Drain	Channel A or B 100 mA Load		2.3	2.75	I	V
Power Supply							
I_S	Power Supply Current	Inputs High		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

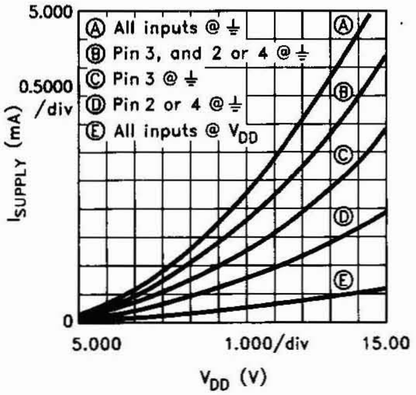
AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
$t_{D\text{-}ON}$	Turn-On Delay Time			18	25	IV	ns
$t_{D\text{-}OFF}$	Turn-Off Delay Time			20	25	IV	ns

Rise and Fall times (t_R and t_F) are load dependant.

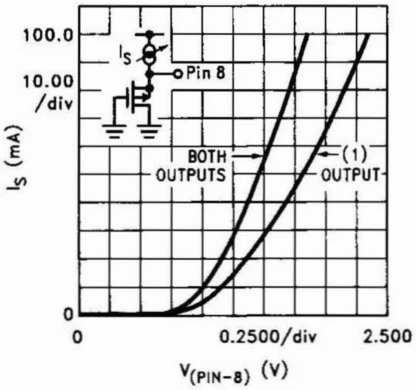
Typical Performance Curves

Supply Current vs V_{DD} and Input Connection



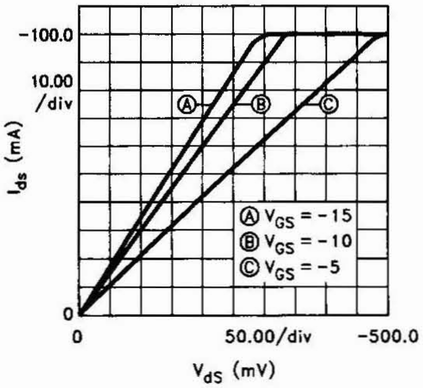
7240-3

Source Voltage vs Current (Grounded Drain)



7240-4

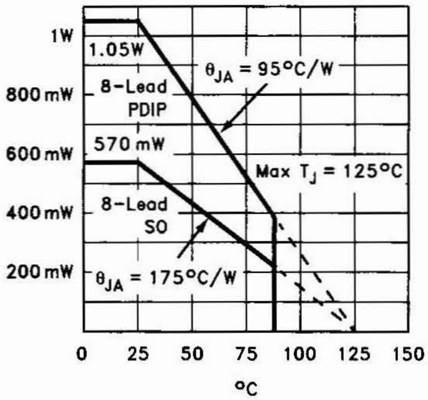
Output Conduction vs V_{GS}



7240-5

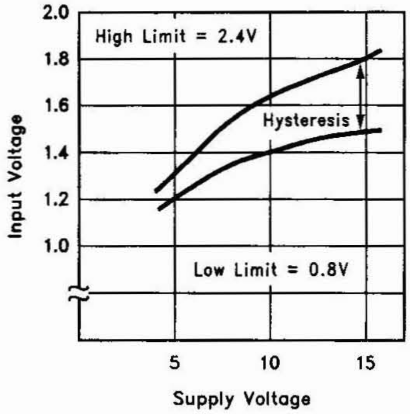
Typical Performance Curves — Contd.

Max Power/Derating Curves



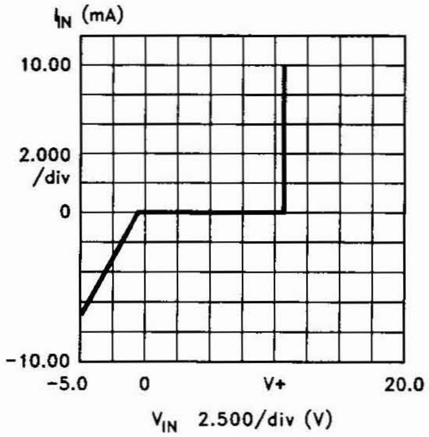
7240-6

Switch Threshold vs Supply Voltage



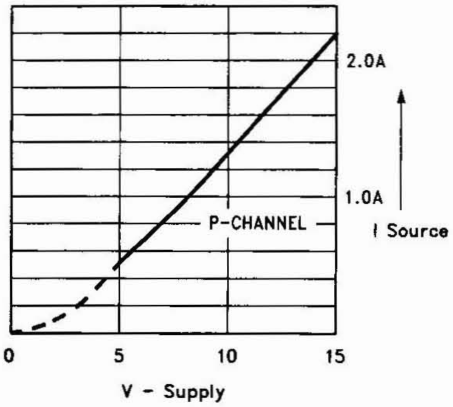
7240-7

Input Current vs Voltage



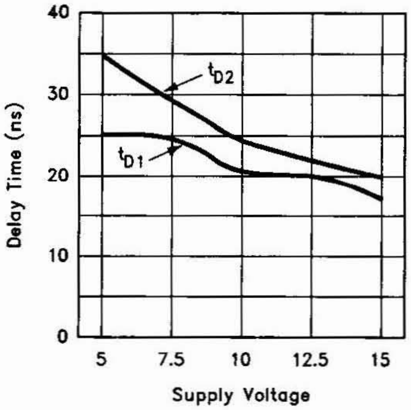
7240-8

Peak Drive vs Supply Voltage



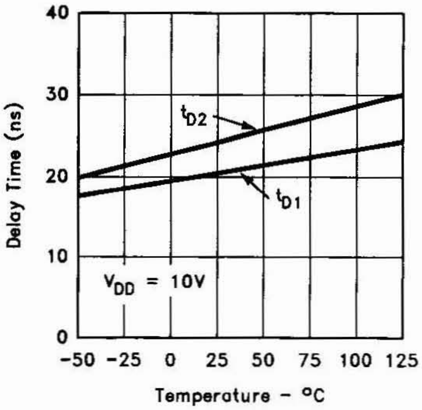
7240-9

Propagation Delay vs Supply Voltage



7240-10

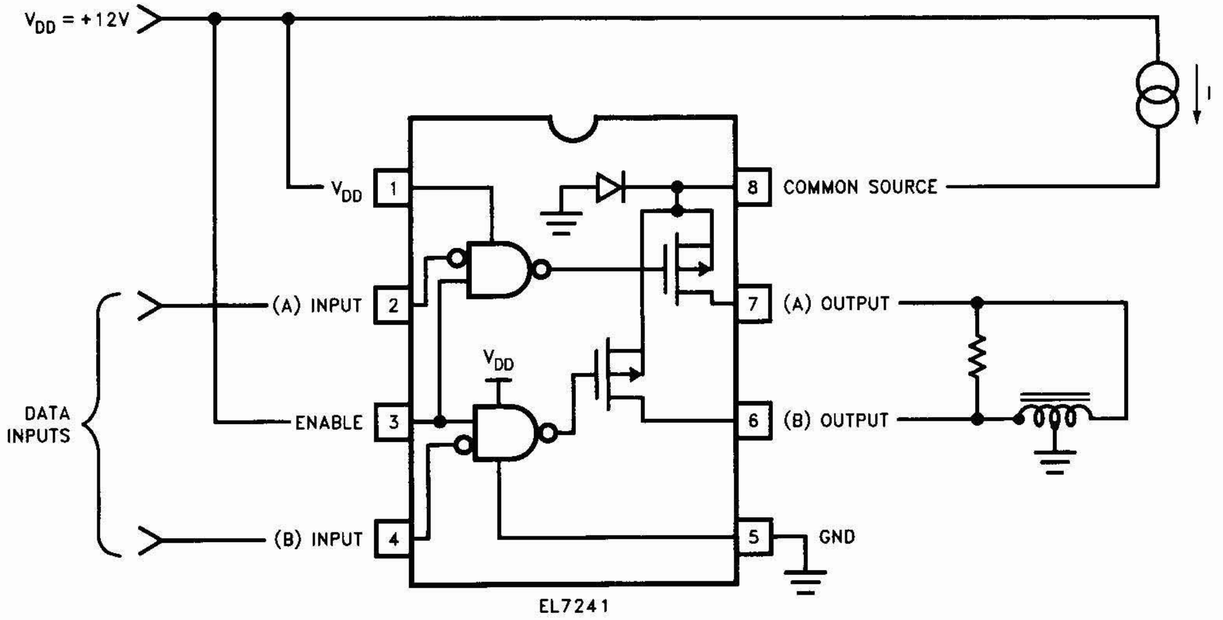
Delay vs Temperature



7240-11

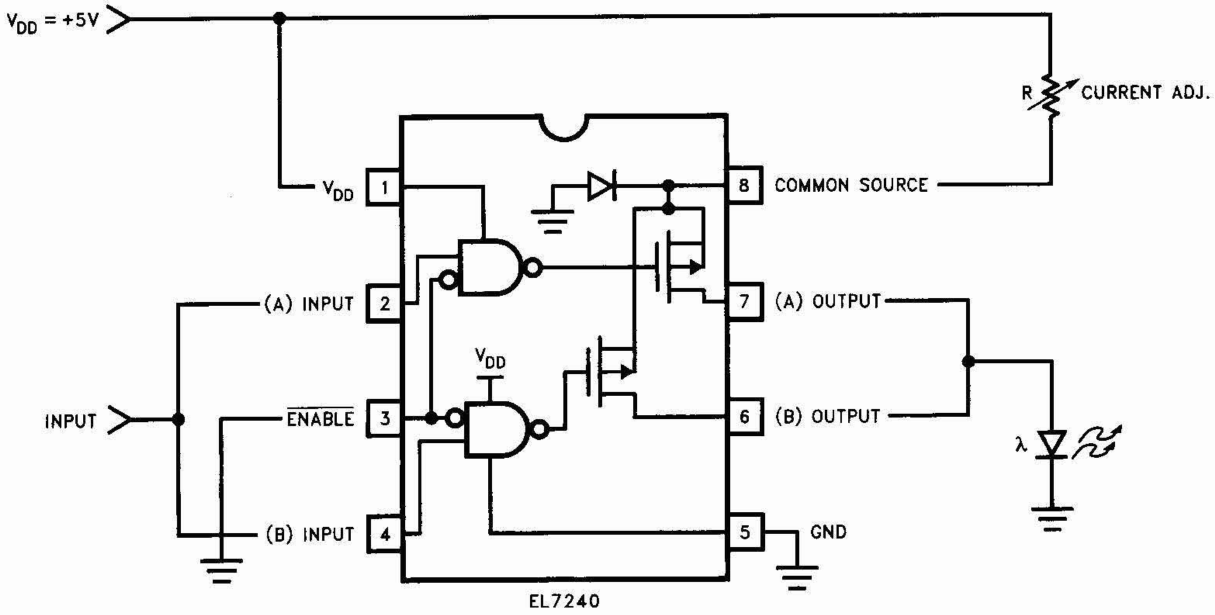
Typical Applications

Write Head Driver


V_DD = +12V
I
V_DD
1
COMMON SOURCE
8
(A) INPUT
2
7
(A) OUTPUT
DATA INPUTS
V_DD
ENABLE
3
6
(B) OUTPUT
(B) INPUT
4
5
GND
EL7241

7240-12

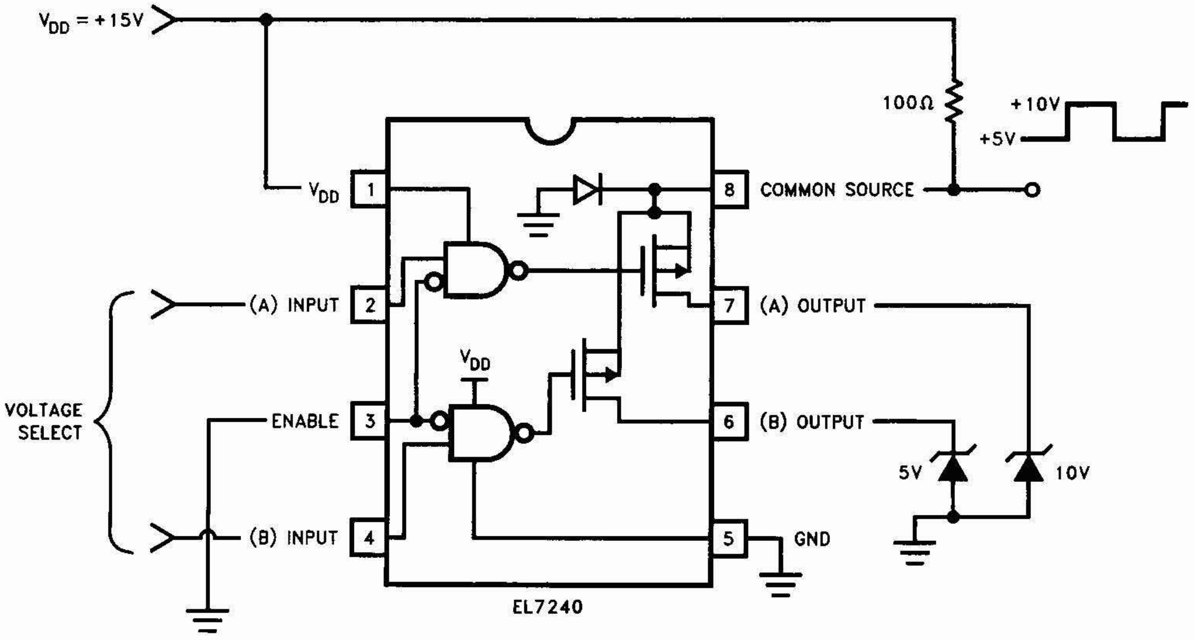
High Current LED/Laser Diode Driver


V_DD = +5V
R
CURRENT ADJ.
V_DD
1
8
COMMON SOURCE
(A) INPUT
2
7
(A) OUTPUT
V_DD
INPUT
ENABLE
3
6
(B) OUTPUT
λ
(B) INPUT
4
5
GND
EL7240

7240-13

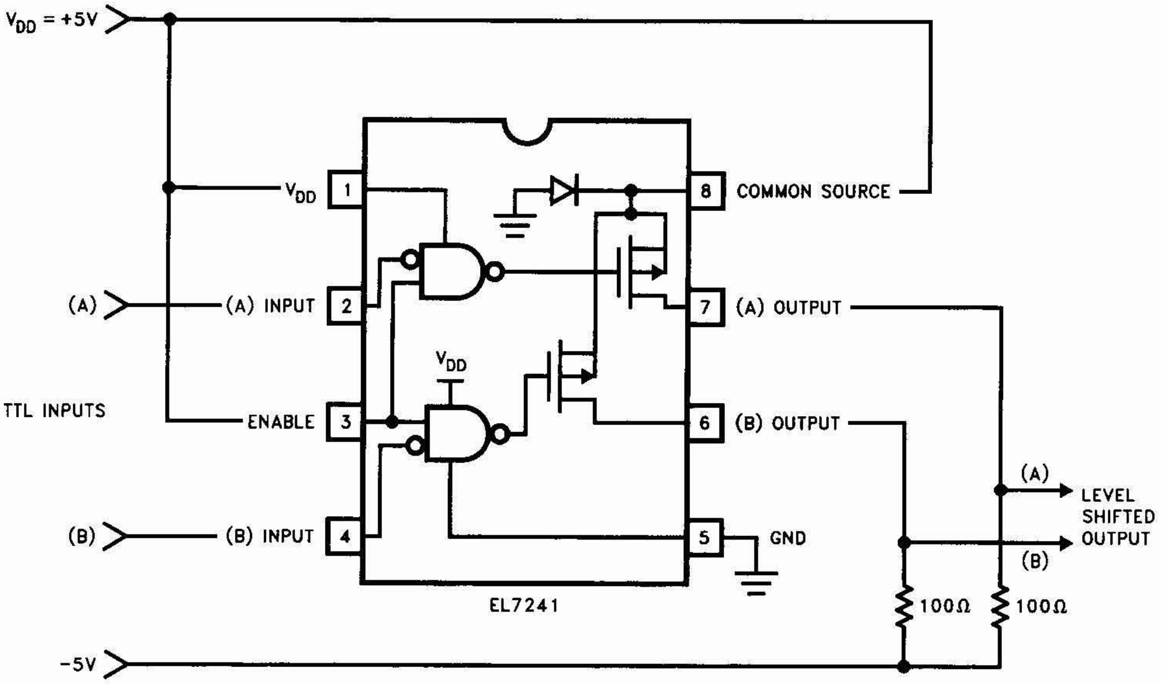
Typical Applications — Contd.

Bi-Level Step Generator


V_{DD} = +15V
100Ω
+10V
+5V
V_{DD}
1
8
COMMON SOURCE
(A) INPUT
2
7
(A) OUTPUT
V_{DD}
VOLTAGE SELECT
ENABLE
3
6
(B) OUTPUT
5V
10V
(B) INPUT
4
5
GND
EL7240

7240-14

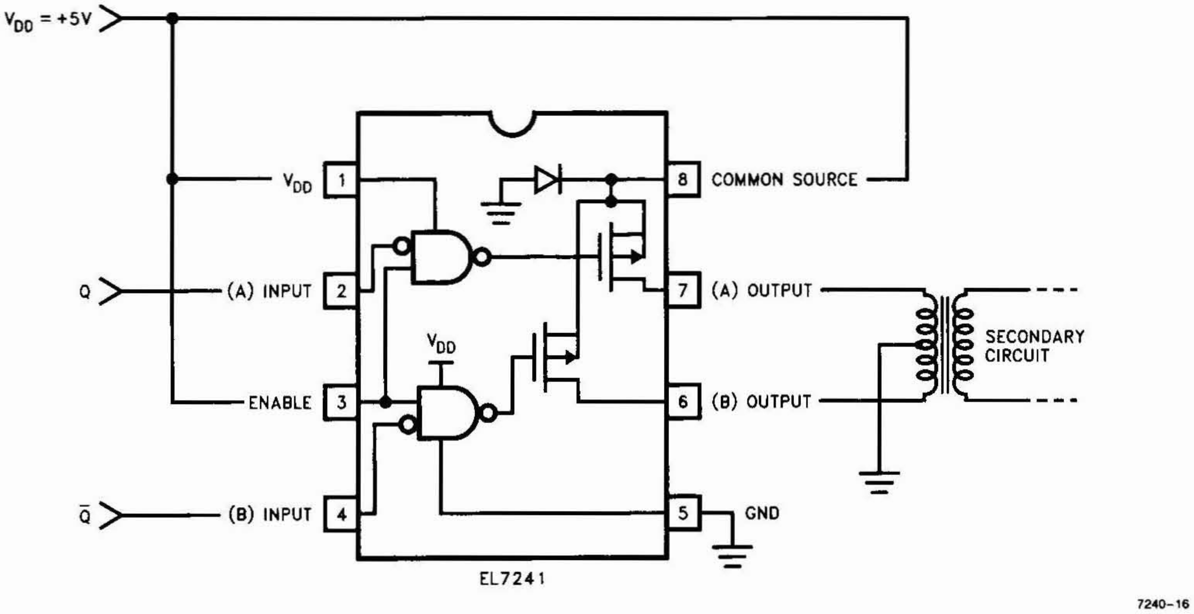
Level Shifter


V_{DD} = +5V
V_{DD}
1
8
COMMON SOURCE
(A)
(A) INPUT
2
7
(A) OUTPUT
V_{DD}
TTL INPUTS
ENABLE
3
6
(B) OUTPUT
(A)
LEVEL SHIFTED OUTPUT
(B)
(B) INPUT
4
5
GND
EL7241
100Ω
100Ω
-5V

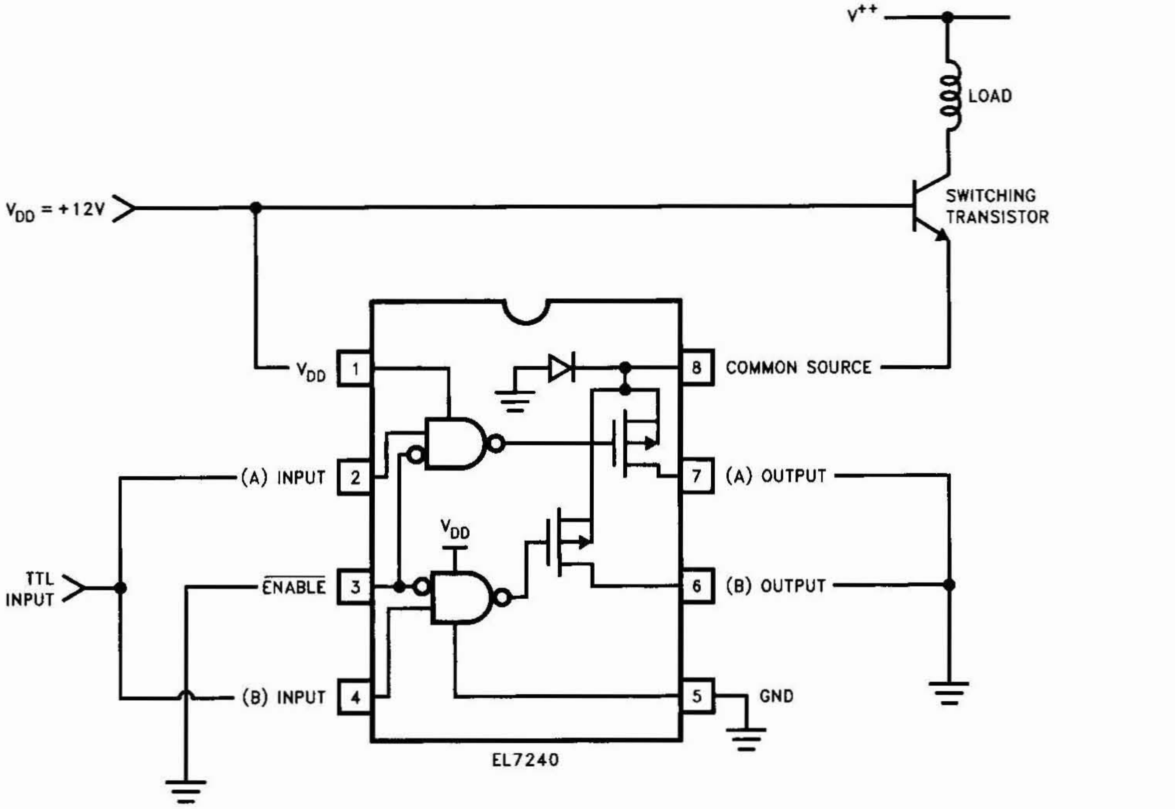
7240-15

Typical Applications — Contd.

Push-Pull Transformer Driver

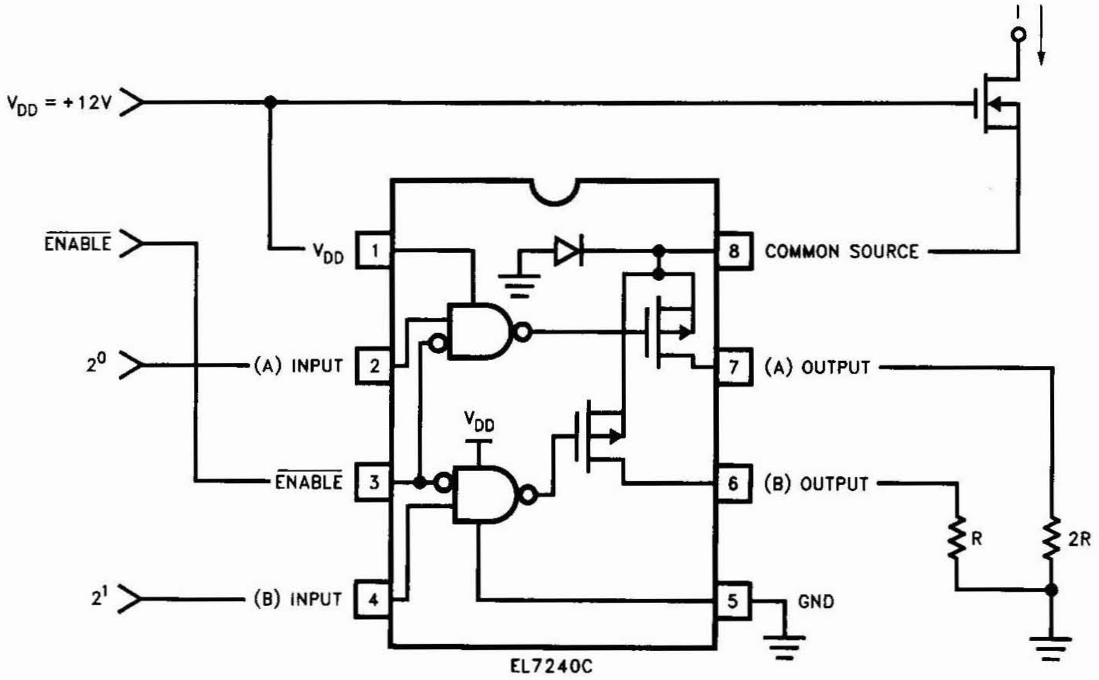

V_{DD} = +5V
V_{DD}
1
Q
(A) INPUT
2
ENABLE
3
$\overline{Q}$
(B) INPUT
4
V_{DD}
8
COMMON SOURCE
7
(A) OUTPUT
6
(B) OUTPUT
5
GND
SECONDARY CIRCUIT
EL7241
7240-16

High Speed Bipolar Drive Circuit


V^{++}
LOAD
SWITCHING TRANSISTOR
V_{DD} = +12V
V_{DD}
1
(A) INPUT
2
TTL INPUT
$\overline{ENABLE}$
3
(B) INPUT
4
V_{DD}
8
COMMON SOURCE
7
(A) OUTPUT
6
(B) OUTPUT
5
GND
EL7240
7240-17

Typical Applications — Contd.

"Two-Bit" Current Source with Gating


I
V_{DD} = +12V
ENABLE
2^0
2^1
V_{DD}
(A) INPUT
ENABLE
(B) INPUT
1
2
3
4
8
7
6
5
COMMON SOURCE
(A) OUTPUT
(B) OUTPUT
GND
R
2R
V_{DD}
EL7240C

7240-18

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7242C/EL7252C

Dual Input, High Speed, Dual Channel Power MOSFET Driver

Features

- Logic AND/NAND input
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Isolated drains
- Low output impedance
- Low quiescent current
- Wide operating voltage—4.5V–16V

Applications

- Short circuit protected switching
- Under-voltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Shoot-thru protection
- Latching drivers

Ordering Information

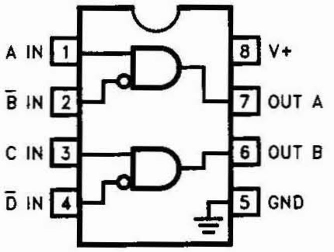
Part No.	Temp. Range	Pkg.	Outline #
EL7242CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7242CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL7252CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7252CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL7242C/EL7252C dual input, 2-channel drivers achieve the same excellent switching performance of the EL7212 family while providing added flexibility. The 2-input logic and configuration is applicable to numerous power MOSFET drive circuits. As with other Elantec drivers, the EL7242C/EL7252C are excellent for driving large capacitive loads with minimal delay and switching times. "Shoot-thru" protection and latching circuits can be implemented by simply "cross-coupling" the 2-channels.

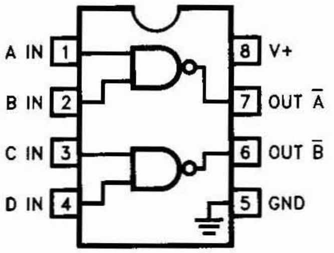
Connection Diagrams

EL7242C



7242-1

EL7252C



7242-2

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

January 1996 Rev. B

EL7242C/EL7252C

Dual Input, High Speed, Dual Channel Power MOSFET Driver

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V
Input Pins	−0.3V to +0.3V above V^+
Combined Peak Output Current	4A
Storage Temperature Range	−65°C to +150°C
Ambient Operating Temperature	−40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	
SOIC	570 mW
PDIP	1050 mW

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

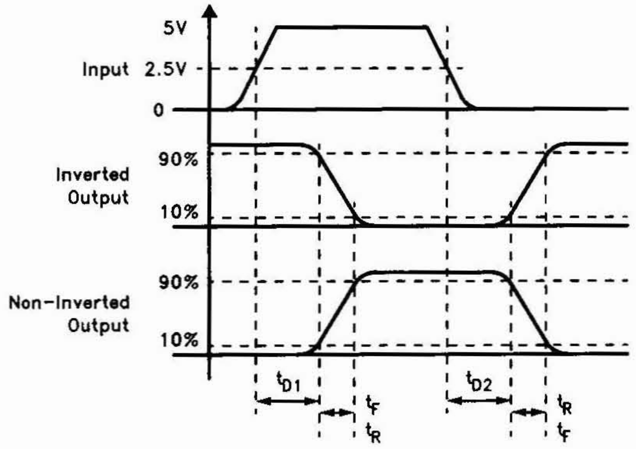
DC Electrical Characteristics $T_A = 25°C$, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	μA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	μA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	$I_{OUT} = -100$ mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	$I_{OUT} = +100$ mA		4	6	I	Ω
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Inputs High		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

AC Electrical Characteristics $T_A = 25°C$, V = 15V unless otherwise specified

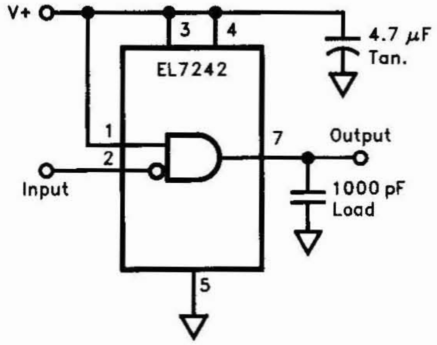
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF			10 20	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF			10 20	IV	ns
$t_{D\text{-}ON}$	Turn-On Delay Time			20	25	IV	ns
$t_{D\text{-}OFF}$	Turn-Off Delay Time			20	25	IV	ns

Timing Table


5V
Input
2.5V
0
Inverted Output
90%
10%
Non-Inverted Output
90%
10%
t_{D1}
t_F
t_R
t_{D2}
t_R
t_F

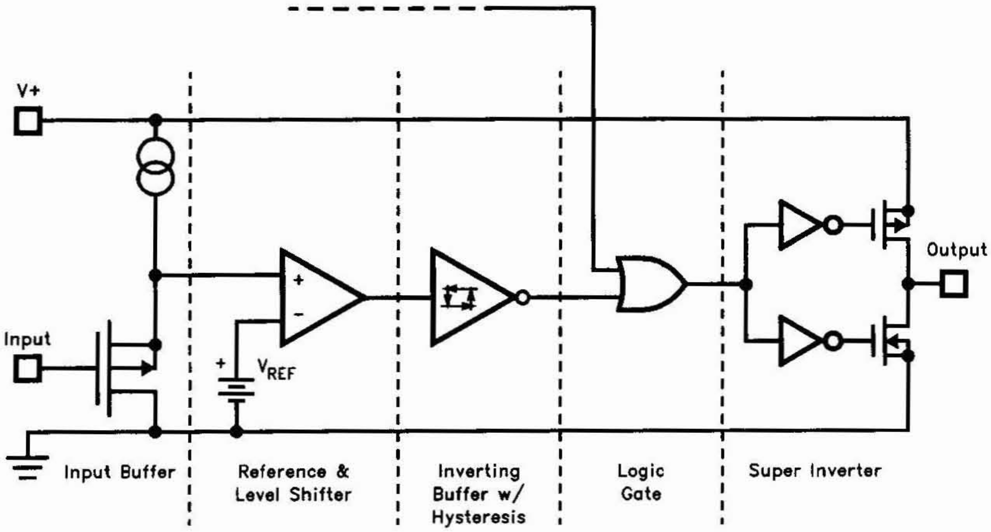
7242-3

Standard Test Configuration


V+
3
4
4.7 µF
Tan.
EL7242
1
2
7
Output
Input
1000 pF
Load
5

7242-4

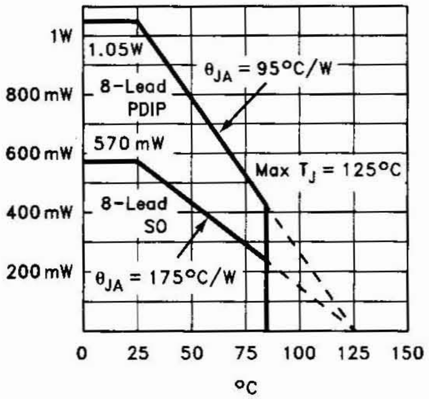
Simplified Schematic


V+
Input
+
−
+
V_{REF}
Output
Input Buffer
Reference & Level Shifter
Inverting Buffer w/ Hysteresis
Logic Gate
Super Inverter

7242-5

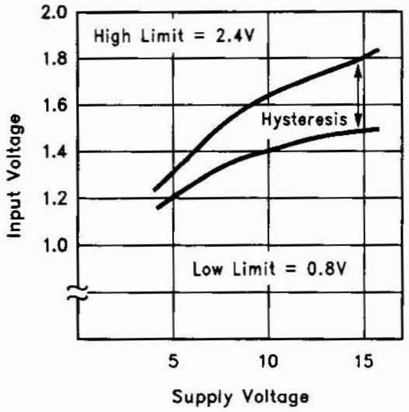
Typical Performance Curve

Max Power/Derating Curves



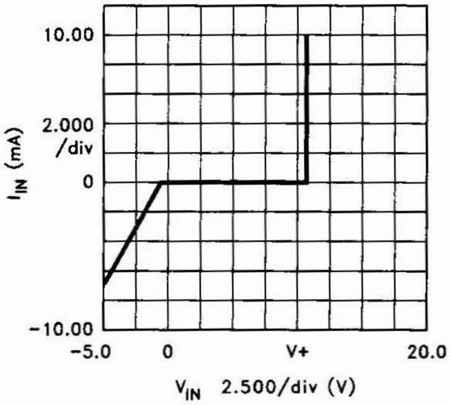
7242-17

Switch Threshold vs Supply Voltage



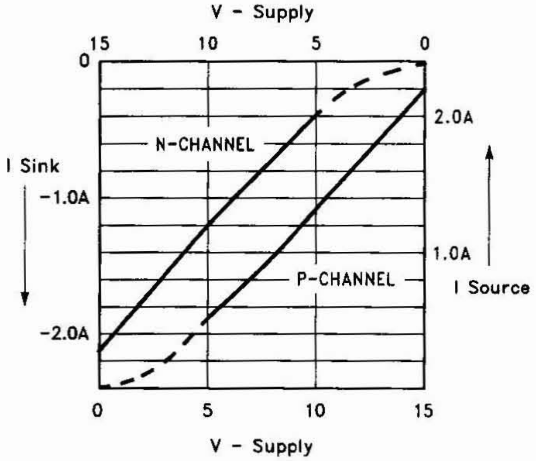
7242-6

Input Current vs Voltage



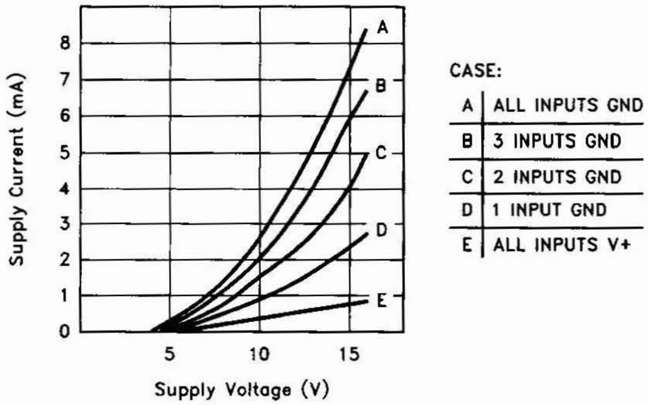
7242-7

Peak Drive vs Supply Voltage



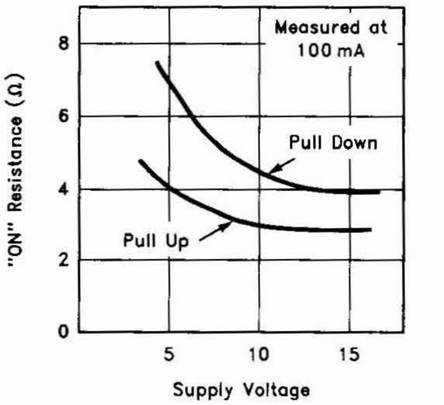
7242-8

Quiescent Supply Current



7242-9

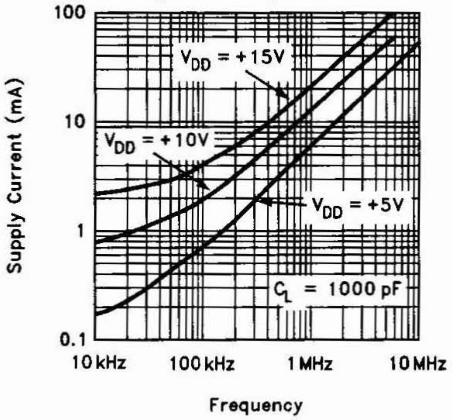
"ON" Resistance vs Supply Voltage



7242-18

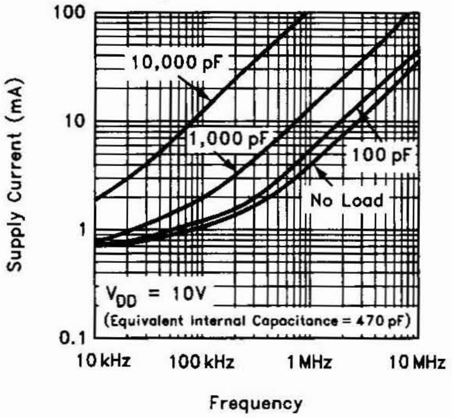
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



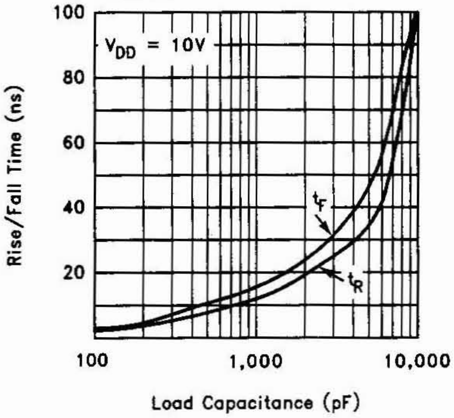
7242-10

Average Supply Current vs Capacitive Load



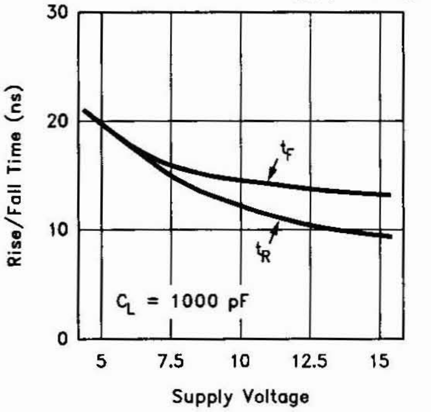
7242-11

Rise/Fall Time vs Load



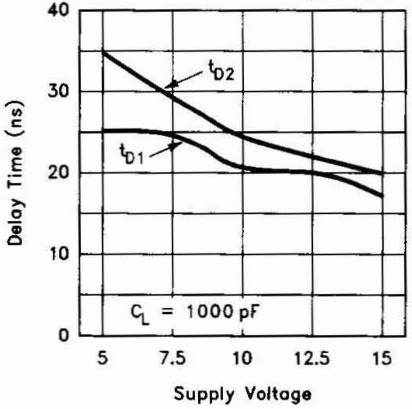
7242-16

Rise/Fall Time vs Supply Voltage

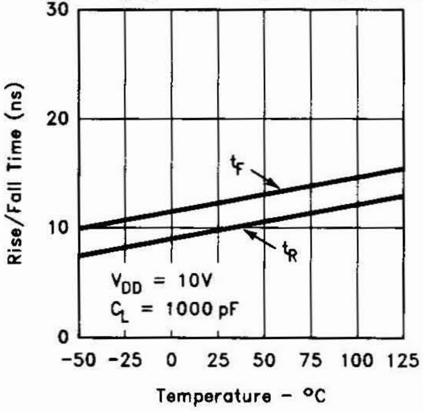


7242-12

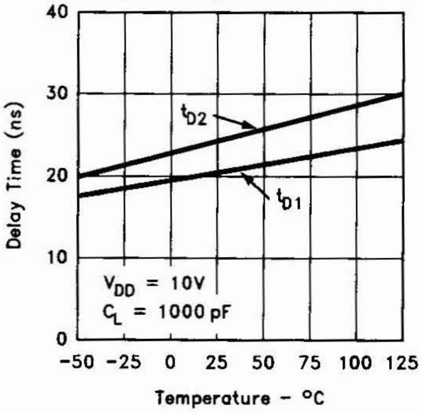
Typical Performance Curve — Contd.


Rise/Fall Time vs Temperature

7242-13


Propagation Delay vs Supply Voltage

7242-14


Delay vs Temperature

7242-15

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7243C

Dual Input, High Speed, Dual Channel CCD Driver

Features

- Logic AND/NAND input
- 3V and 5V Input compatible
- Clocking speeds up to 20 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Isolated drains
- Low output impedance
- Low quiescent current
- Wide operating voltage—4.5V–16V

Applications

- CCD Drivers
- Short circuit protected switching
- Under-voltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Shoot-thru protection
- Latching drivers

Ordering Information

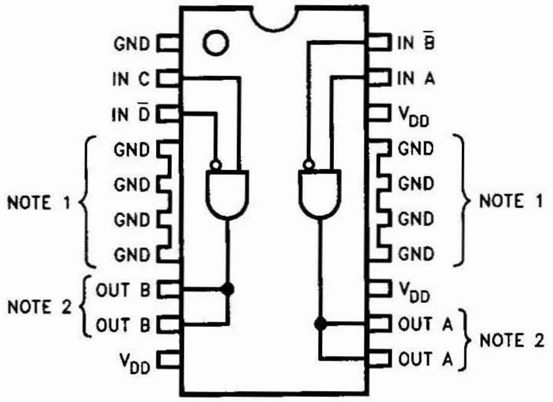
Part No.	Temp. Range	Pkg.	Outline #
EL7243CM	−40°C to +85°C	20-Lead Thermal SOL	MDP0027*

General Description

The EL7243C dual input, 2-channel driver achieves the same excellent switching performance of the EL7212 family while providing added flexibility. The power package makes this part extremely well suited for high frequency and heavy loads as in CCD applications. The 2-input logic and configuration is applicable to numerous power MOSFET drive circuits. As with other Elantec drivers, the EL7243C is excellent for driving large capacitive loads with minimal delay and switching times. "Shoot-thru" protection and latching circuits can be implemented by simply "cross-coupling" the 2-channels.

Connection Diagram

20-Lead Thermal SOL Package
EL7243C



Note 1: Pins 4–7 and 14–17 are electrically connected.
Note 2: Output pins must be tied together.

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

EL7243C

Dual Input, High Speed, Dual Channel CCD Driver

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V
Input Pins	−0.3V to +0.3V above V+
Combined Peak Output Current	4A
Storage Temperature Range	−65°C to +150°C
Ambient Operating Temperature	−40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	
20-pin "Batwing" SOIC	1500 mW

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

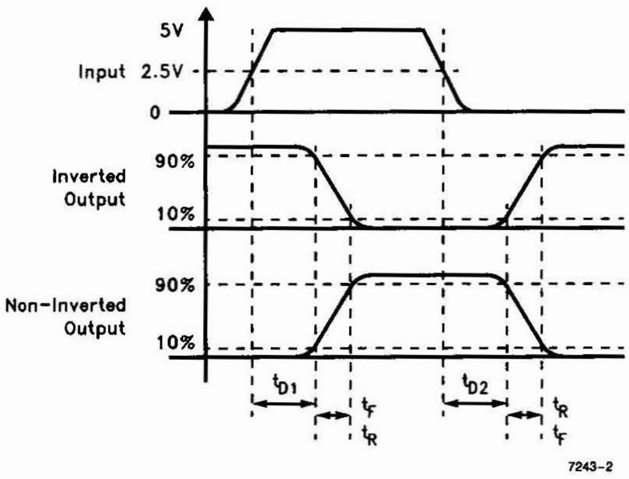
DC Electrical Characteristics T_A = 25°C, V_{DD} = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V_{DD}		0.1	10	I	μA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	μA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		4	6	I	Ω
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I_S	Power Supply Current	Inputs High		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

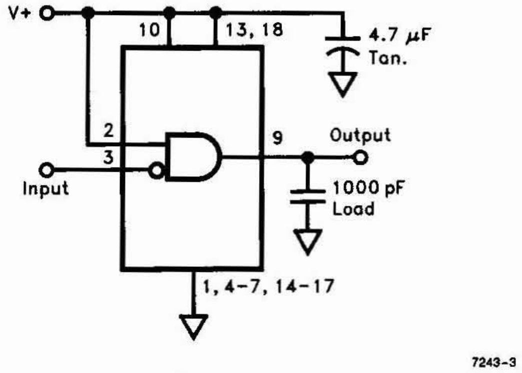
AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF			10 20	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF			10 20	IV	ns
$t_{D\text{-}ON}$	Turn-On Delay Time			20	25	IV	ns
$t_{D\text{-}OFF}$	Turn-Off Delay Time			20	25	IV	ns

Timing Table

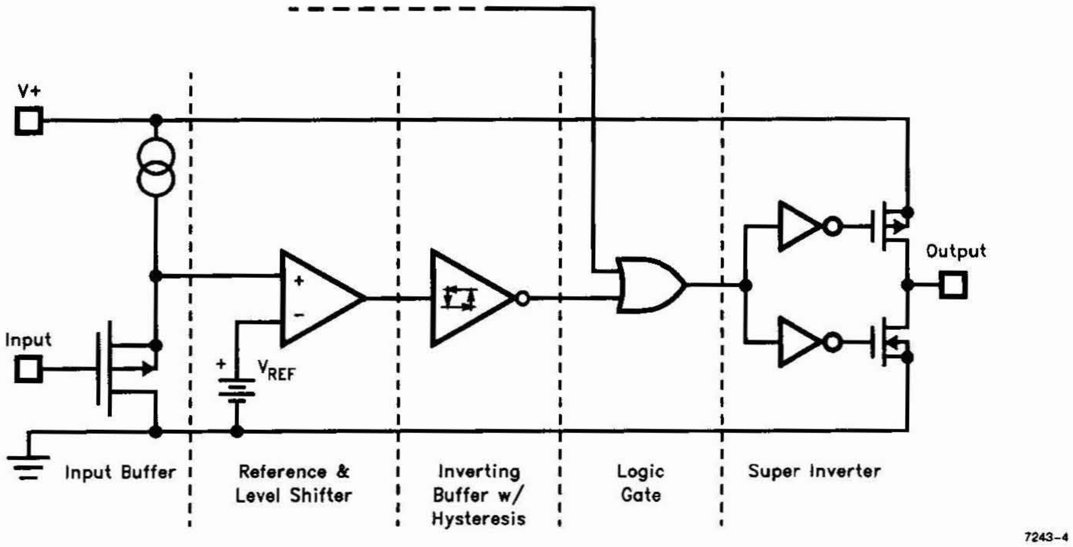


Standard Test Configuration


V+
10
13, 18
4.7 μF Tan.
2
3
9
Output
Input
1000 pF Load
1, 4-7, 14-17
7243-3

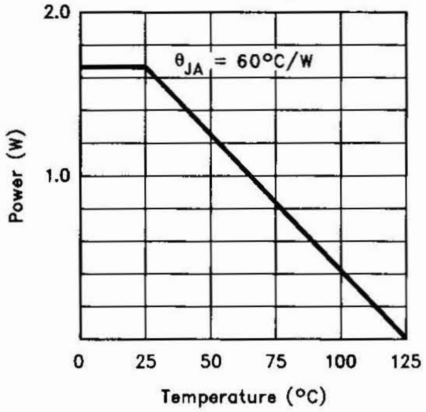
Pins 19, 20 connected to V+.

Simplified Schematic


V+
Input
+
-
+
V_{REF}
Output
Input Buffer
Reference & Level Shifter
Inverting Buffer w/ Hysteresis
Logic Gate
Super Inverter
7243-4

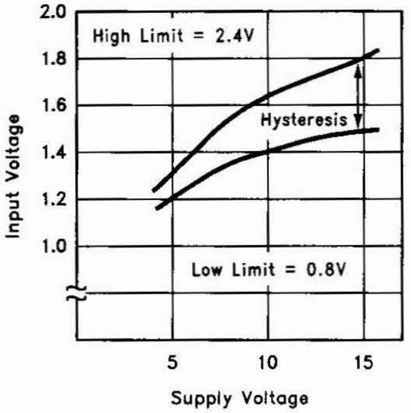
Typical Performance Curves

Max Power/Derating Curves



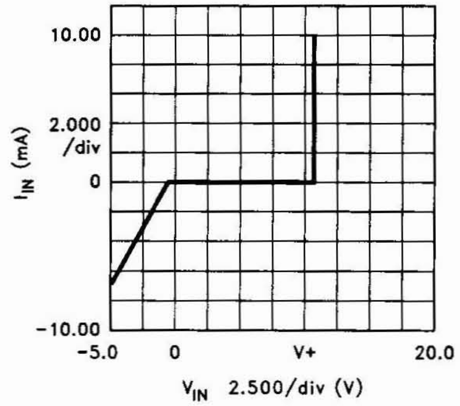
7243-5

Switch Threshold vs Supply Voltage



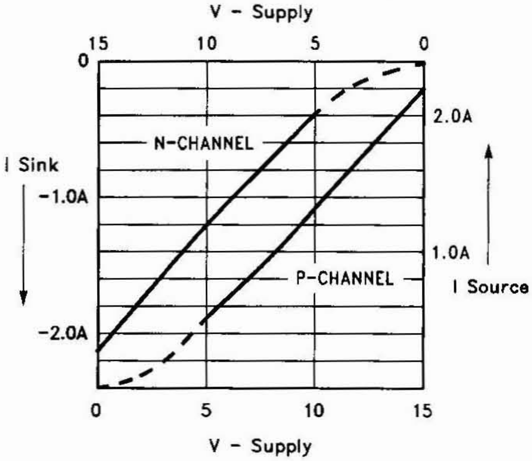
7243-6

Input Current vs Voltage



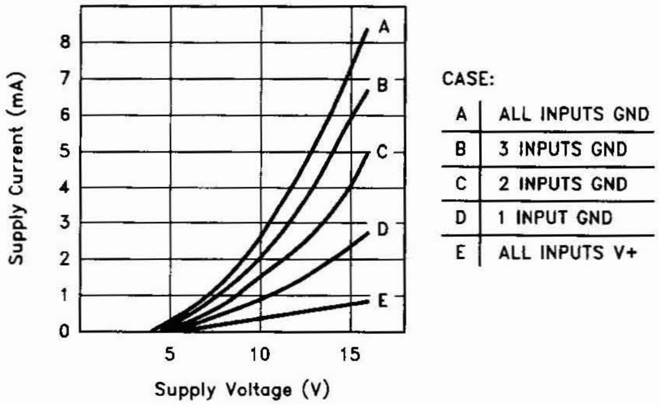
7243-7

Peak Drive vs Supply Voltage



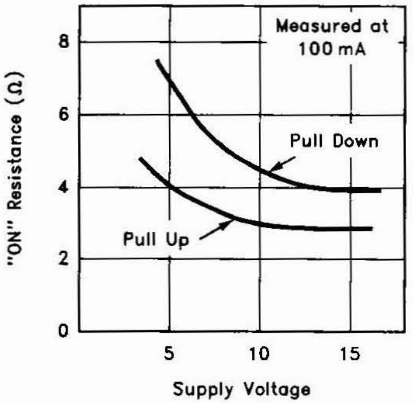
7243-8

Quiescent Supply Current



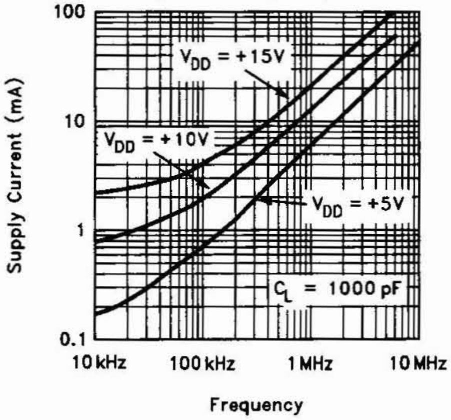
7243-9

"ON" Resistance vs Supply Voltage



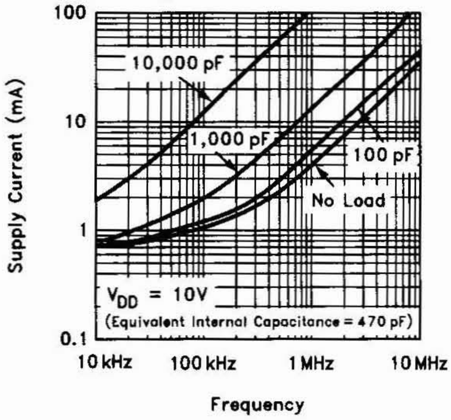
7243-10

Typical Performance Curves — Contd.



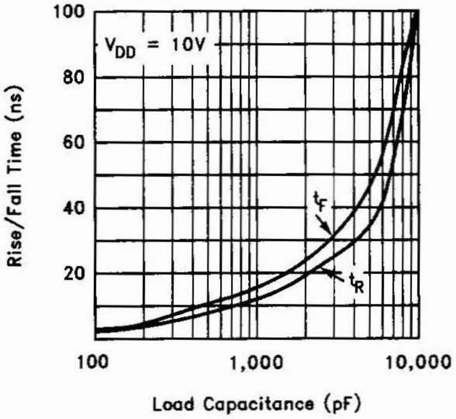
Average Supply Current vs Voltage and Frequency

7243-11



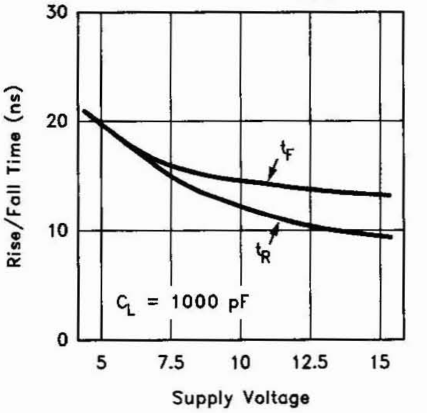
Average Supply Current vs Capacitive Load

7243-12



Rise/Fall Time vs Load

7243-13

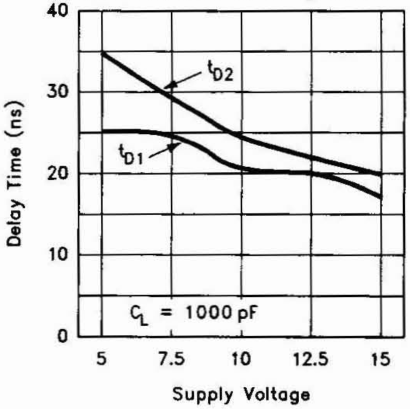


Rise/Fall Time vs Supply Voltage

7243-14

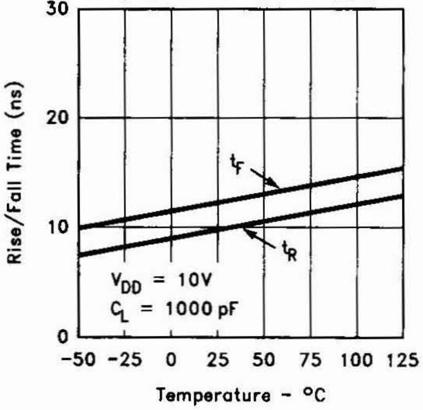
Typical Performance Curves — Contd.

Rise/Fall Time vs Temperature



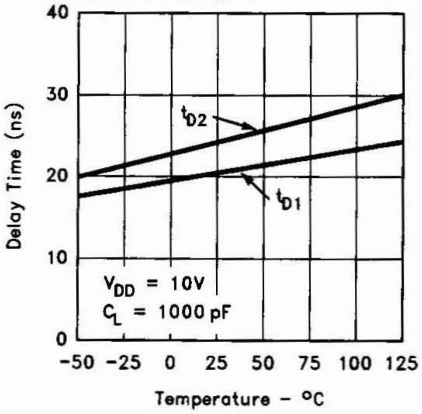
7243-15

Propagation Delay vs Supply Voltage



7243-16

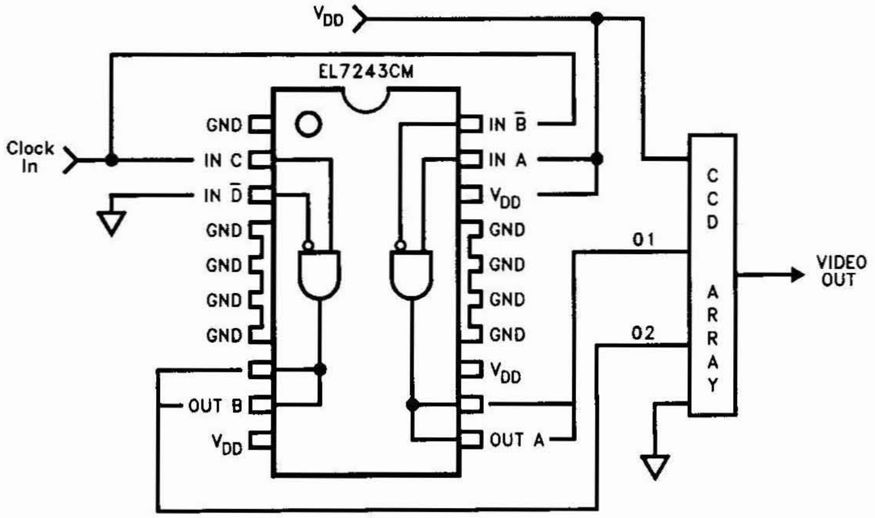
Delay vs Temperature



7243-17

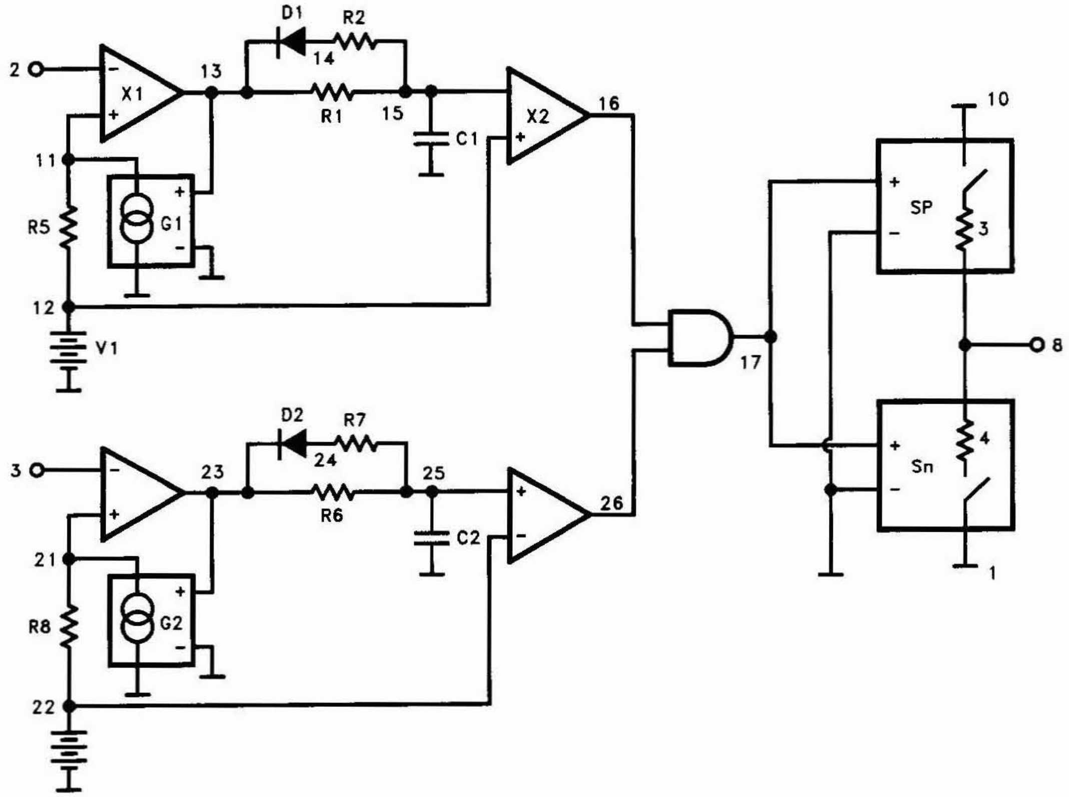
Applications Information

Typical CCD Configuration


V_{DD}
EL7243CM
Clock In
GND
IN C
IN $\overline{D}$
GND
GND
GND
GND
OUT B
V_{DD}
IN $\overline{B}$
IN A
V_{DD}
GND
GND
GND
GND
V_{DD}
OUT A
01
02
CCD ARRAY
VIDEO OUT

7243-18

EL7243 Macromodel


2
X1
13
D1
R2
14
R1
15
C1
X2
16
11
R5
G1
12
V1
10
SP
3
8
17
4
Sn
1
3
23
D2
R7
24
R6
25
C2
26
21
R8
G2
22

7243-19

EL7243 Macromodel

```
* EL7243 Macromodel
* Revision A, January 1996
* Connections       Gnd
*                   |    Inp+
*                   |    |    Inp-
*                   |    |    |    out
*                   |    |    |    |    VCC
.subckt M7243       1    2    3    8    10
V1 12 1 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 1 43.3pF
D1 14 13 dmod
X1 13 11 2 1 comp1
X2 16 12 15 1 comp1
V2 22 1 1.6
R6 23 25 1K
R7 24 25 5K
R8 21 22 100
C2 25 1 43.3pF
D2 24 23 dmod
X3 23 21 3 1 comp1
X4 26 25 22 1 comp1
X5 16 26 17 1 And-gate
sp 10 8 17 1 spmod
sn 8 1 17 1 snmod
g1 11 1 13 1 938u
g2 21 1 23 1 938u
.model dmod d
.model spmod vswitch ron=3 roff=2meg von=1 voff=1.5
.model snmod vswitch ron=4 roff=2meg von=3 voff=2
.ends M7243
* AND Gate Subcircuit*
.subckt And-gate inp1 inp2 out-AS Vss-A
el out-A Vss-A table {v(inp1)*v(inp2)} = (0, 3.2) (3.2, 0)
Rout-a out-a vss-a 10 meg
rinpa inp1 vss-a 10 meg
rinpb inp2 vss-a 10 meg
.ends and-gate
* Comparator Subcircuit *
.subckt comp1 out inp inm vss
el out vss table {(v(inp)-v(inm))*5000} = (0,0) (3.2, 3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
.ends omp1
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7262C/EL7272C

Dual Channel, High Speed, Power MOSFET w/Isolated Drains

Features

- Separate drain connections
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Low output impedance
- Low quiescent current
- Wide operating voltage

Applications

- Asymetrical switching
- Cascoded switching
- Resonant charging
- Floating load circuits
- Bridge circuits

Ordering Information

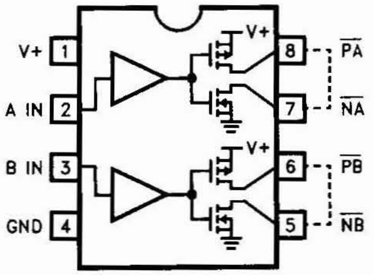
Part No.	Temp. Range	Pkg.	Outline #
EL7262CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7262CS	−40°C to +85°C	8-Pin SO	MDP0027
EL7272CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7272CS	−40°C to +85°C	8-Pin SO	MDP0027

General Description

The EL7262C/EL7272C, dual channel, power MOSFET drivers achieve the same excellent switching performance of the EL7202 family, with the added flexibility derived through the isolated drain architecture. The outputs can be configured in numerous ways, depending upon the application. The EL7262C and EL7272C are available in 8-pin P-DIP and 8-lead SO packages.

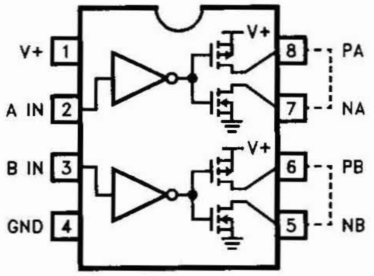
Connection Diagrams

EL7262C



7262-1

EL7272C



7262-2

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current	4A	SOIC	570 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

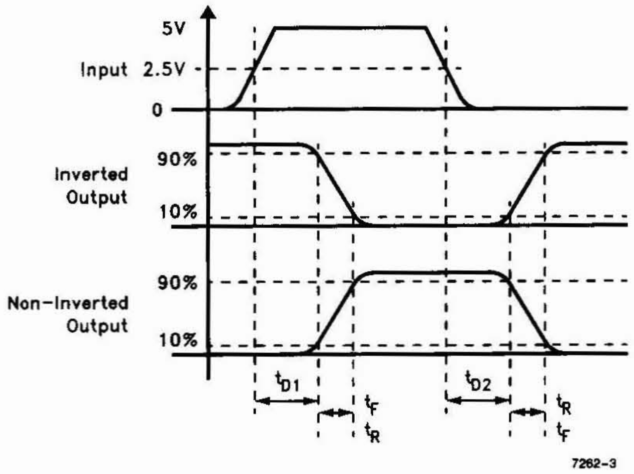
DC Electrical Characteristics $T_A = 25°C$, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	µA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	$I_{OUT} = -100$ mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	$I_{OUT} = +100$ mA		4	6	I	Ω
I_{OFF}	Output Leakage	$V_{OUT} = V+$ $V_{OUT} = 0V$		0.2	10	I	µA
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Inputs EL7262 High EL7272		1 4.5	2.5 7.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

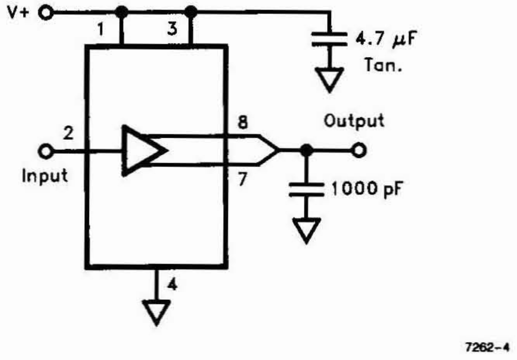
AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		7.5 10	 20	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		10 13	 20	IV	ns
$t_{D\text{-}ON}$	Turn-On Delay Time	See Timing Table		18	25	IV	ns
$t_{D\text{-}OFF}$	Turn-Off Delay Time	See Timing Table		20	25	IV	ns

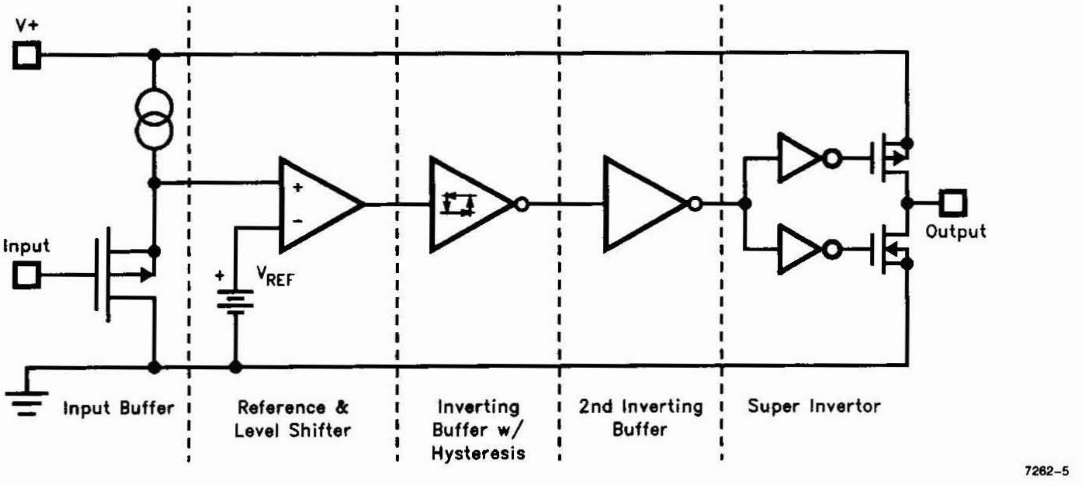
Timing Table


5V
Input
2.5V
0
Inverted Output
90%
10%
Non-Inverted Output
90%
10%
tD1
tF
tR
tD2
tR
tF
7262-3

Standard Test Configuration

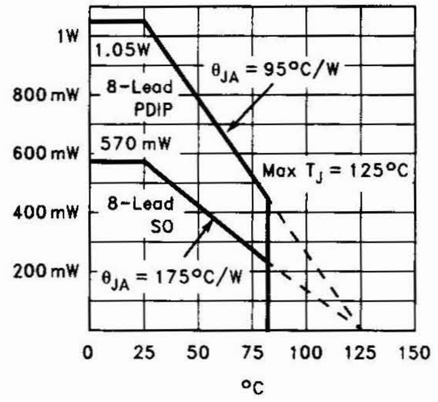

V+
1
3
4.7 µF Tan.
2
Input
8
7
Output
1000 pF
4
7262-4

Simplified Schematic


V+
Input
+
−
+
VREF
Output
Input Buffer
Reference & Level Shifter
Inverting Buffer w/ Hysteresis
2nd Inverting Buffer
Super Invertor
7262-5

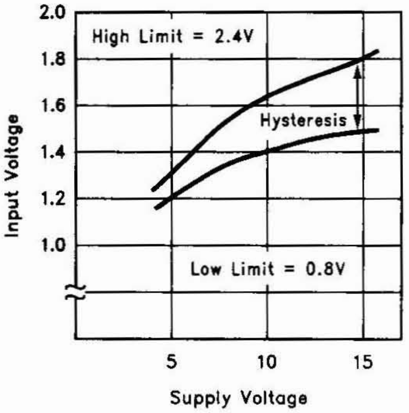
Typical Performance Curve

Max Power/Derating Curves



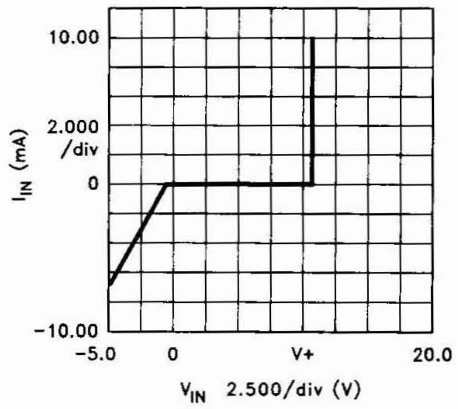
7262-12

Switch Threshold vs Supply Voltage



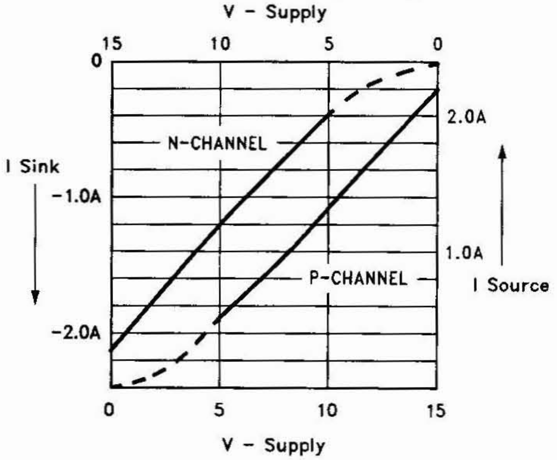
7262-6

Input Current vs Voltage



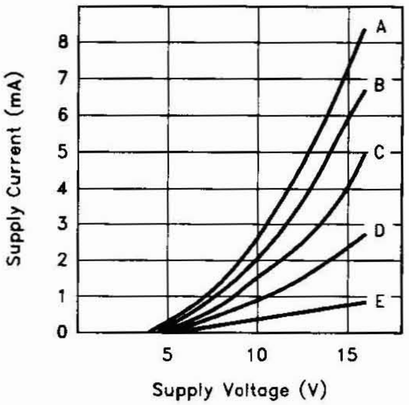
7262-7

Peak Drive vs Supply Voltage



7262-8

Quiescent Supply Current

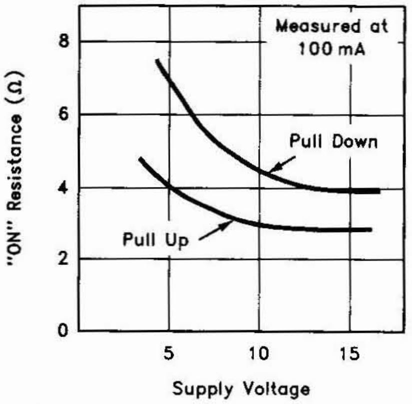


CASE:

Device	Input Level	Curve
EL7262	GND	C
EL7262	GND, V+	D
EL7262	V+	E
EL7272	GND	A
EL7272	GND, V+	B
EL7272	V+	C

7262-9

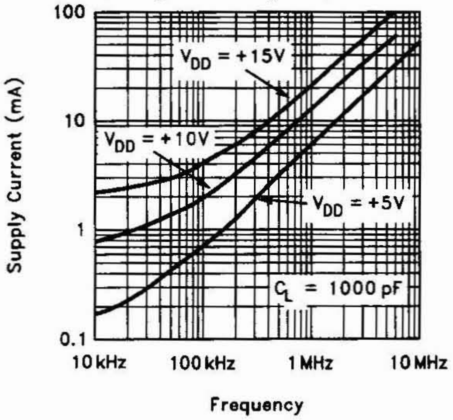
"ON" Resistance vs Supply Voltage



7262-10

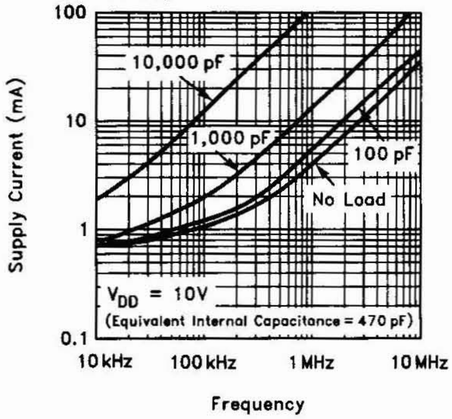
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



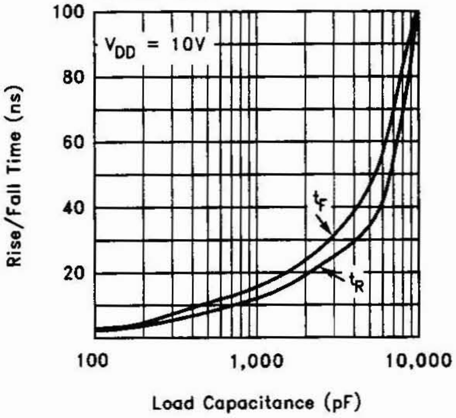
7262-13

Average Supply Current vs Capacitive Load



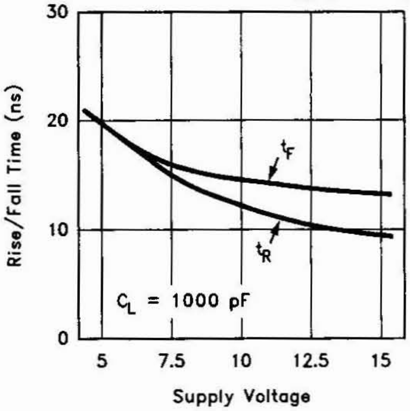
7262-14

Rise/Fall Time vs Load



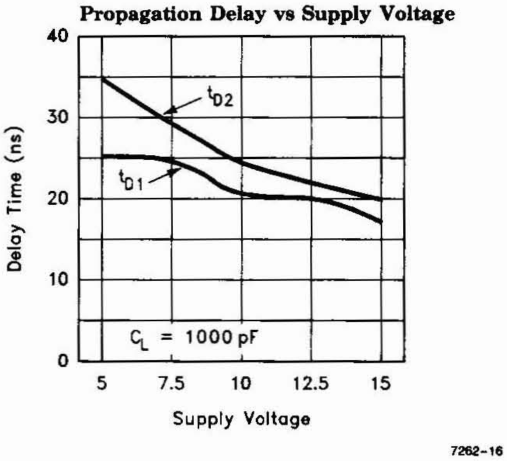
7262-11

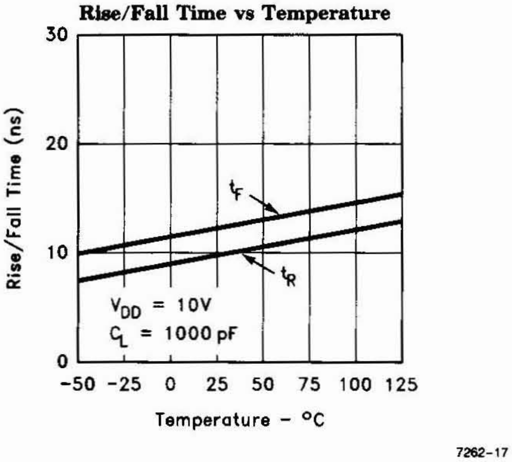
Rise/Fall Time vs Supply Voltage

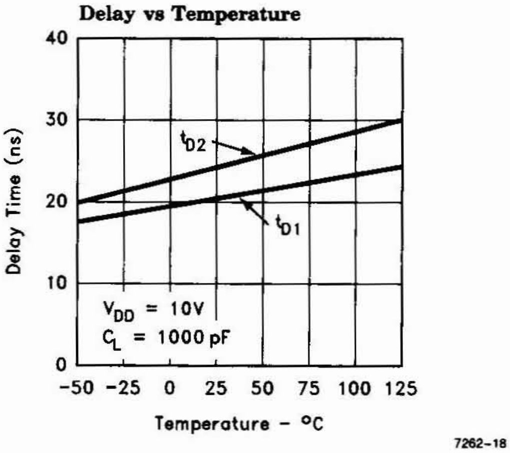


7262-15

Typical Performance Curve — Contd.







élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7412C

High Speed, Four Channel Power MOSFET Drivers

Features

- Excellent response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating voltage range

Applications

- Full bridge drivers
- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Class D switching amplifiers
- Ultrasonic and RF generators
- Pulsed circuits

Ordering Information

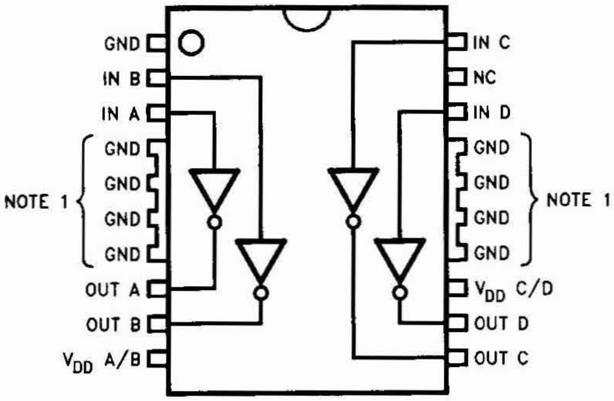
Part No.	Temp. Range	Pkg.	Outline #
EL7412CM	−40°C to +85°C	20 Lead Thermal SOL	MDP0027

General Description

The EL7412C contains (4) high performance matched drivers. These very high speed drivers are capable of delivering peak currents of 2.0 amps into highly capacitive loads and are ideally suited for "Full bridge" and ultrasound applications. The high speed performance is achieved by means of a proprietary "Turbo-Driver" circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. The matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices. Dynamic switching losses are minimized with non-overlapped drive techniques.

Connection Diagram

20 Lead Thermal SOL Package



7412-1

Note 1: Pins 4–7 and 14–17 are electrically connected.

Manufactured under U.S. Patent Nos. 5,334,883, #5,331,047

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V
Input Pins	−0.3V to +0.3V above V+
Combined Peak Output Current	8A
Storage Temperature Range	−65°C to +150°C
Ambient Operating Temperature	−40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	
20-Pin "Batwing" SOIC	1500 mW

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	**Test Procedure**
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

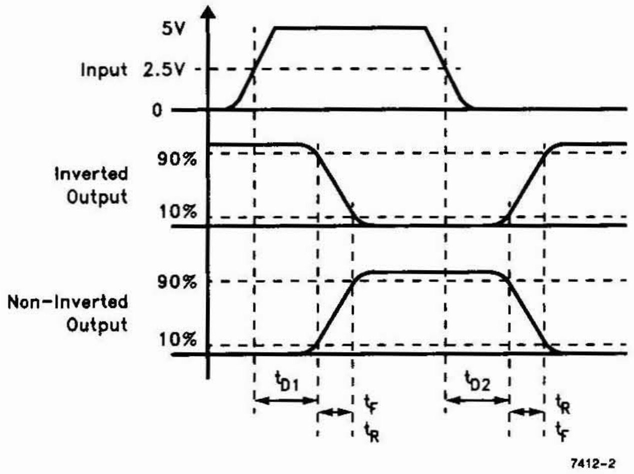
DC Electrical Characteristics $T_A = 25°C$, $V_{DD} = 15V$ unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V_{DD}		0.1	10	I	μA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	μA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	$I_{OUT} = -100$ mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	$I_{OUT} = +100$ mA		4	6	I	Ω
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Inputs High		2	5	I	mA
V_S	Operating Voltage		4.5		15	I	V

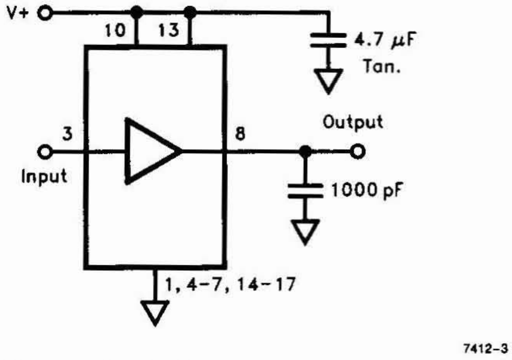
AC Electrical Characteristics $T_A = 25°C, V = 15V$ unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	$C_L = 500\ pF$ $C_L = 1000\ pF$		7.5 10	 20	IV	ns
t_F	Fall Time	$C_L = 500\ pF$ $C_L = 1000\ pF$		10 13	 20	IV	ns
t_{D1}	Turn-On Delay Time	See Timing Table		18	25	IV	ns
t_{D2}	Turn-Off Delay Time	See Timing Table		20	25	IV	ns

Timing Table

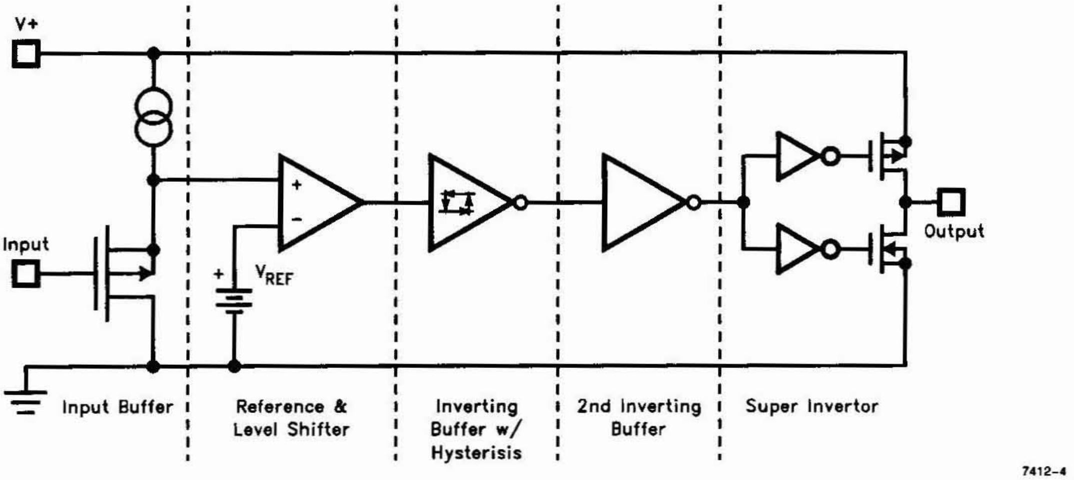

5V
Input
2.5V
0
Inverted Output
90%
10%
Non-Inverted Output
90%
10%
t_{D1}
t_F
t_R
t_{D2}
t_R
t_F
7412-2

Standard Test Configuration


V+
10
13
4.7 μF Tan.
3
Input
8
Output
1000 pF
1, 4-7, 14-17
7412-3

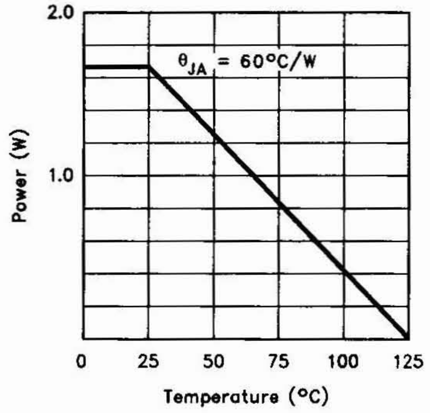
Pins 2, 18, 20 connected to V_{DD}

Simplified Schematic


V+
Input
+
−
+
V_{REF}
Output
Input Buffer
Reference & Level Shifter
Inverting Buffer w/ Hysterisis
2nd Inverting Buffer
Super Invertor
7412-4

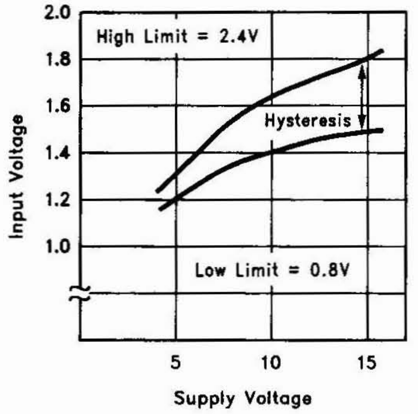
Typical Performance Curves

Max Power/Derating Curves



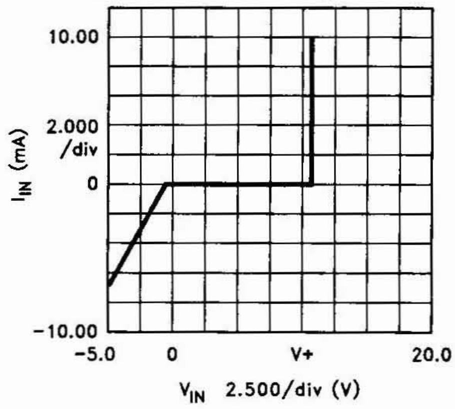
7412-5

Switch Threshold vs Supply Voltage



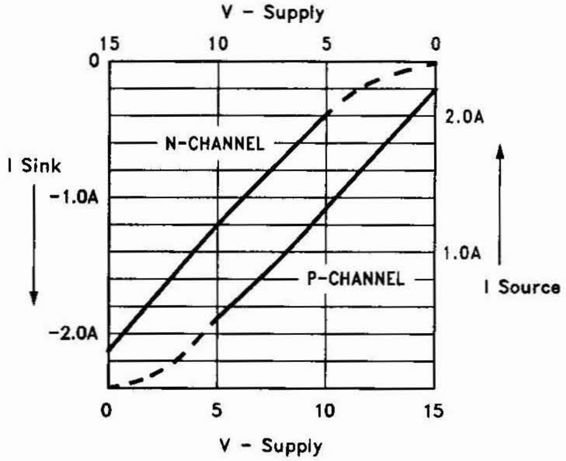
7412-6

Input Current vs Voltage



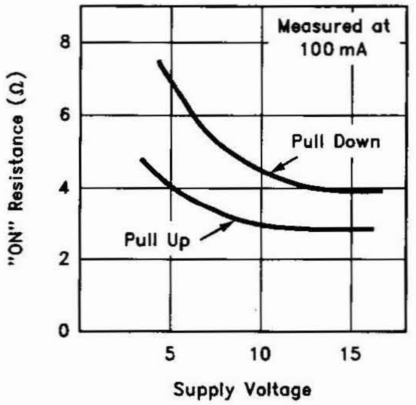
7412-7

Peak Drive vs Supply Voltage



7412-8

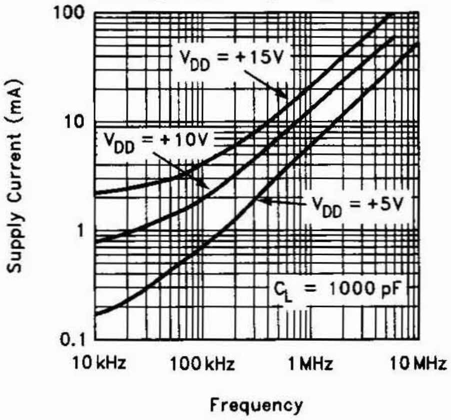
"ON" Resistance vs Supply Voltage



7412-10

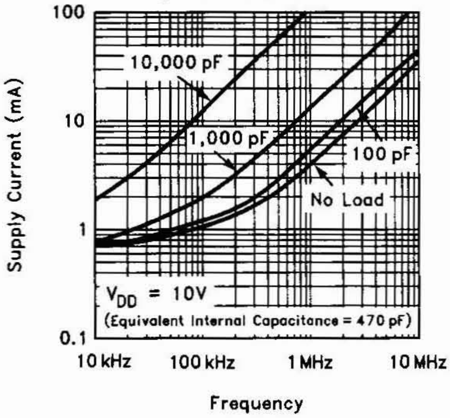
Typical Performance Curves — Contd.

Average Supply Current vs Voltage and Frequency



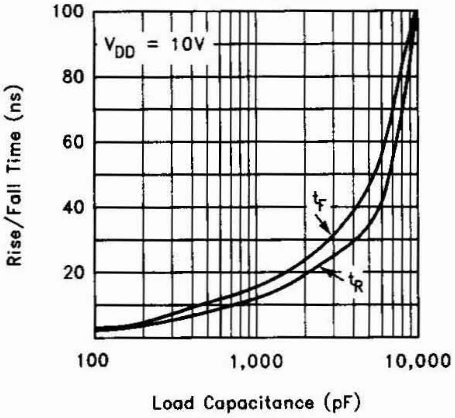
7412-11

Average Supply Current vs Capacitive Load



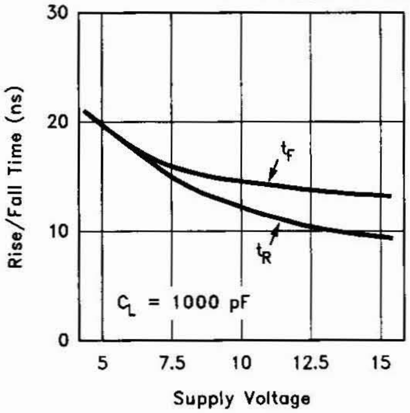
7412-12

Rise/Fall Time vs Load



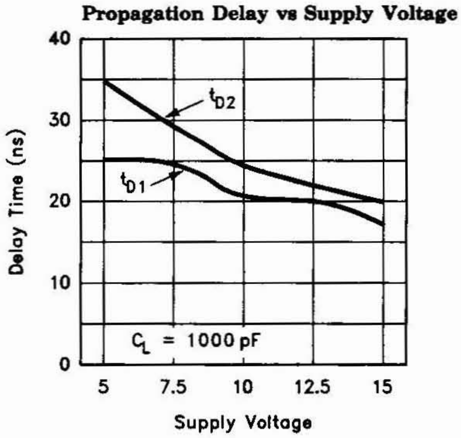
7412-13

Rise/Fall Time vs Supply Voltage

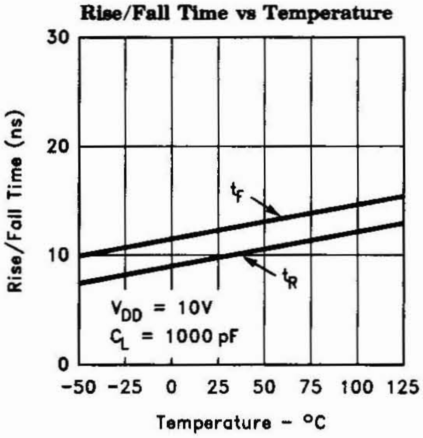


7412-14

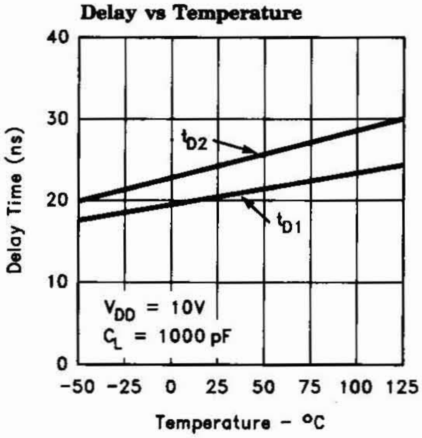
Typical Performance Curves — Contd.



7412-15



7412-16



7412-17

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7501C

100V High Side Driver

Features

- 100V High Side Voltage
- Rail to Rail Output
- 1 MHz Operation
- 1.0A Peak Current
- Matched Rise and Fall Times
- Direct Coupled
- No Start Up Ambiguity

Applications

- Uninterruptible Power Supplies
- DC-DC Converters
- Motor Control
- Power MOSFET Driver

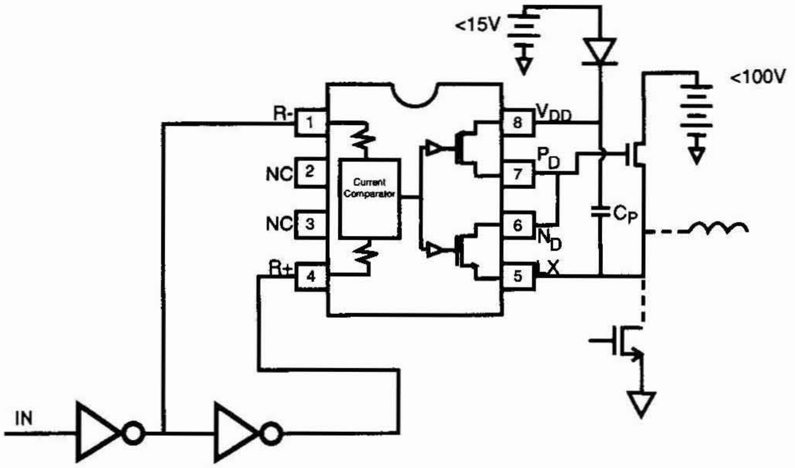
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7501CN	−40°C to +85°C	8-Pin P-Dip	MDP0031
EL7501CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

The EL7501 provides a low cost solution to many high side drive applications. The EL7501 is DC coupled so there are no start up problems associated with AC coupled schemes. The EL7501 is driven by user supplied complementary signals.

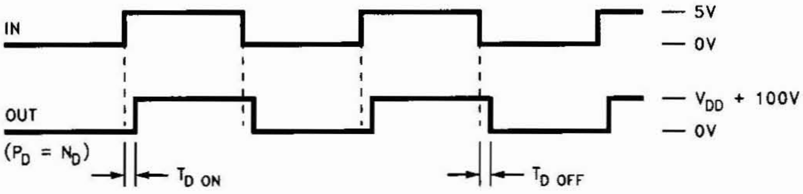
Connection Diagram



7501-1

Figure 1

7501 Waveform Example



7501-6

EL7501C

100V High Side Driver

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{DD} or LX to R− or R+)	100V	Ambient Operating Temperature		−40°C to +85°C
Supply (V_{DD} to LX)	16.5V	Storage Temperature Range		−65°C to +150°C
Output Pins	−0.3V below GND, +0.3V above V_{DD}	Operating Junction Temperature		125°C
		Power Dissipation	SOIC	570 mW
Peak Output Current	2A		PDIP	1050 mW

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (T_A = 25°C, V_{DD} = 15V, C_{LOAD} = 1000 pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Test Level	Units
Input/Output							
$V_{DIFF\ (Min)}$	Minimum Differential Input Signal to Switch Output		1.0			I	V
$I_{DS\ OFF}$	Output Leakage	GND < V_{OUT} < V_{DD}	−10.0	0.2	+10.0	I	µA
R_{OH}	Pull-up Resistance	I_{OUT} = −100 mA		5.0	10.0	I	Ω
R_{OL}	Pull-down Resistance	I_{OUT} = +100 mA		5.0	10.0	I	Ω
I_{PK}	Peak Output Current			1.0		IV	A
I_{DC}	Continuous Output Current Source/Sink		50.0			IV	mA
Power Supply							
I_{DD}	Supply Current into V_{DD}				4.0	I	mA
V_{DD}	Operating Voltage		4.5		15.0	I	V

AC Electrical Characteristics (T_A = 25°C, V_{DD} = 15V, C_{LOAD} = 1000 pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	40.0	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	40.0	IV	ns
$t_{D\ OFF}$	Turn Off Delay Time			90.0	140.0	IV	ns
$t_{D\ ON}$	Turn On Delay Time			90.0	140.0	IV	ns

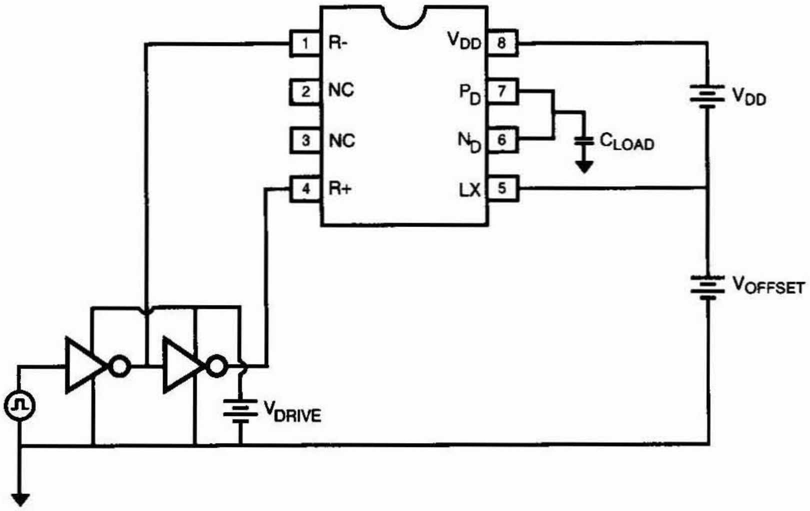

1
R-
2
NC
3
NC
4
R+
VDD
8
PD
7
ND
6
LX
5
VDD
CLOAD
VOFFSET
VDRIVE
7501-2

Figure 2. EL7501 Test Circuit

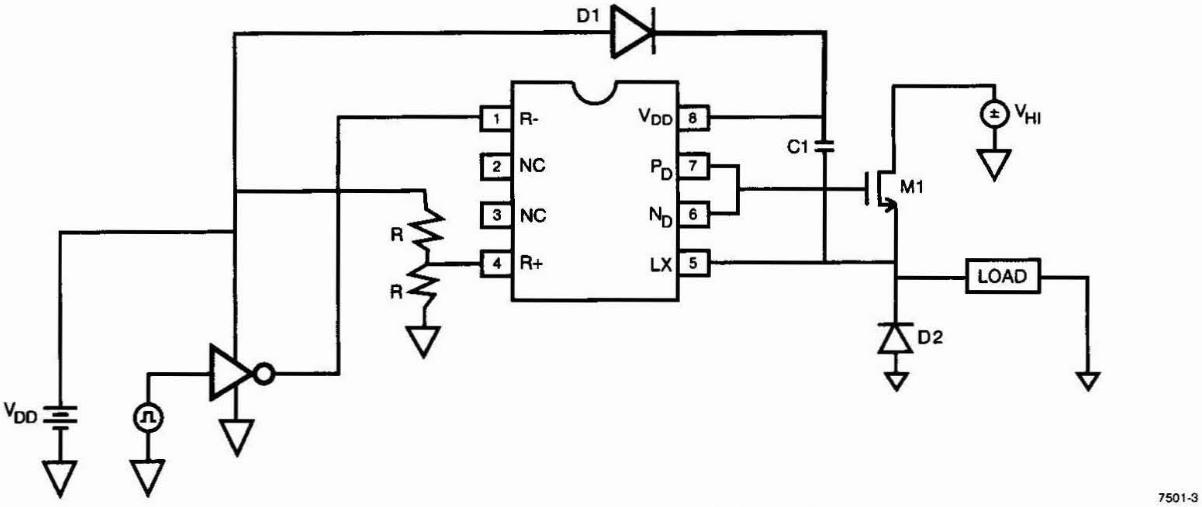
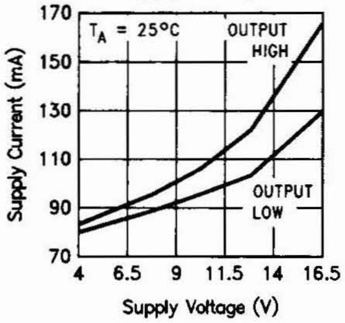

D1
1
R-
2
NC
3
NC
4
R+
VDD
8
PD
7
ND
6
LX
5
C1
M1
VHI
±
R
R
LOAD
D2
VDD
7501-3

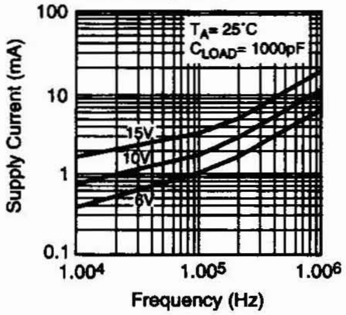
Figure 3. EL7501 Alternate Drive Method

Typical Performance Curves

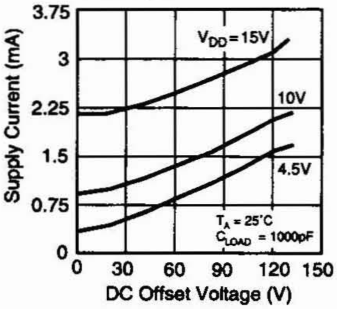
Quiescent Supply Current vs Supply Voltage



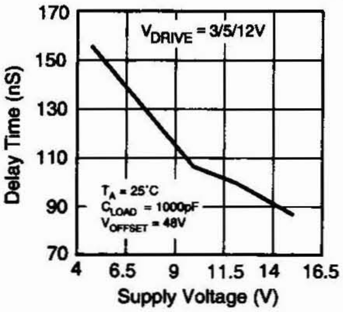
Average Supply Current vs Voltage and Frequency



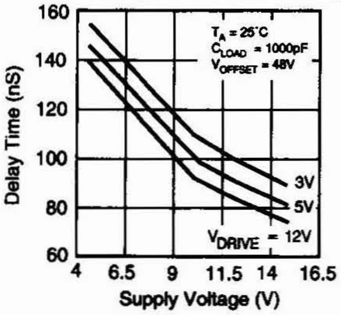
Supply Current vs DC Offset Voltage and V_{DD}



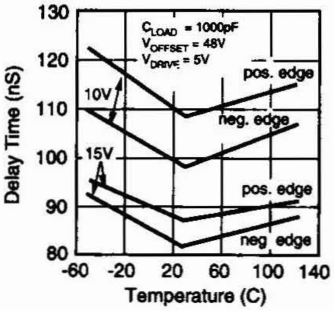
Output Rising Edge Delay Time vs Supply Voltage and Drive Voltage



Output Falling Edge Delay Time vs Supply Voltage and Drive Voltage



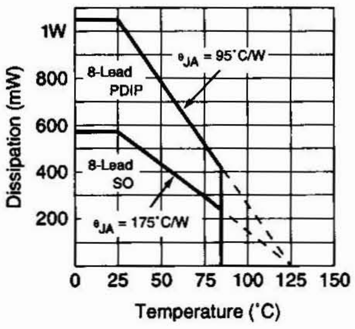
Delay Time vs Temperature and Supply Voltage



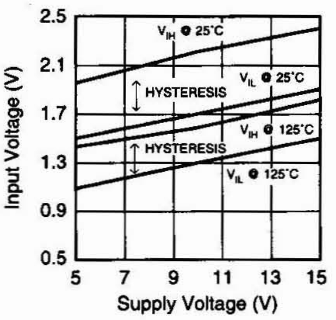
7501-4

Typical Performance Curves — Contd.

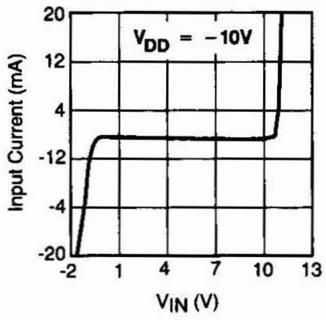
Max. Power/ Derating Curves 8-Pin Package



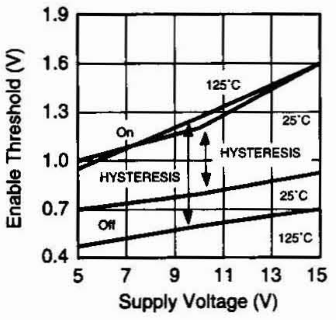
Input Threshold vs Supply Voltage



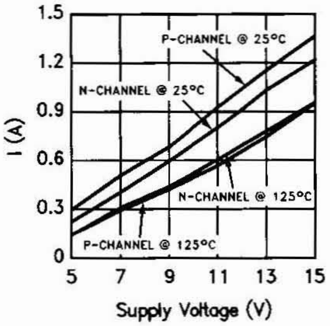
Input Current vs Input Voltage



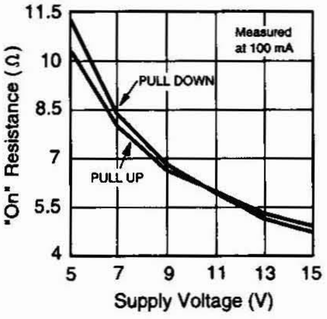
Enable Threshold vs Supply Voltage



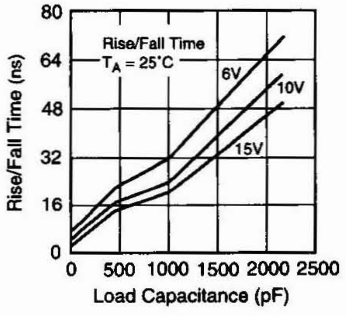
Peak Drive vs Supply Voltage



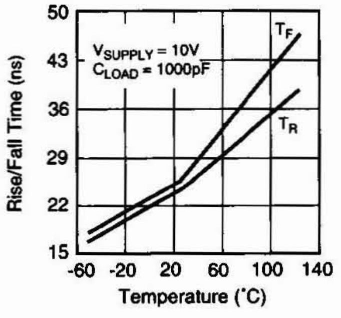
"On" Resistance vs Supply Voltage



Rise/Fall Time vs Load and Supply



Rise/Fall Time vs Temperature



7501-5

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7661C
100V Full Bridge Driver

Features

- 100V High Side Voltage
- Programmable Delay
- Direct Coupled
- No Start Up Ambiguity
- Rail to Rail Output
- 1 MHz Operation
- 1.0 Amp Peak Current
- Improved Response Times
- Matched Rise and Fall Times
- Low Supply Current
- Low Output Impedance
- Low Input Capacitance

Applications

- Uninterruptible Power Supplies
- Distributed Power Systems
- IGBT Drive
- DC-DC Converters
- Motor Control
- Power MOSFET Drive
- Switch Mode Power Supplies

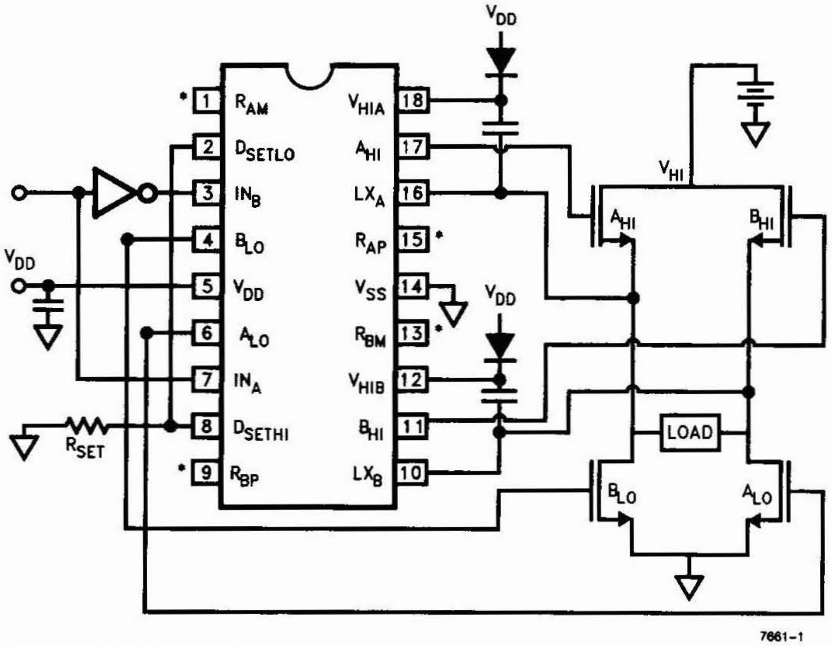
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7661CN	−40°C to +85°C	18-Pin P-DIP	MDP0031

General Description

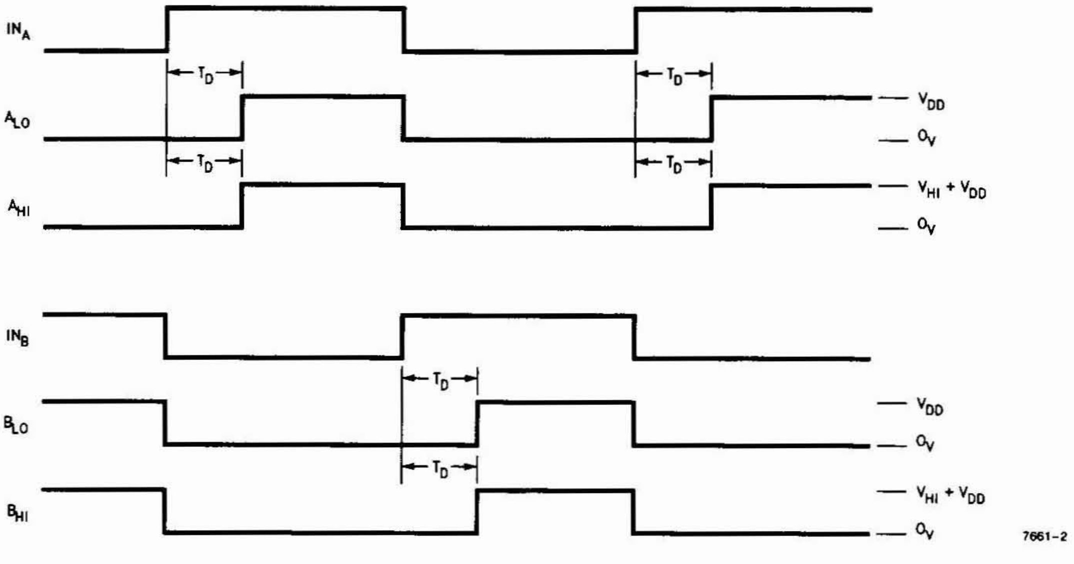
The EL7661 provides a low cost solution to many full bridge applications. The EL7661 is DC coupled so that there are no start up problems associated with AC coupled schemes. A single resistor from the D_{SET} pins to V_{SS} provides "dead time" programmability. Shorting the D_{SET} pins to V_{DD} gives the minimum delay (~100 ns).

Connection Diagram


V_{DD}
*1 R_{AM}
2 D_{SETLO}
3 IN_B
4 B_{LO}
5 V_{DD}
6 A_{LO}
7 IN_A
8 D_{SETHI}
*9 R_{BP}
18 V_{HIA}
17 A_{HI}
16 LX_A
15* R_{AP}
14 V_{SS}
13* R_{BM}
12 V_{HIB}
11 B_{HI}
10 LX_B
V_{DD}
V_{DD}
R_{SET}
V_{HI}
A_{HI}
B_{HI}
LOAD
B_{LO}
A_{LO}
7661-1

*Pins 1, 9, 13, 15 must be open.

Timing Diagram


IN_A
T_D
T_D
A_{LO}
V_{DD}
0_V
T_D
T_D
A_{HI}
$V_{HI} + V_{DD}$
0_V
IN_B
T_D
B_{LO}
V_{DD}
0_V
T_D
B_{HI}
$V_{HI} + V_{DD}$
0_V
7661-2

March 1995 Rev A

EL7661C

100V Full Bridge Driver

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{HIA} and V_{HIB} to V_{SS})	100V	Storage Temperature Range		−65°C to +150°C
Supply (V_{DD} to GND)	16.5V	Ambient Operating Temperature		−40°C to +85°C
Input Pins	−0.3V below V_{SS}, +0.3V above V_{DD}	Power Dissipation	PDIP	1600 mW
Operating Junction Temperature	125°C			
Combined Peak Output Current	4A			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

(T_A = 25C, V_{DD} = 15V, V_{SS} = 0V, C_{LOAD} = 1000 pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input/Output							
V_{IL}	Logic "1" Input Voltage		3.0	2.4		I	V
I_{IH}	Logic "1" Input Current			0.1	10.0	I	µA
V_{IL}	Logic "0" Input Voltage			1.8	0.8	I	V
V_{HYS}	Input Hysteresis			0.5		IV	V
I_{IL}	Logic "0" Input Current			0.1	10.0	I	µA
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		5.0	10.0	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		5.0	10.0	I	Ω
I_{PK}	Peak Output Current			1.0		IV	A
I_{DC}	Continuous Output Current Source/Sink		50.0			IV	mA
Power Supply							
I_{DD}	Supply Current into V_{DD}	R_{SET} = 5.1k Inputs = 15V			15.0	I	mA
I_{HIA}	Supply Current into V_{HIA}				4.0	I	mA
I_{HIB}	Supply Current into V_{HIB}				4.0	I	mA
V_{DD}	Operating Voltage		4.5		15.0	I	V

AC Electrical Characteristics

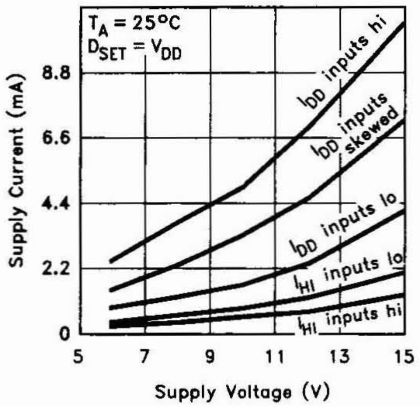
(T_A = 25C, V_{DD} = 15V, V_{SS} = 0V, C_{LOAD} =1000 pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	40.0	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	40.0	IV	ns
$t_{D\ ON\ HI}$	High Side Turn On Delay Time	D_{SET} = V_{DD} R_{SET} = 5.1k R_{SET} = 200k	50.0 75.0 750.0	100.0 125.0 1150.0	150.0 200.0 1500.0	IV I I	ns
$t_{D\ ON\ LO}$	Low Side Turn On Delay Time	D_{SET} = V_{DD} R_{SETLO} = 5.1k R_{SETLO} = 200k	50.0 75.0 750.0	100.0 125.0 1150.0	150.0 200.0 1500.0	IV I I	ns
$t_{D\ OFF\ HI}$	High Side Turn Off Delay Time	D_{SET} = V_{DD}		100.0	150.0	IV	ns
$t_{D\ OFF\ LO}$	Low Side Turn Off Delay Time	D_{SET} = V_{DD}		100.0	150.0	IV	ns
$t_{D\ MISMATCH}$	A_{HI} to A_{LO} Delay Mismatch	D_{SET} = 200k			+/-10.0	I	%
$t_{D\ MISMATCH}$	B_{HI} to B_{LO} Delay Mismatch	D_{SET} = 200k			+/-10.0	I	%
$t_{D\ MISMATCH}$	A_{HI} to B_{HI} Delay Mismatch	D_{SET} = 200k			+/-10.0	I	%
$t_{D\ MISMATCH}$	A_{LO} to B_{LO} Delay Mismatch	D_{SET} = 200k			+/-10.0	I	%

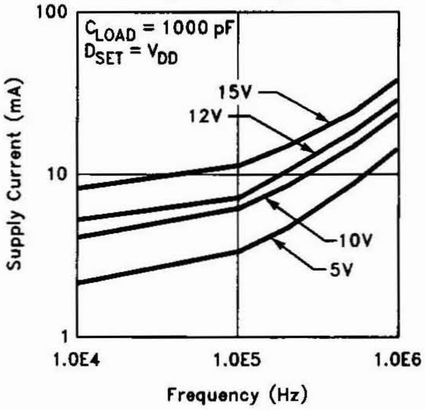
EL7661 Pin Description

Pin #	Name	Description
1	R_{AM}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. This pin is out of phase with IN_A. Normally this pin should be unconnected to any external circuitry.
2	D_{SETLO}	Connection for the delay setting resistor. This pin must be connected externally to the D_{SETHI} pin. This pin is connected internally to a PMOS diode referenced to V_{DD}.
3	IN_B	Digital input for the "B" drivers. Its polarity is non-inverting with respect to the "B" outputs.
4	B_{LO}	"B" lo-side output. Swings from V_{SS} to V_{DD}.
5	V_{DD}	Positive supply for the lo-side circuitry.
6	A_{LO}	"A" lo-side output. Swings from V_{SS} to V_{DD}.
7	IN_A	Digital input for the "A" drivers. Its polarity is non-inverting with respect to the "A" outputs.
8	D_{SETHI}	Connection for the delay setting resistor. This pin must be connected externally to the D_{SETLO} pin. This pin is connected internally to a PMOS diode referenced to V_{DD}.
9	R_{BP}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. It is in phase with IN_B. Normally this pin should be unconnected to any external circuitry.
10	LX_B	Negative supply for the "B" hi-side driver.
11	B_{HI}	"B" hi-side output. Swings from LX_B to V_{HIB}.
12	V_{HIB}	Positive supply for the "B" hi-side driver.
13	R_{BM}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. It is out of phase with IN_B. Normally this pin should be unconnected to any external circuitry.
14	V_{SS}	Negative supply for lo-side circuitry.
15	R_{AP}	Internal circuit connection. This pin swings from V_{SS} to V_{DD}. It is in phase with IN_A. Normally this pin should be unconnected to any external circuitry.
16	LX_A	Negative supply for the "A" hi-side driver.
17	A_{HI}	"A" hi-side output. Swings from LX_A to V_{HIA}.
18	V_{HIA}	Positive supply for the "A" hi-side driver.

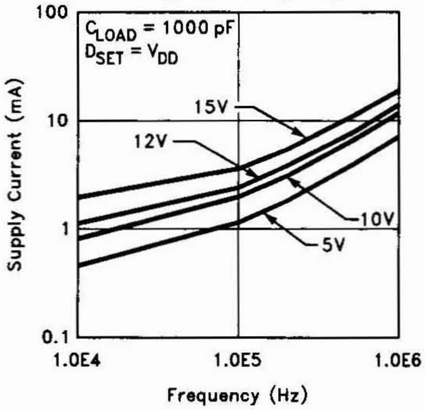
Typical Performance Curves


Quiescent Supply Current vs Supply Current

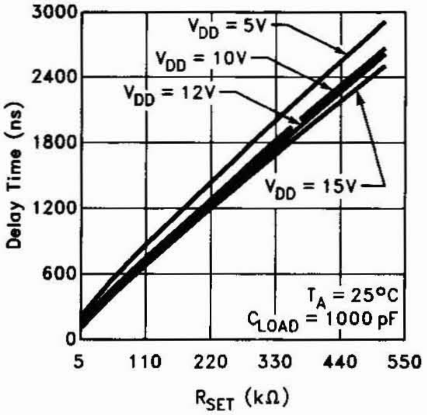
7661-3


Average Supply Curent into V_{DD} vs Voltage and Frequency

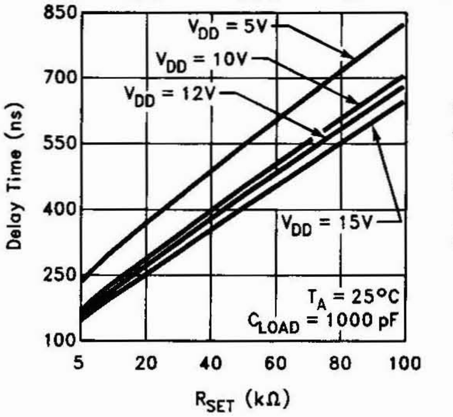
7661-4


Average Supply Curent into V_{HI} vs Voltage and Frequency

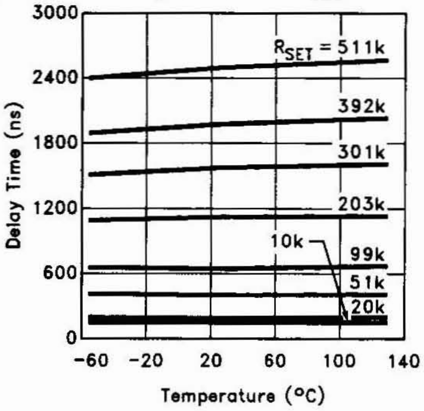
7661-5


Output Rising Edge Delay vs R_{SET} and Supply Voltage

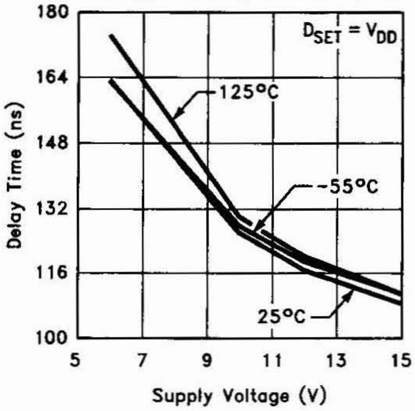
7661-6


Output Rising Edge Delay vs R_{SET} and Supply Voltage (Detail)

7661-7


Output Rising Edge Delay vs Temperature and R_{SET}

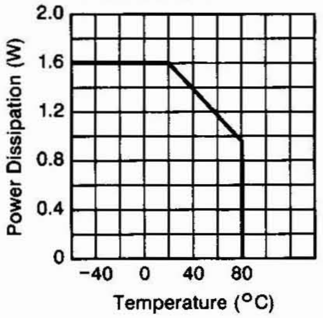
7661-8


Output Falling Edge Delay vs Supply Voltage and Temperature

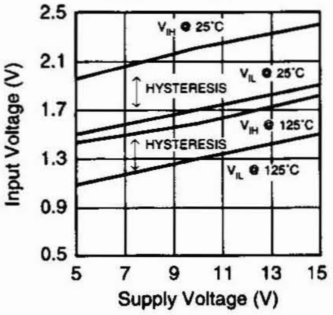
7661-9

Typical Performance Curves — Contd.

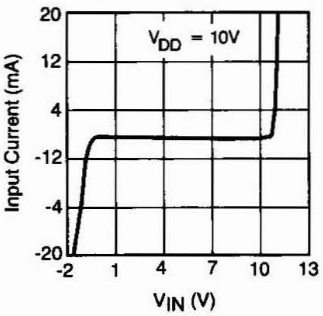
Power Dissipation vs Temperature



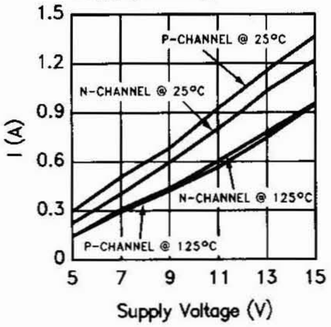
Input Threshold vs Supply Voltage



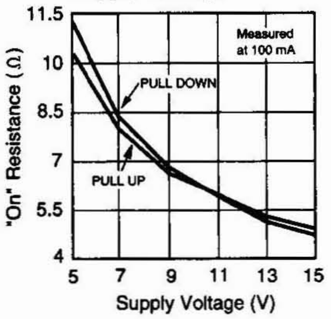
Input Current vs Input Voltage



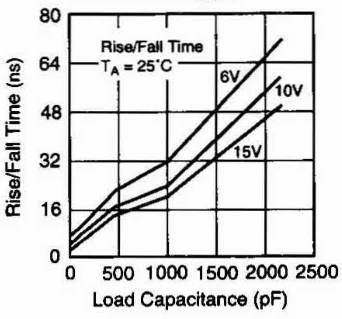
Peak Drive vs Supply Voltage



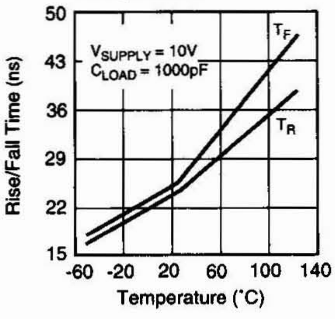
"On" Resistance vs Supply Voltage



Rise/Fall Time vs Load and Supply



Rise/Fall Time vs Temperature



7661-10

Theory of Operation

The EL7661 consists of, among other things, 4 CMOS super inverter output stages. The super inverter configuration minimizes the possibility of simultaneous conduction of the two output complementary MOS devices. Each output stage can source or sink up to 1 amp of peak current. The state of the two output stages denoted "A_{LO}" and "A_{HI}" is determined by the input "IN_A". In a like manner the state of the two output stages denoted "B_{LO}" and "B_{HI}" is determined by the input "IN_B". The lo-side output stages, "A_{LO}" and "B_{LO}" have V_{SS} as their negative supply and V_{DD} as their positive supply. The negative supply of the "A_{HI}" output stage is LX_A. The positive supply of the "A_{HI}" output stage is V_{HIA}. Similarly, the positive and negative supplies of the "B_{HI}" output stage are denoted V_{HIB} and LX_B. The hi-side supplies, LX_A, LX_B, V_{HIA}, and V_{HIB} can float with respect to V_{SS}. In fact the hi-side supplies can easily be 100V higher than V_{SS}. However, the differential voltage between V_{HIA} and LX_A, and between V_{HIB} and LX_B, should never exceed 15V.

The input signals, IN_A and IN_B, are level shifted from their quasi TTL levels to V_{SS} to V_{DD} voltages. After the level shift stage the rising edge of the signal is delayed some amount determined by the value of the resistor at the D_{SET} pin. (The falling edge of the signal has no extra delay added to it at this stage.) The delayed signal then drives its respective output drivers. The signals which drive the hi-side drivers are level shifted up to the appropriate levels while the signals which drive the lo-side drivers have an additional delay added to mimic the delay inherent in the hi-side level shift circuitry.

The circuitry which produces the resistor controlled delay of the rising edge of the output reduces down to a simple RC time constant. The R is provided by the user and the C is built into the delay circuitry. Ideally the delay would have no dependency on supply voltage or temperature since the R and C are well controlled, however, due to nonidealities of the exact implementation, the delay times are a weak function of supply voltage and temperature.

Macromodel

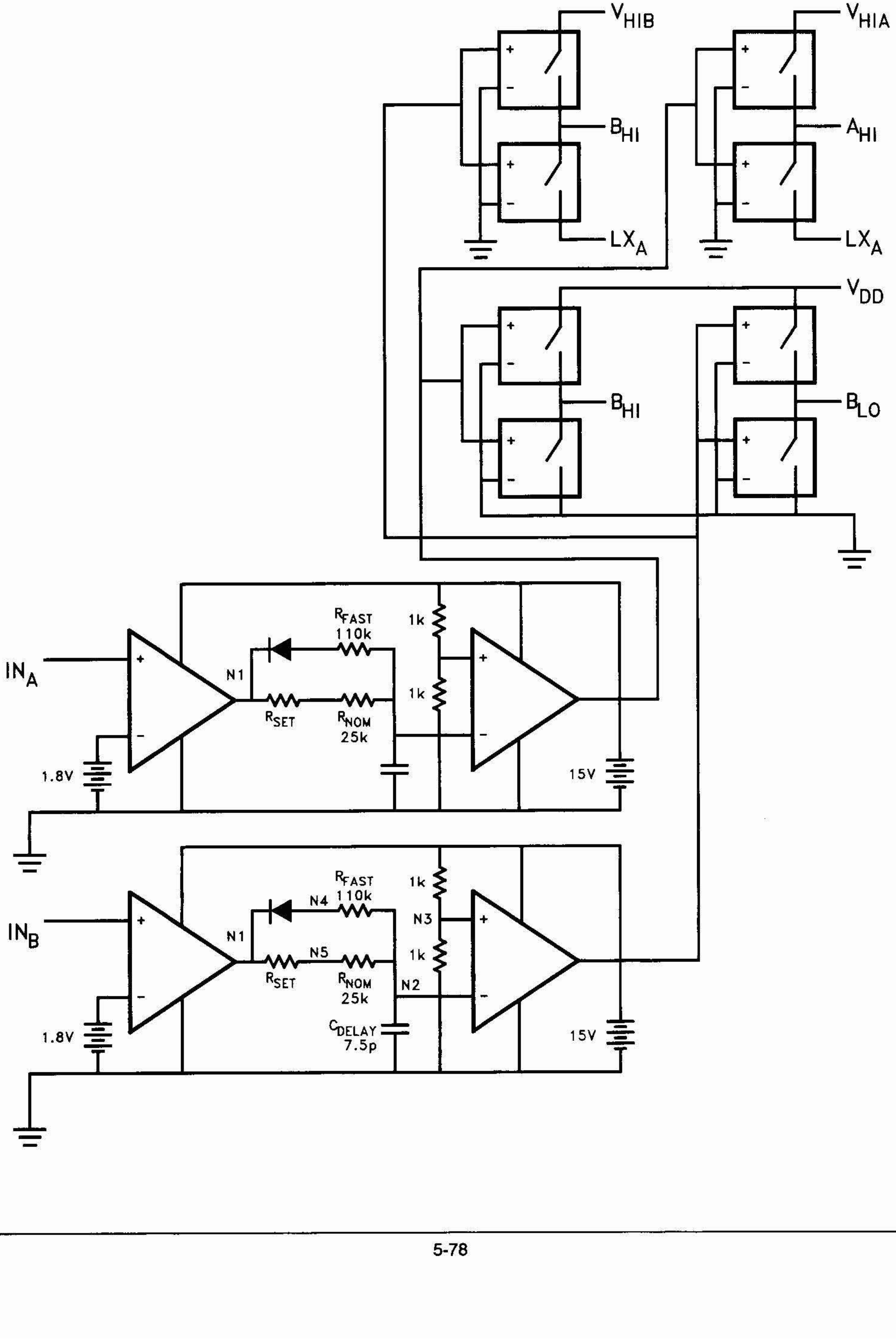
```
****EL7661 model****
*** top level circuit starts here ***
*                  a-input
*                  |       b-input
*                  |       |       a lo-side output
*                  |       |       |       b lo-side output
*                  |       |       |       |       a hi-side output
*                  |       |       |       |       |       b hi-side output
*                  |       |       |       |       |       |       a hi-side neg supply
*                  |       |       |       |       |       |       |       b hi-side neg supply
*                  |       |       |       |       |       |       |       |       lo-side neg supply
*                  |       |       |       |       |       |       |       |       |       a hi-side pos supply
*                  |       |       |       |       |       |       |       |       |       |        b hi-side pos supply
*                  |       |       |       |       |       |       |       |       |       |        |        lo-side pos supply
*                  |       |       |       |       |       |       |       |       |       |        |        |
.subckt M7661      ina     inb     alo     blo     ahi     bhi     lxa     lxb     vss     vhia     vhib     vdd
****top level subcircuit calls****
xdela ina outa vss delay
xdelb inb outb vss delay
xalo alo outa vdd vss vss outstg
xblo blo outb vdd vss vss outstg
xahi ahi outa vhia lxa vss outstg
xbhi bhi outb vhib lxb vss outstg
.ends M7661
****put in value of rset resistor here****
.param rset=50e3
****comparator subcircuit****
.subckt comp10 out inp inm vss
el out vss table {(v(inp)-v(inm))*5000} (0,0,15,15)
rout out vss 10meg
rinp inp vss 10meg
rinm inm vss 10meg
.ends comp10
```

Macromodel — Contd.

```
****input, delay, and level shift subcircuit****
.subckt delay vin compout vss
vinref vinref vss 1.8
x1 n1 vin vinref vss comp10
rslow n1 n5 {rset}
rnom n5 n2 25k
cdelay n2 vss 7.5p
ddelay n4 n1 modd
rfast n4 n2 110k
rdiv1 vddint n3 1k
rdiv2 n3 vss 1k
x2 compout n3 n2 vss comp10
vddint vddint vss 15
.model modd d is=1e-7
.ends delay
****5 ohm output stage subcircuit****
.subckt outstg out gate vhi lx vss
sp vhi out gate vss spmod
sn out 1x gate vss snmod
.model spmod vswitch ron=5 roff=2meg von=2.5 voff=4.5
.model snmod vswitch ron=5 roff=2meg von=7.5 voff=5.5
.ends outstg
```

Macromodel — Contd.

EL7661 Macromodel Schematic


VHIB
VHIA
BHI
AHI
LXA
LXA
VDD
BHI
BLO
INA
N1
RFAST 110k
RSET
RNOM 25k
1k
1k
1.8V
15V
INB
N4
N1
N5
N3
N2
CDELAY 7.5p
7661-11

EL7761C

100V Half Bridge Driver

Features

- 100V High Side Voltage
- Programmable Delay
- Direct Coupled
- No Start Up Ambiguity
- Rail to Rail Output
- 1 MHz Operation
- Shutdown Function
- 1.0 Amp Peak Current
- Improved Response Times
- Matched Rise and Fall Times
- Low Supply Current
- Low Output Impedance
- Low Input Capacitance

Applications

- Uninterruptible Power Supplies
- Distributed Power Systems
- IGBT Drive
- DC-DC Converters
- Motor Control
- Power MOSFET Drive
- Switch Mode Power Supplies

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7761CN	−40°C to +85°C	16-Pin P-DIP	MDP0031
EL7761CS	−40°C to +85°C	16-Pin SOIC	MDP0027*

*Contact factory

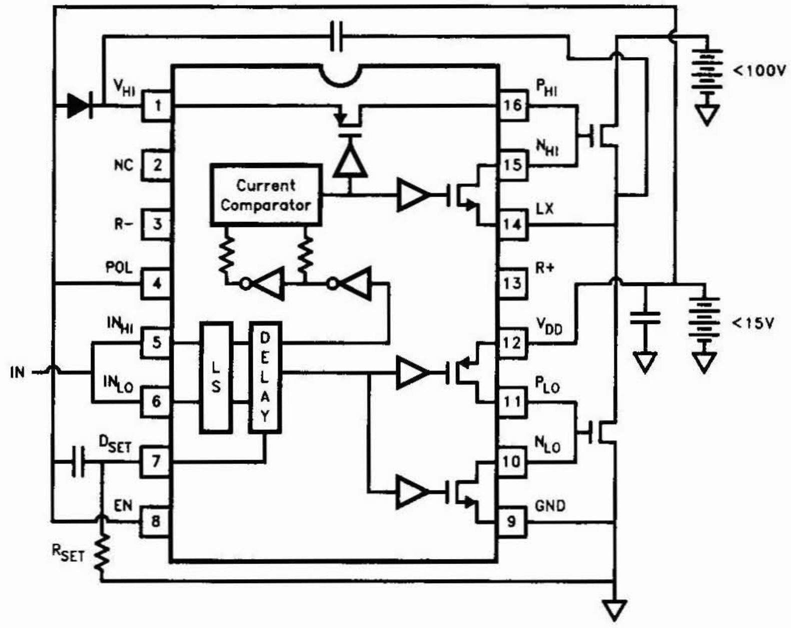
	POL	Polarity
Low Side	GND	Inverting
	V_{DD}	Non-Inverting
Hi Side	X	Inverting

General Description

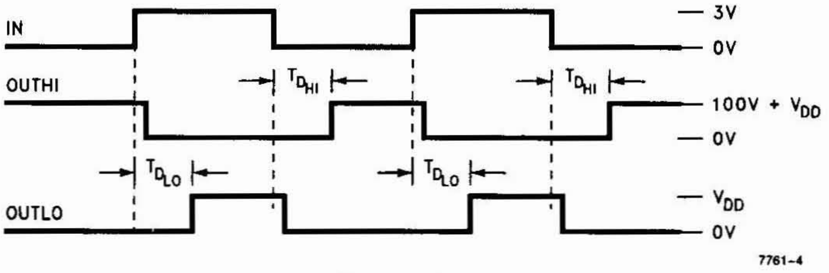
The EL7761 provides a low cost solution to many half bridge applications. The EL7761 is DC coupled so that there are no start up problems associated with AC coupled schemes. A single resistor from D_{SET} to GND provides "dead time" programmability. Shorting D_{SET} to V_{DD} gives the shortest delay (~100 ns).

The POL pin controls the polarity of the low side driver. The polarity of the upper driver is always inverting. The EN pin, when low, forces the high and low side outputs into their low state.

Connection Diagram



EL7761 Waveform Example



$T_{DLO} = T_{DHI}$
POL = V_{DD}

EL7761C

100V Half Bridge Driver

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{HI} to GND)	100V
Supply (V_{DD} to GND)	16.5V
Input Pins	−0.3V below GND, +0.3V above V_{DD}
Peak Current per Output	2A

Storage Temperature Range		−65°C to +150°C
Ambient Operating Temperature		−40°C to +85°C
Operating Junction Temperature		125°C
Power Dissipation	SOIC	1100 mW
	PDIP	1800 mW

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (T_A = 25°C, V_{DD} = 15V, C_{LOAD} = 1000pF, unless otherwise specified)

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input/Output							
V_{IH}	Logic "1" Input Voltage		3.0	2.4		I	V
I_{IH}	Logic "1" Input Current			0.1	10.0	I	μA
V_{IL}	Logic "0" Input Voltage			1.8	0.8	I	V
I_{IL}	Logic "0" Input Current			0.1	10.0	I	μA
V_{HVS}	Input Hysteresis			0.5		V	V
V_{EN_H}	Enable Threshold	Positive Edge	2.8	1.6		I	V
V_{EN_L}	Disable Threshold	Negative Edge		0.9	0.6	I	V
$V_{EN\ HYS}$	Enable Hysteresis			0.7		V	V
$I_{DS\ OFF}$	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}	−10.0	0.2	10.0	I	μA
R_{OH}	Pull-up Resistance	I_{OUT} = −100 mA		5.0	10.0	I	Ω
R_{OL}	Pull-down Resistance	I_{OUT} = +100 mA		5.0	10.0	I	Ω
I_{PK}	Peak Output Current			1.0		IV	A
I_{DC}	Continuous Output Current Source/Sink		50.0			IV	mA
Power Supply							
I_{DD}	Supply Current into V_{DD}	R_{SET} = 5.1k		6.0	10.0	I	mA
I_{HI}	Supply Current into V_{HI}			2.0	4.0	I	mA
$I_{DD\ OFF}$	Supply Current into V_{DD}	V_{EN} = 0.6V			750.0	I	uA
V_{DD}	Operating Voltage		4.5		15.0	I	V

AC Electrical Characteristics (T_A = 25°C, V_{DD} = 15V, C_{LOAD} = 1000pF, unless otherwise specified)

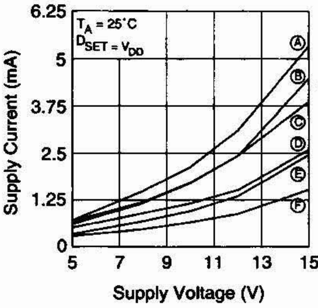
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500pF C_L = 1000pF		15.0 20.0	 40.0	IV	ns
t_F	Fall Time	C_L = 500pF C_L = 1000pF		15.0 20.0	 40.0	IV	ns
$t_{D\ ON\ HI}$	High Side Turn On Delay Time	D_{SET} = V_{DD} R_{SET} = 5.1k R_{SET} = 400k	50.0 75.0 750.0	100.0 125.0 1150.0	150.0 200.0 1500.0	IV I I	ns
$t_{D\ ON\ LO}$	Low Side Turn On Delay Time	D_{SET} = V_{DD} R_{SET} = 5.1k R_{SET} = 400k	50.0 75.0 750.0	100.0 125.0 1150.0	150.0 200.0 1500.0	IV I I	ns
$t_{D\ OFF\ HI}$	High Side Turn Off Delay Time	D_{SET} = V_{DD}		100.0	150.0	IV	ns
$t_{D\ OFF\ LO}$	Low Side Turn Off Delay Time	D_{SET} = V_{DD}		100.0	150.0	IV	ns
$t_{D\ MISMATCH}$	High to Lo Side Turn On Delay Mismatch	R_{SET} = 400k			±10.0	I	%

Pin Description

Pin #	Name	Function
1	V_{HI}	Positive supply for the high side driver.
2	NC	
3	R^-	Internal connection between the low side and high side driver. This pin is normally unconnected.
4	P_{OL}	Controls the polarity of the low side driver.
5	IN_{HI}	Logic input for the high side driver.
6	IN_{LO}	Logic input for the low side driver.
7	D_{SET}	Connection for the delay adjust resistor.
8	EN	A high voltage on this pin enables the part.
9	GND	Negative supply of the low side driver and control circuitry.
10	N_{LO}	Low side driver output pull down.
11	P_{LO}	Low side driver output pull up.
12	V_{DD}	Positive supply of the low side driver and control circuitry.
13	R^+	Internal connection between the low side and high side driver. This pin is normally unconnected.
14	LX	Negative supply for the high side driver.
15	N_{HI}	High side driver output pull down.
16	P_{HI}	High side driver output pull up.

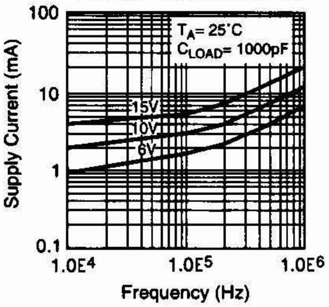
Typical Performance Curves

Quiescent Supply Current vs. Supply Voltage

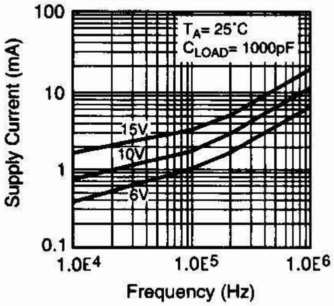


Curve	Supply I	Condition
Ⓐ	I_{DD}	$V_{IN} = 0V$, POL = 0V
Ⓑ	I_{DD}	$V_{IN} = 0V$, POL = 0V
Ⓒ	I_{DD}	$V_{IN} = V_{DD}$, POL = 0V
Ⓓ	I_{DD}	$V_{IN} = V_{DD}$, POL = V_{DD}
Ⓔ	I_{HI}	$V_{IN} = V_{DD}$
Ⓕ	I_{HI}	$V_{IN} = 0V$

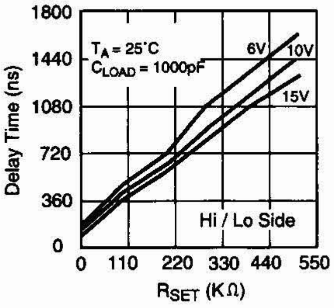
Avg. Supply Current into V_{DD} vs. Voltage and Frequency



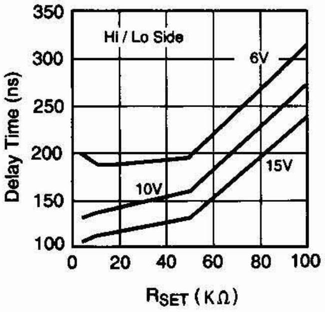
Average Supply Current into V_{HI} vs. Voltage and Frequency



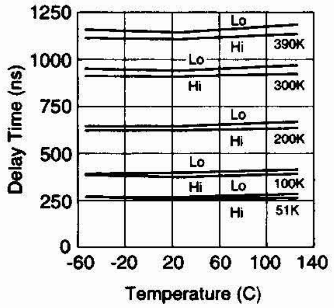
Output Rising Edge Delay vs. R_{SET} and Supply Voltage



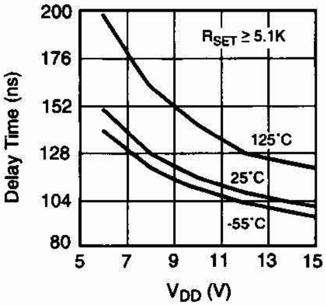
Output Rising Edge Delay vs. R_{SET} and Supply Voltage (Detail)



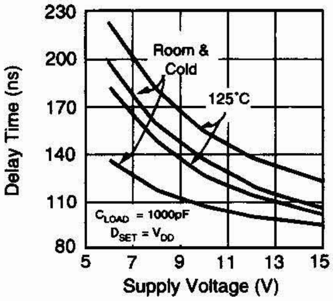
Output Rising Edge Delay vs. Temperature and R_{SET}



Output Falling Edge Delay vs. Supply Voltage and Temperature



Delay Times* vs. Supply Voltage and Temperature

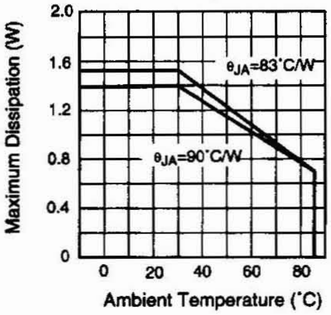


7761-2

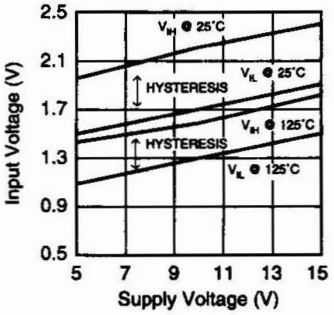
*Minimum Rising and Falling Edge Delay Times

Typical Performance Curves — Contd.

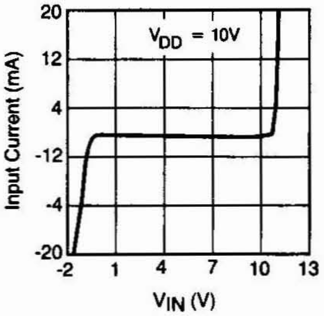
Max. Power/Derating Curves 16 Pin Package



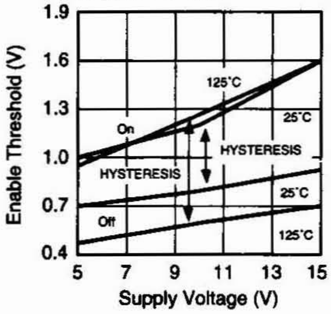
Input Threshold vs. Supply Voltage



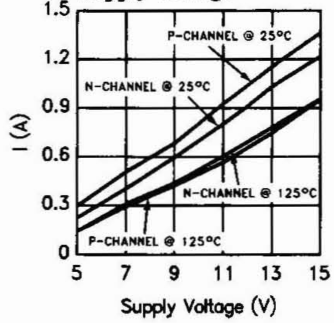
Input Current vs. Input Voltage



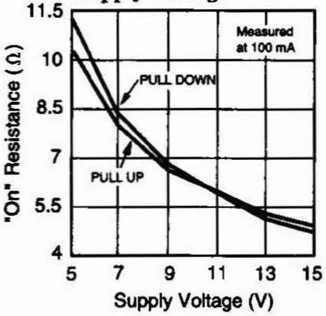
Enable Threshold vs. Supply Voltage



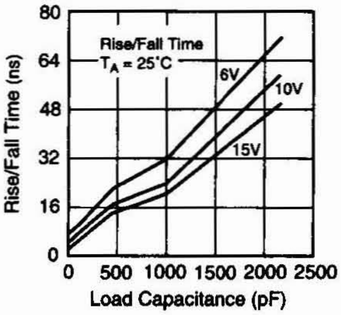
Peak Drive vs. Supply Voltage



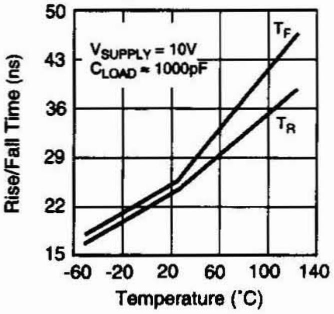
"On" Resistance vs. Supply Voltage



Rise/Fall Time vs. Load and Supply



Rise/Fall Time vs. Temperature



7761-3

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7861C
Rising Edge Delay Driver

Features

- Programmable Delay
- 1 MHz Operation
- Shutdown Function
- 1.0 Amp Peak Current
- Matched Rise and Fall Times
- Low Supply Current
- Low Output Impedance
- Low Input Capacitance

Applications

- Uninterruptible Power Supplies
- Distributed Power Systems
- IGBT Drive
- DC-DC Converters
- Motor Control
- Power MOSFET Drive
- Switch Mode Power Supplies

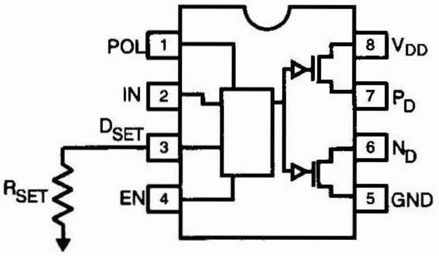
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7861CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7861CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

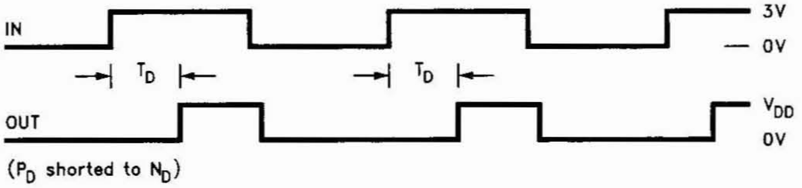
The EL7861 provides 1.0A of peak current for many driver applications. The rising edge of the output can be delayed up to 1.5 μs from the corresponding input edge. A single resistor from D_{SET} to GND sets the delay time. Connecting the D_{SET} pin to V_{DD} disables the delay block giving approximately 30 ns delay times. The circuit contains an enable feature as well as user definable polarity. The programmable delay is useful in applications requiring compensation for long switch turn off times and applications using resonant mode technology.

Connection Diagram



7861-1

7861 Waveform Example
POL = V_{DD}



7861-4

POL	Polarity
V_{DD}	Non-Inverting
GND	Inverting

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{DD} to GND)	16.5V
Input Pins	−0.3V below GND, +0.3V above V_{DD}
Operating Junction Temperature	125°C
Peak Output Current	2A

Ambient Operating Temperature		−40°C to +85°C
Storage Temperature Range		−65°C to +150°C
Power Dissipation	SOIC	570 mW
	PDIP	1050 mW

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (T_A = 25°C, V_{DD} = 15V, C_{LOAD} = 1000 pF, unless otherwise specified)

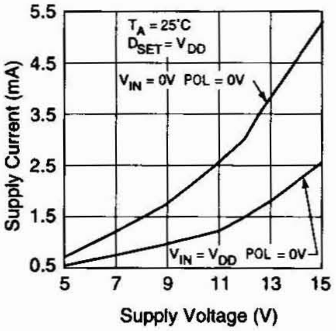
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input/Output							
V_{IH}	Logic "1" Input Voltage		3.0	2.4		I	V
I_{IH}	Logic "1" Input Current			0.1	10.0	I	μA
V_{IL}	Logic "0" Input Voltage			1.6	0.8	I	V
I_{IL}	Logic "0" Input Current			0.1	10.0	I	μA
V_{HVS}	Input Hysteresis			0.5		V	V
V_{ENH}	Enable Threshold	Positive Edge	2.8	1.6		I	V
V_{ENL}	Disable Threshold	Negative Edge		0.9	0.6	I	V
$V_{EN\ HYS}$	Enable Hysteresis			0.7		V	V
$I_{DS\ OFF}$	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}		0.2	10.0	I	μA
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		5.0	10.0	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		5.0	10.0	I	Ω
I_{PK}	Peak Output Current			1.0		IV	A
I_{DC}	Continuous Output Current Source/Sink		50.0			IV	mA
Power Supply							
I_{DD}	Supply Current into V_{DD}	R_{SET} = 5.1k		6.0	10.0	I	mA
$I_{DD\ OFF}$	Supply Current into V_{DD}	V_{EN} = 0.6V			750.0	I	μA
V_{DD}	Operating Voltage		4.5		15.0	I	V

AC Electrical Characteristics (T_A = 25°C, V_{DD} = 15V, C_{LOAD} = 1000 pF, unless otherwise specified)

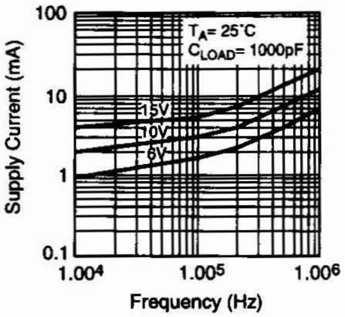
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Power Supply							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	 40.0	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	 40.0	IV	ns
$t_{D\ ON}$	Turn On Delay Time	D_{SET} = V_{DD} R_{SET} = 5.1k R_{SET} = 400k	10.0 25.0 750.0	30.0 50.0 1150.0	150.0 200.0 1500.0	IV I I	ns
$t_{D\ OFF}$	Turn Off Delay Time	D_{SET} = V_{DD}		30.0	50.0	IV	ns

Typical Performance Curves

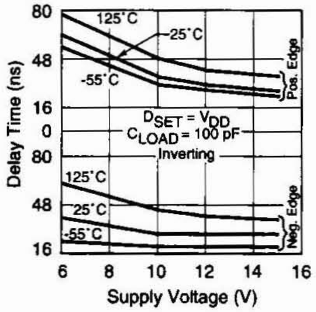
Quiescent Supply Current vs Supply Voltage



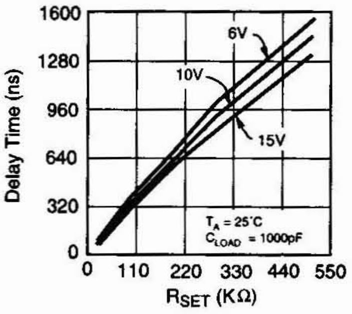
Average Supply Current vs Voltage and Frequency



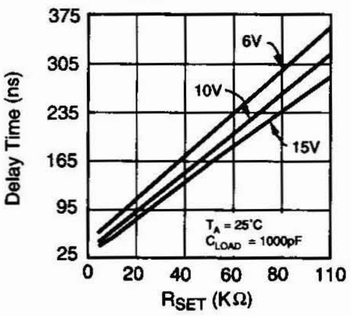
Delay Times vs Supply Voltage and Temp



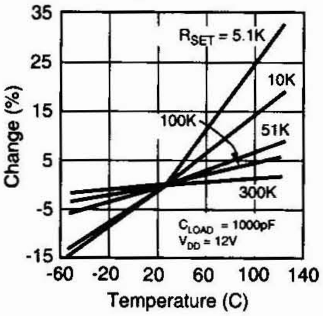
Output Rising Edge Delay vs R_{SET} and Supply Voltage



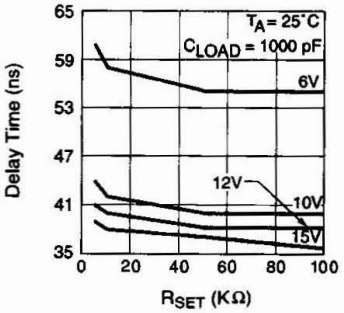
Output Rising Edge Delay vs R_{SET} and Supply Voltage (Detail)



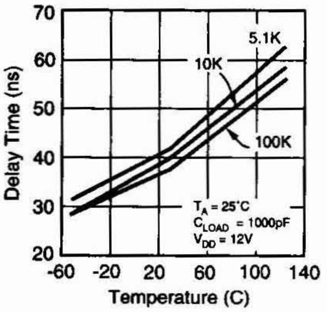
Output Rising Edge Delay Change vs Temperature



Output Falling Edge Delay vs R_{SET} and V_{DD}

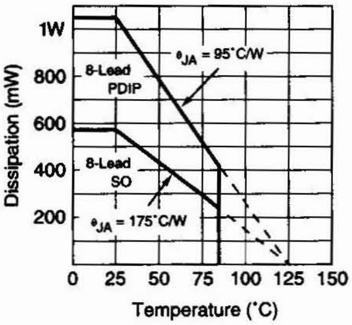


Output Falling Edge Delay vs Temperature and R_{SET}

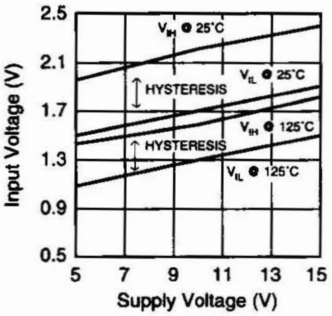


7861-2

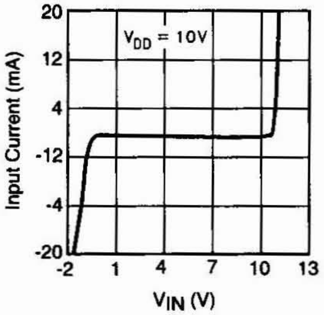
Typical Performance Curves — Contd.



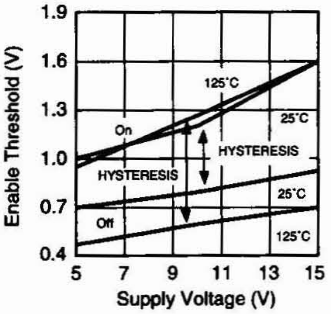
Max. Power/Derating Curves 8-Pin Package



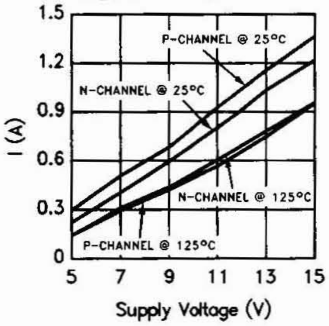
Input Threshold vs. Supply Voltage



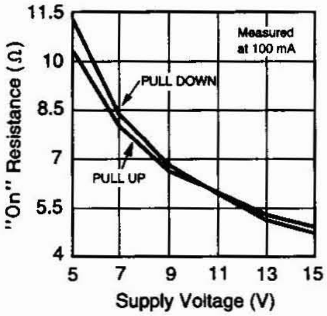
Input Current vs Input Voltage



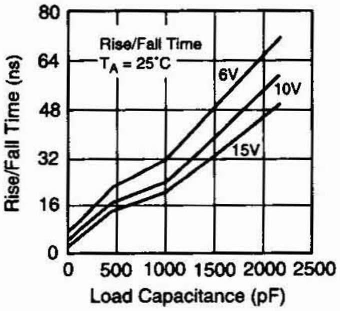
Enable Threshold vs Supply Voltage



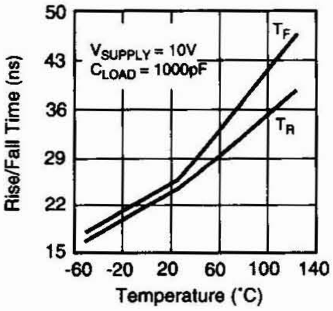
Peak Drive vs Supply Voltage



"On" Resistance vs Supply Voltage



Rise/Fall Time vs Load and Supply



Rise/Fall Time vs Temperature

7861-3

EL7961C/EL7971C/EL7981C

Dual Rising Edge Delay Driver

Features

- Programmable delay
- 1 MHz operation
- 1.0A peak current
- Matched rise/fall times
- Low power
- Rail to rail output
- Low output impedance
- Low input capacitance

Applications

- Uninterruptible power supplies
- IGBT driver
- DC-DC converters
- Motor control
- Power MOSFET drivers
- Switch mode power supplies

Ordering Information

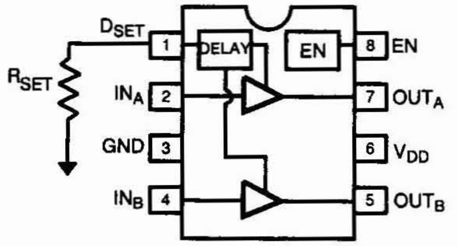
Part No.	Temp. Range	Package	Outline #
EL7961CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7961CS	−40°C to +85°C	8-Lead SO	MDP0027
EL7971CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7971CS	−40°C to +85°C	8-Lead SO	MDP0027
EL7981CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7981CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

The EL7961/EL7971/EL7981 provides 1.0A peak current for many driver applications. The rising edge of the output can be delayed up to 1.5 μs from the input edge. A resistor from D_{SET} to GND sets the delay time for both channel A and B. This programmable delay is useful in applications requiring compensation for long switch turn off times. Pulling D_{SET} high disables the delay block giving approximately 30 ns delay times.

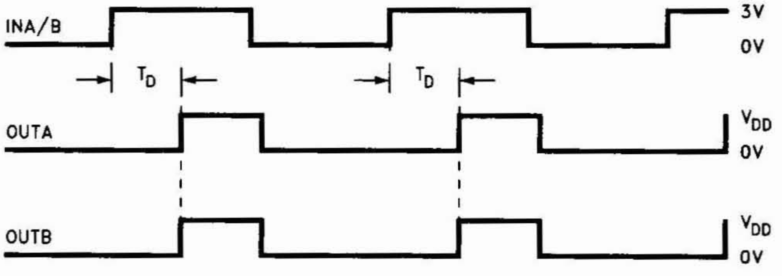
EL7961 - Non-Inverting
EL7971 - Inverting
EL7981 - Channel A - Inverting
Channel B - Non-Inverting

Connection Diagram



7961-1

7961 Waveform Example



7961-4

EL7961C/EL7971C/EL7981C

Dual Rising Edge Delay Driver

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{DD} to GND)	16.5V
Input Pins	−0.3V below GND, +0.3V above V_{DD}
Operating Junction Temperature	125°C
Peak Output Current	2A

Ambient Operating Temperature		−40°C to +85°C
Storage Temperature Range		−65°C to +150°C
Power Dissipation	SOIC	570 mW
	PDIP	1050 mW

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (T_A = 25°C, V_{DD} = 15V, C_{LOAD} = 1000 pF unless otherwise specified)

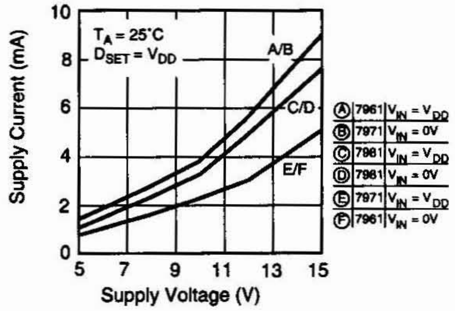
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input/Output							
V_{IH}	Logic "1" Input Voltage		3.0	2.4		I	V
I_{IH}	Logic "1" Input Current			0.1	10.0	I	μA
V_{IL}	Logic "0" Input Voltage			1.8	0.8	I	V
I_{IL}	Logic "0" Input Current			0.1	10.0	I	μA
V_{HVS}	Input Hysteresis			0.5		V	V
V_{ENH}	Enable Threshold	Positive Edge	2.8	1.6		I	V
V_{ENL}	Disable Threshold	Negative Edge		0.9	0.6	I	V
$V_{EN\ HYS}$	Enable Hysteresis			0.7		V	V
R_{OH}	Pull-up Resistance	I_{OUT} = −100 mA		5.0	10.0	I	Ω
R_{OL}	Pull-down Resistance	I_{OUT} = +100 mA		5.0	10.0	I	Ω
I_{PK}	Peak Output Current			1.0		IV	A
I_{DC}	Continuous Output Current Source/Sink		50.0			IV	mA
Power Supply							
I_{DD}	Supply Current into V_{DD}	R_{SET} = 5.1k Inputs = 15V			10.0	I	mA
$I_{DD\ OFF}$	Supply Current into V_{DD}	V_{EN} = 0V			1.5	I	mA
V_{DD}	Operating Voltage		4.5		15.0	I	V

AC Electrical Characteristics (T_A = 25C, V_{DD} = 15V, C_{LOAD} = 1000 pF unless otherwise specified)

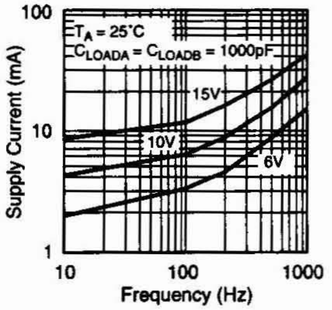
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	40.0	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	40.0	IV	ns
$t_{D\ ON}$	Turn On Delay Time	D_{SET} = V_{DD}	10.0	30.0	50.0	IV	ns
		R_{SET} = 5.1k	30.0	60.0	120.0	I	ns
		R_{SET} = 200k	750.0	1150.0	1500.0	I	ns
$t_{D\ OFF}$	Turn Off Delay Time	D_{SET} = V_{DD}		30.0	50.0	IV	ns
$t_{D\ MISMATCH}$	Channel A to B Turn On Delay Mismatch	R_{SET} = 200k			±15.0	I	%

Typical Performance Curves

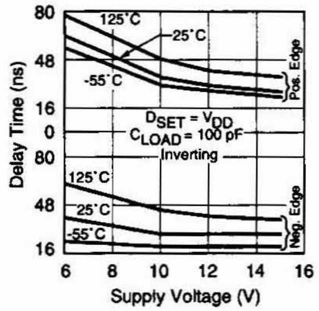
Quiescent Supply Current vs Supply Voltage



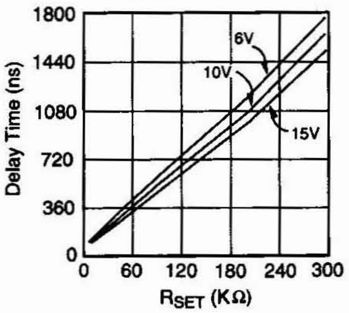
Average Supply Current vs Voltage and Frequency



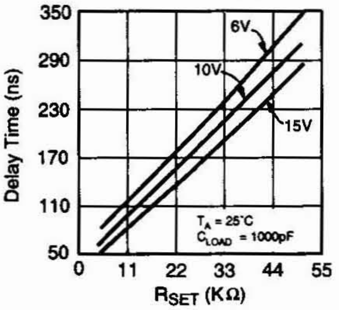
Delay Times vs Supply Voltage and Temperature



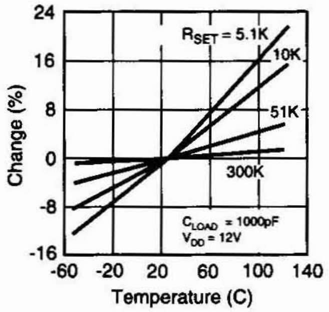
Output Rising Edge Delay vs R_{SET} and Supply Voltage



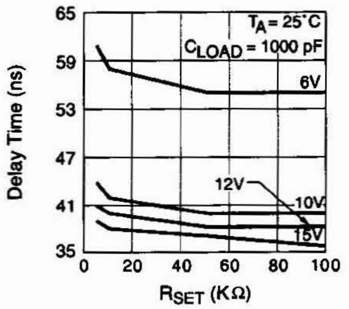
Output Rising Edge Delay vs R_{SET} and Supply Voltage (Detail)



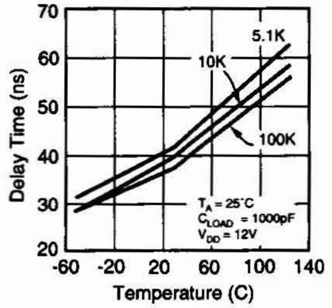
Output Rising Edge Delay Percentage Change vs Temperature



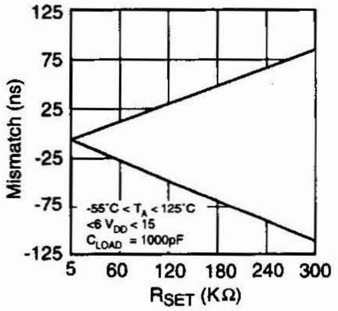
Output Falling Edge Delay vs R_{SET} vs V_{DD}



Output Falling Edge Delay vs Temperature and R_{SET}



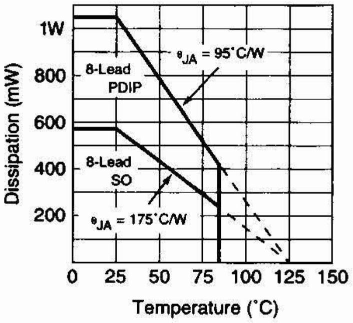
Output Rising Edge Delay Channel to Channel Mismatch vs R_{SET}



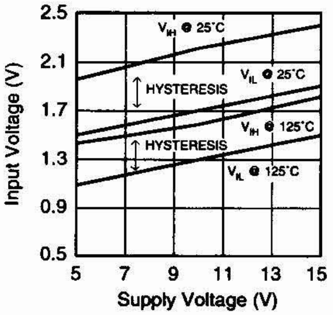
7961-2

Typical Performance Curves — Contd.

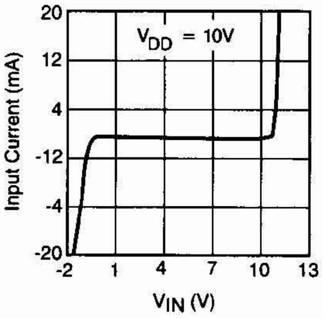
Max Power/Derating Curves
8-Pin Package



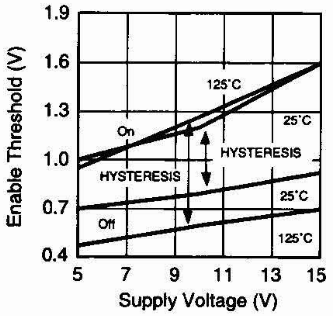
Input Threshold
vs Supply Voltage



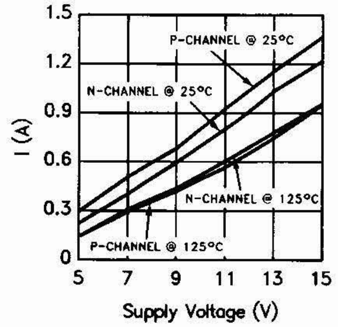
Input Current
vs Input Voltage



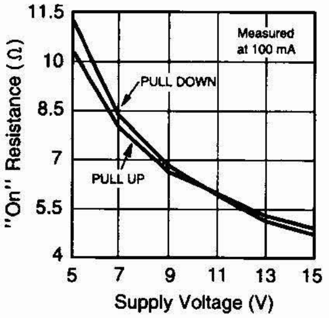
Enable Threshold
vs Supply Voltage



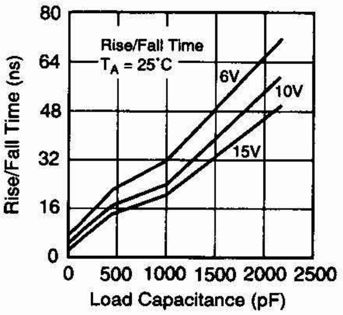
Peak Drive
vs Supply Voltage



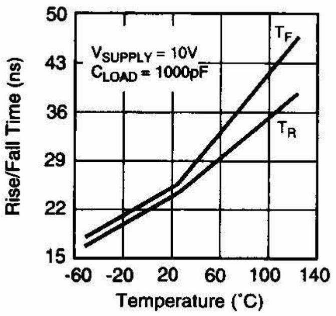
"On" Resistance
vs Supply Voltage



Rise/Fall Time
vs Load and Supply



Rise/Fall Time
vs Temperature



7961-3

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7962C/EL7972C/EL7982C
Dual Rising Edge Delay Driver

Features

- Programmable delay
- 1 MHz operation
- 1.0A peak current
- Matched rise and fall times
- Low supply current
- Rail-to-Rail output
- Low output impedance
- Low input capacitance

Applications

- Uninterruptible power supplies
- Distributed power systems
- IGBT drive
- DC-DC converters
- Motor control
- Power MOSFET drive
- Switch mode power supplies

Ordering Information

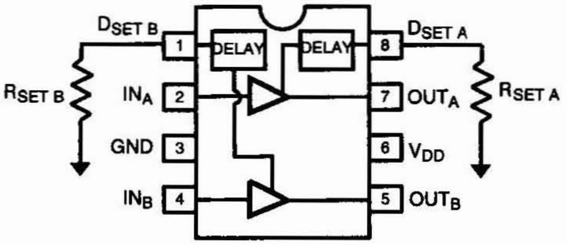
Part No.	Temp. Range	Package	Outline #
EL7962CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7972CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7982CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7762CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL7772CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL7782CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL7962/72/82 provides 1.0A of peak current for many driver applications. The rising edge of the output can be delayed up to 1.5 μs from the corresponding input edge. A resistor from $D_{SET\ A}$ to GND sets the delay time for channel A. Likewise a resistor from $D_{SET\ B}$ to GND sets the delay time for channel B. Connecting the $D_{SET\ A}$ pin to V_{DD} disenables the delay blocks, giving approximately 30 ns delay times for both channels. This programmable delay is useful in applications requiring compensation for long switch turn off times and applications using resonant mode technology

EL7962 - both channels non-inverting
EL7972 - both channels inverting
EL7982 - channel A inverting
channel B non-inverting

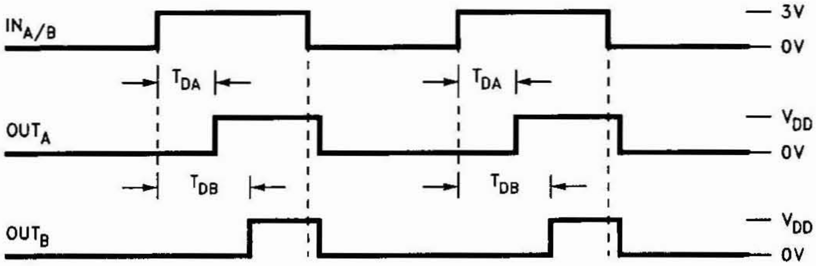
Connection Diagram



7962-1

7962 Waveform Example

$T_{DA} \neq T_{DB}$



7962-4

$R_{SET\ B} > R_{SET\ A} \rightarrow T_{DB} > T_{DA}$

January 1996 Rev B

EL7962C/EL7972C/EL7982C

Dual Rising Edge Delay Driver

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{DD} to GND)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V below GND, +0.3V above V_{DD}	Storage Temperature Range	−65°C to +150°C
		Power Dissipation	
Peak Current per Output	2A	SOIC	570 mW
Ambient Operating Temperature	−40°C to +85°C	PDIP	1050 mW

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterisation Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (T_A = 25°C, V_{DD} = 15V, C_{LOAD} = 1000 pF, unless otherwise specified)

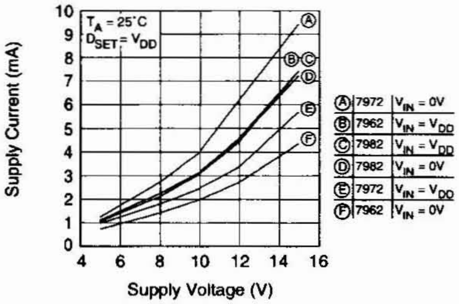
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input/Output							
V_{IH}	Logic "1" Input Voltage		3.0	2.4		I	V
I_{IH}	Logic "1" Input Current			0.1	10.0	I	μA
V_{IL}	Logic "0" Input Voltage			1.8	0.8	I	V
I_{IL}	Logic "0" Input Current			0.1	10.0	I	μA
V_{HVS}	Input Hysteresis			0.5		V	V
R_{OH}	Pull-up Resistance	I_{OUT} = −100 mA		5.0	10.0	I	Ω
R_{OL}	Pull-down Resistance	I_{OUT} = +100 mA		5.0	10.0	I	Ω
I_{PK}	Peak Output Current			1.0		IV	A
I_{DC}	Continuous Output Current Source/Sink		50			IV	mA
Power Supply							
I_{DD}	Supply Current into V_{DD}	R_{SET} = 5.1k Inputs = 15V			12.0	I	mA
V_{DD}	Operating Voltage		4.5		15.0	I	V

AC Electrical Characteristics (T_A = 25C, V_{DD} = 15V, C_{LOAD} = 1000 pF, unless otherwise specified)

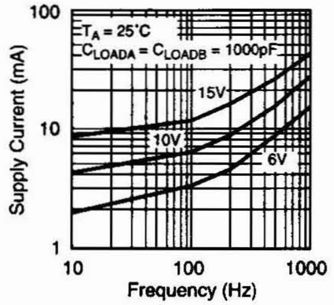
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	 40.0	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		15.0 20.0	 40.0	IV	ns
$t_{D\ ON}$	Turn On Delay Time	D_{SET} = V_{DD}	10.0	30.0	50.0	IV	ns
		R_{SET} = 5.1k	30.0	60.0	120.0	I	ns
		R_{SET} = 400k	750.0	1150.0	1500.0	I	ns
$t_{D\ OFF}$	Turn Off Delay Time	D_{SET} = V_{DD}		30.0	50.0	IV	ns
$t_{D\ MISMATCH}$	Channel A to B Turn On Delay Mismatch	R_{SET} = 400k $R_{SET\ A}$ = $R_{SET\ B}$			± 10.0	I	%

Typical Performance Curves

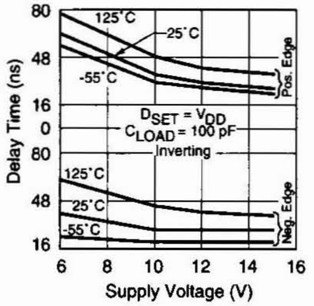
Quiescent Supply Current vs Supply Voltage



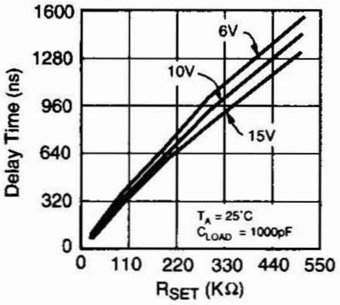
Average Supply Current vs Voltage and Frequency



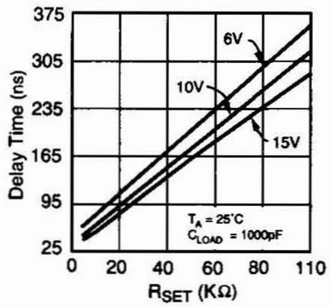
Delay Times vs Supply Voltage and Temp.



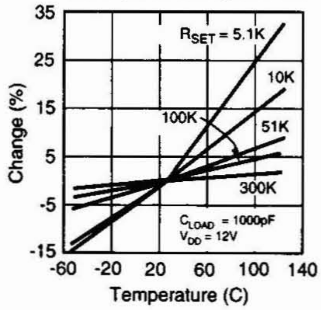
Output Rising Edge Delay vs R_{SET} and Supply Voltage



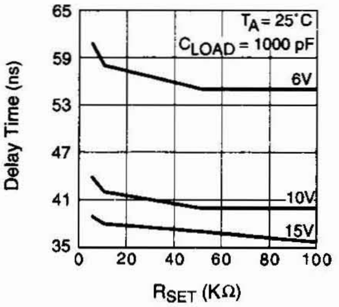
Output Rising Edge Delay vs R_{SET} and Supply Voltage (Detail)



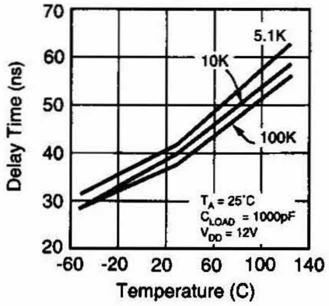
Output Rising Edge Delay Percentage Change vs Temperature



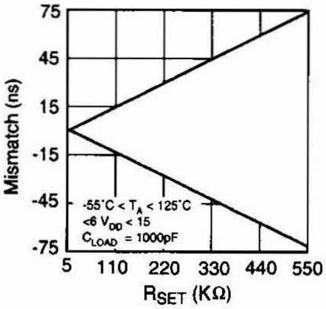
Output Falling Edge Delay vs R_{SET} vs V_{DD}



Output Falling Edge Delay vs Temperature and R_{SET}



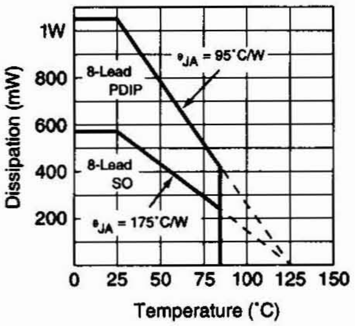
Output Rising Edge Delay Channel to Channel Mismatch



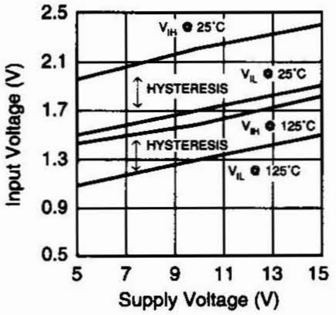
7962-2

Typical Performance Curves — Contd.

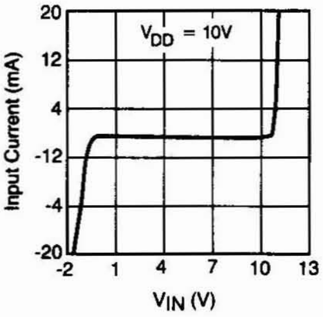
Max Power/Derating Curves 8-Pin Package



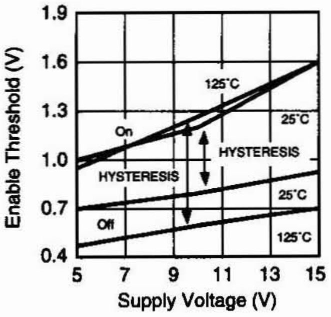
Input Threshold vs Supply Voltage



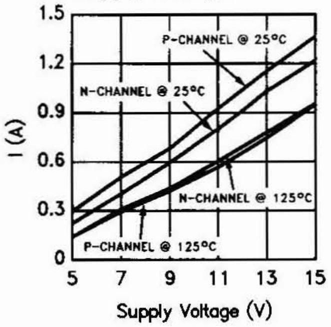
Input Current vs Input Voltage



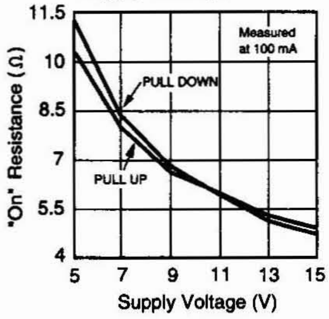
Enable Threshold vs Supply Voltage



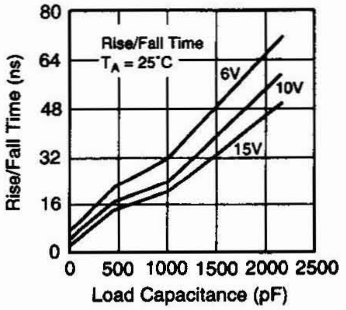
Peak Drive vs Supply Voltage



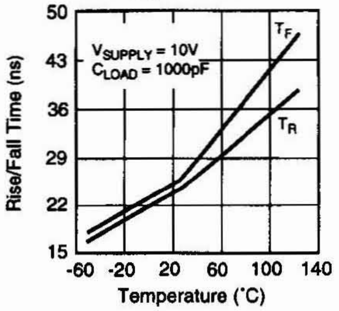
"On" Resistance vs Supply Voltage



Rise/Fall Time vs Load and Supply



Rise/Fall Time vs Temperature



7962-3

Variable Pulse Width Variable Frequency Pulse Generator

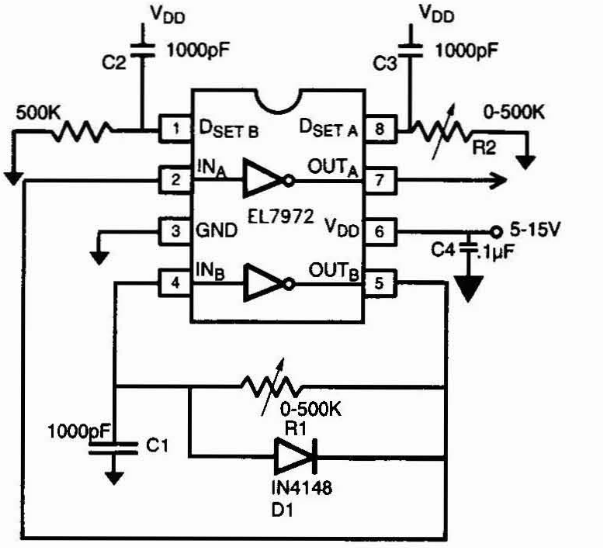
This application uses the "B" driver of the EL7972 as an oscillator to drive the "A" driver. The frequency is set using R1 and C1. The pulse width is set by adjusting R2. Capacitors C2, C3 and C4 are decoupling capacitors. A fixed pulse width output is available at pin 5 while the variable pulse width signal is available at pin 7. For these particular component values a maximum pulse width of 2 μs is available at pin 7.

The frequency is approximated by the relation:

$$f(\mathrm{Hz}) = \frac{(1.5)\sqrt{V_{DD}}}{(R1)(C1)}$$

The pulse width is approximated by the relation:

$$T_{\text{width}}\,(S) = \frac{(4.5 \times 10^{-6})\left(1 - \frac{R2}{500K}\right)}{\sqrt{V_{DD}}} - 100\text{ ns}$$

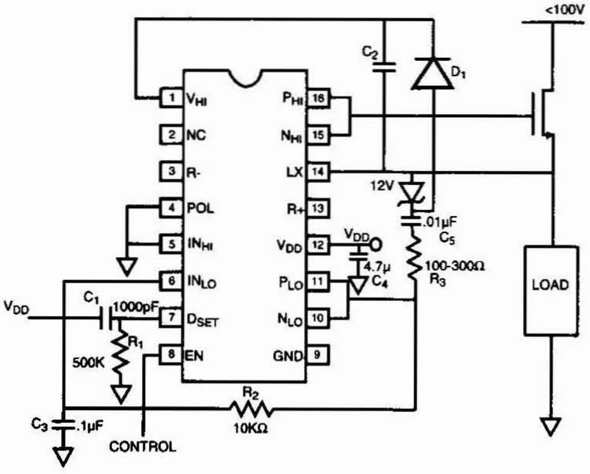

V_DD
C2
1000pF
V_DD
C3
1000pF
500K
1
D_SET B
D_SET A
8
0-500K
R2
2
IN_A
OUT_A
7
3
GND
EL7972
V_DD
6
5-15V
C4
.1μF
4
IN_B
OUT_B
5
0-500K
R1
1000pF
C1
IN4148
D1

0942-1

100V DC Stable High Switch

This application uses an EL7761 to drive the gate of an NMOS FET above the FET's source and drain voltage. This circuit would be useful in applications where the load must be energized continuously as in an automobile headlight circuit or a high side switch to a 48V bus in a distributed power application.

The low side driver self oscillates at a frequency determined by its input hysteresis in conjunction with R2 and C3. The output of the oscillator (pins 10 and 11) drive a charge pump which powers the high side drive section of the EL7761. A low voltage at the EN pin shuts the drive to the external FET off as well as shutting down the charge pump oscillator and putting the chip into a low supply current mode. Capacitors C1 and C4 are used to decouple the supplies. V_{DD} must be at least a diode drop higher than the desired enhancement of the external FET. The reverse breakdown of the zener diode should be less than 15V in order to avoid an overvoltage of the high side driver. Depending on the exact nature of the circuit a zener diode is not always necessary.


<100V
C2
D1
1 V_HI
2 NC
3 R-
4 POL
5 IN_HI
6 IN_LO
7 D_SET
8 EN
P_HI 16
N_HI 15
LX 14
R+ 13
V_DD 12
P_LO 11
N_LO 10
GND 9
12V
.01μF
C5
V_DD
4.7μ
C4
100-300Ω
R3
LOAD
V_DD
C1
1000pF
R1
500K
R2
10KΩ
C3
.1μF
CONTROL

C_1 - 1000pF ceramic
C_2 - .1μF ceramic
C_3 - .1μF ceramic
C_4 - 1-4.7μF Tant.
C_5 - .01μF ceramic 100V

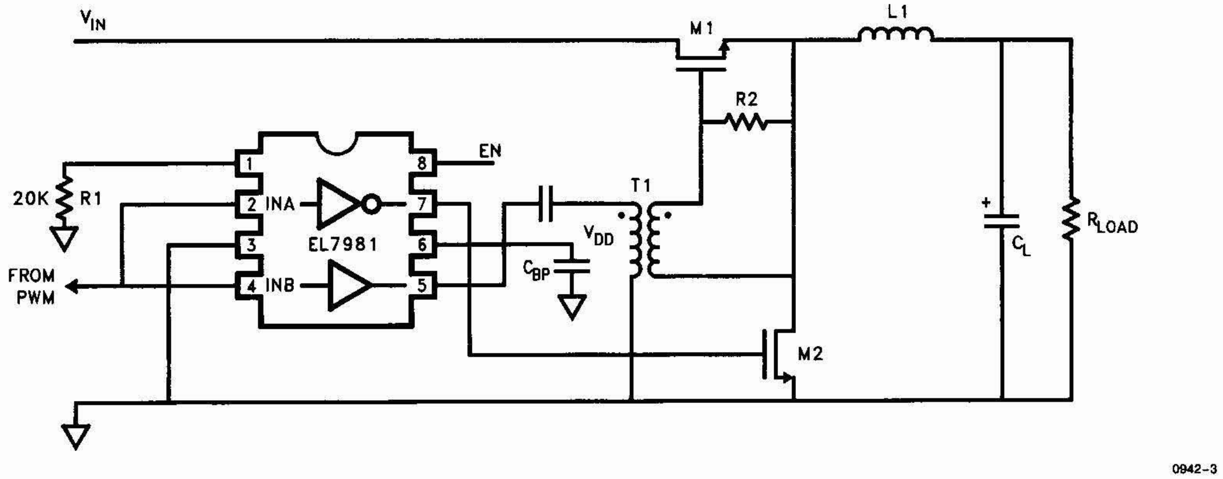
D_1, D_2 - IN4148
R_1 - 500KΩ 1/4w
R_2 - 10KΩ 1/4w
R_3 - 100Ω - 300Ω 1/4w

100V, Single chip, DC stable high side switch

0942-2

Synchronous Buck Regulator Driver

In this application one driver of the EL7981 is used to drive the main switch of a buck regulator while the other driver drives the synchronous switch. A transformer is used to obtain the high side switching voltage for M1. R1 sets the dead time delay between the on times of M1 and M2. The adjustable delay is perfect for devices with long turn off times such as IGBT's.



V_{IN}
M1
L1
R2
EN
T1
20K
R1
1
2 INA
3
4 INB
8
7
6
5
EL7981
V_{DD}
C_{BP}
FROM PWM
+
C_L
R_{LOAD}
M2
0942-3

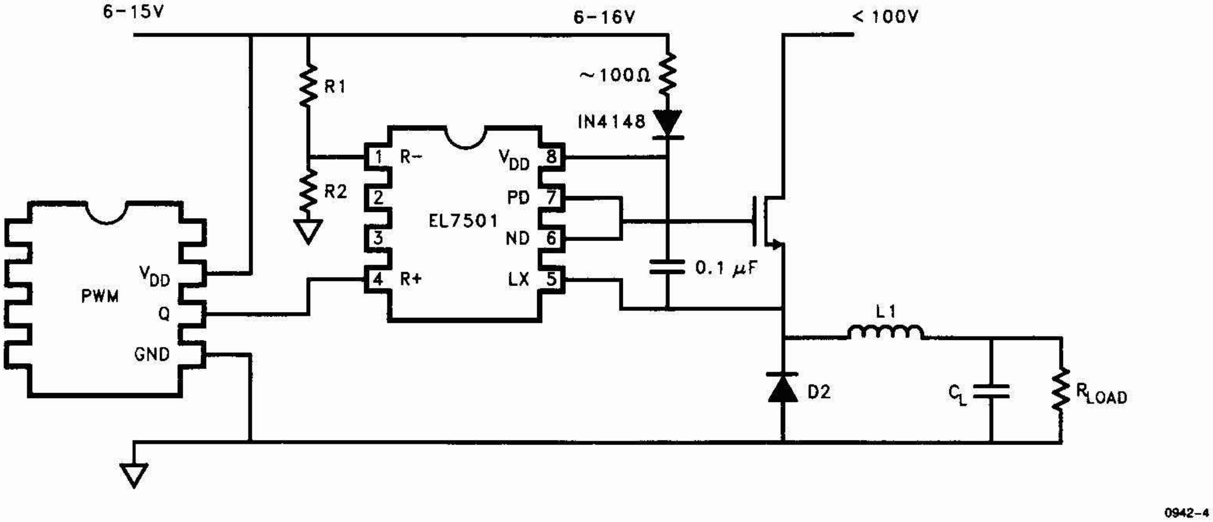
Set dead time with R1.
M1 and M2 can be IGBT's.

Synchronous Buck Regulator

Buck Regulator High Side Drive Using the EL7501

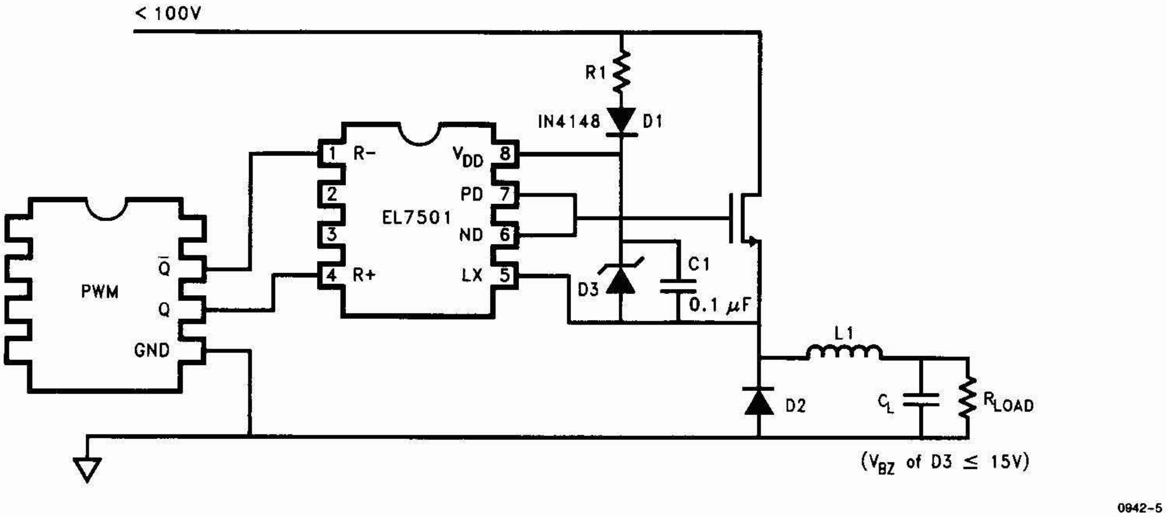
These circuits show two ways of using the EL7501 to drive the high side switch in a buck converter application. The first method uses resistors R1 and R2 to bias pin 1 in the middle of the drive voltage swing at pin 4. This allows the use of a single sided PWM drive. The high side voltage is pumped up from the V_{DD} supply.

The second method uses a complementary drive signal at pins 1 and 4 of the EL7501. It derives its high side supply voltage by charging capacitor C1 through resistor R1 and then using the external FET to pump that voltage above the high side supply.



6-15V
6-16V
< 100V
R1
R2
~100Ω
IN4148
1 R-
2
3
4 R+
EL7501
V_{DD} 8
PD 7
ND 6
LX 5
PWM
V_{DD}
Q
GND
0.1 µF
L1
D2
C_L
R_{LOAD}
0942-4

EL7501 Buck Regulator with High Side Drive
First Method

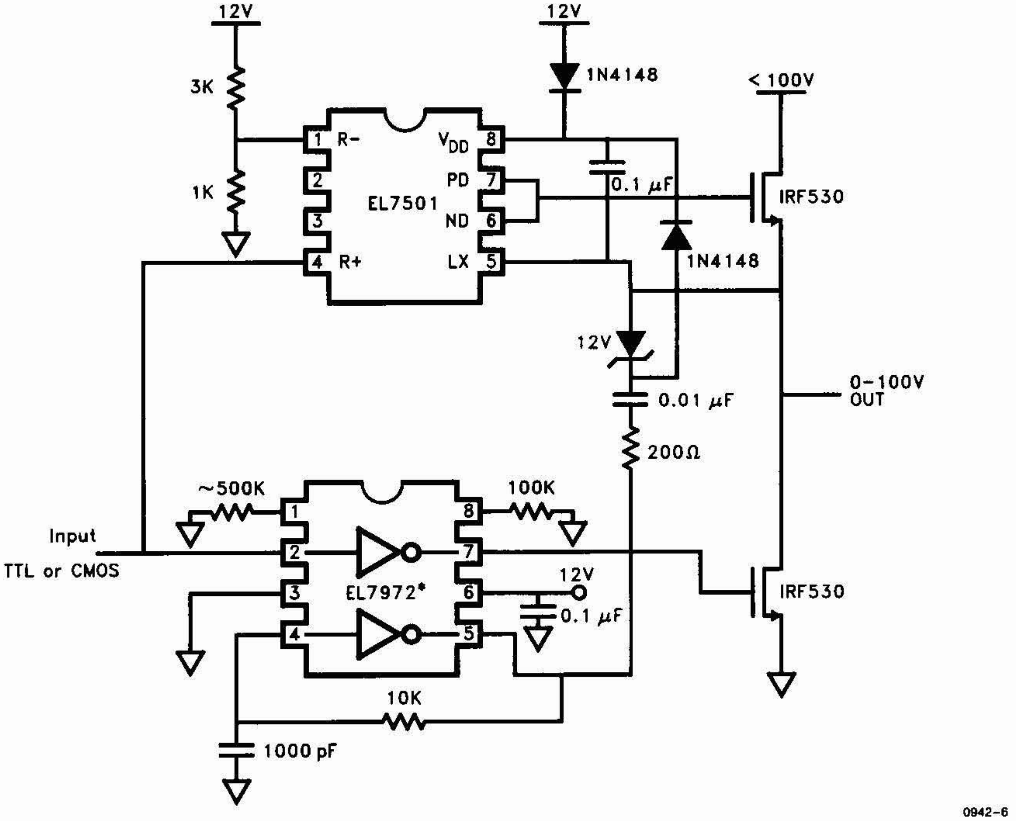


< 100V
R1
IN4148
D1
1 R-
2
3
4 R+
EL7501
V_{DD} 8
PD 7
ND 6
LX 5
PWM
$\bar{Q}$
Q
GND
D3
C1
0.1 µF
L1
D2
C_L
R_{LOAD}
(V_{BZ} of D3 ≤ 15V)
0942-5

EL7501 Buck Regulator with High Side Drive
(Alternate Biasing Scheme)
Second Method

Self Powered DC Stable 100V Half Bridge Driver

This circuit uses one driver of an EL7972 to provide low side drive and the other driver as a charge pump oscillator. The output of the charge pump oscillator drives a capacitor diode network to provide high side supply voltage to the EL7501. The EL7501 drives a high side external N-FET. Due to the addition of the charge pump this circuit will work at any driving frequency from DC to >1 MHz.

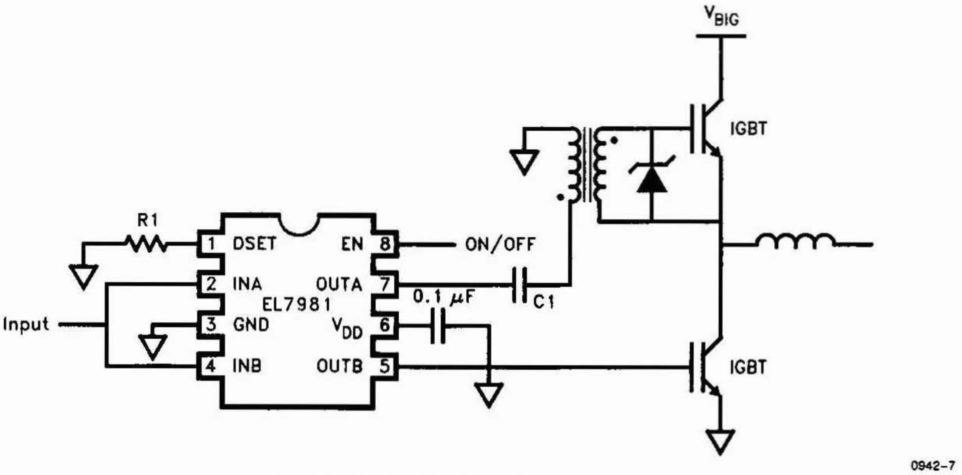

12V
3K
1K
12V
1N4148
< 100V
1 R-
2
3
4 R+
EL7501
VDD 8
PD 7
ND 6
LX 5
0.1 µF
IRF530
1N4148
12V
0.01 µF
200Ω
0-100V
OUT
~500K
100K
Input
TTL or CMOS
1
2
3
4
EL7972*
8
7
6
5
12V
0.1 µF
IRF530
10K
1000 pF
0942-6

An EL7961C can be substituted if an enable feature is desired.

DC Functional Half Bridge Driver

IGBT Half Bridge Driver

This circuit shows the EL7981 being used to drive an IGBT half bridge. The high side IGBT is transformer coupled to the driver. The value of R1 is chosen so that the two IGBT's never conduct at the same time. If the IGBT's have different turn off characteristics then the EL7982 could be used instead of the EL7981. The EL7982 has independent control of each of its driver's rising edge delay.

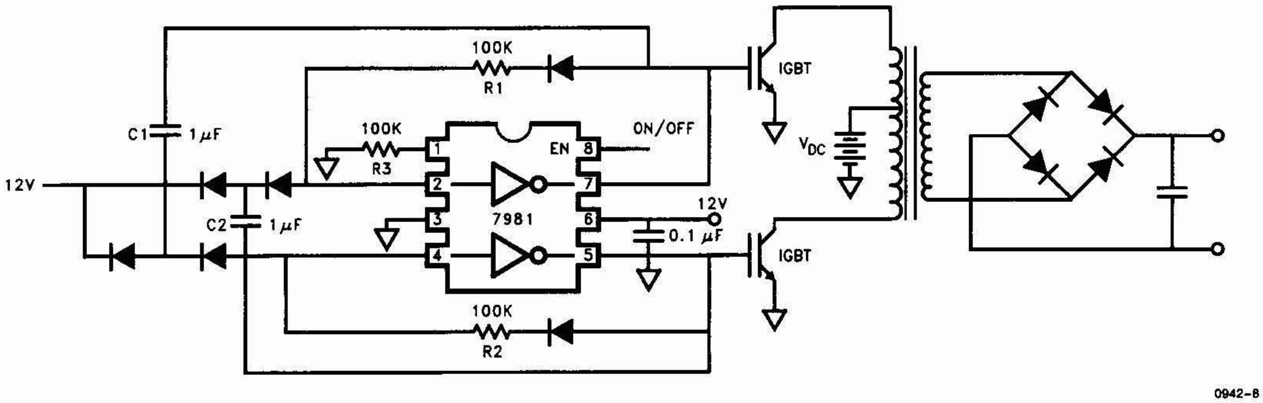


V_{BIG}
IGBT
R1
1 DSET
EN 8
ON/OFF
2 INA
OUTA 7
EL7981
0.1 μF
C1
Input
3 GND
V_{DD} 6
4 INB
OUTB 5
IGBT
0942-7

IGBT Half Bridge Driver

Self Oscillating IGBT Driver

This circuit self oscillates at approximately 25 KHz. The on times of each driver depend on the values of R1, C1, R2 and C2. In order to ensure equal on times accurate component values may need to be used. The resistor, R3, controls the dead time between the on times of both drivers.

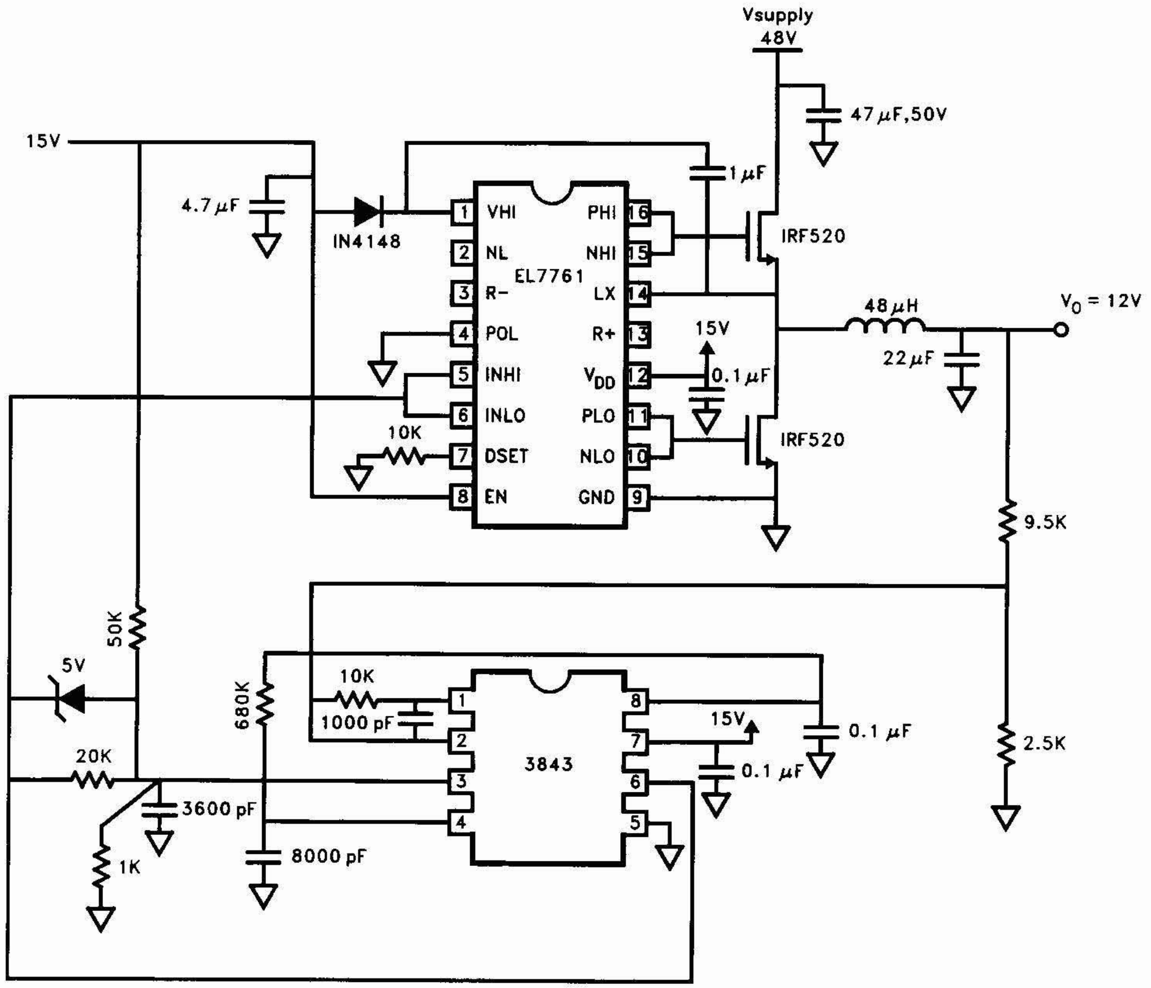

100K
R1
C1
1 µF
100K
R3
ON/OFF
EN
1
2
3
4
5
6
7
8
7981
12V
C2
1 µF
12V
0.1 µF
100K
R2
IGBT
IGBT
V_DC
0942-8

Diodes - 1N4148
R3 sets dead time
Approximately 25 KHz oscillation

Self Oscillating IGBT Driver, DC-DC Step Up (or Down)

40 Watt-12V Step Down Regulator Using a Synchronous Switch

This circuit shows how the EL7761 could be used as a half bridge driver for a step down converter. The circuit switches at 250 KHz.


Vsupply
48V
47 μF, 50V
15V
4.7 μF
IN4148
1 μF
IRF520
EL7761
1 VHI
2 NL
3 R-
4 POL
5 INHI
6 INLO
7 DSET
8 EN
PHI 16
NHI 15
LX 14
R+ 13
VDD 12
PLO 11
NLO 10
GND 9
10K
15V
0.1 μF
48 μH
V0 = 12V
22 μF
9.5K
2.5K
50K
5V
680K
10K
1000 pF
3843
15V
0.1 μF
0.1 μF
20K
3600 pF
1K
8000 pF
0942-9

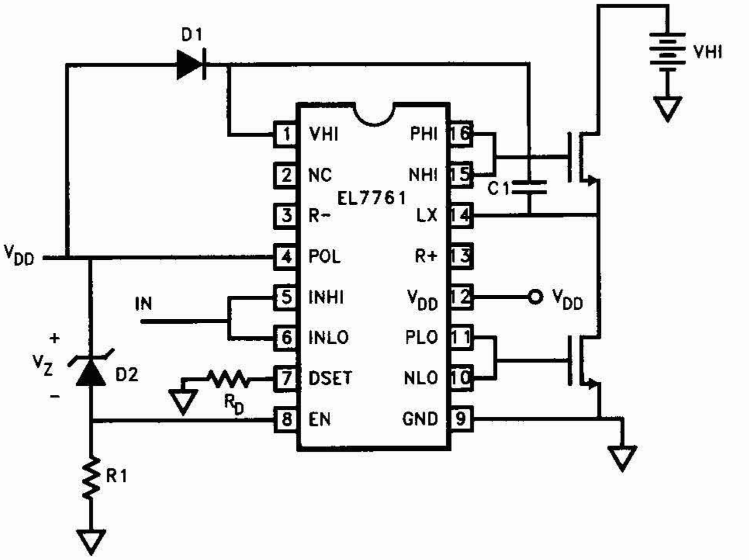
12V Step Down Synchronous Switches

Simple Undervoltage Lockout Circuit

By using a zener diode and a pull down resistor the user can implement a simple UVLO circuit. As V_{DD} increases above the zener voltage the EN pin rises above ground. When EN reaches V_{ton} the chip is enabled. As V_{DD} is lowered such that the voltage at EN falls below V_{toff}, the chip is disenabled. The threshold tolerances are as follows:

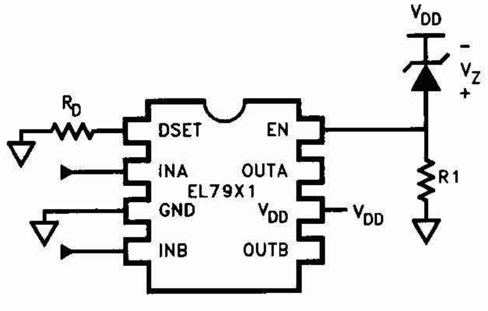
$$1.0V < V_{ton} < 1.6V$$

$$0.3V < V_{ton} - V_{toff} < 1.0V$$


D1
VHI
VDD
IN
+
VZ
-
D2
RD
R1
1 VHI
2 NC
3 R-
4 POL
5 INHI
6 INLO
7 DSET
8 EN
EL7761
PHI 16
NHI 15
LX 14
R+ 13
VDD 12
PLO 11
NLO 10
GND 9
C1
VDD
0942-10

$V_{turn\text{-}on} = V_Z + V_{ton}$
$V_{turn\text{-}off} = V_Z + V_{toff}$

Simple UVLO Circuit for the EL7761

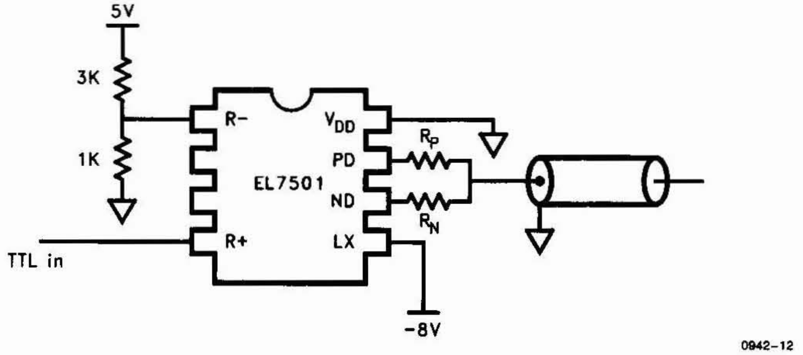

VDD
-
VZ
+
RD
DSET
INA
GND
INB
EL79X1
EN
OUTA
VDD
OUTB
VDD
R1
0942-11

$V_{turn\text{-}on} = V_Z + V_{ton}$
$V_{turn\text{-}off} = V_Z + V_{toff}$

Simple UVLO Circuit for the EL79X1

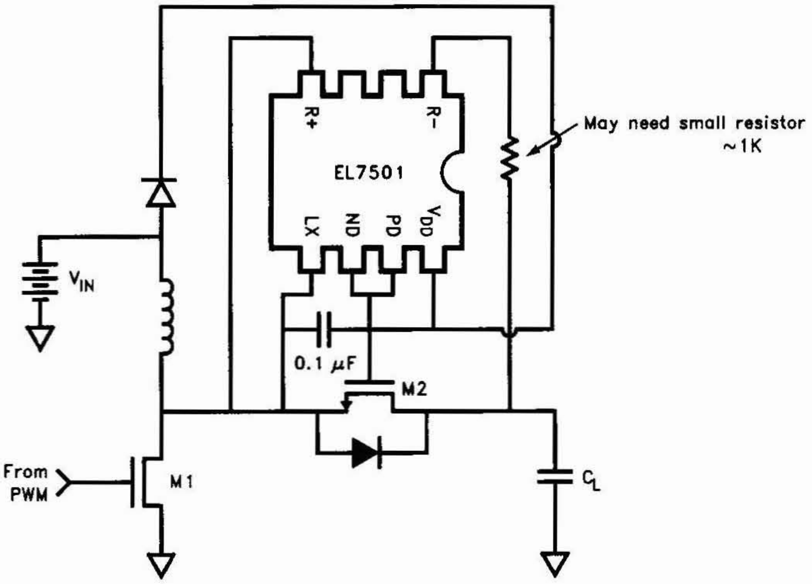
Video Sync Pulse Generator

The EL7501 inputs function outside the power supply rails, allowing a ground referenced TTL signal to control a ground to −8V output swing. The output resistors can be adjusted to tailor the rise and fall times of the circuit.


5V
3K
1K
TTL in
R−
R+
EL7501
V_{DD}
PD
ND
LX
R_P
R_N
−8V
0942–12

Synchronous Switch Increases Boost Efficiency

The EL7501 plus a N-FET replaces the catch diode in a boost regulator. When the R+ pin is higher than the R− pin, the FET is turned on, effectively shorting out the parasitic diode of the FET. A small resistor may be added in series with the R− pin in order to "tune" the turn-on delay of the FET.


R+
R−
EL7501
LX
ND
PD
V_{DD}
May need small resistor
~1K
V_{IN}
0.1 µF
M2
From
PWM
M1
C_L

0942-13

Resonant Gate Driver

Resonant gate driver can be used to boost the gate voltage swing while increasing driver efficiency. In Figure 1, an EL7501 is configured with (2) external "ring" diodes and resonating inductor L_R. For tutorial purposes, the power mosfet load was replaced by a 1000 pF capacitor (C_L). The "ring" diodes are fast switching diodes capable of withstanding the 1 amp peak current, such as the 1N914. Standard de-coupling techniques are applied with 5V applied to V_{DD}, the circuit delivers +10V to −5V output. In "5V only" systems, sufficient output swing is available so as to eliminate the need for costly "logic level" power FETs, and provides below ground swing for superior turn-off.

Principle of Operation

When the input drops below 2.4V, pin 7 pulls high, allowing current to flow from V_{DD} thru D1 and L_R, thus charging C_L. Initially the full voltage appears across the inductor, but as the current starts to flow, C_L begins to charge. When C_L reaches the supply voltage, current continues to flow as the inductor L_R reverses direction and continues to charge the capacitor beyond the supply voltage. When C_L reaches it's peak, the "ring" diode disconnects, holding that potential across C_L. The peak voltage can be controlled by adjusting the circuit "Q". Typically this is accomplished by varying the size of inductor L_R, since the "on" resistance of the driver can limit the circuit "Q". This is governed by the expression:

$$Q = \frac{\omega L}{R}$$

where: $\omega = \frac{1}{\sqrt{LC}}$ or $Q = \frac{1}{R}\sqrt{\frac{L}{C}}$

Thus, higher "Q", and higher voltage swing can be maintained by making $\sqrt{L/C}$ large compared to R. (R ≈ 5Ω typ. for the EL7501.)

Similarly, when pin-6 pulls low, the output resonates below ground to provide good turn-off. Since charge is transferred mostly thru the inductor, rather than a resistor efficiency is much higher. The circuit performance is summarized below.

	Conditions: V_{DD} = 5V F_C = 220 kHz			
	(L) Inductance	V_{OUT} (+)	V_{OUT} −	T_R/T_F
Case 1	1 µH	7V	−2.1V	60 ns
Case 2	47 µH	18V	−12V	300 ns

The power consumption was measured for Case 2, at 40 mW. Using "resistive" charging a power dissipation/consumption of 200 mW is anticipated, thus resulting in a (5) fold improvement in efficiency.

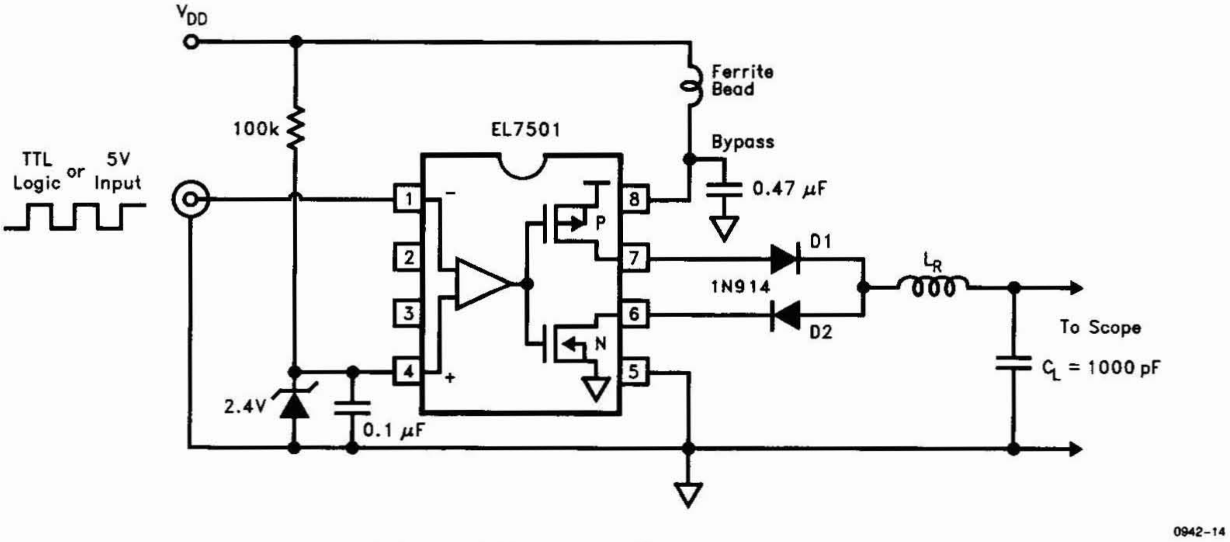
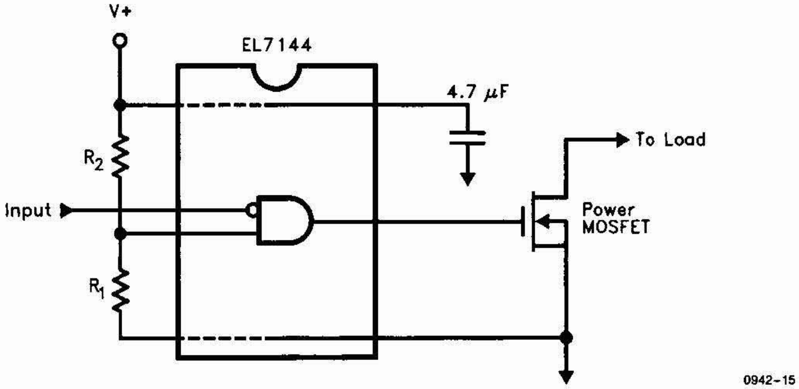


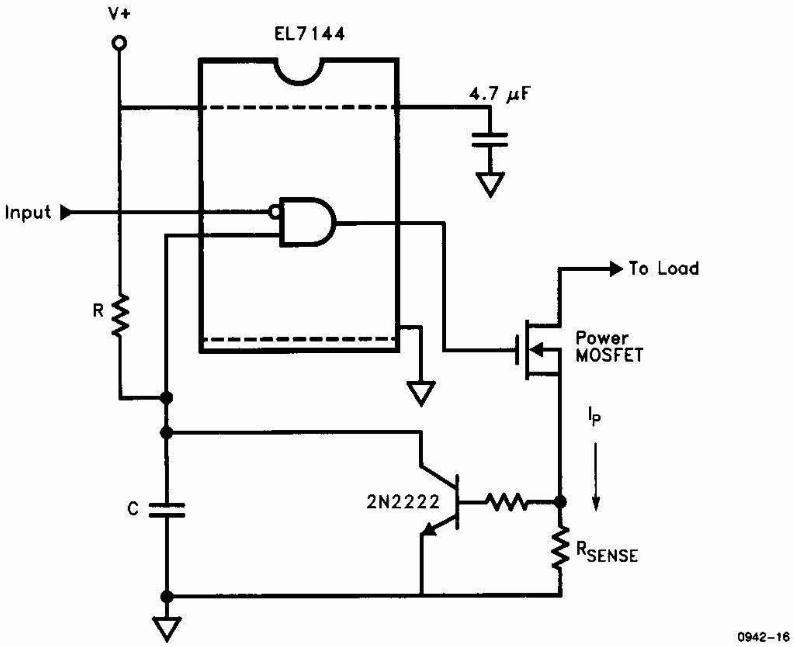
Figure 1. Resonant Gate Driver

MOS Driver with Under-Voltage Lock-Out


V+
EL7144
4.7 µF
To Load
R2
Input
Power MOSFET
R1
0942-15

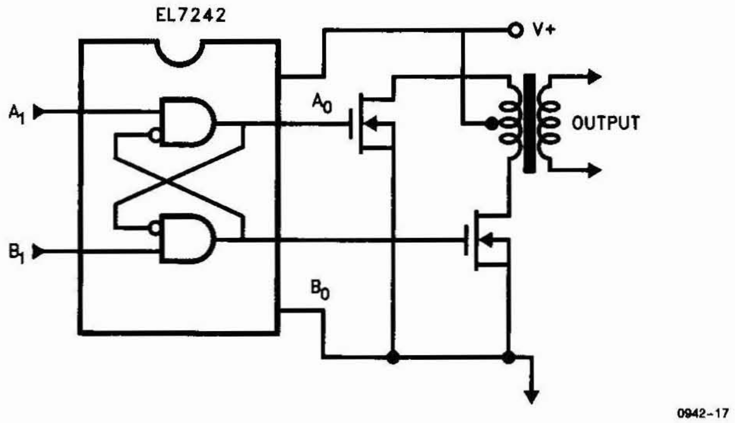
$$UV \approx (1.5)\frac{R_1 + R_2}{R_1}$$

Over-Current Protected Driver


V+
EL7144
4.7 µF
Input
To Load
R
Power MOSFET
I_P
2N2222
C
R_SENSE
0942-16

$$I_P \approx \frac{0.6}{R_{SENSE}} \qquad \text{Recovery Time } T_R \sim RC$$

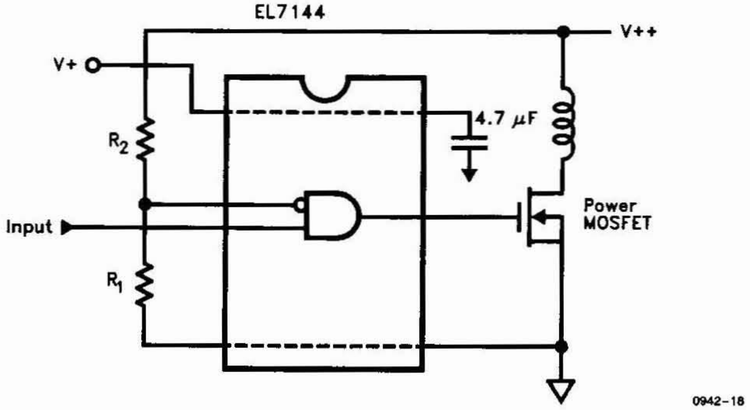
MOS Driver with Simultaneous Conduction Lock-Out


EL7242
V+
A1
A0
OUTPUT
B1
B0
0942-17

Truth Table

A_1	B_1	A_0	B_0
0	0	0	0
0	1	0	1
1	0	1	0
1	0	1/0	0/1

MOS Driver with Over-Voltage Protection


EL7144
V++
V+
R2
4.7 μF
Input
Power MOSFET
R1
0942-18

$$OV \approx (1.5)\frac{R_1 + R_2}{R_1}$$

Mosfet Driver Generates its own +12V supply

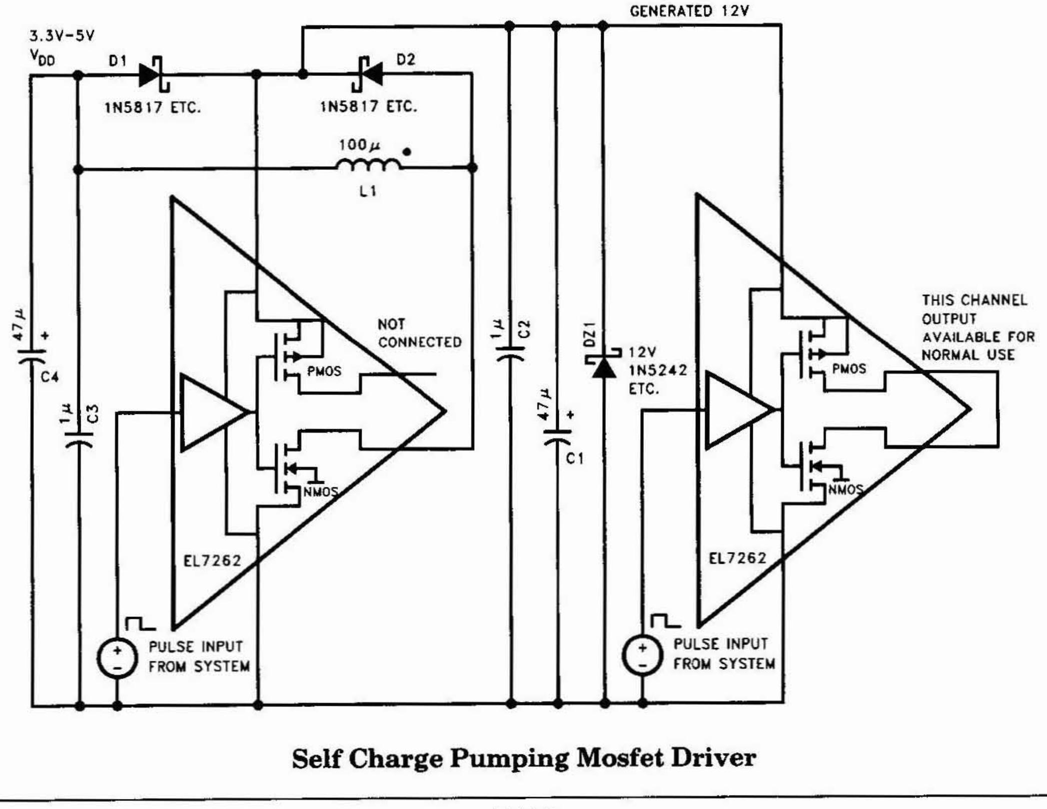
When you want to drive one power Mosfet, from a 5V or a 3.3V system, generating the one extra +12V supply can involve quite a large number of both active and passive components.

Here is a solution that uses the spare second Mosfet Driver channel to derive its own +12V supply. By using a driver with the drains brought out to separated pins, one can connect an inductor between the N-channel drain and the logic supply, without having the P-channel device connected.

In operation, it works as a standard flyback style switched mode circuit. When the output N-channel device is on, current starts flowing in the inductor, storing energy. When the N-channel device is turned off, the current has to continue flowing, so it flows through the diode D2 to charge up capacitors C1 and C2. As the cycle repeats, the voltage on C1 and C2 rises until the zener diode prevents further voltage rise. This is needed to prevent the drivers' derived supply from exceeding the parts' maximum voltage rating.

Since the objective was to minimize the number of external components and cost, additional components which would allow the circuit to self oscillate and regulate were omitted. The logic system was able to supply a drive pulse waveform to the supply generator. With the 5V system, I was using a 1.5 μs pulse every 9 μs. This gave a very solid +12.4V, and the system supply current went up by about 11 mA. The 3.3V system used a 300 kHz square wave, for a similar 12V derived supply, but with nearly 40 mA extra supply current. In both systems, when the Mosfet Driver was not being used, it could be "powered down" by simply stopping the pulses to the switching channel.

Any dual Mosfet Driver can be used, but if the drains of the output stage are not separated, there may be some protection and other parasitic devices that may prevent satisfactory operation. In these cases an external fet can be used to drive the inductor, provided a low threshold device is used. By altering the inductor value and the controlling pulses, enough power can be derived for further Mosfet Drivers or other peripheral devices requiring +12V.


GENERATED 12V
3.3V-5V
V_{DD}
D1
1N5817 ETC.
D2
1N5817 ETC.
100µ
L1
47µ
+
C4
1µ
C3
NOT CONNECTED
PMOS
NMOS
EL7262
PULSE INPUT FROM SYSTEM
1µ
C2
DZ1
12V
1N5242
ETC.
47µ
+
C1
PMOS
NMOS
EL7262
THIS CHANNEL OUTPUT AVAILABLE FOR NORMAL USE
PULSE INPUT FROM SYSTEM
0942-19

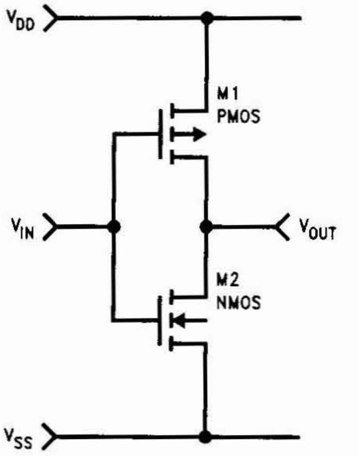
Self Charge Pumping Mosfet Driver

Super Inverters

CMOS is often equated with low power, however dynamic losses can be significant, particularly as the frequency of operation increases. Losses can be attributed to the parasitic capacitance on all internal nodes which toggle (described by $P = CV^2f$), and from simultaneous conduction through CMOS gates during switching. Parasitic capacitance is reduced by shrinking feature sizes and using low overlap, self aligned silicon-gate process technology. Simultaneous conduction (shoot-thru) can be controlled or eliminated completely with "super-inverter" technology. A standard CMOS inverter is shown in Figure 2A. Here, with every transition, there is an interval during which both the NMOS and PMOS transistors are conducting and dissipating energy. Thus the integral of the instantaneous shoot-thru current, multiplied by the supply voltage and clock frequency describes the power loss.

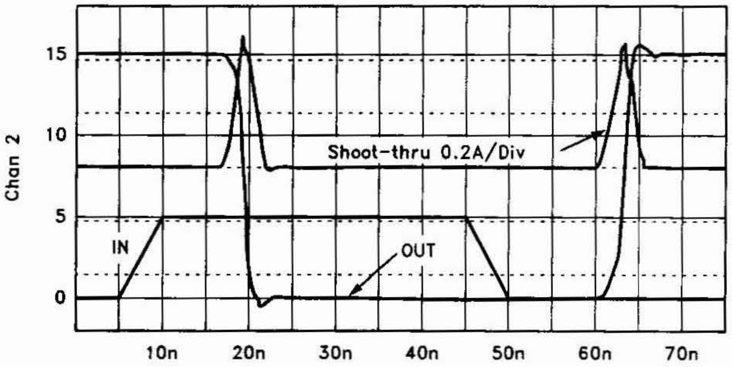
$$P = 2fV\int_{o}^{t} I_S\ (t)dt$$

These losses can be significant, and are illustrated in Figure 2B. The super-inverter shown in Figure 3A overcomes the "shoot-thru" problem with "break before make" asymmetric drive, thereby controlling or eliminating simultaneous conduction. The designer can trade-off shoot-thru current for added propagation delay. The results demonstrated in Figure 3B represent about a 4× improvement. An added benefit is the reduced power supply bounce resulting from di/dt and stray inductance.



0942-21

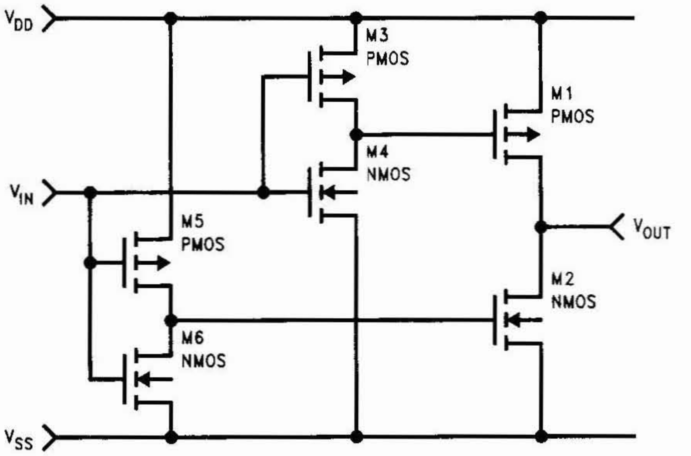
Figure 2A. Standard CMOS Inverter



0942-22

Figure 2B. CMOS Inverter Switching Losses

Super Inverters — Contd.



V_DD
V_IN
V_SS
M3
PMOS
M1
PMOS
M4
NMOS
V_OUT
M5
PMOS
M2
NMOS
M6
NMOS
0942-23

Figure 3A. Super Inverter

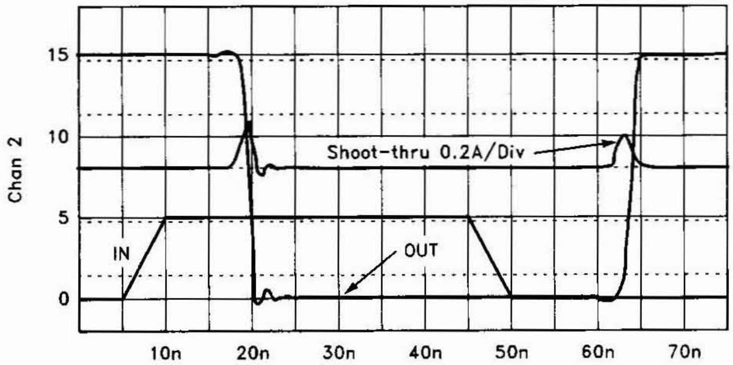
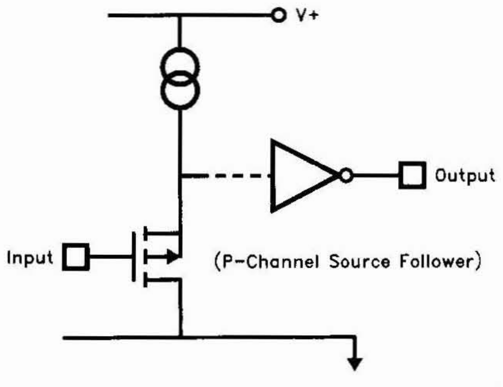


Figure 3B. Super Inverter Switching Losses

Input Source Follower

To accommodate moderately high source inpedances, a source follower input stage similar to the circuit shown in Figure 4 is used. This eliminates both the "Miller" gate capacitance, and gate to source capacitance seen in typical designs. The "boot-strapping" effect eliminates all but the gate-drain capacitance. This feature allows direct drive from low current logic, without any degradation in performance.



V+
Output
Input
(P-Channel Source Follower)
0942-25

Figure 4. Low Input Capacitance Source Follower

Precision Level Shifting

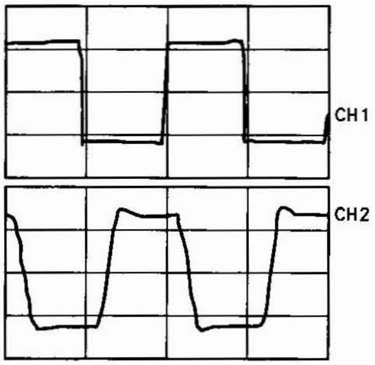
Generating rail to rail drive from a logic level input is accomplished with a Class AB push-pull amplifier and an internal 1.2V reference. This produces a well controlled threshold with minimal propagation delay. The known switch point can be used to generate under-voltage lock-out protection. Hysterisis is also introduced to boost the noise immunity.

3-State and Gated Inputs

Additional logic functions are also provided to insure greater flexibility. 3-State control is often useful in "Bridge" and "Bus" applications. Gated inputs can be used for chip enable/shut-down, latching, and various other functions.

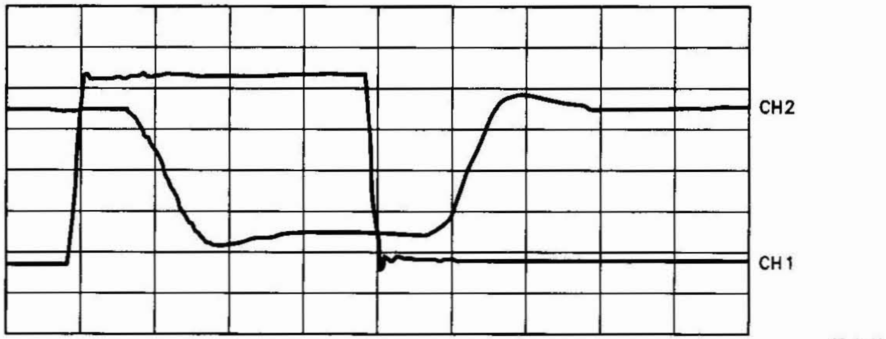
Overall Performance

The resulting CMOS Drivers offer both functionality and performance. Figure 5 shows the switching characteristics into a 1000 pF load. Rise time, fall time, and delay are all matched to minimize pulse distortion, and are less than 20 ns. Figure 6 illustrates the waveform integrity at 5 MHz, into 1000 pF.



Ch. 1 = 2.000V/div
Ch. 2 = 4.000V/div
Timebase = 100 ns/div

Figure 6. 5 MHz Output into 1000 pF Load



Ch. 1 = 1.000V/div
Ch. 2 = 5.000V/div
Timebase = 20.0 ns/div

Figure 5. Step Response into 1000 pF Load

Application Specific Data Processing Products

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Laser Diode Driver

Part #	Features	Tr	I_{OUT}	R_{OUT}	Supply	Package P = Pins M = SOL
		Typ	Max (Both Channels)	Typ (Both Channels)		
EL6251C	2-Channel + Sense	2 ns	320 mA	7.5Ω	5V ±10%	24P-M †

DC:DC Converters

Part #		Features	Ipeak	V_{OUT}	Accuracy	V_{SUPPLY}	Package
EL7556C	Int Ref	Integrated PWM + FETs IC	6A	Variable	1%	6V	28P-M †
EL7560C	Ext Ref	Integrated PWM + FETs IC	12.4A	2.1V–3.5V	1%	6V	28P-M †
EL7561C	Int Ref	Integrated PWM + FETs IC	12.4A	2.1V–3.5V	1%	6V	28P-M †
EL7571C	Int Ref	PWM Controller IC	Variable	1.3V–3.5V	1%	4.5V–13.2V	20P-M †

† See Ordering Information section in this databook.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL6251C

Laser Diode Power Amp W/Sense Amp

Features

- High-performance laser diode driver and power monitor
- Voltage-controlled read and write currents up to 320 mA total (160 mA read/160 mA write)
- 1.7 ns rise time
- 3.2 ns fall time
- Single +5V supply
- Power supply fault sensing for laser diode protection
- Laser diode power sense amplifier with two transimpedance levels compatible with read and write modes
- Uses external set resistors for both read and write transconductance

Applications

- Writeable optical drives

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL6251CM	−40°C to +85°C	24 Pin SOL	MDP0027

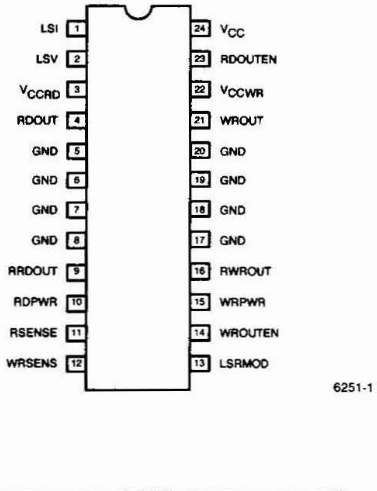
General Description

The EL6251C is a Laser Power Amplifier which provides pulsed write/erase current as well as DC or pulsed read current to a common-cathode laser diode connected to output pins WROUT and RDOUT respectively. Separate pins are provided so that the read output may be inductively isolated from the write output and the laser diode. The levels of these currents are individually set by analog input voltages applied to the WRPWR and RDPWR pins respectively. Write output current pulses are achieved by a TTL "L" signal at the $\overline{\text{WROUTEN}}$ pin. Similarly, Read output pulses are achieved (if a simple DC level is not desired) by a TTL "L" signal at the $\overline{\text{RDOUTEN}}$ pin. Power-down of both the RDOUT and WROUT pins is also accomplished by applying a TTL "L" signal to the LSRMOD pin. Protection at low power supplies is also provided, with the RDOUT and WROUT outputs turning off when the supply voltage falls below about 4V. Laser Diode Protection is additionally provided since, when open, the LSRMOD floats low, and $\overline{\text{RDOUTEN}}$ and $\overline{\text{WROUTEN}}$ float high, thereby disabling any output current.

The EL6251C also contains all the necessary sense circuitry to produce an output voltage at the LSV pin proportional to the input current at the LSI pin, which is from a laser power-monitor photodiode. Two values of sense circuitry are available, selected by a TTL input on the WRSENS pin (floats high when open).

Three external resistors at pins RSENSE, RRDOUT, and RWROUT are used to accurately set the transimpedance of the sense amplifier, and the read and write transconductance. The output current at RDOUT and WROUT varies inversely with resistor value, while the transimpedance of the sense amplifier varies directly with the value of RSENSE.

Connection Diagram



Absolute Maximum Ratings (T_A = 25°C)

Voltages Applied to:	
V_{CC}, VCCRD, VCCWR	−0.5V to 6.0V
TTL Inputs	−0.5V to V_{CC} + 0.5V
WRPWR and RDPWR	−0.5V to V_{CC} + 0.5V
LSI	−0.5V to 2.5V
WROUT and RDOUT	−0.5V to V_{CC} + 0.5V
LSV	−0.5V to V_{CC} + 0.5V

Power Dissipation (maximum)	See Curves
Operating Temperature Range	−40°C to +85°C
Operating Junction Temperature	+150°C
Storage Temperature Range	−65°C to 150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics

V_{CC} = 5V, RRDOUT = 10 kΩ, RWROUT = 6.2 kΩ, RDOUT and WROUT load = 10Ω to GND, RSENSE = 10 kΩ, T_A = 25°C unless otherwise specified

General

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{CCF}	V_{CC} Fault Voltage	(Note 1)	3.3	3.8	4.1	I	V
I_{S1}	Supply Current	WRPWR = RDPWR = 2.88V, LSRMOD=H		237	270	I	mA
I_{S2}	Supply Current	WRPWR = RDPWR = 0V, LSRMOD=H or L	35	46	58	I	mA

Logic Control Signals (LSRMOD, WRSENS, $\overline{\text{RDOUTEN}}$, $\overline{\text{WROUTEN}}$)

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{IL}	Input Low Voltage				0.8	I	V
V_{IH}	Input High Voltage		2.0			I	V
I_{IL}	Input Low Current	V_{IN} = 0V	−250			I	μA
I_{IH1}	Input High Current 1	V_{IN} = 2.00V (all inputs)	−50	0		I	μA
I_{IH2}	Input High Current 2	V_{IN} = 5.00V (excluding LSRMOD)		0	10	I	μA
I_{IH3}	Input High Current 3	V_{IN} = 5.00V (LSRMOD only)		400	500	I	uA

Note 1: When V_{CC} < VCC_F, WROUT and RDOUT are disabled while the Laser Sense Amplifier circuitry remains active.

V To I Stages

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OFFSET}	V to I Offset Voltage	RDPWR - RRDOUT, WRPWR - WROUT, RDPWR = WRPWR = 2.88V	−11	−1	10	I	mV
GS1	Gain Scale 1	RRDOUT = 3.6 kΩ (Note 2)	97	100	103	I	%
GS2	Gain Scale 2	RWROUT = 3.6 kΩ (Note 3)	97	100	103	I	%

Electrical Characteristics — Contd.

V_{CC} = 5V, RRDOUT = 10 kΩ, RWROUT = 6.2 kΩ, RDOUT and WROUT load = 10Ω to GND, RSENSE = 10 kΩ, T_A = 25°C unless otherwise specified

Laser Sense Amplifier Input (LSI Pin)

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{LSI}	Voltage at LSI Pin	WRSENS = 0.8V, I_{LSI} = 100 μA (Note 4)	1.4	1.5	1.6	I	V
I_{LSI1}	Input Current Range 1	WRSENS = 2.0V	0		1600	I	μA
I_{LSI2}	Input Current Range 2	WRSENS = 0.8V	0		200	I	μA
C_{LSI}	Input Capacitance			2		V	pF

Laser Sense Amplifier

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{MAX}	Max. Output Voltage	R_{LOAD} = 2 kΩ to GND, LSI = 1.6 mA, WRSENS = 2V	3.70	3.86		I	V
V_{MIN}	Min. Output Voltage	R_{LOAD} = 2 kΩ to GND, LSI = 1 μA, WRSENS = 2V	25	75	110	I	mV
TCV_{MIN}	Min. Output V Drift	R_{LOAD} = 2 kΩ to GND, T_{MIN} to T_{MAX}	−300		300	IV	μV/°C
V_{LIN}	Output Linearity	Best Fit Method, Measured at LSI = 10%, 50%, 90% of ILSI1, ILSI2.	−2	0.1	+2	I	%
Z_{OUT}	Output Impedance	I_{LOAD} = ±1 mA		0.5		V	Ω
I_{OUT}	Current Drive	V_{OUT} from V_{MIN} to V_{MAX}	−1		+2	I	mA
e_{OUT}	Output Noise Voltage	BW = 3.5 MHz		0.7		V	mV RMS
SR	Slew Rate	R_{LOAD} = 2 kΩ to GND	10	15		IV	V/μs
R_{M1}	Transimpedance 1	WRSENS = 2.0V, Note 5, Note 6	2.393	2.467	2.541	I	kΩ
V_{OO1}	Output Offset Voltage 1	WRSENS = 2.0V, Note 5	−100	-54	10	I	mV
R_{M2}	Transimpedance 2	WRSENS = 0.8V, Note 5, Note 6	18.93	19.52	20.11	I	kΩ
V_{OO2}	Output Offset Voltage 2	WRSENS = 0.8V, Note 5	−25	+3	+25	I	mV
TCR_M	Transimpedance Drift		0	65	150	V	ppm/°C
BW	Bandwidth	−3 dB Bandwidth	3	8		V	MHz
PKNG	Peaking			0	3	V	dB
T_{RCVRY}	Recovery Time	WRSENS L to H or H to L, Output Settling to ±20 mV, LSI = 100 μA		100	300	V	ns

Note 2: Output current ($IOUT_{GS1}$) is measured with RRDOUT = 3.6 kΩ, RDPWR = 1.200V. This value is compared to the output current ($IOUT_{NOM}$) with RRDOUT = 10 kΩ, RDPWR = 3.333V. GS1 = ($IOUT_{NOM}$/$IOUT_{GS1}$)

Note 3: Output current ($IOUT_{GS2}$) is measured with RWROUT = 3.6 kΩ, WRPWR = 1.200V. This value is compared to the output current ($IOUT_{NOM}$) with RWROUT = 6.2 kΩ, RDPWR = 2.067V. GS2 = ($IOUT_{NOM}$/$IOUT_{GS2}$)

Note 4: $V_{LSI} = (2 * Vbe) + (I_{LSI} * 200\ \Omega)$.

Note 5: The transfer function for the Laser Sense Amplifier is as follows:
WRSENS = 2.0 V: $V_{LSI} = (I_{LSI} * R_{M1}) + V_{OO1}$
WRSENS = 0.8 V: $V_{LSI} = (I_{LSI} * R_{M2}) + V_{OO2}$

Note 6: $R_{M1} \approx 0.247 * \text{RSENSE}$
$R_{M2} \approx 1.952 * \text{RSENSE}$

Electrical Characteristics — Contd.

V_{CC} = 5V, RRDOUT = 10 kΩ, RWROUT = 6.2 kΩ, RDOUT and WROUT load = 10Ω to GND, RSENSE = 10 kΩ, T_A = 25°C unless otherwise specified

Laser Current Amplifier Inputs (RDPWR and WRPWR Pins)

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
R_{IN}	Input Resistance	RDPWR and WRPWR. Meas. at 0.576V, 2.88V	18	24		I	kΩ
I_{IB}	Input Bias Current	V_{IN} = 2.88V		115	200	I	μA
C_{IN}	Input Capacitance			1		V	pF
BW	−3 dB Bandwidth	V_{IN} = 2.88V	40	70		V	MHz

Laser Current Amplifier Outputs DC Performance (RDOUT and WROUT pins)

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
I_{RDOUT1}	RDOUT Output I 1	RDPWR = 2.88V	−61	−67	−74	I	mA
I_{RDOUT2}	RDOUT Output I 2	RDPWR = 0.576V	−13	−16	−19	I	mA
I_{WROUT1}	WROUT Output I 1	WRPWR = 2.88V	−89	−98	−107	I	mA
I_{WROUT2}	WROUT Output I 2	WRPWR = 0.576V	−17	−21	−25	I	mA
GM_{RD}	RD Transconductance	Rload = 10Ω Note 7, Note 8, Note 9	0.0208	0.0224	0.0240	I	1/Ω
RDGAIN	Read Current Gain	RDGAIN = GMRD*RRDOUT	208	224	240	I	mA/mA
IOO_{RD}	RD Out. Offset Current	Note 7	−7	−3.4	+0	I	mA
GM_{WR}	WR Transconductance	Rload = 10Ω Note 7, Note 8, Note 9	0.0310	0.0334	0.0358	I	1/Ω
WRGAIN	Write Current Gain	WRGAIN = GMWR*RWROUT	192	207	222	I	mA/mA
IOO_{WR}	WR Out. Offset Current	Note 7	−6	−2.0	+1	I	mA
TCIout1	Output Current Drift	RDOUT and WROUT, Iout = 32 mA	100	500	800	IV	ppm/°C
TCIout2	Output Current Drift	RDOUT and WROUT, Iout = 160 mA	200	900	1250	IV	ppm/°C
I_{LIN}	Output Curr. Linearity	RDPWR = WRPWR = 0.576V to 2.88V, Best Fit Method. Note 7.	−3		3	I	%
I_{OFF1}	Output Off Current 1	WRPWR and RDPWR open.	−1.5	−0.6	0	I	mA
I_{OFF2}	Output Off Current 2	WRPWR = RDPWR = 2.88V, WROUTEN = RDOUTEN = 2V.	−1.5	−0.4	0	I	mA
R_{OUT}	Output Impedance	Iout = 50 mA		750		V	Ω
C_{OUT}	Output Capacitance	Iout = 50 mA		40		V	pF

Note 7: The transfer function for each Laser Current Amplifier is calculated using a best-fit method at 3 points. The input voltages applied to WRPWR and RDPWR for the 3 points are 0.576V, 1.728V, and 2.88V. The transfer functions for I_{RDOUT} and I_{WROUT} are defined as follows:

$-I_{RDOUT} = (V_{RDPWR} * GM_{RD}) + IOO_{RD}$

$-I_{WROUT} = (V_{WRPWR} * GM_{WR}) + IOO_{WR}$

Note 8: $GM_{RD} \approx 224/RRDOUT$ (Nominally)

$GM_{WR} \approx 207/RWROUT$ (Nominally)

Note 9: Datasheet values are based on tester data which implies part is not warmed up, so Tj is similar to Ta.

For precise values, see curves or use the temperature coefficient data.

Laser Current Amplifier Outputs AC Performance

(RDOUT and WROUT pins) V_{CC} = +5V, RWROUT=RRDOUT=3.6 kΩ, RSENSE=10 kΩ, T_A=25°C unless otherwise specified.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
t_r	Output Curr. Rise Time	WRPWR = RDPWR = 2.88V (10%–90%)	1.0	1.7	3.0	IV	ns
t_f	Output Curr. Fall Time	WRPWR = RDPWR = 2.88V (10%–90%)	2.2	3.2	4.2	IV	ns
OS	Output Curr. Overshoot	WRPWR = RDPWR = 2.88V		8	20	IV	%
t_{PD2A}	$\overline{\text{WROUTEN}}$ L-H Prop. Delay A	From $\overline{\text{WROUTEN}}$ 50% L-H to WROUT at 50% of Initial Value. I(WROUT) = 150mA		2.9	6.0	IV	ns
t_{PD2B}	$\overline{\text{WROUTEN}}$ L-H Prop. Delay B	From $\overline{\text{WROUTEN}}$ 50% L-H to WROUT at 50% of Initial Value. I(WROUT) = 30mA		3.6	7.0	IV	ns
t_{PD3A}	$\overline{\text{WROUTEN}}$ H-L Prop. Delay A	From $\overline{\text{WROUTEN}}$ 50% H-L to WROUT at 50% of Final Value. I(WROUT) = 150mA		3.2	6.0	IV	ns
t_{PD3B}	$\overline{\text{WROUTEN}}$ H-L Prop. Delay B	From $\overline{\text{WROUTEN}}$ 50% H-L to WROUT at 50% of Final Value. I(WROUT) = 30mA		3.3	7.0	IV	ns

Pin Descriptions

Name	Pin Number	Type	Description
GND	5–8, 17–20	Power Supply	Ground
LSRMOD	13	TTL Input	RDOUT and WROUT Output Current Enable. Outputs enabled when "H".
VCC_{RD}	3	Power Supply	+5V
VCC_{WR}	22	Power Supply	+5V
V_{CC}	24	Power Supply	+5V
LSV	2	Analog Output	Laser Sense Voltage. See Notes 5,6 for formula.
LSI	1	Analog Input	Laser Sense Current
WRSENS	12	TTL Input	I-to-V Sensitivity Selection. 0.25 * RSENSE when "H", 2 * RSENSE when "L"
RSENSE	11	R Connection	Sense Amplifier Gain Control Resistor. Nominally 10 kΩ to ground.
RDPWR	10	Analog Input	Voltage Input to Control RDOUT Current
RDOUT	4	Analog Output	Read Output Current. See Notes 7, 8 for formula.
$\overline{\text{RDOUTEN}}$	23	TTL Input	RDOUT Enable. RDOUT is enabled when "L" and LSRMOD is "H".
RRDOUT	9	R Connection	Read transconductance resistor. Nominally 3.6 kΩ to ground.

Laser Driver (Write Channel)

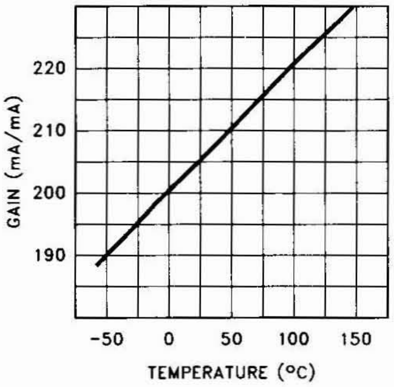
WRPWR	15	Analog Input	Voltage Input to Control WROUT Current
WROUT	21	Analog Output	Write Output Current. See Notes 7, 8 for formula.
WROUTEN	14	TTL Input	WROUT Enable. WROUT is enabled when "L" and LSRMOD is "H".
RWROUT	16	R Connection	Write transconductance resistor. Nominally 3.6 kΩ to ground.

Control Truth Table

LSRMOD	$\overline{\text{WROUTEN}}$	$\overline{\text{RDOUTEN}}$	Function Description
1	0	0	Ir = ON, Iw = ON
1	0	1	Ir = OFF, Iw = ON
1	1	0	Ir = ON, Iw = OFF
1	1	1	Iw = Ir = 0
0	0	0	Iw = Ir = 0
0	0	1	Iw = Ir = 0
0	1	0	Iw = Ir = 0
0	1	1	Iw = Ir = 0

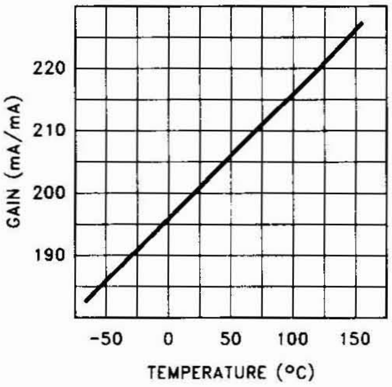
Typical Performance Curves

Read Current Gain vs Temperature (VRDPWR = 2.88V, RRDOUT = 3.6 kΩ)



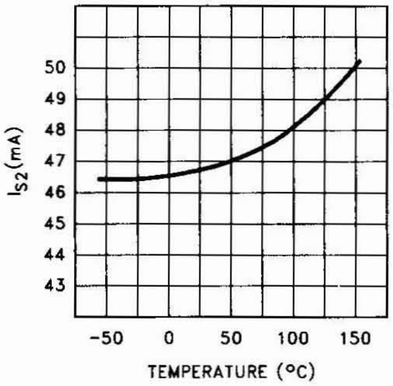
6251-2

Write Current Gain vs Temperature (VWRPWR = 2.88V, RWROUT = 3.6 kΩ)



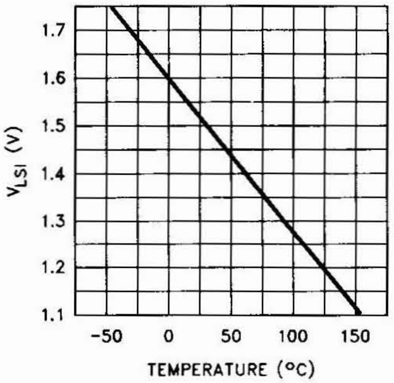
6251-3

IS2 vs Temperature



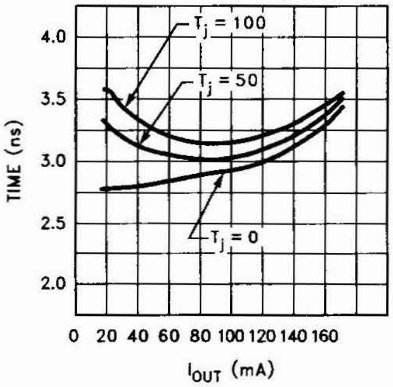
6251-4

VLSI vs Die Temperature (I_{LSI} through 20 kΩ to 5.0V)



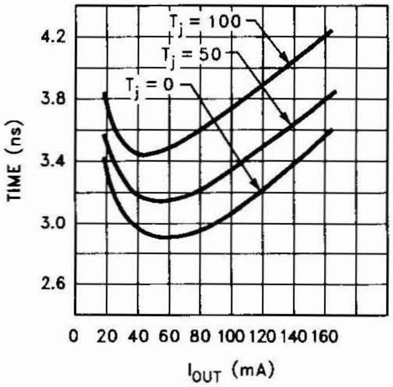
6251-5

Turn-On Delay vs I_{OUT}



6251-6

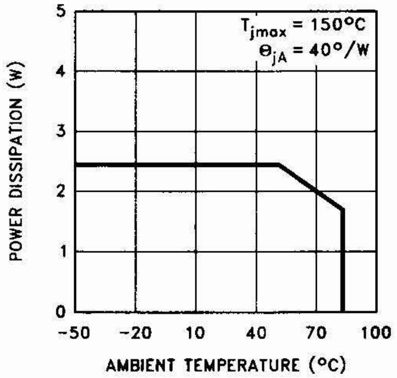
Turn-Off Delay vs I_{OUT}



6251-7

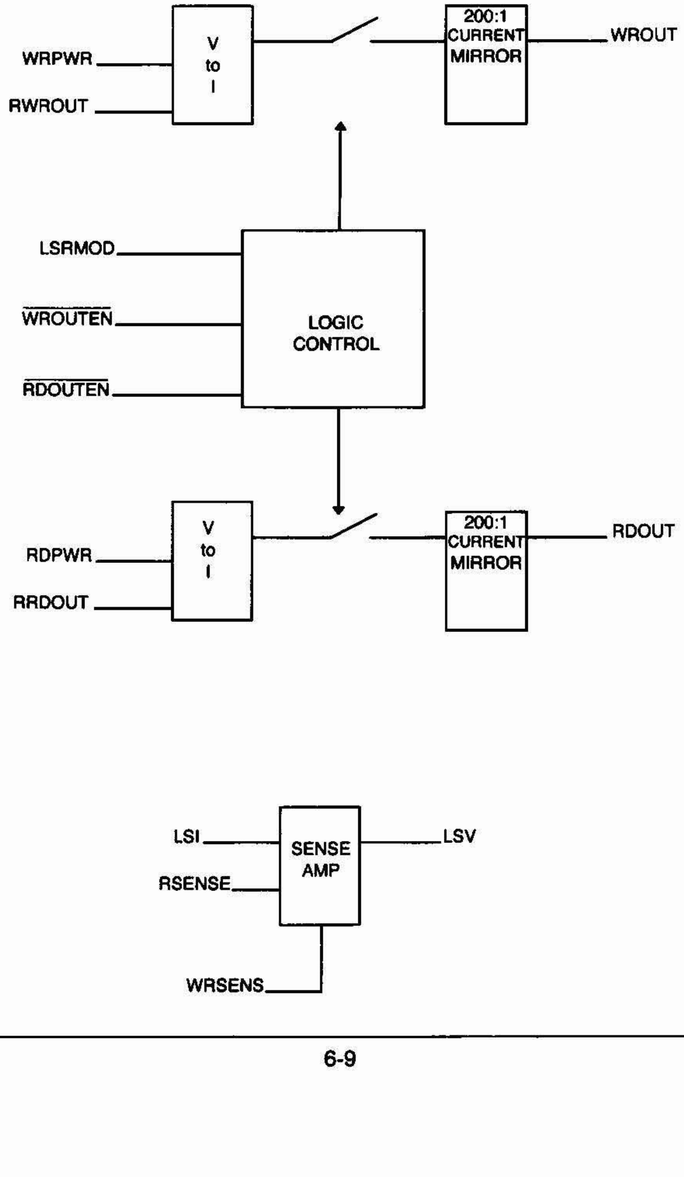
Typical Performance Curves — Contd.

24-Pin Plastic Fuselead Maximum Power Dissipation vs Ambient Temperature



6251-8

EL6251 Block Diagram

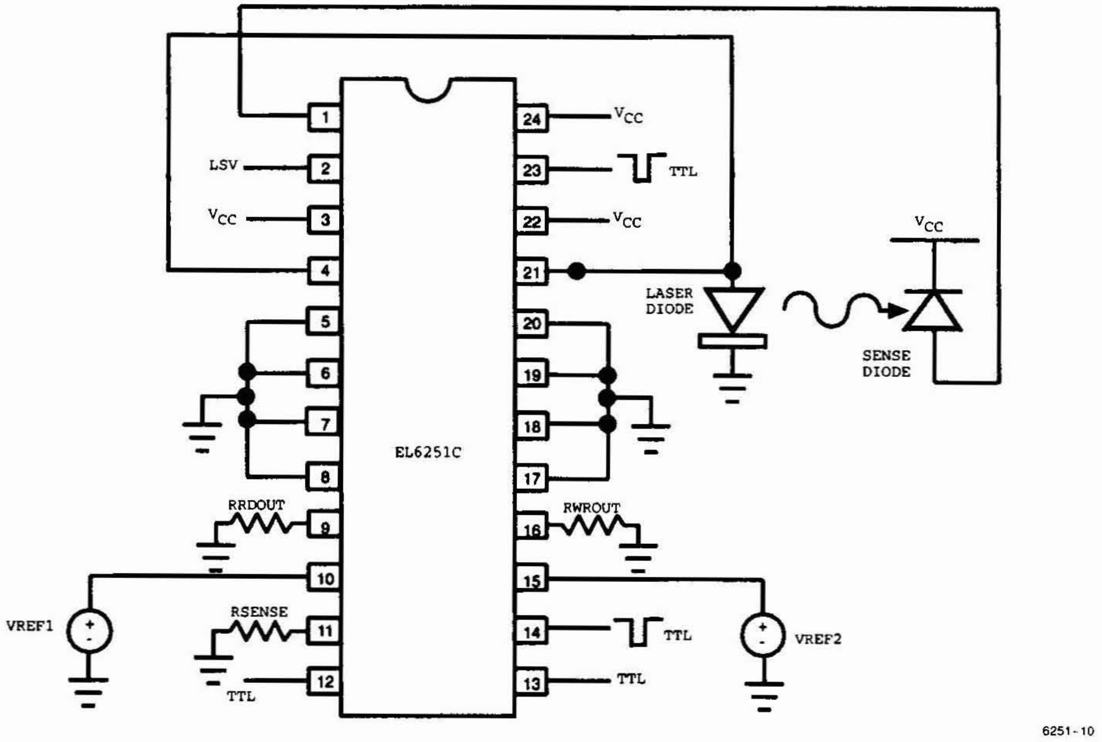

WRPWR
RWROUT
V to I
200:1 CURRENT MIRROR
WROUT
LSRMOD
$\overline{\text{WROUTEN}}$
$\overline{\text{RDOUTEN}}$
LOGIC CONTROL
RDPWR
RRDOUT
V to I
200:1 CURRENT MIRROR
RDOUT
LSI
RSENSE
SENSE AMP
LSV
WRSENS

6251-9

Recommended Operating Conditions

V_{CC} Supply Voltage	5.0V ±10%
RRDOUT Resistor	1.8 kΩ to 10 kΩ
RWROUT Resistor	1.8 kΩ to 10 kΩ
RSENSE Resistor	5.0 kΩ to 20.0 kΩ
Write Current	0 to 160 mA
Read Current	0 to 160 mA
WROUT Applied Voltage	0V to V_{CC} − 0.3−(15*Iwrite)
RDOUT Applied Voltage	0V to V_{CC} − 0.3−(15*Iread)
RDPWR and WRPWR Input Range	0V to V_{CC} − 1.5V

Typical Circuit Configuration


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
LSV
VCC
VCC
VCC
VCC
TTL
TTL
TTL
TTL
EL6251C
LASER DIODE
SENSE DIODE
RRDOUT
RWROUT
RSENSE
VREF1
VREF2
6251-10

Application Notes:

NOTES:

Due to the high values of current being switched rapidly on and off, it is important to ensure that the power supplies are well decoupled to ground. To this end, the EL6251C has three V_{CC} pins, all of which should be connected, and users should ensure that supply inductance to these pins is minimized. Symptoms that could arise include poor rise/fall times, current ringing during switching, current overshoot, and poor settling response.

Oscillation can also occur due to capacitance on pins RRDOUT and RWROUT. It is important to minimize any stray capacitance on these pins and use the suggested resistors to ground, otherwise current ringing when switching (or even sustained oscillation) may occur.

It is also important to minimize the lead inductance between the WROUT pin and the laserdiode. If the read current is also to be switched, then the same caution applies as well. Too much inductance in series with WROUT will produce an underdamped ringing response on both the rising and falling edges of the current pulse. The ringing can sometimes be reduced with a parallel RC snubber right at the device output, but lack of headroom prevents the use of a series resistor on WROUT as an alternative..

Thermal Considerations:

The total device power consumption is highly dependant on the amount of current flowing through the laserdiode, and may further be altered by any duty cycle effects. Despite this, the equation below is fairly accurate:

$$PD = ((Is2 + (1.1 \times Idiode)) \times V_{CC}) - (Idiode \times Vdiode)$$

where Is2 = Supply current when LSRMOD = 0 (46 mA typical)
Idiode = Total current through the laserdiode (Iread + Iwrite)
Vdiode = The voltage dropped across the laserdiode
V_{CC} = The EL6251C supply voltage

The die temperature will rise 40°C/W on a typical board where the EL6251C is soldered to a substantial groundplane, due to the 4 ground pins on either side of the device being attached to the mounting pad. Alternatively, the LSI pin acts as a good thermometer, by which the on-chip temperature may be monitored directly if so desired.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7556C

Adjustable CPU Power Supply Unit-6A

Features

- Precision internal 1% reference
- 3.3V @ 6 amps continuous
- Internal FETs
- >90% Efficiency
- Synchronous switching
- User adjustable slope compensation
- Internal soft start
- Over temperature indicator
- Low current sleep mode
- Low parts count
- Pulse by pulse current limiting
- High efficiency at light load
- Operates up to 1 MHz
- 1% Output accuracy
- Sync function
- Power good signal
- Power-saver mode
- Intel P54 and P55 compatible
- VCC2DET Interface

Applications

- PC Motherboards
- Local high power CPU supplies
- 5V to 1.0V DC-DC conversion
- Portable electronics/instruments
- P54 and P55 regulators

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7556CM	−40°C to +85°C	28-Pin SOIC	MDP0027

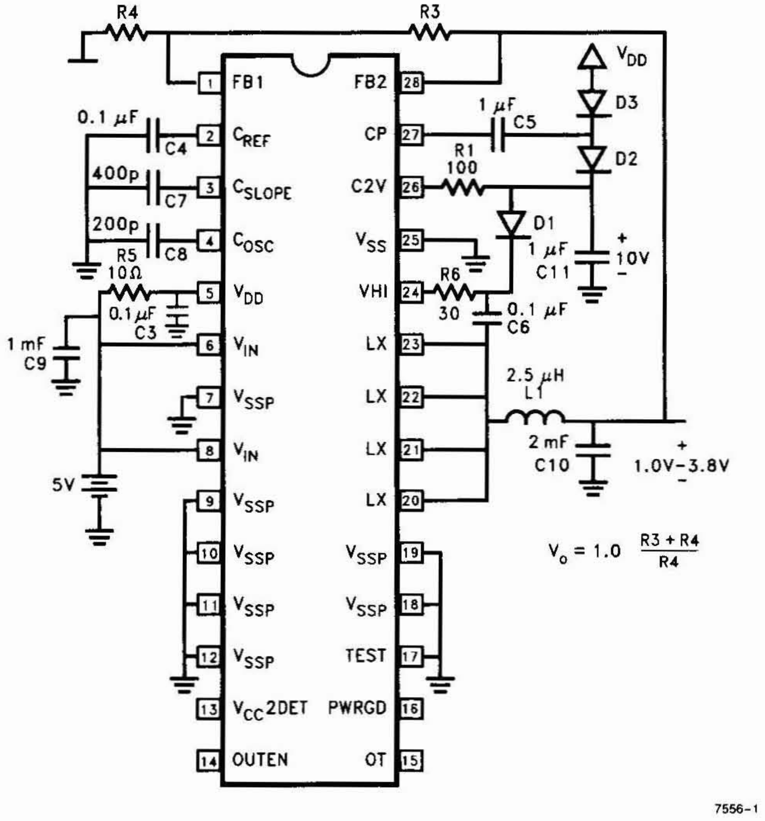
General Description

The EL7556C is the simplest, most cost effective method for powering modern high power CPUs which require a user adjustable output voltage. Although it is particularly designed to function with next generation CPUs, its simple design can provide low cost solutions for any 1.0V to 3.8V application from a 5V bus.

The circuit uses on chip resistorless current sensing for high efficiency, stable current mode control. An on chip temperature sensor resets the OT pin. The OT pin can be tied directly to the OUTEN pin for automatic overtemperature shutdown. The user can adjust the oscillator frequency as well as the slope compensation.

The EL7556C also incorporates the VCC2DET function to directly interface with the Intel P54 and P55 microprocessors. Depending on the state of VCC2DET pin, the output voltage is either set internally or adjustable using two external resistors. A power OK signal "PWRGD" pulls high when the regulator output is within ±10% of the desired voltages.

Connection Diagram


R4
R3
VDD
D3
D2
D1
1 FB1
FB2 28
0.1 µF
C4
2 CREF
CP 27
1 µF
C5
R1
100
400p
C7
3 CSLOPE
C2V 26
200p
C8
4 COSC
VSS 25
1 µF
C11
10V
R5
10Ω
5 VDD
VHI 24
R6
30
0.1 µF
C6
0.1 µF
C3
1 mF
C9
6 VIN
LX 23
2.5 µH
L1
7 VSSP
LX 22
8 VIN
LX 21
2 mF
C10
1.0V–3.8V
5V
9 VSSP
LX 20
10 VSSP
VSSP 19
$V_o = 1.0 \frac{R3 + R4}{R4}$
11 VSSP
VSSP 18
12 VSSP
TEST 17
13 VCC2DET
PWRGD 16
14 OUTEN
OT 15
7556-1

June 1996 Preliminary

Absolute Maximum Ratings ($T_A = 25°C$)

Storage Temperature Range	−65°C to +150°C	Operating Junction Temperature	125°C
Supply (V_{IN})	6V	Combined Peak Output Current	9A
Ambient Operating Temperature	0°C to +75°C	Power Dissipation	2W
Output Pins	−0.3V below GND, +0.3V above V_{DD}		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

DC Electrical Characteristics $T_A = 25°C$, $V_{IN} = 5V$ unless otherwise specified.

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
V_{2X}	Voltage Doubler Output	$V_{DD} = 5V$, ILOAD = 20 mA	7.9	8.4	8.9	I	V
V_{REF}	Reference Absolute Value	ILOAD = 0	1.150		1.250	I	V
V_{REFTC}	Reference Voltage Tempco			50			ppm
$V_{REFLOAD}$	Reference Voltage Load Regulation	0 < ILOAD < 1 mA	−0.5%		0.5	I	%
F_{OSC}	Oscillator Initial Accuracy	$C_{OSC} = 1000$ pF	90	100	110	I	kHz
F_{OSCTC}	Oscillator Tempco	$0 < T_A < 125$ $C_{OSC} = 1000$ pF	−0.1		0.1	V	%/deg
F_{RAMP}	Oscillator Ramp Amplitude	$C_{OSC} = 1000$ pF	1.1		1.3	V	V
M_{SS}	Soft Start Slope	$F_{OSC} = 500$ kHz	0.1		0.5	V	V/msec
VCC2DET	VCC2DET Pull Up Current			13		V	μA
I_{CSLOPE}	CSLOPE Charging Current		10		14	I	μA
I_{DD}	Supply Current	OUTEN = 4V		9	14	I	mA
I_{DDOFF}	Stdby Current	OUTEN = 0		9	15	I	mA
R_{DSON}	Composite FET Resistance			15	25	I	mΩ
V_{OUT}	Output Initial Accuracy	VCC2DET = High	3.465	3.5	3.535	I	V
I_{LMAX}	Maximum Current	$V_{OUT} = 0$	6.5	7.5		V	amps
V_{OUTTC}	Output Tempco		−1	0	1	V	%
$V_{OUTLINE}$	Output Line Regulation	$V_{out} = 2.5$ $4 < V_{IN} < 5.5$	−1		1	I	%
$V_{OUTLOAD}$	Output Load Regulation	$1A < I_{LOAD} < 6A$	−1		1	V	%
V_{OUTTOT}	Output Total Variation		−2		2	V	%

EL7556C
Adjustable CPU Power Supply Unit-6A

DC Electrical Characteristics — Contd.

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
T_{OFF}	Over Temperature Threshold			150		V	C
T_{HYS}	Over Temperature Hysteresis			20		V	C
V_{GOOD}	Power Good Threshold with Respect to Desired Output Voltage		±6	±10	±14	I	%
V_{DDON}	Minimum V_{DD} form Startup				4	I	V
V_{DDOFF}	Maximum V_{DD} for Shutdown		3.75			I	V

EL7556C Pin Description

Pin No.	Pin Name	Description
1	FB1	Voltage feedback pin for the buck regulator. Active when VCC2DET is low. Normally connected to a resistor divider externally.
2	C_{REF}	Reference bypass pin. Use at least 0.1 µF bypass to ground.
3	C_{SLOPE}	Slope compensation capacitor. A 10 µA current flows out of this pin. The voltage at this pin is reset to the reference voltage each clock period during the dead time.
4	C_{OSC}	Oscillator timing capacitor. The oscillator frequency is approximately: F_{OSC} (HZ) = 0.0001/C_{OSC}(F) The duty cycle is approximately 4%.
5	V_{DD}	This pin supplies power to the internal control circuitry. It will draw some tens of milliamps when operating.
6	V_{IN}	Positive power supply input to the buck regulator. This is one of two pins connected to the drain of a very large NMOS FET called the "Main" FET.
7	VSSP	Ground return to the buck regulator. This pin is connected to the source of a very large NMOS FET called the "synchronous" FET.
8	V_{IN}	Same as pin 6.
9	VSSP	Same as pin 7.
10	VSSP	Same as pin 7.
11	VSSP	Same as pin 7.
12	VSSP	Same as pin 7.
13	VCC2DET	VCC2DET interface. When High FB2 is selected. When low, FB1 is selected.
14	OUTEN	Enables the switching regulator. High is "on". The reference, oscillator, and voltage doubler operate whenever the power supply qualified regardless of the state of this pin.
15	OT	Over temperature indicator. This pin is normally high. It pulls low when the die temperature exceeds 150°C. There is 10–20 degrees of hysteresis in the comparator.
16	PWRGD	This pin pulls high whenever the FB pin is within 7% of its programmed value.
17	TEST	Test pin. Must be connected to ground.
18	VSSP	Same as pin 7.
19	VSSP	Same as pin 7.
20	LX	This is the halfway point between the two large intemal FETs. It drives the inductor of the buck regulator circuit. These are high current outputs.
21	LX	Same as pin 20.

EL7556C Pin Description — Contd.

Pin No.	Pin Name	Description
22	LX	Same as pin 20.
23	LX	Same as pin 20
24	VHI	Positive supply for the high side driver. This pin is bootstrapped from LX pin with a 0.1 μF capacitor.
25	V_{SS}	Ground return for the control circuitry.
26	C2V	Voltage doubler output. This pin requires at least a 1 μF capacitor to GND. The voltage on this pin will be 9V–10V depending on the load.
27	CP	Input for the charge pump bootstrap capacitor.
28	FB2	Voltage feedback pin. Active when VCC2DET is high. Normally connected to a resistor divider internally.

Applications Information

The EL7556 incorporates a VCC2DET function to directly interface with the Intel P54 and P55 microprocessors. When this pin is shorted to ground as in the P55 processor, the feedback path of EL7556 is internally switched to FB1. The regulator output is determined by the external resistor divider ratio, $V_{OUT} = 1.0\,(1+R3/R4)$. When this pin is open as in the P54 processor, the feedback path of the EL7556 is switched to FB2. The regulator output is set internally to 3.5V nominal.

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7560C
Programmable CPU Power Supply Unit

Features

- 3.3V @ 12.4 amps continuous
- Internal FETs
- >90% efficiency
- Synchronous switching
- 4-bit digitally adjustable output voltage
- User adjustable slope compensation
- Internal soft start
- Over temperature indicator
- Low current sleep mode
- Low parts count
- Pulse by pulse current limiting
- High efficiency at light load
- Operates up to 1 MHz
- 1% output accuracy
- Sync function
- Power good signal

Applications

- PC motherboards
- Local high power CPU supplies

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7560CM	−40°C to +85°C	28-Pin SOIC	MDP0027

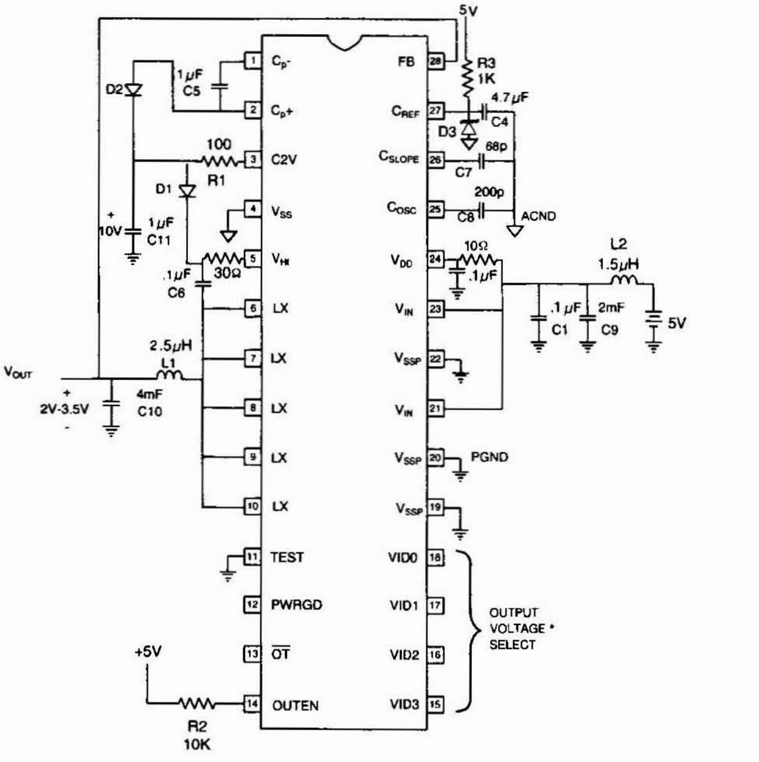
General Description

The EL7560C is the simplest, most cost effective method for powering modern high power CPUs which require a user adjustable output voltage. Although it is particularly designed to function with next generation CPUs, its simple design can provide low cost solutions for any 5V to 3V application.

The circuit uses on chip resistorless current sensing for high efficiency, stable current mode control. An on chip temperature sensor resets the OT pin. The OT pin can be tied directly to the OUTEN pin for automatic overtemperature shutdown. The user can adjust the oscillator frequency as well as the slope compensation.

The output voltage is adjustable using a 4-bit parallel interface. A power OK signal "PWRGD" pulls high when the FB pin is within −7% of the programmed value.

Connection Diagram


5V
R3
1K
4.7µF
C4
D3
68p
C7
200p
C8
ACND
10Ω
.1µF
L2
1.5µH
.1µF
C1
2mF
C9
5V
PGND
OUTPUT
VOLTAGE *
SELECT
1 Cp-
2 Cp+
3 C2V
4 VSS
5 VHI
6 LX
7 LX
8 LX
9 LX
10 LX
11 TEST
12 PWRGD
13 OT
14 OUTEN
28 FB
27 CREF
26 CSLOPE
25 COSC
24 VDD
23 VIN
22 VSSP
21 VIN
20 VSSP
19 VSSP
18 VID0
17 VID1
16 VID2
15 VID3
D2
1µF
C5
100
R1
D1
+
10V
1µF
C11
.1µF
C6
30Ω
2.5µH
L1
VOUT
+
2V-3.5V
-
4mF
C10
+5V
R2
10K
7560-1

*See VID table on page 3

Note: AGND and PGND should be connected at C10
D3 is 1.235V reference

July 1996 Rev A

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{IN}, V_{DD})	5.5V	Storage Temperature Range	−65°C to +150°C
Output Pins	−0.3V below GND, +0.3V above V_{DD}	Ambient Operating Temperature	−40°C to +85°C
Instantaneous Peak Output Current	16A	Operating Junction Temperature	135°C
		Power Dissipation	3W

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

$V_{DD} = V_{IN} = 5V$, $C_{OSC} = 1$ nF, $C_{SLOPE} = 68$ pF, $T_A = 25°C$, unless otherwise specified

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
V_{2X}	Voltage Doubler Output	$V_{DD} = 5V$, $I_{LOAD} = 20$ mA	8.0	9	9.5	I	V
DAC_{LSB}	DAC Resolution		0.095		0.105	I	V
F_{OSC}	Oscillator Initial Accuracy		105	120	135	I	kHz
F_{OSCTC}	Oscillator Tempco	$0°C < T_A < 125°C$		±0.1		V	%/° C
V_{RAMP}	Oscillator Ramp Amplitude			1.2		V	V
M_{SS}	Soft Start Slope	$F_{OSC} = 500$ kHz		0.3		V	V/msec
I_{VID}	VID Pull Up Current	VID = 0V	9	13	18	I	µA
I_{CSLOPE}	C_{SLOPE} Charging Current		32	40	48	I	µA
I_{DD}	Supply Current	OUTEN = 4V Fosc = 120 kHz		25	35	I	mA
I_{DDOFF}	Stdby Current	OUTEN = 0V		3	5	I	mA
R_{DSON}	Composite FET Resistance		18		25	I	mΩ
R_{DSONTC}	R_{DSON} Tempco			0.1		V	mΩ/°C
V_{OUT}	Output Initial Acurracy	VID = 0111	2.765	2.8	2.835	I	V
V_{RANGE}	Output Voltage Range	VID = 1110 to 0000	2.065		3.535	I	V
I_{LMAX}	Maximum current	$V_{OUT} = 0$		14.0		V	amps
$V_{OUT\text{-}TC}$	Output Tempco	$0°C < T_A < 70°C$		±1		V	%
$V_{OUT\text{-}LINE}$	Output Line Regulation	$V_{OUT} = 2.8$, $4.5V_{DD} < 5.5$, $V_{DD} = V_{IN}$	−1		1	I	%
$V_{OUT\text{-}LOAD}$	Output Load Regulation	$0.3A < I_{LOAD} < 12.4A$	−1		1	IV	%
$V_{OUT\text{-}TOT}$	Output Total Variation		−2		2	IV	%

DC Electrical Characteristics

$V_{DD} = V_{IN} = 5V$, $C_{OSC} = 1$ nF, $C_{SLOPE} = 68$ pF, $T_A = 25°C$, unless otherwise specified — Contd.

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
OT_{OFF}	Over Temperature Threshold			135		V	°C
OT_{HYS}	Over Temperature Hysteresis			50		V	°C
V_{PWRGD}	Power Good Threshold with Respect to Desired Output Voltage	VID = 0111	−9	−7	−5	I	%
$V_{DD\text{-}ON}$	Minimum V_{DD} form Startup				4	I	V
$V_{DD\text{-}OFF}$	Maximum V_{DD} for Shutdown		3.75			I	V

Note 1: The oscillator and voltage doubler operate normally when V_{DD} exceeds $V_{DD\text{-}ON}$ threshold, independent of the OUTEN logic level.

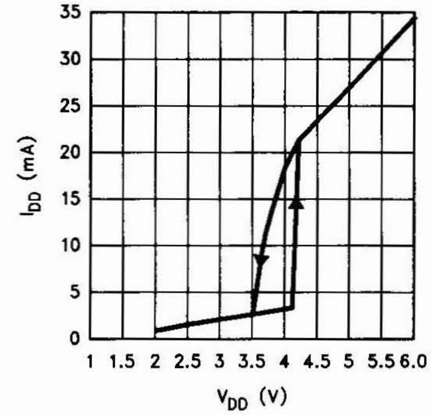
Voltage Identification Codes

P6 Pins				
V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	V_{DC}
1	1	1	1	0, No CPU
1	1	1	0	2.1
1	1	0	1	2.2
1	1	0	0	2.3
1	0	1	1	2.4
1	0	1	0	2.5
1	0	0	1	2.6
1	0	0	0	2.7
0	1	1	1	2.8
0	1	1	0	2.9
0	1	0	1	3.0
0	1	0	0	3.1
0	0	1	1	3.2
0	0	1	0	3.3
0	0	0	1	3.4
0	0	0	0	3.5

EL7560 Pin Description

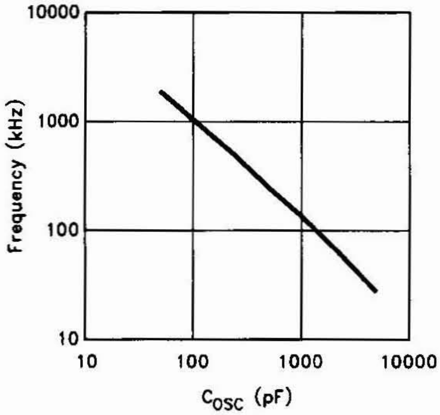
Pin Number	Name	Description
1	C_P-	Negative input for the charge pump bootstrap capacitor. (Note 1)
2	C_P+	Positive input for the charge pump bootstrap capacitor. (Note 1)
3	C2V	Voltage doubler output. Pin requires at least a 1μF capacitor to GND. (Note 1)
4	V_{SS}	Ground return for the control circuitry.
5	V_{HI}	Positive supply for the high side driver. This pin is bootstrapped from the LX pin with a 0.1μF capacitor.
6	LX	Common connection between the two large internal FETs. External inductor connection.
7	LX	Same as pin 6.
8	LX	Same as pin 6.
9	LX	Same as pin 6.
10	LX	Same as pin 6.
11	TEST	This is test pin and **must remain grounded at all times**
12	PWRGD	Pin pulls high when the FB pin is within − 7%(typ) of its programmed value.
13	$\overline{\text{OT}}$	Overtemperature indicator. Pulls low when the die temperature exceeds 135°C. Pin has 10 mA pull-up.
14	$\overline{\text{OT}}$	A logic high on OUTEN enables the regulator (Note 1)
15	VID3	Bit 3(MSB) of the output voltage select DAC.
16	VID2	Bit 2 of the output voltage select DAC.
17	VID1	Bit 1 of the output voltage select DAC.
18	VID0	Bit 0(LSB) of the output voltage select DAC.
19	V_{SSP}	Ground return to the buck regulator.
20	V_{SSP}	Same as pin 19.
21	V_{IN}	Positive power supply input to the buck regulator.
22	V_{SSP}	Same as pin 19.
23	V_{IN}	Same as pin 21.
24	V_{DD}	Pin supplies power to the internal control circuitry.
25	C_{OSC}	Oscillator timing capacitor. Oscillator Frequency is approximately: $F_{OSC}(Hz) = 0.0001/C_{OSC}(F)$. The duty cycle is approximately 5%. (Note 1)
26	C_{SLOPE}	Slope compensation capacitor.
27	C_{REF}	External reference input pin.
28	FB	Voltage feedback pin for the buck regulator.

Typical Performance Curves



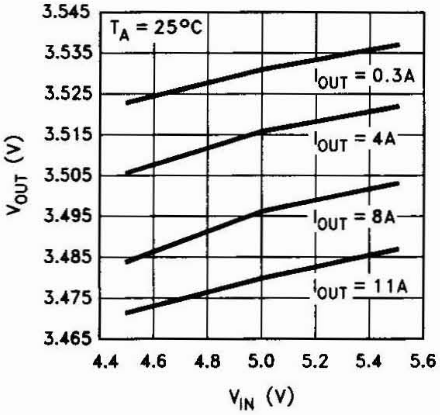
I_{DD} vs V_{DD}

7560-2



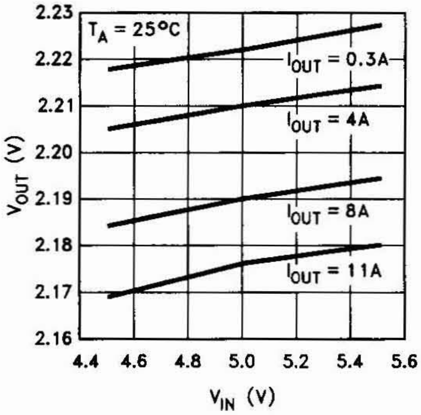
Oscillator Frequency vs C_{OSC}

7560-3



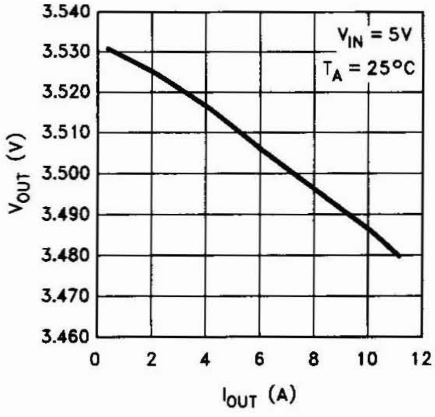
Line Regulation (VID3:0 = 0000)

7560-4



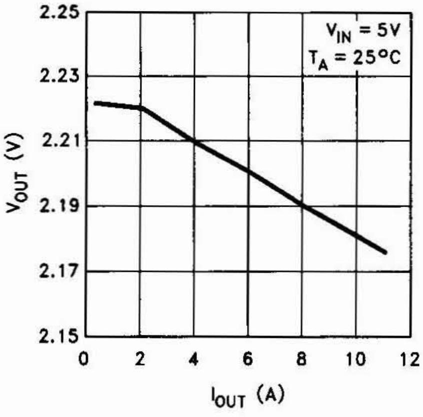
Line Regulation (VID3:0 = 1101)

7560-5



Load Regulation (VID3:0 = 0000)

7560-6

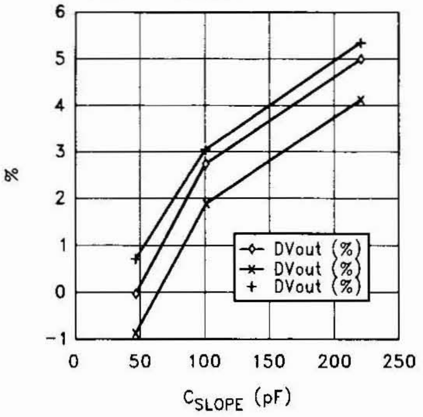


Load Regulation (VID3:0 = 1101)

7560-7

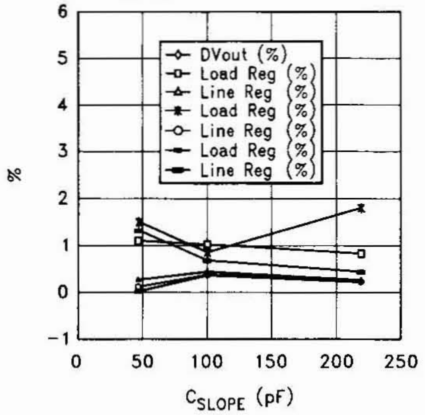
Typical Performance Curves — Contd.

V_{OUT} vs C_{SLOPE}



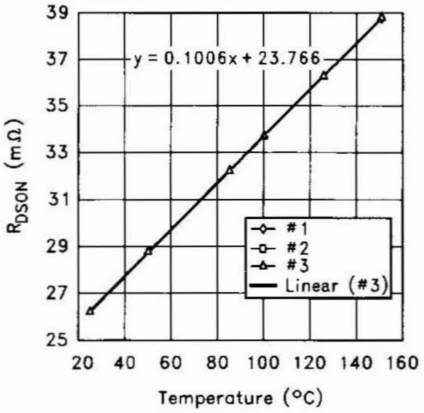
7560-11

Load and Line Regulation vs C_{SLOPE}



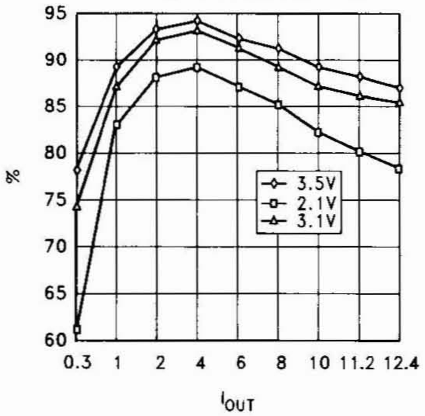
7560-12

R_{DSON} vs Temp



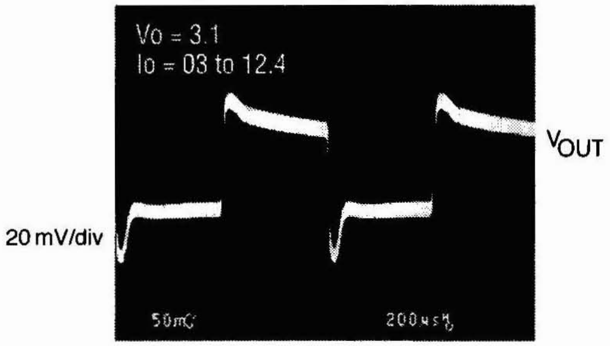
7560-13

Efficiency vs Output Current



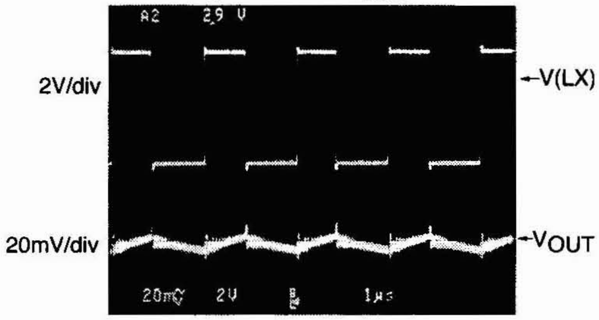
7560-14

Transient Load Step
0.3 Amp → 12.4 Amp



7560-8

Switching Waveforms I_{LOAD} = 2A



7560-9

Block Diagram

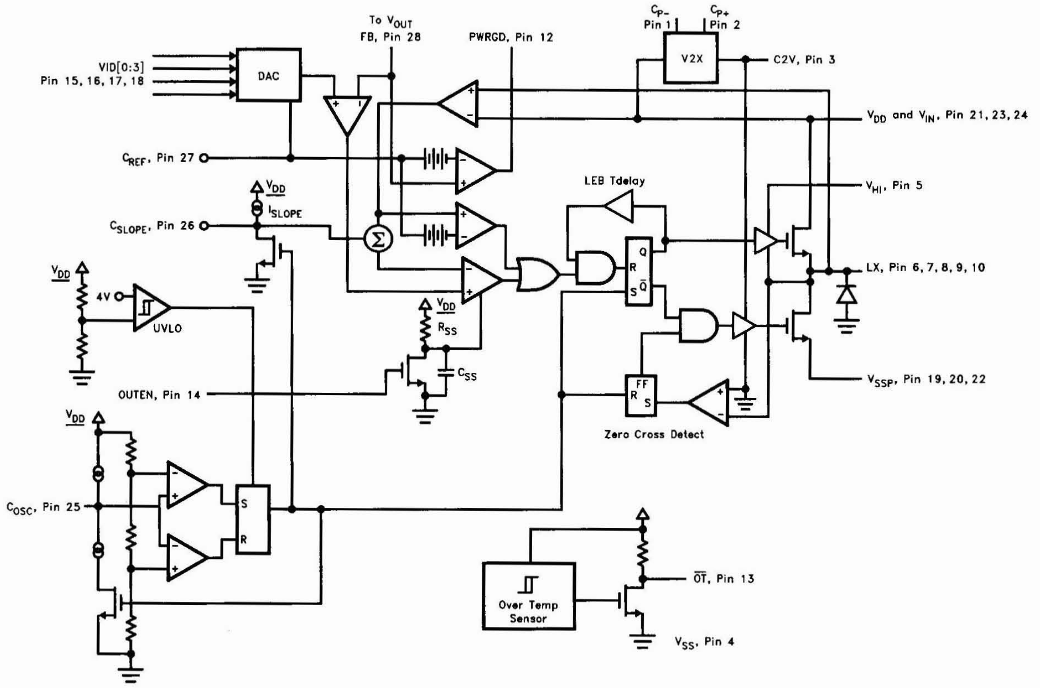

VID[0:3]
Pin 15, 16, 17, 18
DAC
To V_{OUT}
FB, Pin 28
PWRGD, Pin 12
C_{P-}
Pin 1
C_{P+}
Pin 2
V2X
C2V, Pin 3
V_{DD} and V_{IN}, Pin 21, 23, 24
C_{REF}, Pin 27
V_{DD}
I_{SLOPE}
C_{SLOPE}, Pin 26
LEB Tdelay
Q
R
S
$\bar{Q}$
V_{HI}, Pin 5
LX, Pin 6, 7, 8, 9, 10
V_{DD}
4V
UVLO
V_{DD}
R_{SS}
C_{SS}
OUTEN, Pin 14
FF
R
S
Zero Cross Detect
V_{SSP}, Pin 19, 20, 22
V_{DD}
C_{OSC}, Pin 25
S
R
$\overline{OT}$, Pin 13
Over Temp Sensor
V_{SS}, Pin 4
7560-10

Figure 1. EL7560 Functional Block Diagram

EL7561C
Programmable CPU Power Supply Unit

Features

- 3.3V @ 12.4 amps continuous
- Internal FETs
- > 90% Efficiency
- Synchronous switching
- 4-Bit digitally adjustable output voltage
- User adjustable slope compensation
- Internal soft start
- Precision 0.5% reference
- Over temperature indicator
- Low current sleep mode
- Low parts count
- Pulse by pulse current limiting
- High efficiency at light load
- Operates up to 1 MHz
- 1% Output accuracy
- Sync function
- Power good signal

Applications

- PC Motherboards
- Local high power CPU supplies

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7561CM	−40°C to +85°C	28-Pin SOIC	MDP0027

General Description

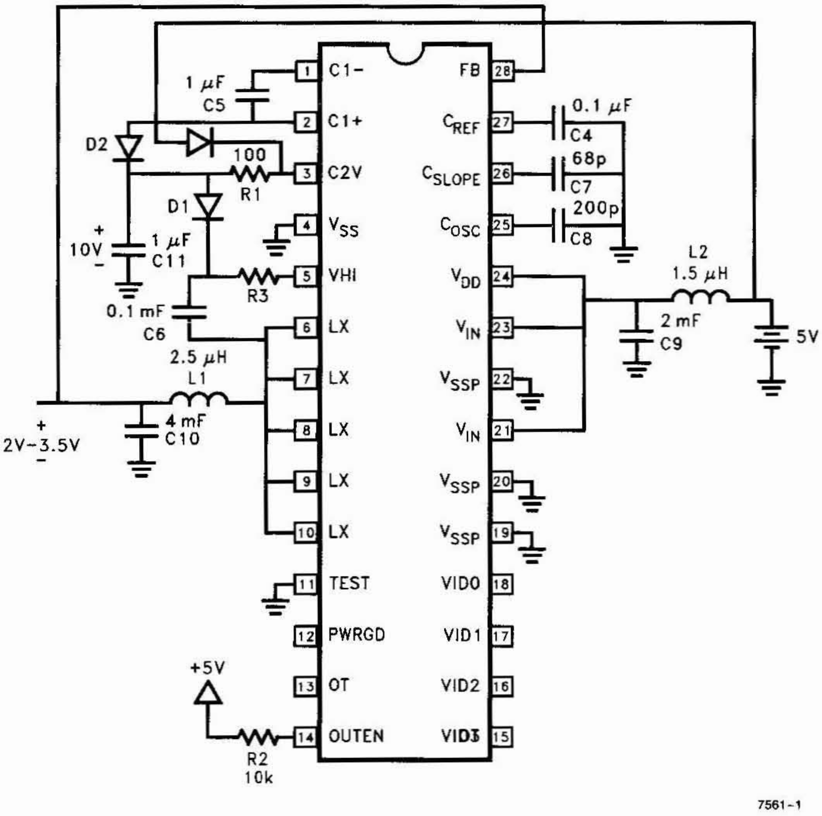
The EL7561C is the simplest, most cost effective method for powering modern high power CPUs which require a user adjustable output voltage. Although it is particularly designed to function with next generation CPUs, its simple design can provide low cost solutions for any 5V to 3V application.

The circuit uses on chip resistorless current sensing for high efficiency, stable current mode control. An on chip temperature sensor resets the OT pin. The OT pin can be tied directly to the OUTEN pin for automatic overtemperature shutdown. The user can adjust the oscillator frequency as well as the slope compensation.

The output voltage is adjustable using a 4-bit parallel interface. A power OK signal "PWRGD" pulls high when the FB pin is within 7% of the programmed value.

Preliminary

Connection Diagram


1 C1−
2 C1+
3 C2V
4 VSS
5 VHI
6 LX
7 LX
8 LX
9 LX
10 LX
11 TEST
12 PWRGD
13 OT
14 OUTEN
28 FB
27 CREF
26 CSLOPE
25 COSC
24 VDD
23 VIN
22 VSSP
21 VIN
20 VSSP
19 VSSP
18 VID0
17 VID1
16 VID2
15 VID3
1 μF
C5
D2
100
R1
D1
+
10V
−
1 μF
C11
R3
0.1 mF
C6
2.5 μH
L1
4 mF
C10
+
2V−3.5V
−
+5V
R2
10k
0.1 μF
C4
68p
C7
200p
C8
L2
1.5 μH
2 mF
C9
5V
7561-1

Absolute Maximum Ratings (T_A = 25°C)

Supply (V_{IN})	5.5V
Output Pins	−0.3V below GND, +0.3V above V_{DD}
Momentary Peak Output Current	16A
Storage Temperature Range	−65°C to +150°C
Ambient Operating Temperature	−40°C to +85°C
Operating Junction Temperature	135°C
Power Dissipation	3W

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
V_{2X}	Voltage Doubler Output	V_{DD} = 5V, I_{LOAD} = 20 mA	8.0	9	9.5	I	V
V_{REF}	Reference Absolute Value	I_{LOAD} = 0	1.150		1.250	I	V
V_{REFTC}	Reference Voltage Tempco			50			ppm/°C
$V_{REFLOAD}$	Reference Voltage Load Regulation	$0 < I_{LOAD} < 0.5$ mA	−0.5		0.5	I	%
DAC_{LSB}	DAC Resolution		0.095		0.105	I	V
F_{OSC}	Oscillator Initial Accuracy	C_{OSC} = 1000 pF	105	120	135	I	kHZ
F_{OSCTC}	Oscillator Tempco	$0 < T_A < 125$ C_{OSC} = 1000 pF		±0.1		V	%/°C
V_{RAMP}	Oscillator Ramp Amplitude	C_{OSC} = 1000 pF	1.1	1.2	1.3	V	V
M_{SS}	Soft Start Slope	F_{OSC} = 500 kHz		0.3		V	V/ms
I_{VID}	VID Pull Up Current			10		V	µA
I_{CSLOPE}	C_{SLOPE} Charging Current		32	40	48	I	µA
I_{DD}	Supply Current	OUTEN = 4V F_{OSC} = 120 kHz		25	35	I	mA
I_{DDOFF}	Stdby Current	OUTEN = 0		3	5	I	mA
R_{DSON}	Composite FET Resistance		18		25	I	Ω
R_{DSONTC}	R_{DSON} Tempco	$0 < T_A < 70$°C		0.1		V	mΩ/°C

DC Electrical Characteristics — Contd.

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
V_{OUT}	Output Initial Accuracy	VID = 0111	2.765	28	2.835	I	V
V_{RANGE}	Output Voltage Range	VID = 1110 to 0000	2.065		3.535	V	V
I_{LMAX}	Maximum Current	$V_{OUT} = 0$	12.5	15.0		V	A
V_{OUTTC}	Output Tempco	$0 < T_A < 25°C$		±1		V	%
$V_{OUTLINE}$	Output Line Regulation	$V_{OUT} = 2.8$ $4.5 < V_{DD} < 5.5$ $V_{DD} = V_{IN}$	−1		1	I	%
$V_{OUTLOAD}$	Output Load Regulation	$0.3A < I_{LOAD} < 12.4$	−1		1	IV	%
V_{OUTTOT}	Output Total Variation		−2		2	IV	%
OT_{OFF}	Over Temperature Threshold			135		V	C
OT_{HYS}	Over Temperature Hysteresis			50		V	C
V_{PWRGD}	Power Good Threshold with Respect to Desired Output Voltage	VID = 0111	±8		±15	I	%
V_{DDON}	Minimum V_{DD} form Startup				4	I	V
V_{DDOFF}	Maximum V_{DD} for Shutdown		3.75			I	V

EL7561C Pin Description

Pin Number	Name	Description
1	C_P-	Negative input for the charge pump bootstrap capacitor. (Note 1)
2	C_P+	Positive input for the charge pump bootstrap capacitor. (Note 1)
3	C2V	Voltage doubler output. Pin requires at least a 1 μF capacitor to GND. (Note 1)
4	V_{SS}	Ground return for the control circuitry.
5	V_{HI}	Positive supply for the high side driver. This pin is bootstrapped from the LX pin with a 0.1 μF capacitor.
6	LX	Common connection between the two large internal FETs. External inductor connection.
7	LX	Same as pin 6.
8	LX	Same as pin 6.
9	LX	Same as pin 6.
10	NC	
11	TEST	This is test pin and **must remain grounded at all times**
12	PWRGD	Pin pulls high when the FB pin is within ±10% (typ) of its programmed value.
13	$\overline{OT}$	Overtemperature indicator. Pulls low when the die temperature exceeds 135°C. Pin has 10 mA pull-up.
14	OUTEN	A logic high on OUTEN enables the regulator (Note 1)
15	VID3	Bit 3(MSB) of the output voltage select DAC.

EL7561 Pin Description — Contd.

Pin Number	Name	Description
16	VID2	Bit 2 of the output voltage select DAC.
17	VID1	Bit 1 of the output voltage select DAC.
18	VID0	Bit 0(LSB) of the output voltage select DAC.
19	V_{SSP}	Substrate connection.
20	V_{SSP}	Ground return to the buck regulator.
21	V_{IN}	Positive power supply input to the buck regulator.
22	V_{SSP}	Same as pin 20.
23	V_{IN}	Same as pin 21.
24	V_{DD}	Pin supplies power to the internal control circuitry.
25	C_{OSC}	Oscillator timing capacitor. Oscillator Frequency is approximately: $F_{OSC}(Hz) = 0.0001/C_{OSC}(F)$. The duty cycle is approximately 5%. (Note 1)
26	C_{SLOPE}	Slope compensation capacitor.
27	C_{REF}	External reference input pin.
28	FB	Voltage feedback pin for the buck regulator.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7571C
Programmable DC/DC Converter

Features

- Pentium® Pro Compatible, DAC controlled output voltage
- Greater than 90% efficiency
- 4.5V–13.2V input range
- Fixed frequency, current mode control
- Adjustable oscillator with external sync. capability
- Synchronous switching
- Internal soft start
- User adjustable slope compensation
- Low current sleep mode
- Pulse by pulse current limiting
- 1% Output accuracy
- Power good signal

Applications

- Pentium Pro Voltage regulation modules (VRM's)
- PC Motherboards
- Synchronous rectification

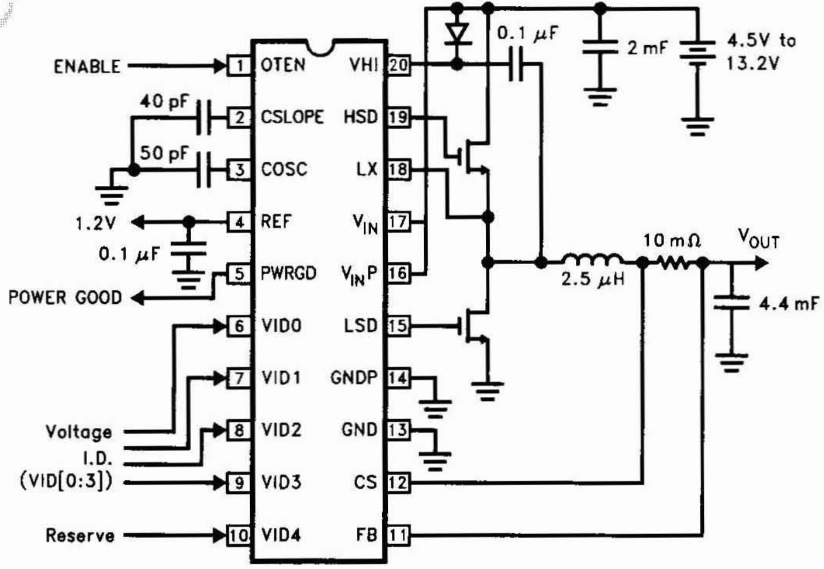
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL7571CM	−40°C to +85°C	20-Pin SOIC	MDP0027

General Description

The EL7571C is a flexible, high efficiency, PWM step down controller incorporating five bit DAC adjustable output voltage control which conforms to the Pentium Pro Voltage ID specification. The controller employs synchronous rectification to deliver efficiencies greater than 90% over a wide range of supply voltages and load conditions. A low power sleep mode minimizes quiescent current when the regulator is disabled. The onboard oscillator frequency is externally adjustable, or may be slaved to a system clock, allowing optimization of RFI performance in critical applications. For maximum flexibility, the control section may be powered from either 5V or 12V supplies.

Connection Diagram


ENABLE
40 pF
50 pF
1.2V
0.1 µF
POWER GOOD
Voltage
I.D.
(VID[0:3])
Reserve
1 OTEN
2 CSLOPE
3 COSC
4 REF
5 PWRGD
6 VID0
7 VID1
8 VID2
9 VID3
10 VID4
VHI 20
HSD 19
LX 18
V_{IN} 17
$V_{IN}P$ 16
LSD 15
GNDP 14
GND 13
CS 12
FB 11
0.1 µF
2 mF
4.5V to
13.2V
10 mΩ
V_{OUT}
2.5 µH
4.4 mF

7571-1

Pentium® is a registered trademark of Intel Corporation.

6

June 1996 Preliminary

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage	−0.5V to 15V	Operating Temperature Range	−40°C to +85°C
Input Pin Voltage	−0.3V below Ground, +0.3V above supply	Operating Junction Temperature	125°C
VHI	< 30V	Peak Output Current	2A
Storage Temperature Range	−65°C to +150°C	Power Dissipation	SOIC 500 mW

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics T_A = 25°C, V_{IN} = 5V unless otherwise specified

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
V_{IN}	Input Voltage Range		4.5		13.2	I	V
V_{UVLO_HI}	Under Voltage Lockout High Threshold	Positive Going Input Voltage	3.6		4.4	I	V
V_{UVLO_LO}	Under Voltage Lockout Low Threshold	Negative Going Input Voltage	3.15		3.85	I	V
V_{OUT}	Output Voltage	See VID Table	1.3		3.5	I	V
V_{REF}	Band Gap Voltage		1.26		1.29	I	V
V_{ILIM}	Current Limit Voltage	$V_{ILIM} = (V_{CS} - V_{REF})$	135		165	I	mV
V_{OTEN_LO}	Power Down Input Low Level	$I_{IN} = -10\ \mu A$	0		1.5	I	V
V_{OTEN_HI}	Power Down Input High Level		$(V_{IN}-1.5)$		V_{IN}	I	V
V_{ID_LO}	Voltage I.D. Input Low Level		0		1.5	I	V
V_{ID_HI}	Voltage I.D. Input High Level		$(V_{IN}-1.5)$		V_{IN}	I	V
V_{OSC}	Oscillator Voltage Swing			1		V	V
V_{PWRGD_LO}	Power Good Output Low Level	I_{OUT} = 3.2 mA			0.5	I	V

DC Electrical Characteristics $T_A = 25°C, V_{IN} = 5V$ unless otherwise specified — Contd.

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
R_{DS_ON}	HSD, LSD Switch On-Resistance	$I_{OUT} = -100$ mA $(V_{HI}-LX) > 4.5V$			5	I	Ω
R_{FB}	FB Input Impedance			9.5		V	kΩ
I_{VIN}	Quiescent Supply Current	$V_{OTEN} > (V_{DD}-0.5)$		1.5	3	I	mA
I_{VIN_SLEEP}	Supply Current in Sleep Mode	$V_{OTEN} < 0.5V$			100	I	µA
$I_{SOURCE/SINK}$	Driver Output Current	Measured at HSD, LSD, (VHI−LX) > 4.5V		1		IV	A
I_{RAMP}	CSLOPE Ramp Current	High Side Switch Enabled	6		14	I	µA
I_{OSC_CHARGE}	Oscillator Charge Current	$1.2 > V_{OSC} > 0.2V$		50		V	µA
$I_{OSC\_DISCHARGE}$	Oscillator Discharge Current	$1.2 > V_{OSC} > 0.2V$		1.6		V	mA
I_{REF_MAX}	V_{REF} Output Current				25	V	µA
I_{VID}	VID Input Pull-Up Current		3		7	I	µA
I_{OTEN}	OTEN Input Pull-Up Current		3		7	I	µA

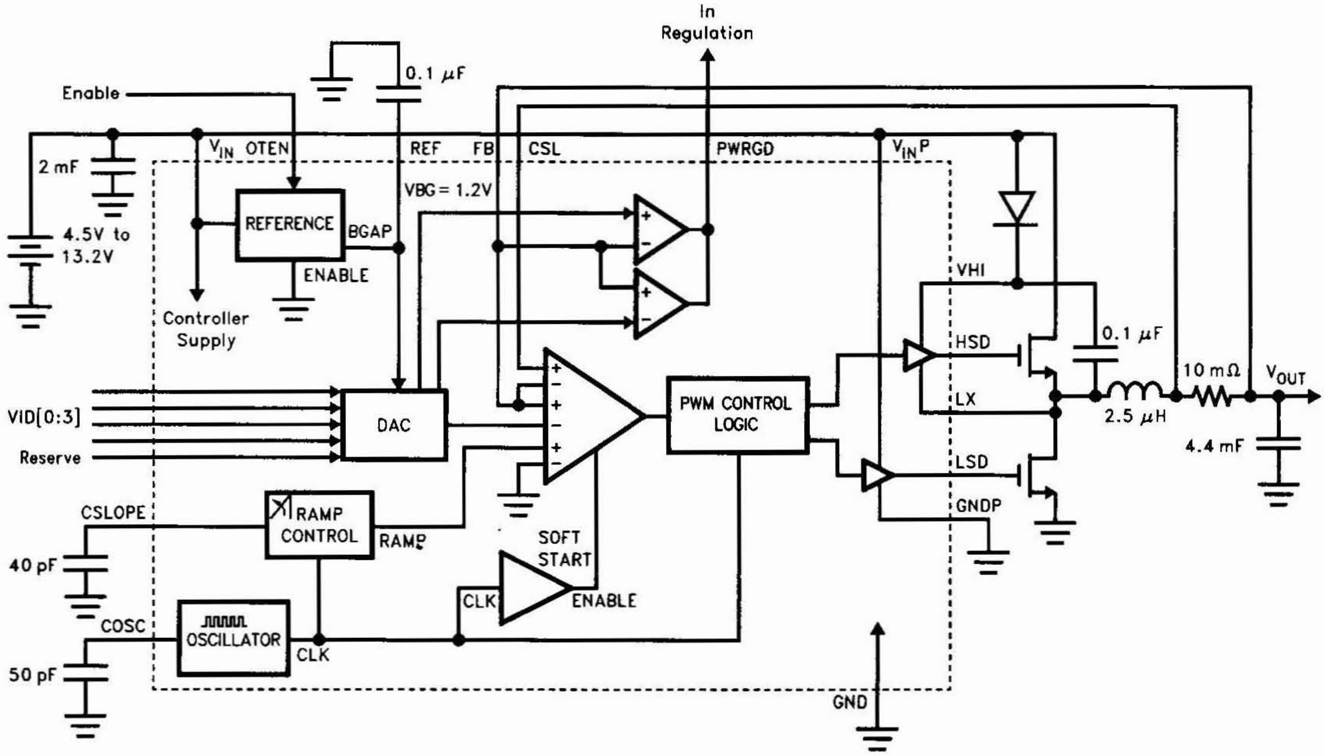
AC Electrical Characteristic $T_A = 25°C, V_{IN} = 5V$ unless otherwise specified

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
f_{OSC}	Nominal Oscillator Frequency	$C_{OSC} = 400$ pF	102		138	I	kHz
f_{CLK}	Clock Frequency		100	500	1000	IV	kHz
f_{OTEN}	Shutdown Delay	$V_{OTEN} = 0.8V$	100			V	ns
t_{SYNC}	Sync. Pulse Width		10		50	IV	ns
T_{START}	Soft Start Period				$100/f_{CLK}$	V	µs
D_{MAX}	Maximum Duty Cycle			97		V	%

Pin Description

Pin No.	Pin Name	Pin Type	Function
1	OTEN	I	Chip enable input, internal pull-up (5 μA typical). Active high.
2	CSLOPE	I	With a capacitor attached from CLSOPE to GND, generates the voltage ramp compensation for the PWM current mode controller. Slope rage is determined by an internal 10 μA pull up and the CSLOPE capacitor value. V_{CSLOPE} is reset to ground at the termination of the high side cycle.
3	COSC	I	Multi-function pin: with a timing capacitor attached, sets the internal oscillator rate f_{CLK}; when pulsed low for a duration t_{SYNC} synchronizes device to an external clock.
4	REF	O	Band gap reference output. Decouple to GND with 0.1 μF.
5	PWRGD	O	Power good, open drain output. Set low whenever the output voltage *is not* within ±10% of the programmed value.
6	VID0	I	Bit 0 of the output voltage select DAC. Pull up sets input high when not driven.
7	VID1	I	Bit 1 of the output voltage select DAC. Pull up sets input high when not driven.
8	VID2	I	Bit 2 of the output voltage select DAC. Pull up sets input high when not driven.
9	VID3	I	Bit 3 of the output voltage select DAC. Pull up sets input high when not driven.
10	VID4	I	Bit 4 of the output voltage select DAC. Pull up sets input high when not driven.
11	FB	I	Voltage regulation feedback input. Tie to V_{OUT} for normal operation.
12	CS	I	Current Sense. Current feedback input of PWM controller and over current comparator input. Current Limit threshold set at +150 mV with respect to FB. Connect sense resistor between CS and FB for normal operation.
13	GND	S	Ground.
14	GNDP	S	Power ground for low side FET Driver. Tie to GND for normal operation.
15	LSD	O	Low side gate drive output.
16	VINP	S	Input supply voltage for low side FET driver. Tie to VIN for normal operation.
17	VIN	S	Input supply voltage for control circuit.
18	LX	I	Negative supply input of high side drive circuit.
19	HSD	O	High side gate drive output. Driver ground referenced to LX. Driver supply may be bootstrapped to enhance low controller input voltage operation.
20	VHI	I	Positive supply input of high side drive circuit.

Block Diagram


In Regulation
0.1 µF
Enable
2 mF
4.5V to 13.2V
V_IN OTEN
REF
FB
CSL
PWRGD
V_IN P
VBG = 1.2V
REFERENCE
BGAP
ENABLE
Controller Supply
VHI
HSD
LX
LSD
GNDP
0.1 µF
10 mΩ
V_OUT
2.5 µH
4.4 mF
VID[0:3]
Reserve
DAC
PWM CONTROL LOGIC
CSLOPE
40 pF
RAMP CONTROL
RAMP
SOFT START
CLK
ENABLE
COSC
50 pF
OSCILLATOR
CLK
GND

7571-2

Application Specific
A.T.E./Comparators

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Drivers - Bipolar

Part #	Features	V_O		I_O	Slew Rate		I_S	Standby I_S	Package P = Pins J = CerDIP M = SOL
		Min	Max	Min	Min	Max	Max	Max	
EL2021C	3-State Output Programmable Slew Rate, Short Circuit Current Sense	−6.1V to +10.9V	−5.9V to +11.1V	±500 mA	40V/μs	360V/μs	45 mA	2.5 mA	18P-J
EL1056C EL1056AC	Adjustable Slew Rate, Wide Voltage Range, Power Down	−12V	−12V	±50 mA DC ±150 mA DC	0.1V/ns	1.2V/ns	60 mA	25 mA	24P-M Thermal

Drivers - CMOS

Part #	Features	I_{peak}	R_{ON}	T_r/T_f	V_{supply}	Package P = Pins N = PDIP S = SOIC
POWER MOSFET DRIVERS						
EL7134C	Single, 3-State	4A	3Ω	20 ns/20 ns	16.5V	8P-N-S
EL7232C	Dual, 3-State	2A	6Ω	20 ns/20 ns	16.5V	8P-N-S
Special Function Drivers						
EL7154C	ATE/±15V to −5V Outputs, Level Shifter/3-State	2A	2.5Ω	20 ns/20 ns	16.5V	8P-N-S

Comparators

Part #	Features	Typ Prop Delay (5 mV Overdrive)	Typ Open Loop Gain	Input Common Mode Range		Typ Input Bias Current	Max Supply Current		Package P = Pin N = PDIP M = SOL
				(V_{CC} = ±15V)	(V_{CC} = ±5V)		Output Active	Output 3-State	
EL2018C	Fast, High Voltage w/Latch 3-State Output	20 ns	40,000V/V (92 dB)	±12V (Min)	±3V (Typ)	±100 nA	+11 mA/−18 mA	+7 mA/−6.5 mA	8P-N
EL2252C	50 MHz, Dual, High Voltage	6 ns	8,000V/V	−12V, +13V		17 μA	+19 mA/20 mA (Both Comparators)		14P-N 20P-M

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1056AC/EL1056C
Monolithic High-Speed Pin Driver

Features

- Wide ±12V output levels
- 250 ps dispersion
- 3 ns delay times
- 1V/ns slew rate—adjustable
- Low overshoot and aberrations in 50Ω systems
- 3-state output
- Power-down mode reduces output leakage to nanoamperes
- Overcurrent sense flag available to protect internal output devices
- Buffered analog inputs
- Differential logic inputs are compatible with ECL, TTL, and CMOS

Applications

- Memory testers
- ASIC testers
- Functional board testers
- Analog/digital incoming component verifiers
- Logic emulators

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1056CM	0°C to +75°C	24-Lead Thermal SOL	MDP0027
EL1056ACM	0°C to +75°C	24-Lead Thermal SOL	MDP0027

General Description

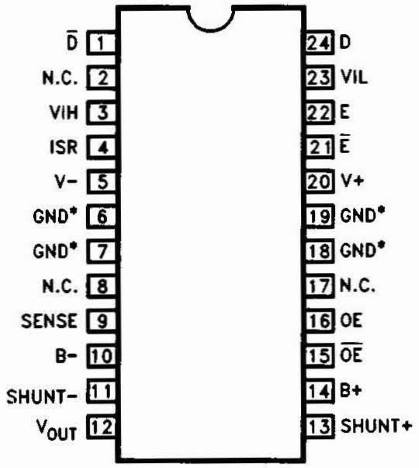
The EL1056 is designed to drive high-quality test signals into close or terminated loads. It has a dispersion of 250 ps or less — whether due to signal size or direction of edge. It can output a very wide 24V output span, encompassing all logic families as well as analog levels. The EL1056 is fabricated in Elantec's oxide isolated process, which eliminates the possibility of latch-up and provides a very durable circuit.

The output can be turned off in two ways; the OE pins allow the output to be put in a high-impedance state which makes the output look like a large resistance in parallel with 3 pF, even for back-driven signals with as much as 2.5V/μs slew rate. The E pins put the output in an even higher impedance state, guaranteed to 150 nA leakage in the EL1056A. This allows accurate measurements on the bus without disconnecting the EL1056 with a relay.

The EL1056 incorporates an output current sense which can warn the system controller that excessive output current is flowing. The trip point is set by two external resistors.

Connection Diagram

24-Lead Thermal SOL Package



*and Heat-spreader

1056-1

Top View

EL1056AC/EL1056C

Monolithic High-Speed Pin Driver

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	+33V
V−	Supply Voltage	−18V
B+	Supply Voltage	V_{INH} to V+
B−	Supply Voltage	V− to V_{INL}
I_{SR}	Input Current	0 mA to 3 mA
V_{SR}	Input Voltage, Power-Down Mode	−0.3V to +6V
Shunt+	Input Voltage	(B+) −5V to B+
Shunt−	Input Voltage	B− to (B−) +5V
Data, $\overline{\text{Data}}$	Input Voltages	V− to V+ or ±6V Differential
OE, $\overline{\text{OE}}$	Input Voltages	V− to V+ or ±6V Differential
E, $\overline{\text{E}}$	Input Voltages	V− to V+ or ±6V Differential
Sense	Output Voltage	V− to V+
V_{INH}	Input Voltage	V_{INL} −0.3V to B+
V_{INL}	Input Voltage	B− to V_{INH} +0.3V
I_{OUT}	Output Current	−60 mA to +60 mA
T_J	Junction Temperature	150°C
T_A	Operating Ambient Temperature Range	−0°C to +75°C
T_{ST}	Storage Temperature	−65°C to +150°C
P_D	Power Dissipation (T_A = 25°C) (See Curves)	3.1W

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	**Test Procedure**
I	**100% production tested and QA sample tested per QA test plan QCX0002.**
II	**100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.**
III	**QA sample tested per QA test plan QCX0002.**
IV	**Parameter is guaranteed (but not tested) by Design and Characterization Data.**
V	**Parameter is typical value at T_A = 25°C for information purposes only.**

DC Electrical Characteristics

T_A = 25°C, V+ = B+ = 15V, V− = B− = −10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω, no load. Data, E, and OE from −1.6V to −0.8V. I_{SR} = 800 μA. V_{INH} = 5V, V_{INL} = −1.6V

Parameter	Description	Min	Typ	Max	Test Level	Units
I_S	(V+) + (B+), (V−) + (B−) Supply Currents		52	60	I	mA
I_S, dis	(V+) + (B+), (V−) + (B−) Supply Currents, Disabled		17	25	I	mA
I_{VINH}		−20	−3	20	I	μA
I_{VINL}		−20	2	20	I	μA
I_{DATA}		−30	−15	30	I	μA
I_{OE}	OE Input Current	−30	−14	30	I	μA
I_E	E Input Current	−20	7	20	I	μA
V_{SR}	Voltage at I_{SR} Pin	0	20	40	I	mV
I_{SHUNT+}, I_{SHUNT-}			4	7	I	mA
V_{SHUNT+}, V_{SHUNT-}	Sense Threshold at Shunts	160	200	250	I	mV
I_{SENSE}	Sense Output Currents	1	1.5	2	I	mA
V_{OS}	Output Offset, Data High, V_{INH} = 0V, V_{INL} = −1.6V	−50		50	I	mV
	Data Low, V_{INL} = 0V, V_{INH} = 5V	−100		100	I	mV

DC Electrical Characteristics — Contd.

T_A = 25°C, V+ = B+ = 15V, V− = B− = −10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω, no load. Data, E, and OE from −1.6V to −0.8V. I_{SR} = 800 μA. V_{INH} = 5V, V_{INL} = −1.6V

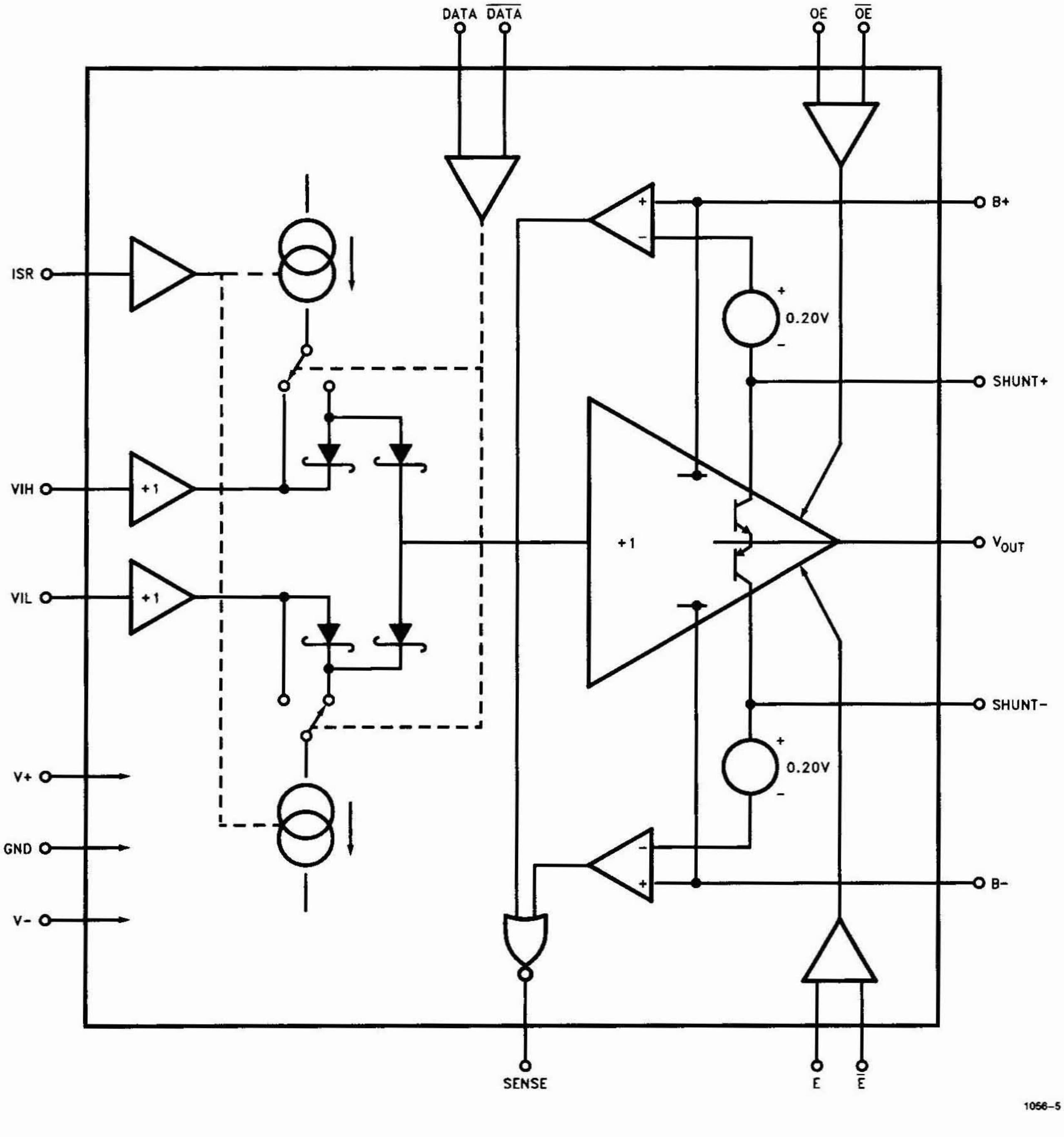
Parameter	Description	Min	Typ	Max	Test Level	Units
Eg	Gain Error Data High, V_{INH} from 0V to 5V, V_{INL} = −1.6V, No Load	−1.5	−0.6	0	I	%
	Data Low, V_{INH} = 5V, V_{INL} from −5V to 0V, No Load	−1.5	−0.6	0	I	%
NL	Gain Nonlinearity Data High, V_{INH} from 0V to 10V, V_{INL} = −1.6V, No Load		0.04		V	%
	Data Low, V_{INH} = 5V, V_{INL} from −10V to 0V, No Load		0.06		V	%
PSRR	Power Supply Rejection Ratio of V_{OUT} with Respect to B+, B−, Shunt+, or Shunt− Potential		2.2		V	mV/V
R_o, en	Output Resistance, Enabled, Il = ±20 mA	4.5	6	7.5	I	Ω
R_o, dis	Output Resistance, Output Disabled, V_O = −1.6V to −5V, EL1056C	20K	100K		I	Ω
	EL1056AC	100K	200K			
I_o, dis	Output Current, Output, Disabled, V_O = 0V	−20	5	20	I	μA
I_o, off	Output Leakage, E Low, (Shut-Down), V_O = 0V, EL1056C	−20		20	I	μA
	EL1056AC	−150		150	I	nA

AC Electrical Characteristics

T_A = 25°C, V+ = B+ = +15V, V− = B− = −10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω. R_L = 500Ω. 50Ω + 22 pF snubber included at output. Data E, and OE from −1.6V to −0.8V. I_{SR} = 800 μA. ECL swing is defined by V_{INH} = −0.8V and V_{INL} = −1.6V, CMOS swing defined by V_{INH} = 5V and V_{INL} = 0V. Propagation delay is measured at 0.4V movement of output.

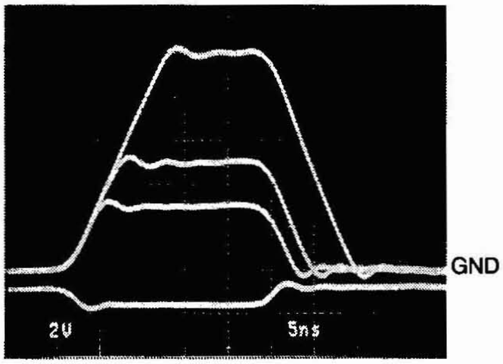
Parameter	Description	Min	Typ	Max	Test Level	Units
T_{PD}	Propagation Delay, CMOS Swing	1.0	3.0	4.5	I	ns
Dis	Propagation Delay Dispersion					
	Due to Output Edge Direction		250	450	I	ps
	From ECL to CMOS Swings		250	450	I	ps
	Due to Repetition Rate		80		V	ps
SR	Output Slew Rate, CMOS Swing, 20%–80%	0.8	1	1.2	I	V/ns
SR_{sym}	Slew Rate Symmetry		3	10	I	%
TR	Output Rise Time, ECL Swing, 20%–80%		2.2		V	ns
OS	Output Overshoot					
	CMOS Swing		190	500	I	mV
	ECL Swing (I_{SR} = 350 μA)		65		V	mV
T_{dis}	Output Disable Delay Time		4.7	6.5	I	ns
T_{en}	Output Enable Delay Time		6.0	8.5	I	ns
C_o, dis	Output Capacitance in Disable		3		V	pF
T_{off}	Power-Down Delay Time		0.5		V	μs
T_{on}	Power-On Delay Time		90		V	ns
C_o, off	Output Capacitance in Power-Down		50		V	pF
T_{sense}	Comparator Delay Time — Switching ON		1.5		V	μs
	Switching Off		0.4		V	μs

Block Diagram


DATA
DATA
OE
OE
B+
ISR
0.20V
SHUNT+
VIH
+1
VIL
+1
+1
VOUT
SHUNT−
0.20V
V+
GND
V−
B−
SENSE
E
E
1056–5

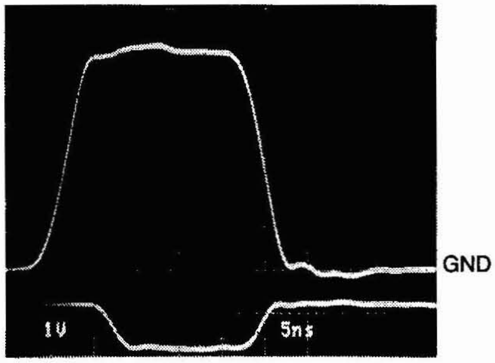
Typical Performance Curves

10V, CMOS, TTL, and ECL Outputs into 550Ω Load



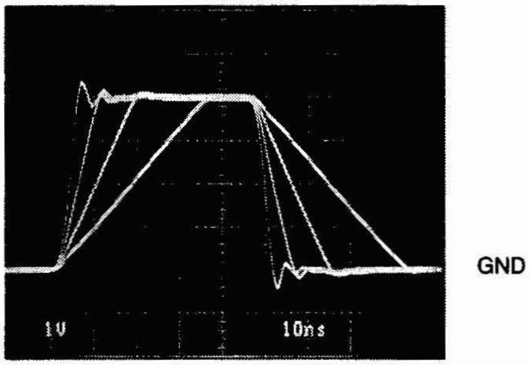
1056-6

CMOS and ECL Outputs As Seen at the End of an Unterminated Cable, Backmatched at Driver



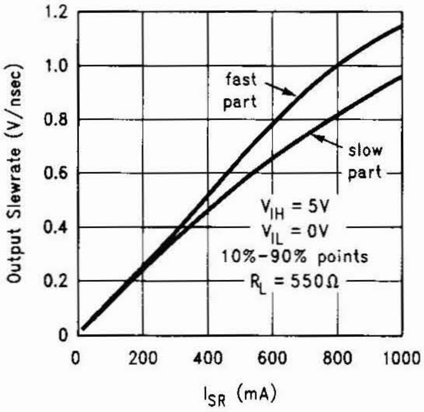
1056-7

CMOS Output at I_{SR} = 100 μA, 200 μA, 400 μA, and 1000 μA



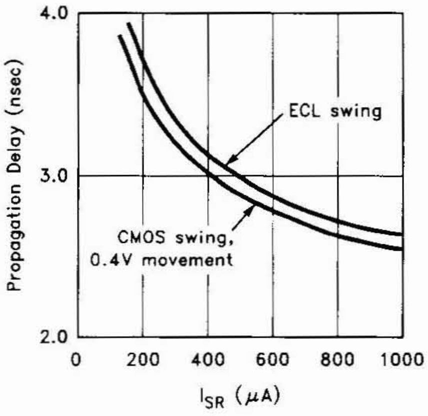
1056-8

Output Slewrate vs I_{SR} (Two Samples)



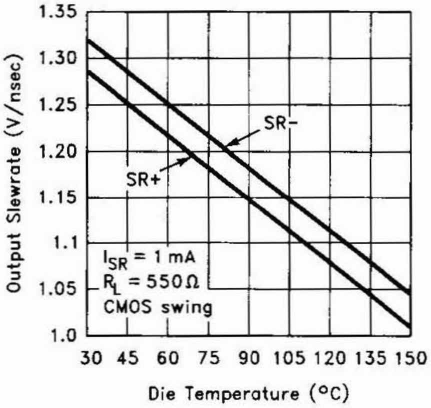
1056-9

Propagation Delay vs I_{SR}



1056-10

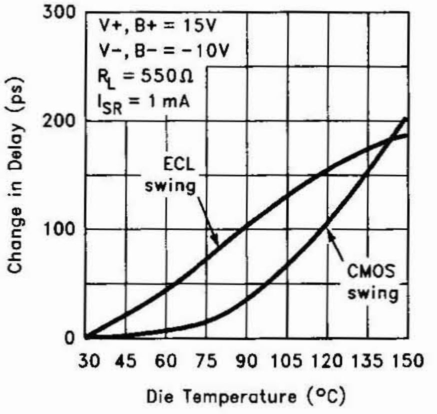
Output Slewrate vs Die Temperature



1056-11

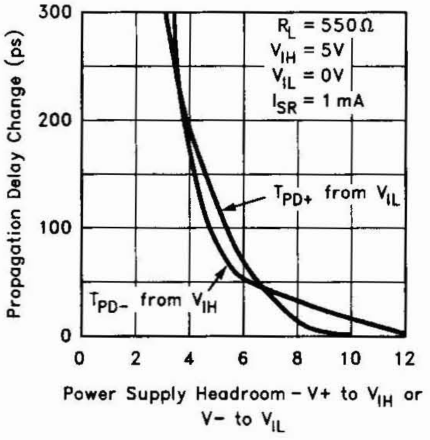
Typical Performance Curves — Contd.

Propagation Delay Change with Die Temperature



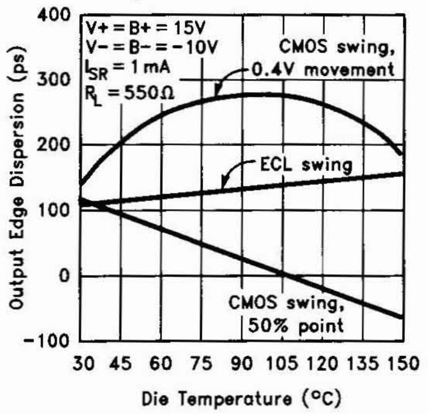
1056-12

Change in Propagation Delay with Power Supply Headroom



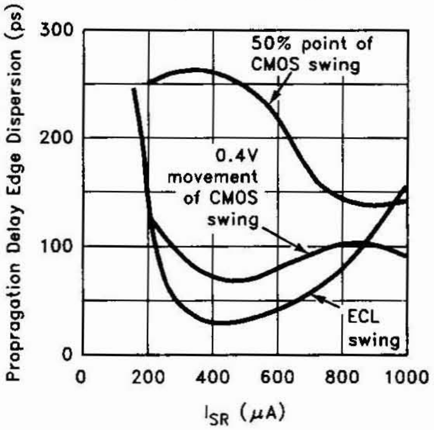
1056-13

Output Edge Dispersion vs Temperature



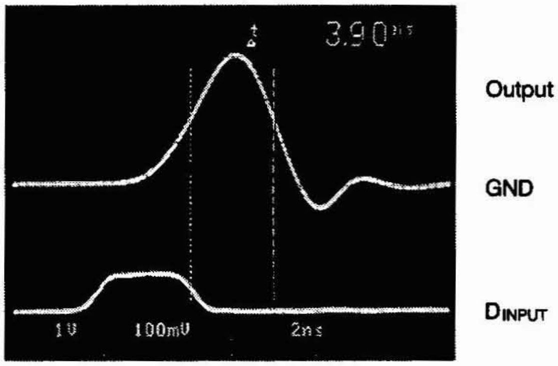
1056-14

Edge Dispersion vs I_{SR}



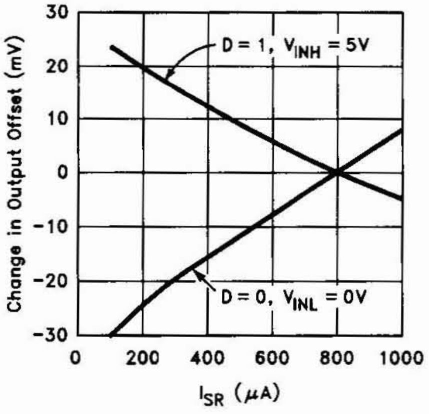
1056-15

Minimum Output Pulse Width



1056-16

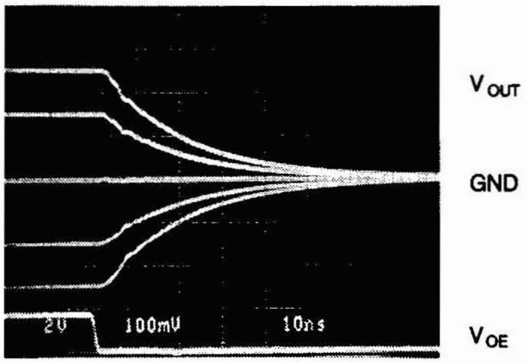
Output Offset vs I_{SR}



1056-17

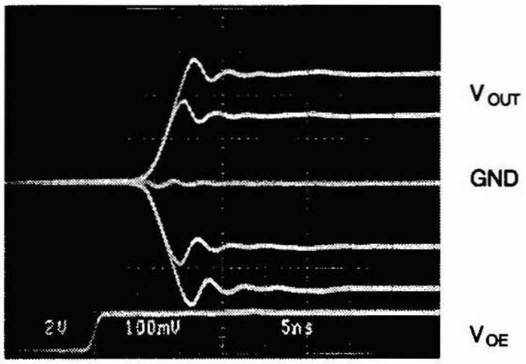
Typical Performance Curves — Contd.

Tristate Turn-off Waveforms



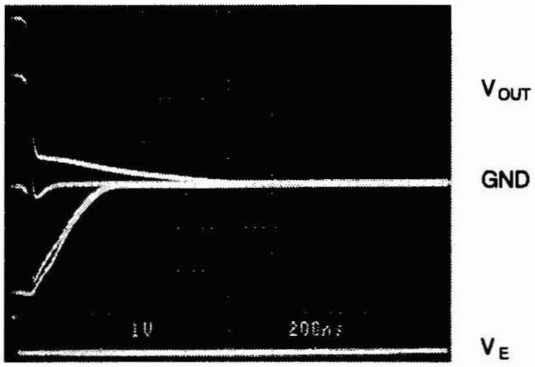
1056-18

Tristate Turn-on Waveforms



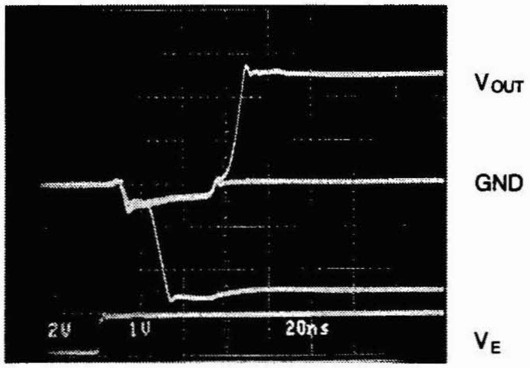
1056-19

Power-Down Disable Waveforms



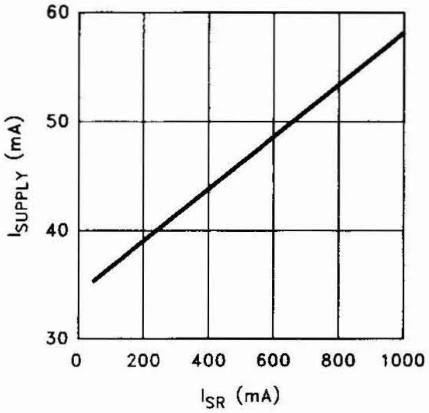
1056-20

Power-Down Enable Waveforms



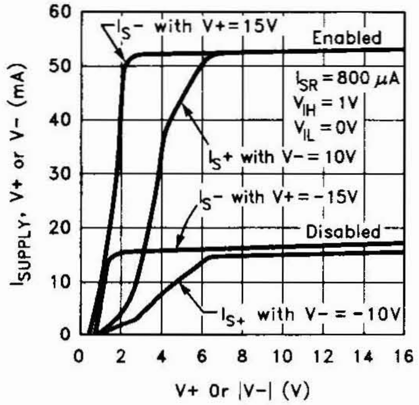
1056-21

Supply Current vs I_{SR}



1056-22

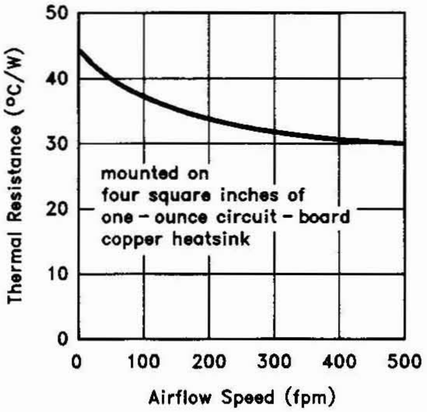
Total Supply Current vs Supply Voltage



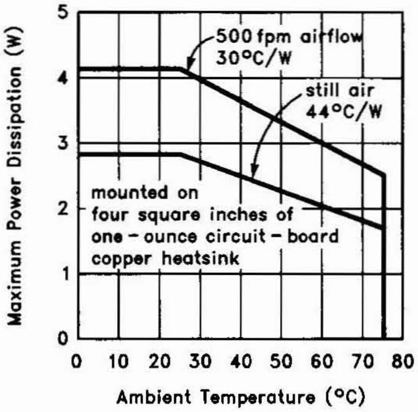
1056-23

Typical Performance Curves — Contd.

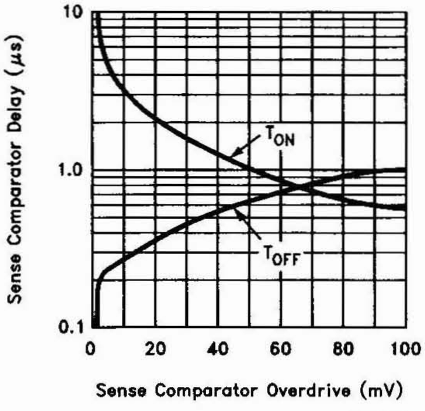
Mounted Thermal Resistance of Package vs Airflow Speed



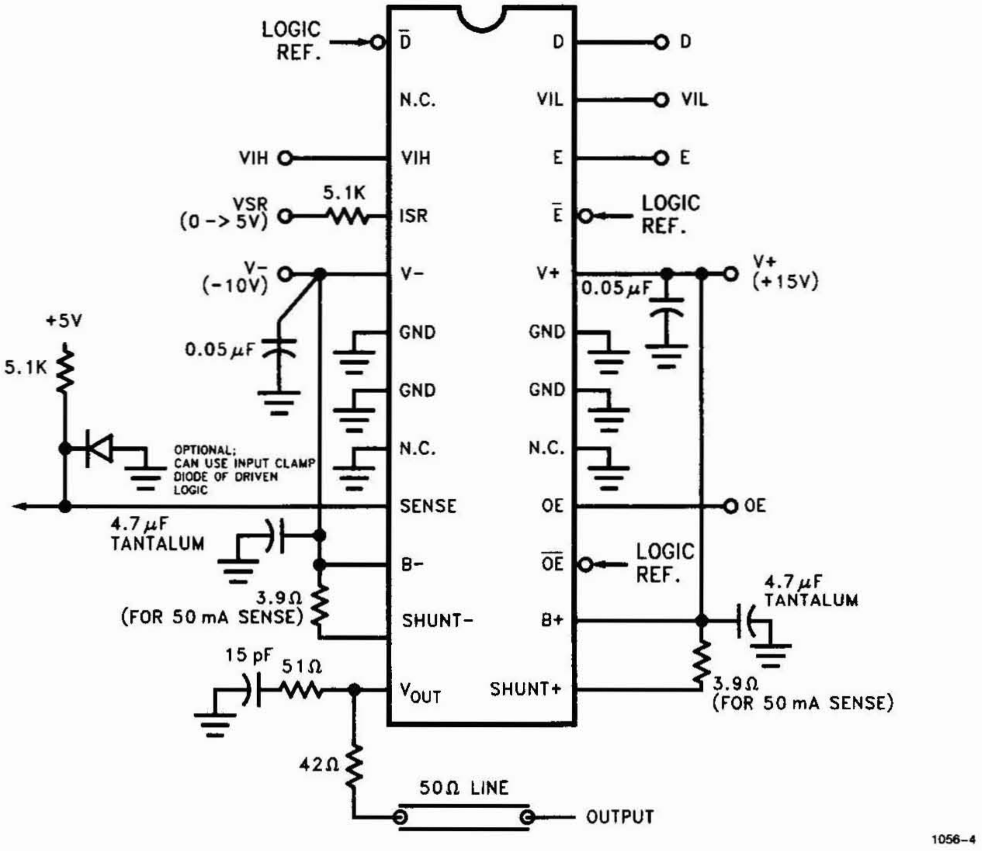
Package Power Dissipation vs Ambient Temperature



Sense Comparator Delay vs Overdrive



EL1056 Used in CMOS and TTL Systems


LOGIC REF.
D̅
D
D
N.C.
VIL
VIL
VIH
VIH
E
E
VSR (0 -> 5V)
5.1K
ISR
E̅
LOGIC REF.
V- (-10V)
V-
V+
0.05μF
V+ (+15V)
+5V
5.1K
0.05μF
GND
GND
GND
GND
N.C.
N.C.
OPTIONAL; CAN USE INPUT CLAMP DIODE OF DRIVEN LOGIC
SENSE
OE
OE
4.7μF TANTALUM
B-
O̅E̅
LOGIC REF.
3.9Ω (FOR 50 mA SENSE)
SHUNT-
B+
4.7μF TANTALUM
15 pF
51Ω
V_OUT
SHUNT+
3.9Ω (FOR 50 mA SENSE)
42Ω
50Ω LINE
OUTPUT
1056-4

Applications Information

Functional Description

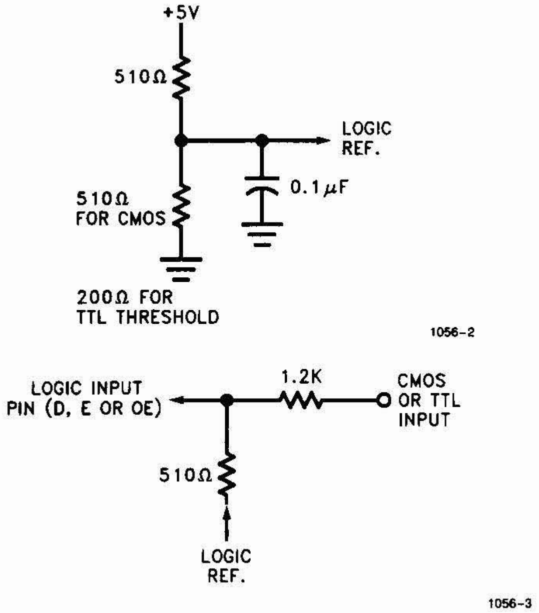
The EL1056 is a fully integrated pin driver for automatic test systems. Pin drivers are essentially pulse generators whose high and low levels can be externally programmed and accurately switched in time, as well as incorporating an output switch to disconnect the driver from a measurement bus. Additionally, the EL1056 has programmable slewrate.

Control Voltage Inputs

The analog level inputs are named V_{INH} and V_{INL}, and the output replicates them as controlled by logic inputs. The analog inputs are buffered and have bandwidths of 35 MHz and slewrates of 25V/µs. For full slewrate, 4V of headroom should be given to the inputs, that is V_{INH} should be 4V less than V+ or B+, and V_{INL} should be 4V more positive than V− or B−. At lower slewrates (I_{SR} = 500 µA or less), 3V of headroom will suffice. Insufficient headroom causes distorted output waveforms or delay errors in output transitions. V_{INH} may be lower in voltage than V_{INL}, but the output will not follow the control logic correctly. Furthermore, V_{INH} should be 200 mV more positive than V_{INL} (the minimum output amplitude) for accurate switching.

Logic Inputs

The logic inputs are all differential types, with both NPN and PNP transistors connected to each terminal. They are optimized for differential ECL drive, which optimizes + to − edge delay time matching. Larger logic levels can introduce feedthrough glitches into the output waveform. For CMOS input logic levels, an ECL output waveform will show feedthrough when the input risetime is shorter than 8 ns, differential or single-ended. CMOS output swings show less aberration, and the EL1056 can tolerate a 4 ns single-ended risetime or 2 ns risetime for differential inputs. Attenuating CMOS or TTL inputs to 1 Vp-p will eliminate all logic feedthrough as shown in Figure 1.



Alternate Logic Interface
Figure 1

Slewrate Control

The slewrate is controlled by the I_{SR} input. This is a current input and scales the output slewrate by a nominal 1.25V/ns/mA. The slewrate maintains calibration and symmetry to at least as slow as 0.2V/ns. The practical upper end of I_{SR} is 1 mA, and supply current increases with increasing I_{SR}.

The I_{SR} control can be used to adjust individual pin drivers to a system standard, by adjusting the value of its series resistor. Slewrate can also be slowed to reduce output ringing and crosstalk.

With ECL output swings, there is not enough voltage excursion to incur slewrate delays to 50% logic threshold. The risetime, delays, and dispersions do not degrade with reasonably reduced I_{SR}, and overshoot will reduce markedly. An I_{SR} of 350 µA produces a very good ECL output, and driver dissipation is also reduced.

Applications Information — Contd.

The I_{SR} pin is connected to the emitter of a PNP transistor whose base is biased a diode below ground (see Figure 2). Thus, the I_{SR} input looks like a low impedance for positive input currents, and is biased close to ground. A protection diode absorbs negative currents, and the input PNP will not conduct. In power-down mode, the PNP releases its current sink and the external circuit must not present more than 6V to the disabled I_{SR} input, or emitter-base damage to the NPN will occur within the driver. A signal diode or zener can be used to clamp the I_{SR} input for positive input voltages if the voltage on the I_{SR} resistor is potentially greater than 6V when the driver is in power-down mode.

Output Stage-Tristate Mode

In tristate mode (OE low) the output transistors have their emitter-base junctions reverse-biased by a diode voltage. This turn-off voltage is in fact provided by an internal buffer whose input is connected to the output pin (see Figure 3). Transistors Q1–Q4 form the output buffer in normal mode. The tristate mode buffer Q5–Q8 replicates externally impressed voltages from the output pin onto the internal schottky switch node. They also turn off Q1–Q4 by a reverse diode voltage between bases and emitters, effectively bootstrapping the internal voltages, so that no transistor's base-emitter junction is reverse-biased by a damaging potential. Another benefit is that the capacitance seen at the output in tristate mode is reduced.

Because the tristate buffer's input is connected to the output terminal, the output is quite "alive" during tristate. For instance, the input bias current of the buffer is seen as the tristate "leakage", and its variation with applied voltage becomes tristate input impedance.

The tristate input current is like a current source, and it can drag an output to unpredictable voltages. It is not a danger to connect a tristated output that has drifted to, say, −6V to a logic pin of a device to be tested. The tristate output current will simply comply with whatever voltage the connected part normally establishes.

The tristate input impedance is also quite active over frequency. The output can oscillate when presented with resonant or inductive impedances. To prevent this, a snubber should be connected from output to ground, consisting of a resistor in series with a small capacitor. The snubber can also reduce the reflections of the coaxial line when driven from the far end, since the line appears to have an open termination during tristate. Typical values for the resistor are 50Ω to 75Ω, and 12 pF to 22 pF for the series capacitor. The effect of the snubber is to "de-Q" resonances at the output.

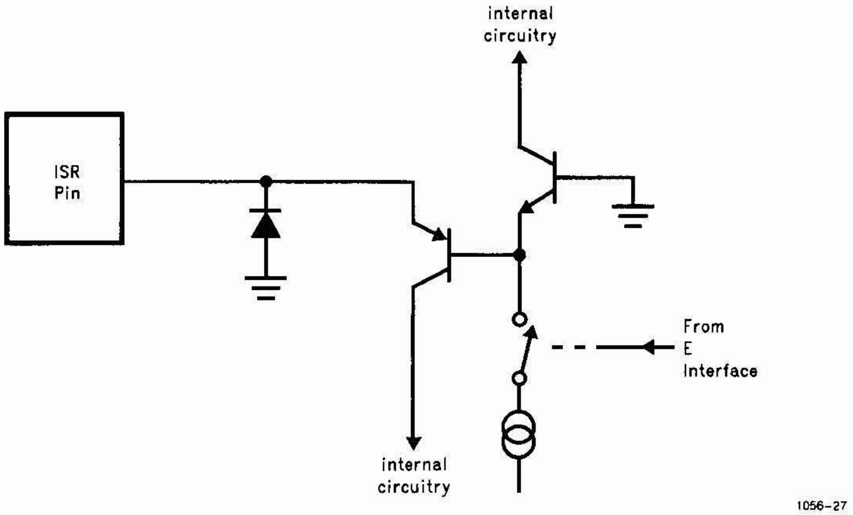


Figure 2. I_{SR} Pin Circuitry

Applications Information — Contd.

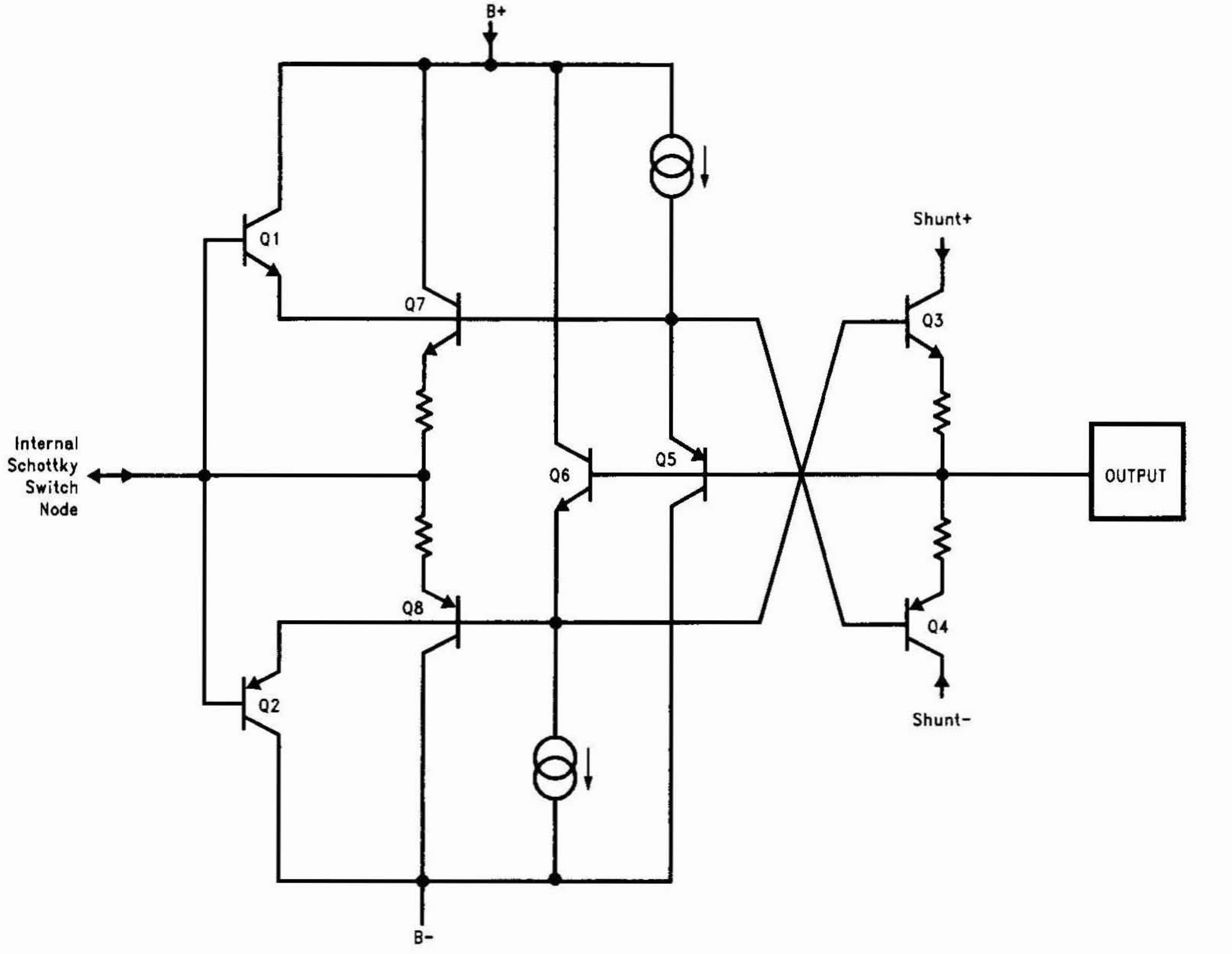


Figure 3. Output Stage Circuit in Tristate Mode

Output Stage-Normal Mode

Capacitive loads can cause the output stage to ring. Little ringing occurs for loads less than 25 pF, but substantial ringing for more than 40 pF. Terminated transmission lines cause no ringing, and actually suppress it as a snubber does. A terminated line draws heavy DC current, however, and greatly raises dissipation.

Driving a back-terminated line also causes little ringing and does not cause DC dissipation. The series matching resistor between the EL1056 output and a back-terminated line also serves to isolate the driver from capacitive loads and short-circuits. The slewrate of the driver slows by about 10% when driving a 50Ω back-matched line, as seen at the end of the line. The snubber can be on either side of the back-match resistor. When placed on the line side it creates a high-frequency termination for the line when the driver is tristated, but it slows the output small-signal risetime by about 10% (although not slew-rate). When placed on the driver side of the back-match resistor, no speed reduction occurs in normal mode but the cable is more poorly terminated in tristate.

The transient currents that occur when driving capacitive or back-matched loads can be very high, approaching 100 mA. The driver is capable of outputting a peak of 140 mA, but long-term

Applications Information — Contd.

load currents must be limited to 60 mA. Short-circuits can rapidly destroy the EL1056, although the part will survive for 20 ms periods. If there is the possibility of output load fault the overcurrent sense circuitry should be used to signal alarm to the controlling system, which should ultimately activate the tristate mode to relieve the output stage. Driving large static currents also raises internal dissipation and should be part of the thermal budget.

The collectors of the output transistors are connected to the Shunt terminals, and the output stage drivers' collectors are connected to the B+ and B− terminals (see Figure 4). The Shunt lines can have transient currents as high as 120 mA and are separated from the V+ and V− terminals to keep switching noise out of the control and logic circuitry. A bypass capacitor should be connected to the B+ and B− terminals.

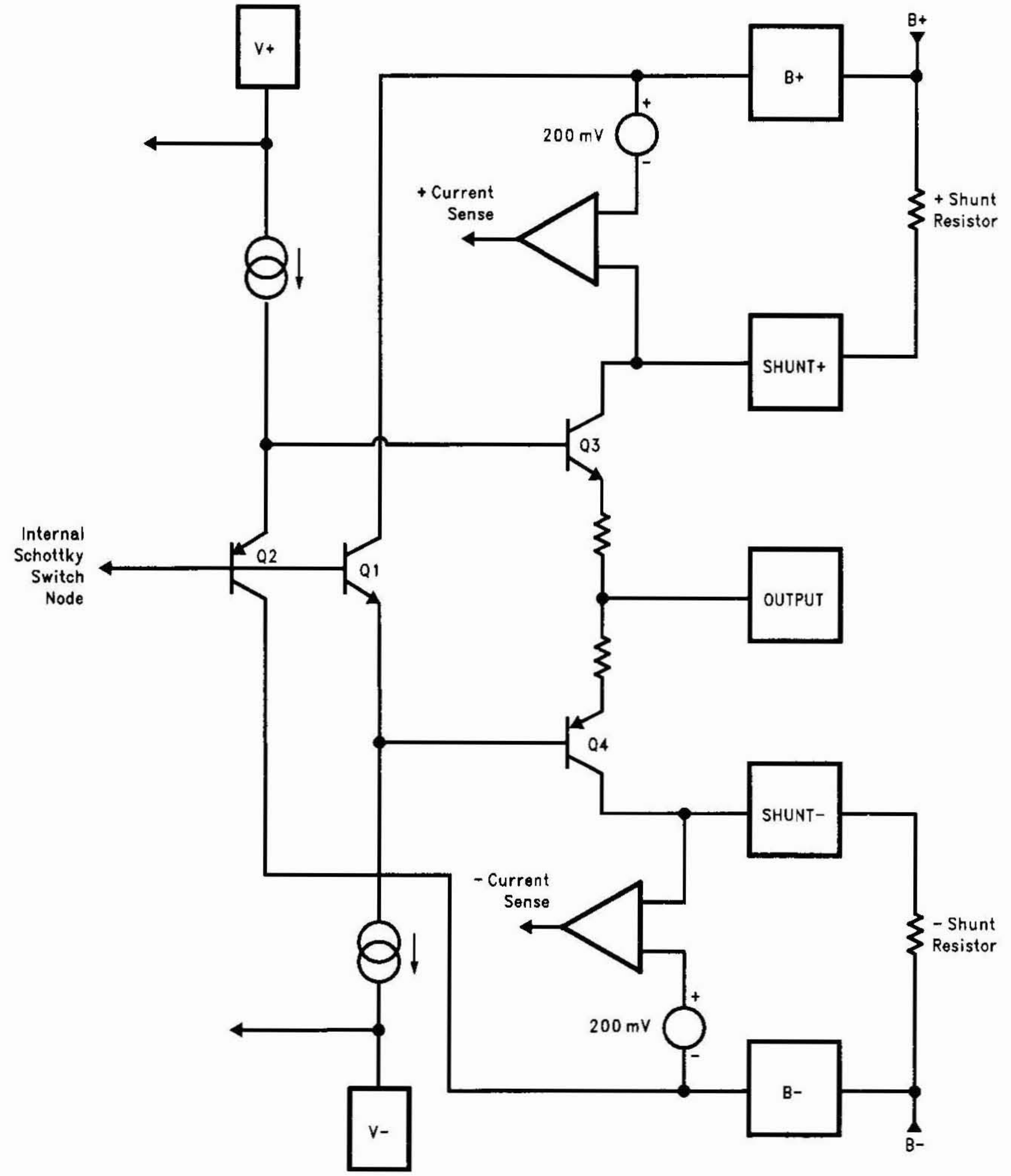

V+
B+
B+
200 mV
+
−
+ Current
Sense
+ Shunt
Resistor
SHUNT+
Q3
Internal
Schottky
Switch
Node
Q2
Q1
OUTPUT
Q4
SHUNT−
− Current
Sense
− Shunt
Resistor
200 mV
+
−
B−
B−
V−
1056-29

Figure 4. Output Stage in Normal Mode

Applications Information — Contd.

Overcurrent Protection

The sense comparators are available to alert the test system's controller that the driver is outputting excessive current. Shunt resistors are connected from B+ to Shunt+ and B− to Shunt−. When the internal comparators sense more than a nominal 200 mV drop on the shunts, they cause a 1.5 mA current to be sunk from the Sense terminal. The comparators are of "slow attack, fast decay" design, so that transient load currents will not trigger a sense output; only a sustained overcurrent will.

The sense resistors must not be inductive, and the skin resistance of long, narrow connections between Shunt and B+ or B− can cause transient voltages that produce output overshoot (but not ringing).

The Sense output is simply a switched current source connected to V−. It can be used to interface to CMOS, TTL, or ECL inputs. For CMOS and TTL, it can be connected to a pull-up resistor to +5V of 10K value. This establishes a logic high value, and a clamp diode (internal to TTL) establishes a low level of −0.6V. For ECL, a gate should be available to provide a static logic high level. An 820Ω pull-up resistor is wired to that output. The logic low will be more negative than is usual for ECL, but this will cause no problem. In all cases, multiple Sense outputs may be connected together from many drivers to effect a wired-or function.

A further protection scheme is to provide a series resistor from B+ to V+ and B− to V−. The resistor serves to limit the output fault current by allowing B+ and B− voltages to sag under heavy load. This also reduces the dissipation on the output transistors for valid loads. Because B+ and B− are separately bypassed, these voltages will sustain under transient loads and dynamics will not be affected.

Output Accuracy

The accuracy of the output voltage depends on several factors. The first is the gain error from V_{INH} or V_{INL} to the output, unloaded. The gain error is nominally −0.6%, and has a few tenths of a percent variation between parts. The second is supply rejection. If the B+, B−, Shunt+, or Shunt− voltages are different from those used by Elantec to test the part, there will be about 2.2 mV systematic shift in output offset per volt of supply variation. The V+ and V− supplies have much less influence on output error. Finally, there is a random V_{OS} error as specified in the data table.

Of course, the finite output impedance of the EL1056 will cause additional output error when the driver is loaded.

Power-Down

The EL1056 incorporates a power-down feature that drastically reduces power consumption of an unused driver and also drops the output leakage current to nanoamperes ("A" grade only). The output is not a low capacitance in this mode, however, and transients driven from the cable can momentarily turn on the output transistors. Power-down is intended to allow the switching of accurate DC meters onto the bus without having to relay out the driver's leakage current. It takes about 40 μs for the output leakage to sag to nanoamperes, but this is still much faster than relays or voltmeters.

Power-down is controlled by the E and $\overline{E}$ differential inputs. There is no problem with logic amplitude or slewrate, and input resistor networks are not needed.

Power Down — Contd.

Supply and Input Bypassing

The V+, B+, V−, and B− leads should be bypassed very closely with 0.1 μF capacitors, preferably chip type. There should be a wide ground plane between bypasses, and this can be the heatsink copper. It is wise to also have a 4.7 μF tantalum bypass capacitor within a couple of inches to the driver.

The logic inputs are active device bases, and can oscillate if presented with inductive lines. A local resistor of 1000Ω or less to ground will suffice in de-Q'ing any resonance. A 100 pF or larger capacitor can also serve as a bypass.

Thermal Considerations

The package of the EL1056 includes two fused leads on each side which are connected to the internal die mounting metal. Heat generated in the die flows through the mounting pad to the fused leads, and then to the circuit-board copper, achieving a thermal resistance to air around 40°/W. Characterization curves show the thermal resistance versus airflow rate. Consult the EL1056 Demonstration Board literature for a suggested board pattern. Note that thicker layers of copper than we used improves the thermal resistance further, to a limit of 22°C/W for an "infinite heatsink" directly soldered to the fused leads.

As a practical limit, the die temperature should be kept to 125°C rather than the allowable 150°C to retain optimum timing accuracies.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2018C

Fast, High Voltage Comparator with Transparent Latch

Features

- Fast response time—20 ns
- Wide input differential voltage range—24V to ±15V supplies
- Precision input stage—V_{OS} = 1 mV
- Low input bias current—I_B = 100 nA
- Low input offset current—I_{OS} = 30 nA
- ±4.5V to ±18V supplies
- 3-State TTL and CMOS compatible output
- No supply current glitch during switching
- High voltage gain—40 V/mV
- 50% power reduction in shutdown mode
- Input and latch remain active in shutdown mode
- P/N compatible with industry standard comparators

Applications

- Analog to digital converters
- ATE pin receiver
- Precision crystal oscillators
- Zero crossing detector
- Window detector
- Pulse width modulation generator
- "Go/no-go" detector

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2018CN	−40°C to +85°C	P-DIP	MDP0031

General Description

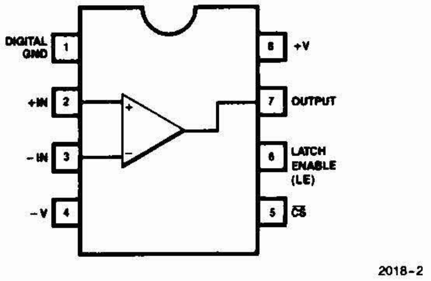
The EL2018 represents a quantum leap forward in comparator speed, accuracy and functionality. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures the part maintains speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and latch remain active.

Not Recommended For New Designs

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see QRA1: *Elantec's Processing-Monolithic Products.*

Connection Diagram

8-Pin Plastic DIP



Top View

EL2018C

Fast, High Voltage Comparator with Transparent Latch

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V
V_{IN}	Input Voltage	$+V_S$ to $-V_S$
ΔV_{IN}	Differential Input Voltage	Limited only by Power Supplies
I_{IN}	Input Current (Pins 1, 2 or 3)	±10 mA
I_{INS}	Input Current (Pins 5 or 6)	±5 mA
P_D	Maximum Power Dissipation (Note 4—See Curves)	1.25W
I_{OP}	Peak Output Current	50 mA
I_O	Continuous Output Current	25 mA
T_A	Operating Temperature Range	−40°C to +85°C
T_J	Operating Junction Temperature Plastic DIP Package	 150°C
T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage (Note 1) V_{CM} = 0V, V_O = 1.4V	25°C		1.0	5	I	mV
		T_{MIN}, T_{MAX}			7	III	mV
I_B	Input Bias Current V_{CM} = 0V, Pin 2 or 3	25°C		100	400	I	nA
		T_{MIN}, T_{MAX}			600	III	nA
I_{OS}	Input Offset Current V_{CM} = 0V	25°C		30	150	I	nA
		T_{MIN}, T_{MAX}			250	III	nA
CMRR	Common Mode Rejection Ratio (Note 2)	25°C	85	105		I	dB
		T_{MIN}, T_{MAX}	80			III	dB
PSRR	Power Supply Rejection Ratio (Note 3)	25°C	85	100		I	dB
		T_{MIN}, T_{MAX}	77			III	dB
V_{CM}	Common Mode Input Range	25°C	±12	±13		I	V
		T_{MIN}, T_{MAX}	±12			III	V
A_V	Voltage Gain V_{OUT} = 0.8V to 2.0V	25°C	15	40		I	V/mV
		T_{MIN}, T_{MAX}	10			III	V/mV
V_{OL}	Output Voltage Logic Low I_{OL} = 0 mA to 8 mA	25°C	−0.05	0.15	0.4	I	V
		T_{MIN}, T_{MAX}	−0.1		0.4	III	V

DC Electrical Characteristics V_S = ±15V unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{oh}	Output Voltage Logic High $V_S = \pm 15V$	25°C	3.5	4.0	4.65	I	V
	$V_S = \pm 15V$	T_{MIN}, T_{MAX}	3.5		4.65	III	V
	$V_S = \pm 5V$	25°C	2.4			I	V
	$V_S = \pm 5V$	T_{MIN}	2.4			III	V
	$V_S = \pm 5V$	T_{MAX}	2.4			III	V
V_{odis1}	V_{OUT} Range, Disabled, $I_{OL} = -1$ mA $V_S = \pm 15V$	25°C	4.65			I	V
	$V_S = \pm 15V$	T_{MIN}, T_{MAX}	4.65			II	V
	$V_S = \pm 5V$	25°C		3.5		V	V
V_{odis2}	V_{OUT} Range, Disabled, $I_{OL} = 1$ mA $V_S = \pm 5V$ to $\pm 15V$	ALL	−0.3	−1		II	V
V_{inh}	LE or $\overline{CS}$ Inputs Logic High Input Voltage	25°C	2.0			I	V
		T_{MIN}, T_{MAX}	2.2			III	V
V_{inl}	LE or $\overline{CS}$ Inputs Logic Low Input Voltage	25°C			0.8	I	V
		T_{MIN}, T_{MAX}			0.8	III	V
I_{in}	LE or $\overline{CS}$ Inputs Logic Input Current $V_{IN} = 0V$ to $5V$	25°C			±200	I	μA
		T_{MIN}, T_{MAX}			±300	III	μA
I_{s+en}	Positive Supply Current Enabled	25°C		8.4	12	I	mA
		T_{MIN}, T_{MAX}			13	III	mA
I_{s+dis}	Positive Supply Current Disabled	25°C		4.7	6	I	mA
		T_{MIN}, T_{MAX}			7	III	mA
I_{s-en}	Negative Supply Current Enabled	25°C		13.0	17	I	mA
		T_{MIN}, T_{MAX}			18	III	mA
I_{s-dis}	Negative Supply Current Disabled	25°C		5.0	6.5	I	mA
		T_{MIN}, T_{MAX}			6.5	III	mA

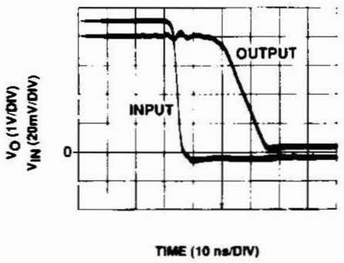
AC Electrical Characteristics $V_S = \pm 15V, T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level	Units
T_{pd}	Propagation Delay, 5 mV Overdrive		20	40	III	ns
T_s	Setup Time		6	12	IV	ns
T_h	Hold Time		−2	0	IV	ns
T_{un}	Unlatch Time		23	40	IV	ns
T_{mpw}	Minimum Clock Pulse Width		12		V	ns
T_{en}	Output 3-State Enable Delay		40	70	IV	ns
T_{dis}	Output 3-State Disable Delay		150	300	IV	ns

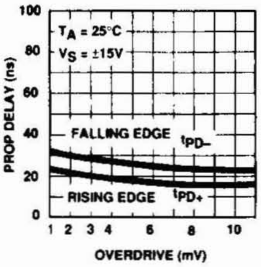
Note 1: $V_{OUT} = 1.4V$.
Note 2: $V_{CM} = 12V$ to $-12V$.
Note 3: $V_S = \pm 5V$ to $\pm 15V$.
Note 4: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

Typical AC Performance Curves

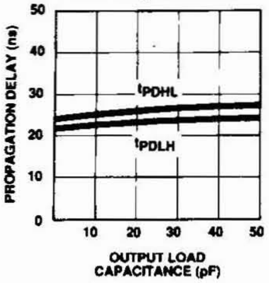
Propagation Delay (−) 5 mV Overdrive



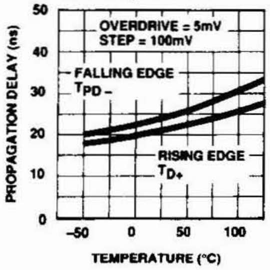
Propagation Delay vs Overdrive



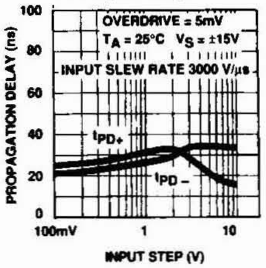
Propagation Delay vs Load Capacitance



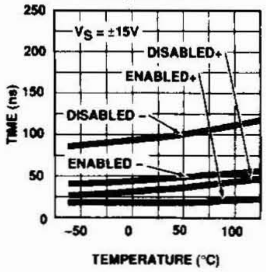
Propagation Delay vs Temperature



Propagation Delay vs Input Step



Enabled/Disabled Time vs Temperature



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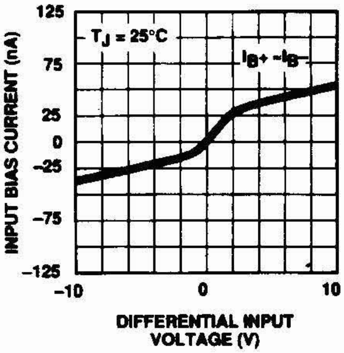
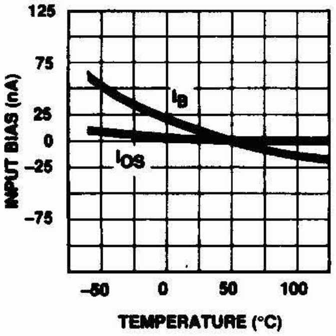
Typical AC Performance Curves — Contd.

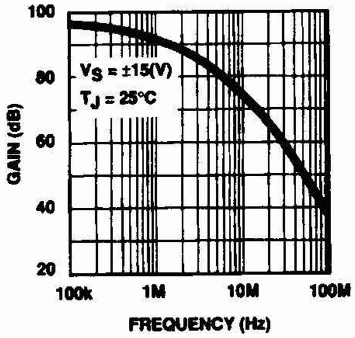
Input Bias Current vs Differential Input Voltage



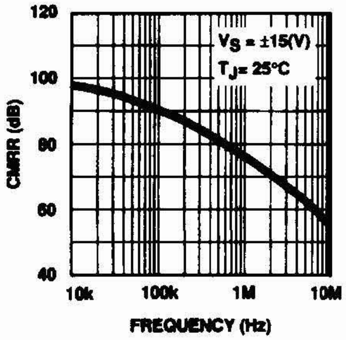
Input Bias Current vs Temperature



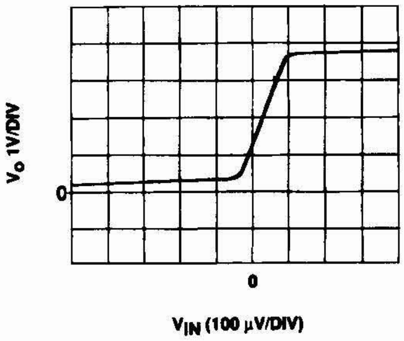
Open-Loop Gain vs Frequency



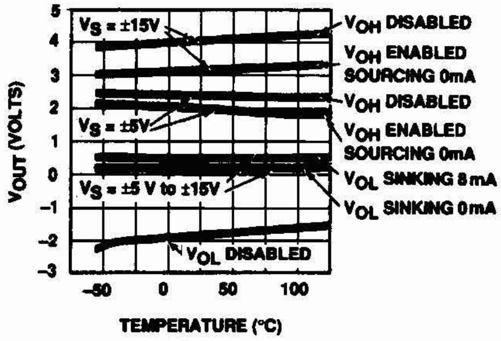
CMRR vs Frequency



V_O/V_I Transfer Characteristic



V_{OUT} vs Temperature



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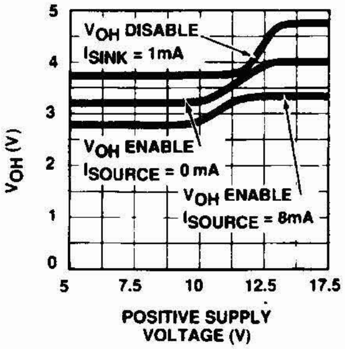
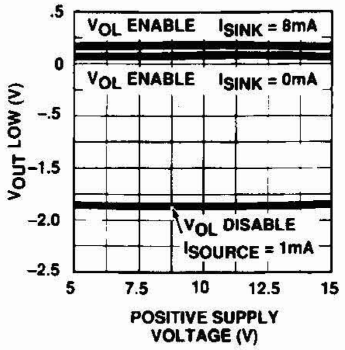
Typical Performance Curves — Contd.

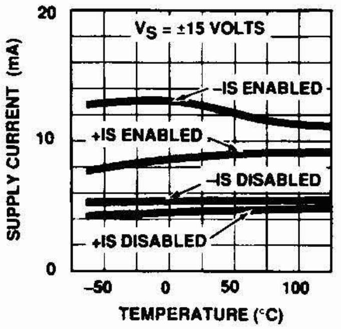
V_{OH} vs Positive Supply Voltage



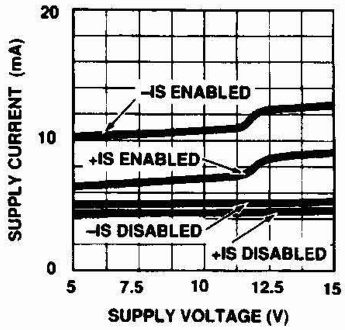
V_{OL} vs Positive Supply Voltage



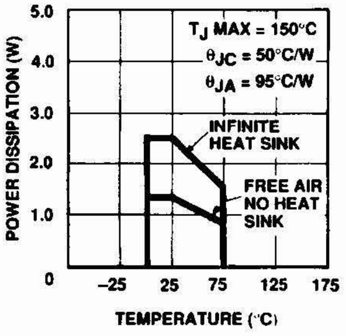
Supply Current vs Temperature



Supply Current vs Supply Voltage

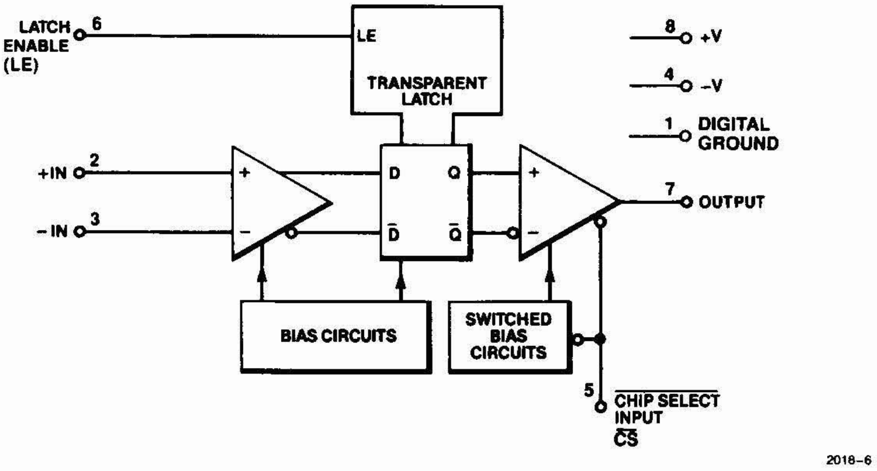


8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2018-5

Block Diagram



Function Table

Inputs (time n − 1)				Internal Q	Notes	Output
+IN	−IN	$\overline{CS}$	LE			
+	−	L	L	H	Normal Comparator Operation	H
−	+	L	L	L		L
+	−	H	L	H	Internal Normal Comparator Operation	High Z
−	+	H	L	L	Output Power Down Mode	High Z
X	X	L	H	Qn − 1	Data Retained in Latch	Qn − 1
X	X	H	H	Qn − 1	Data Retained in Latch Power Down Mode	High Z

Application Hints

Device Overview

The EL2018 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Dielectric Isolation Process, which is immune to power sequencing and latch up problems.

Power Supplies

The EL2018 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.1 μF monolithic ceramic recommended) close to the power supply leads. Good ground plane construction techniques enhance stability, and the lead from pin 1 to ground should be short.

Front End

The EL2018 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V). The transfer function of the EL2018 is linear, and the output is stable when in the linear region.

The large common mode range (±12V minimum) and differental voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

Application Hints — Contd.

Recovery from Large Overdrives

Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device.

Input Slew Rate

All comparators have input slew rate limitations. The EL2018 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators.

Latch

The EL2018 contains a "transparent" latch. A "transparent" latch acts as an amplifier when the LE input is low and it "latches" and holds the value it had just before the LE transition from low to high.

It is possible to make an oscillation resistant design by putting a short duration "0" on the LE input whenever you wish to make a comparison. This gates the comparator on only for a brief instant, long enough to compare, but not long enough to oscillate. The minimum duration of this pulse is specified by the minimum clock width parameter in the AC electrical tables.

The $\overline{\text{CS}}$ input may be left floating and still produce a guaranteed logic "0" input (active). Floating the LE input will normally produce a logic "0" input also, but operation is not guaranteed.

Proper RF technique suggests that these inputs be grounded or pulled to ground if they are not used.

Output Stage

The output stage of the EL2018 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2018 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature

The EL2018 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in a large ATE system where there may be 1000 comparators, but only 10% are in use at any one time.

Due to the power saving feature and linear output stage, the EL2018 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2018 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

System Design Considerations

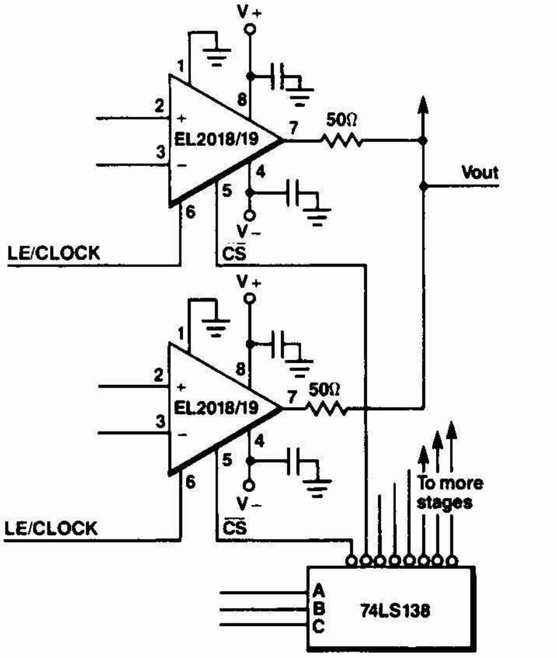
The most common problem users have with high speed comparators is oscillations due to output to input feedback. This can be avoided by using a ground plane, proper supply bypassing, and routing the inputs and outputs away from each other. Since the EL2018 has a gain bandwidth product of about 40 GHz, layout and bypassing are important to a successful system design. A unique alternative to the EL2018 is the EL2019, with its edge triggered master/slave flip flop.

Device Functions

The various operating states of the EL2018 are described in the function table on page 7.

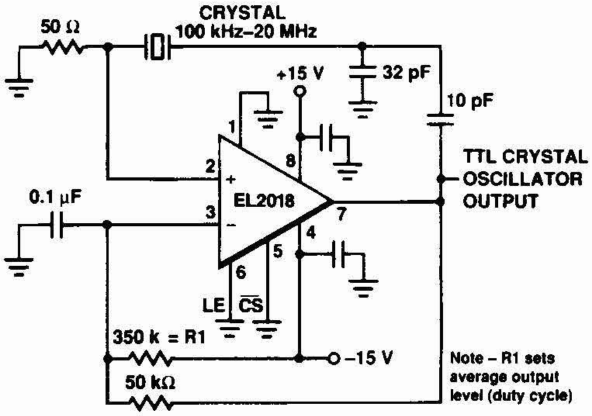
Typical Applications

Using the Power Down/ 3-State Feature


V+
1
8
2
+
EL2018/19
7
50Ω
3
−
4
Vout
5
6
V−
LE/CLOCK
CS
V+
1
8
2
+
EL2018/19
7
50Ω
3
−
4
5
6
V−
To more stages
LE/CLOCK
CS
A
B
C
74LS138

2018-7

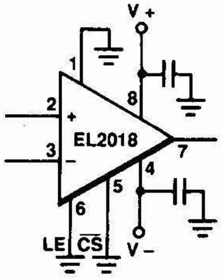
Series Resonant Crystal Oscillator


50 Ω
CRYSTAL
100 kHz–20 MHz
+15 V
32 pF
10 pF
1
8
TTL CRYSTAL OSCILLATOR OUTPUT
0.1 μF
2
+
EL2018
3
−
7
4
5
6
LE
CS
350 k = R1
−15 V
50 kΩ

Note – R1 sets average output level (duty cycle)

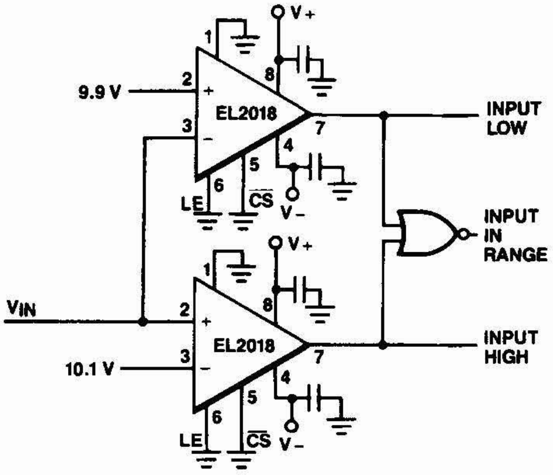
2018-8

Using the EL2018 in the Transparent Mode (Latch Not Used)


V+
1
8
2
+
EL2018
7
3
−
4
5
6
LE
CS
V−

2018-9

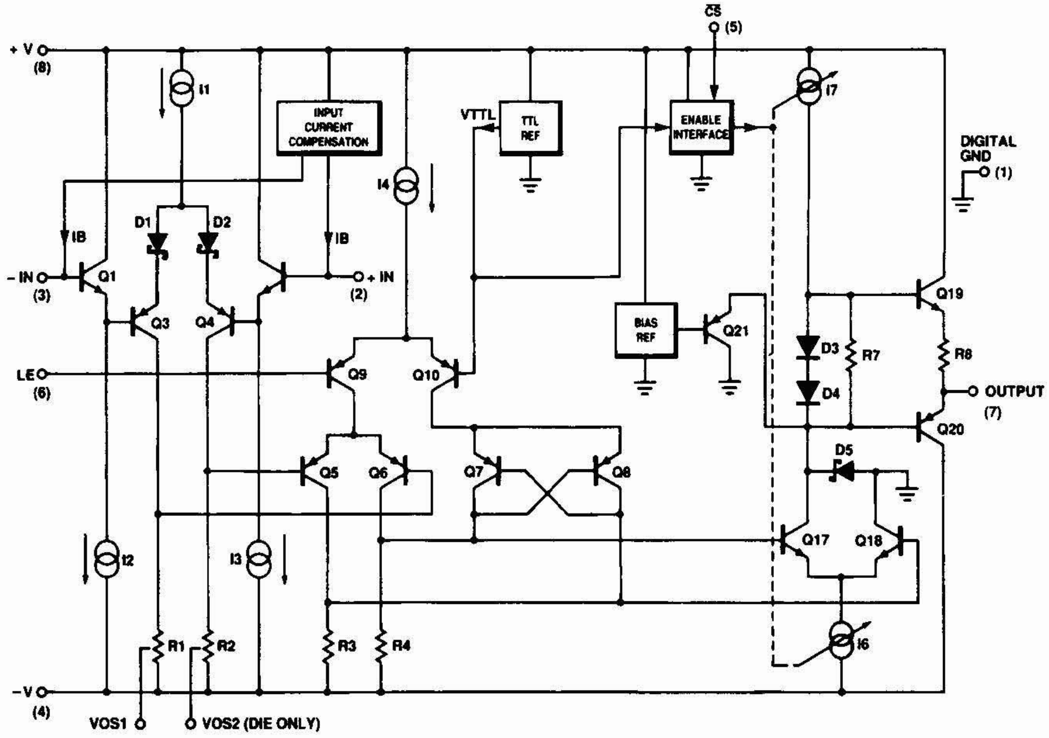
A Wide Input Range Window Comparator


V+
1
8
9.9 V
2
+
EL2018
INPUT LOW
3
−
7
4
5
6
LE
CS
V−
INPUT IN RANGE
V+
1
8
VIN
2
+
EL2018
INPUT HIGH
10.1 V
3
−
7
4
5
6
LE
CS
V−

2018-10

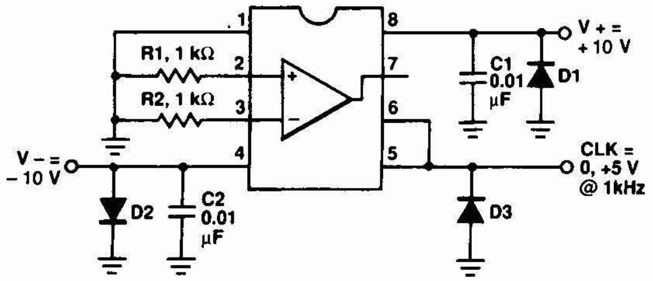
V_{IN} Range +12V to −12V with $V_S = \pm 15V$

Equivalent Schematic


+V (8)
I1
INPUT CURRENT COMPENSATION
VTTL
TTL REF
C̄S̄ (5)
ENABLE INTERFACE
I7
DIGITAL GND (1)
I4
IB
D1
D2
IB
-IN (3)
Q1
Q3
Q4
+IN (2)
BIAS REF
Q21
Q19
D3
R7
R8
D4
OUTPUT (7)
Q20
LE (6)
Q9
Q10
D5
Q5
Q6
Q7
Q8
Q17
Q18
I2
I3
R1
R2
R3
R4
I6
-V (4)
VOS1
VOS2 (DIE ONLY)

2018-11

Burn-In Circuit


1
2
3
4
8
7
6
5
R1, 1 kΩ
R2, 1 kΩ
+
−
V+ = +10 V
C1 0.01 µF
D1
V− = −10 V
D2
C2 0.01 µF
CLK = 0, +5 V @ 1kHz
D3

2018-12

Pin numbers are for DIP packages.
All packages use the same schematic.

EL2018 Macromodel

```
* Connections:   +input
*                |     -input
*                |     |     +V
*                |     |     |     -V
*                |     |     |     |     LE
*                |     |     |     |     |     CS
*                |     |     |     |     |     |    output
*                |     |     |     |     |     |    |
.subckt M2018    2     3     8     4     6     5    7
*
* Input Stage
*
i1 8 10 700µA
r1 13 4 1K
r2 14 4 1K
q1 8 3 11 qn
q2 8 2 12 qn
q3 13 11 10 qp
q4 14 12 10 qp
i2 11 4 200µA
i3 12 4 200µA
*
* 2nd Stage & Flip Flop
*
*i4 8 24 700µA
i4 8 24 1mA
q9 22 6 24 qp
q10 18 17 24 qp
v1 17 0 2.5V
q5 15 14 22 qp
q6 16 13 22 qp
r3 15 4 1K
r4 16 4 1K
q7 16 15 18 qp
q8 15 16 18 qp
*
* Output Stage
*
i7 8 35 2mA
s1 35 20 5 0 sw
d2 35 8 ds
i6 26 34 5mA
s2 34 4 5 0 sw
d3 34 26 ds
q19 8 20 21 qn 2
q20 4 19 7 qp 2
r8 21 7 60
r7 20 19 4K
q17 19 16 26 qn 5
q18 0 15 26 qn 5
q22 20 20 30 qn 5
```

EL2018 Macromodel — Contd.

```
q23 19 19 30 qn 8
d1 0 19 ds
q21 0 17 19 qp
*
* Power Supply Current
*
ips 8 4 4mA
*
* Models
*
.model qn npn (is = 2e − 15 bf = 400 tf = 0.05nS cje = 0.3pF cjc = 0.2pF ccs = 0.2pF)
.model qp pnp (is = 0.6e − 15 bf = 60 tf = 0.3nS cje = 0.5pF cjc = 0.5pF ccs = 0.4pF)
.model ds d(is = 2e − 12 tt = 0.05nS eg = 0.62V vj = 0.58)
.model sw vswitch (von = 0.4V voff = 2.5V)
.ends
```

EL2019C

Fast, High Voltage Comparator with Master Slave Flip-Flop

Features

- Comparator cannot oscillate
- Fast response—5 ns data to clock setup, 20 ns clock to output
- Wide input differential voltage range—24V on ±15V supplies
- Wide input common mode voltage range—±12V
- Precision input stage—V_{OS} = 1.5 mV
- Low input bias current—100 nA
- Low input offset current—30 nA
- ±4.5V to ±18V supplies
- 3 State TTL compatible output
- No supply current glitch during switching
- 103 dB voltage gain (Low input uncertainty ≈ 30 μV)
- 50% power reduction in shutdown mode
- Input and flip-flop remain active in shutdown mode

Applications

- Analog to digital converters
- ATE pin receiver
- Zero crossing detector
- Window detector
- "Go/no-go" detector

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2019CN	−40°C to +85°C	P-DIP	MDP0006

General Description

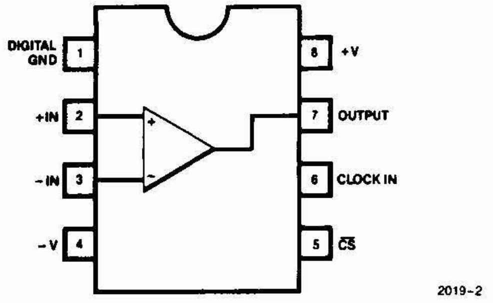
Not Recommended For New Designs

The EL2019 offers a new feature previously unavailable in a comparator before—a master/slave edge triggered flip-flop. The comparator output will only change output state after a positive going clock edge is applied. Thus the output can't feed back to the input and cause oscillation. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate current glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and master slave flip-flop remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see QRA1: *Elantec's Processing-Monolithic Products.*

Connection Diagrams

8-Pin Plastic DIP



Top View

EL2019C

Fast, High Voltage Comparator with Master Slave Flip-Flop

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V
V_{IN}	Input Voltage	$+V_S$ to $-V_S$
ΔV_{IN}	Differential Input Voltage	Limited only by Power Supplies
I_{IN}	Input Current (Pins 1, 2 or 3)	±10 mA
I_{INS}	Input Current (Pins 5 or 6)	±5 mA
P_D	Maximum Power Dissipation (Note 3 - See Curves)	1.25W

I_{OP}	Peak Output Current	50 mA
I_O	Continuous Output Current	25 mA
T_A	Operating Temperature Range	−40°C to +85°C
T_J	Operating Junction Temperature	150°C
T_{ST}	Storage Temperature	−65°C to +150°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, unless otherwise specified

Parameter	Description	Temp	Limits			Test Level	Units
			Min	Typ	Max		
V_{OS}	Input Offset Voltage V_{CM} = 0V, V_O Transition Point	25°C		1.5	6	I	mV
		T_{MIN}, T_{MAX}			8	III	mV
I_B	Input Bias Current V_{CM} = 0V, Pin 2 or 3	25°C		±100	±400	I	nA
		T_{MIN}, T_{MAX}			±600	III	nA
I_{OS}	Input Offset Current V_{CM} = 0V	25°C		30	150	I	nA
		T_{MIN}, T_{MAX}			250	III	nA
CMRR	Common Mode Rejection Ratio (Note 1)	25°C	75	90		I	dB
PSRR	Power Supply Rejection Ratio (Note 2)	25°C	75	95		I	dB
V_{CM}	Common Mode Input Range	25°C	±12	±13		I	V
		T_{MIN}, T_{MAX}	±12			III	V
V_{uncer}	Input Uncertainty Range			30		V	µV/RMS
V_{OL}	Output Voltage Logic Low I_{OL} = 8 mA and I_{OL} = 0 mA)	25°C	−0.05	0.15	0.4	I	V
		T_{MIN}, T_{MAX}	−0.1		0.4	III	V
V_{OH}	Output Voltage Logic High						
	V_S = ±15V	25°C	3.5	4.0	4.65	I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	3.5		4.65	III	V
	V_S = ±5V	25°C	2.4			I	V
	V_S = ±5V	T_{MIN}	2.4			III	V
	V_S = ±5V	T_{MAX}	2.4			III	V

DC Electrical Characteristics $V_S = \pm 15V$, unless otherwise specified — Contd.

Parameter	Description	Temp	Limits			Test Level	Units
			Min	Typ	Max		
V_{ODIS1}	V_{OUT} Range, Disabled, $I_{OL} = -1$ mA						
	$V_S = \pm 15V$	25°C	4.65			I	V
	$V_S = \pm 15V$	T_{MIN}, T_{MAX}	4.65			III	V
	$V_S = \pm 5V$	25°C		3.65		V	V
V_{ODIS2}	V_{OUT} Range, Disabled, $I_{OL} = +1$ mA $V_S = \pm 5V$ to $+15V$	All	−0.3	−1		II	V
V_{INH}	Clock or $\overline{CS}$ Inputs	25°C	2			I	V
	Logic High Input Voltage	T_{MIN}, T_{MAX}	2			III	V
I_{IN}	Clock or $\overline{CS}$ Inputs Logic Input Current	25°C			±200	I	μA
	$V_{IN} = 0V$ and $V_{IN} = 5V$	T_{MIN}, T_{MAX}			±300	III	μA
V_{INL}	Clock or $\overline{CS}$ Inputs Logic Low Input Voltage	25°C			0.8	I	V
		T_{MIN}, T_{MAX}			0.8	III	V
I_{S+EN}	Positive Supply Current Enabled	25°C		8.8	13	I	mA
		T_{MIN}, T_{MAX}			14	II	mA
I_{S+DIS}	Positive Supply Current Disabled	25°C		4.9	6	I	mA
		T_{MIN}, T_{MAX}			7	II	mA
I_{S-EN}	Negative Supply Current Enabled	25°C		14.5	17	I	mA
		T_{MIN}, T_{MAX}			18	II	mA
I_{S-DIS}	Negative Supply Current Disabled	25°C		6.4	8.0	I	mA
		T_{MIN}, T_{MAX}			8.0	II	mA

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
T_S	Setup Time 5 mV Overdrive		12	20	II	ns
T_H	Hold Time		−3	0	IV	ns
T_{OPOUT}	Clock to Output Delay		20	25	IV	ns
T_{OPMIN}	Minimum Clock Width		7		V	ns
T_{EN}	Output 3-State Enable Delay		40	70	IV	ns
T_{DIS}	Output 3-State Disable Delay		150	300	IV	ns

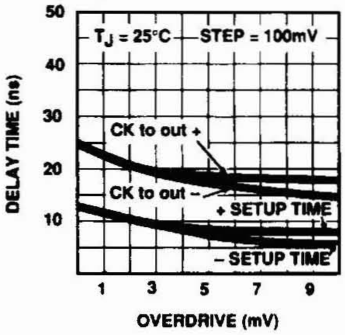
Note 1: $V_{CM} = +12V$ to $-12V$.

Note 2: $V_S = \pm 5V$ to $\pm 15V$.

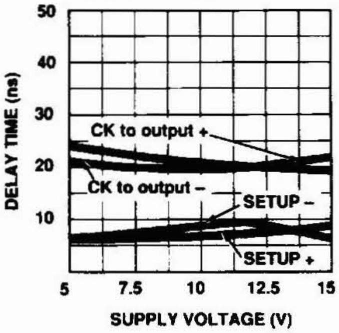
Note 3: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

Typical AC Performance Curves

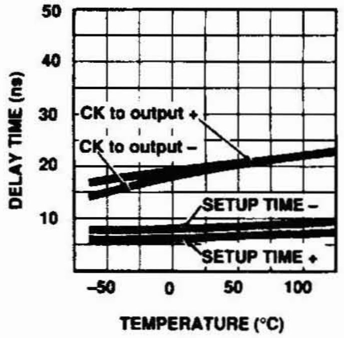
Delay Time vs
Input Overdrive



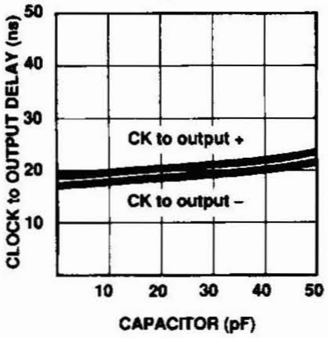
Delay Time vs
Supply Voltage



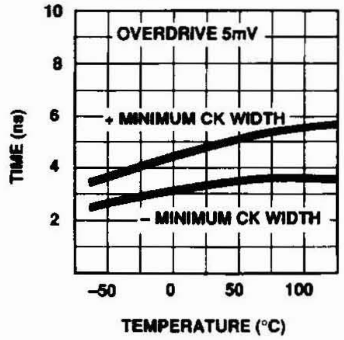
Delay Time vs
Temperature



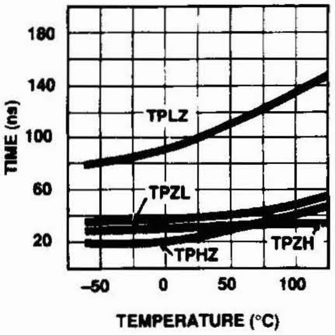
Clock to Output Delay
vs Load Capacitor



Minimum Clock Width
vs Temperature



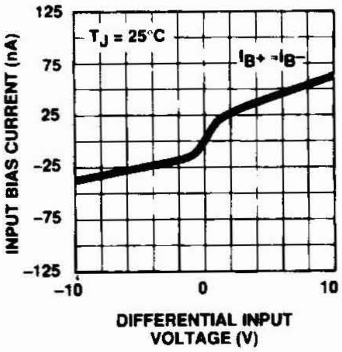
Enabled/Disabled Times
vs Temperature



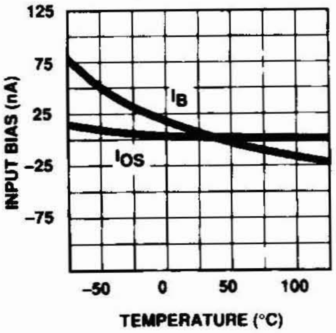
2019-3

Typical AC Performance Curves — Contd.

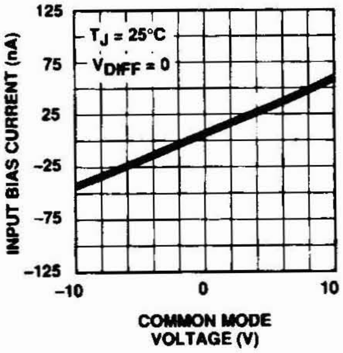
Input Bias Current vs Differential Input Voltage



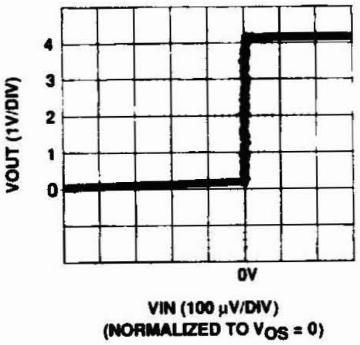
Input Bias Current vs Temperature



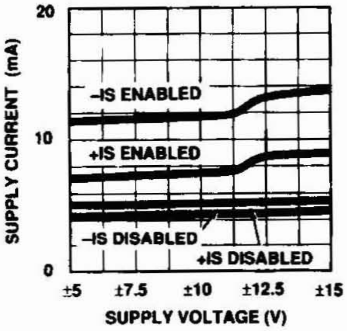
Input Bias Current vs Common Mode Voltage



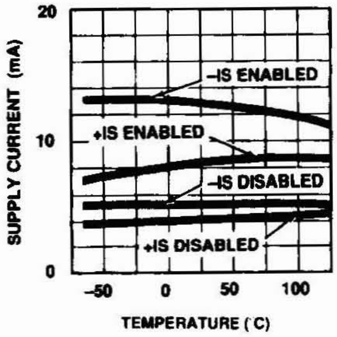
V_O/V_I Transfer Characteristics



Supply Current vs Supply Voltage



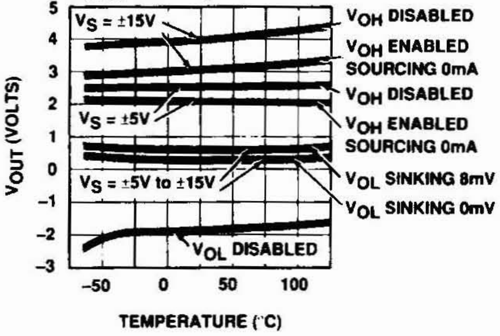
Supply Current vs Temperature



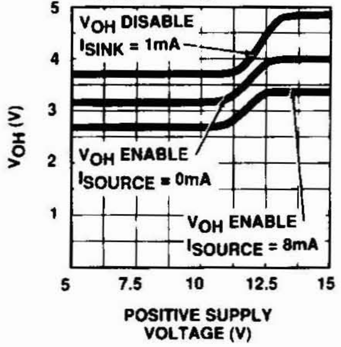
2019-4

Typical AC Performance Curves — Contd.

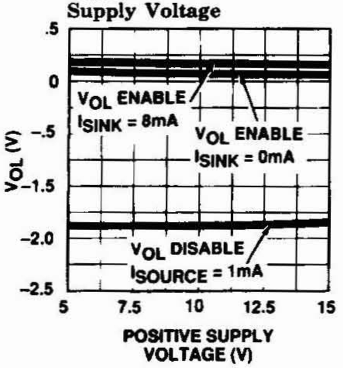
V_{OUT} vs Temperature



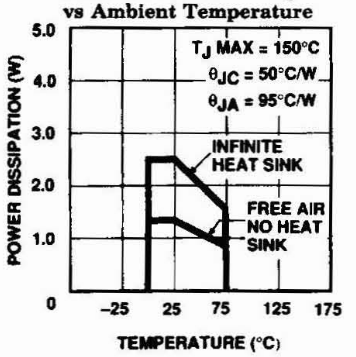
V_{OH} vs Positive Supply Voltage



V_{OL} vs Positive Supply Voltage



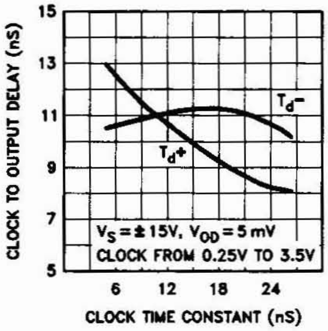
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



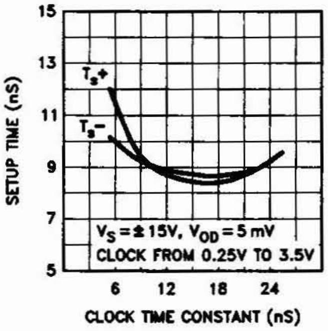
2019–5

Typical AC Performance Curves — Contd.

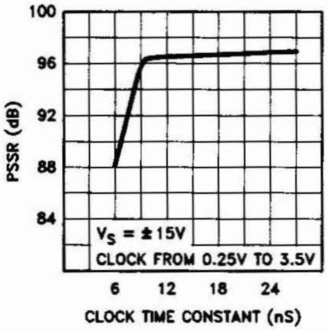
Clock to Output Delay vs Clock Time Constant



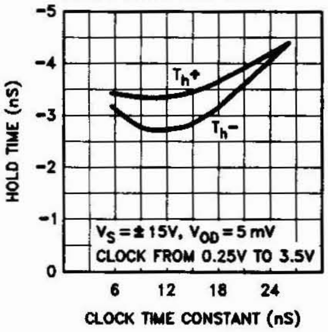
Set-up Time vs Clock Time Constant



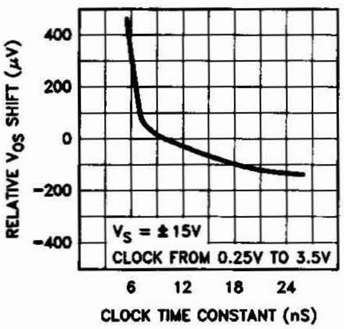
PSRR vs Clock Time Constant



Hold Time vs Clock Time Constant

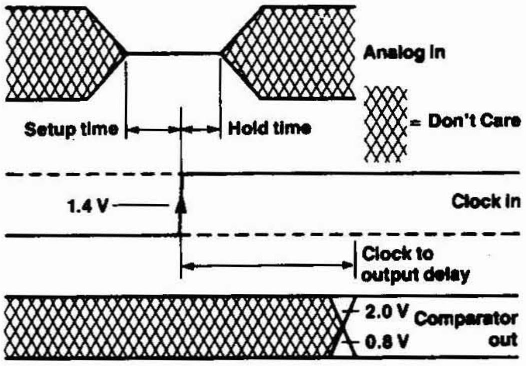


Relative V_{OS} Shift vs Clock Time Constant



2019-6

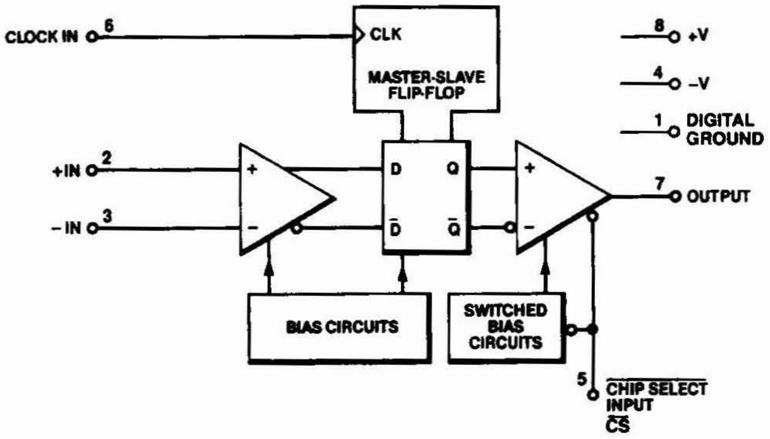
Timing Diagram


Analog In
Setup time
Hold time
= Don't Care
1.4 V
Clock In
Clock to output delay
2.0 V
0.8 V
Comparator out

Note: Since the hold time is negative the input is a don't care at the clock time. This ensures that clock noise will not affect the measurement.

2019-7

Block Diagram


CLOCK IN
6
CLK
MASTER-SLAVE FLIP-FLOP
8
+V
4
−V
1
DIGITAL GROUND
+IN
2
−IN
3
+
−
D
Q
$\overline{D}$
$\overline{Q}$
7
OUTPUT
BIAS CIRCUITS
SWITCHED BIAS CIRCUITS
5
$\overline{\text{CHIP SELECT}}$ INPUT
$\overline{CS}$

2019-8

Function Table

Inputs (Time n − 1)				Internal Q (Time n)	Notes	Output (Time n)
+IN	−IN	$\overline{CS}$	CLK			
+	−	L	↑	H	Normal Comparator Operation	H
−	+	L	↑	L	With "D" Flip-Flop	L
+	−	H	↑	H	Normal Comparator Operation	High Z
−	+	H	↑	L	With "D" Flip-Flop; Power Down Mode	High Z
X	X	L	H	Qn − 1	Data Retained in Flip-Flop	Qn − 1
X	X	L	L	Qn − 1	Data Retained in Flip-Flop	Qn − 1
X	X	L	↓	Qn − 1	Data Retained in Flip-Flop	Qn − 1
X	X	H	H	Qn − 1	Data Retained in Flip-Flop, Output Power Down Mode	High Z
X	X	H	L	Qn − 1	Data Retained in Flip-Flop, Output Power Down Mode	High Z
X	X	H	↓	Qn − 1	Data Retained in Flip-Flop, Output Power Down Mode	High Z

Application Hints

Device Overview

The EL2019 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. The EL2019 has an internal master/slave flip-flop between the input and output. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Process, which is immune to power sequencing and latch up problems.

Power Supplies

The EL2019 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.01 µF monolithic ceramic recommended) within ¼ inch of the power supply leads. Good ground plane construction techniques improve stability, and the lead from pin 1 to ground should be short.

Front End

The EL2019 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V).

The large common mode range (±12V minimum) and differential voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

Recovery from Large Overdrives

Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device, or the supply voltage be raised to encompass the input signal in the common mode range.

Input Slew Rate

All comparators have input slew rate limitations. The EL2019 operates normally with any input slew rate up to 300 V/µs. Input signal slew rates over 300 V/µs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators. This shows up as an increased set-up time.

Master Slave Flip-Flop

The built-in Master/Slave Flip-Flop only allows the output to change when a positive edge is received on the clock input. This feature has some major benefits to the user. First, the device cannot oscillate due to feedback from the output to the inputs. Second, the device *must* make a decision when it receives a clock input, and the difference between deciding on a "0" or a "1" is limited only by the input circuit noise, both internal and external to the EL2019. With low impedance sources and a good layout this uncertainty can be less than 30 µV/RMS. Since a 30 µV change on the input can cause a 4V change on the output this works out to an effective gain of 103 dB, more than adequate for a 16-bit analog to digital converter.

The hold time of the EL2019 is worst case 0 ns, and typically −3 ns. This means that the analog signal is sampled typically 3 ns *before* the clock time and, worst case, concurrent with the clock.

The EL2019 is sensitive to a large clock edge rates. More than a 500 V/µs edge rate at the clock input will induce V_{OS} shifts, reduce PSRR, and cause the device to operate incorrectly at low temperatures and low supply voltages. A good method to control the clock edge rate is to place a resistor in series and a capacitor to ground in parallel with the clock input. Generally, any time constant 10 ns or greater will suffice.

Elantec tests the EL2019 with a nominal 20 ns time constant, using a series 330Ω resistor and 61 pF of capacitance to ground (including strays). All clocks are generated by Schottky TTL and have a 0.25V to 3.5V swing.

Application Hints — Contd.

Output Stage

The output stage of the EL2019 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2019 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature

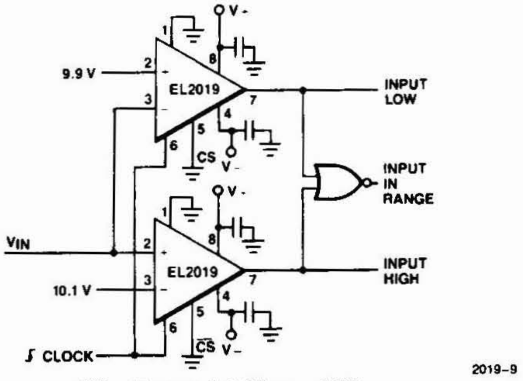
The EL2019 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in large ATE systems where there may be 1000 comparators, but only 10% are in use at any one time.

The EL2019 will work properly with the chip select input (pin 5) floating, however, good R.F. technique would be to ground this input if it is not used.

Due to the power saving feature and linear output stage, the EL2019 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2019 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

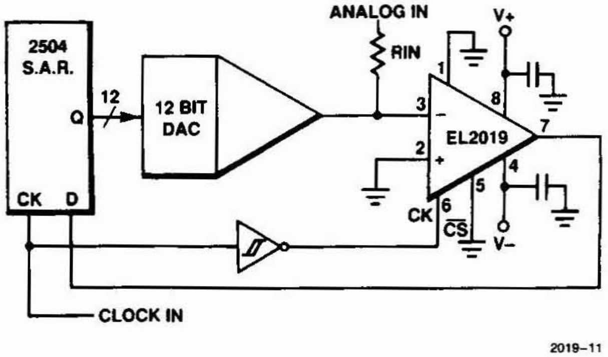
Typical Applications

A Wide Input Range Window Comparator

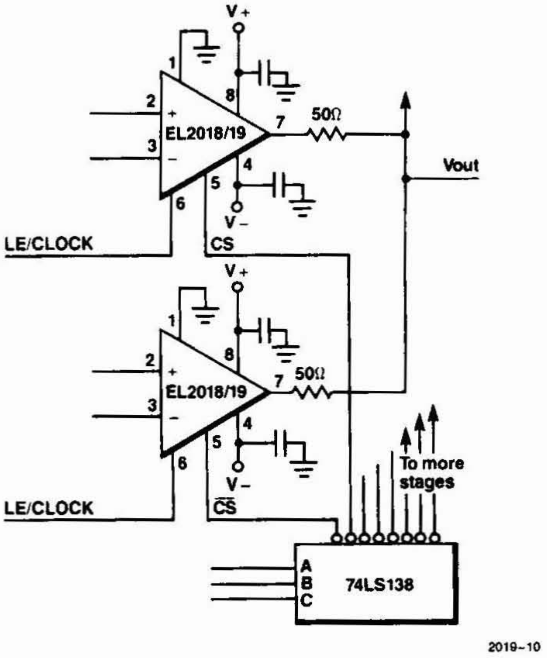

V-
1
2
8
9.9 V
EL2019
7
INPUT LOW
3
4
5
6
CS
V-
INPUT IN RANGE
V-
1
8
VIN
2
EL2019
INPUT HIGH
3
7
10.1 V
4
5
6
CS
V-
CLOCK
2019-9

(V_{IN} Range +12V to −12V with V_S = ±15V)

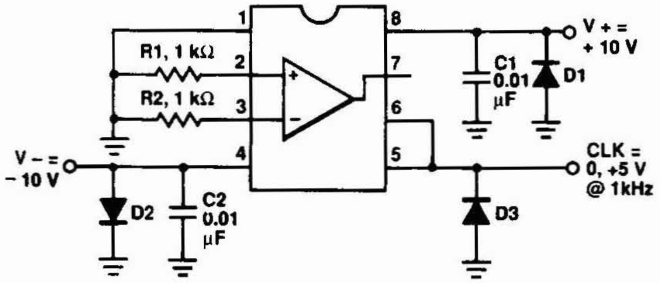
The EL2019 makes an excellent comparator in most analog to digital converters, due to its high gain and fast response. Most 2504 based A to D designs can be modified to use the EL2019 simply by using an inverted clock to the EL2019 as shown below. This results in improved performance due to less jitter of the transition voltages.


ANALOG IN
V+
2504
S.A.R.
RIN
1
12
Q
12 BIT
DAC
3
8
EL2019
7
2
4
5
CK
D
CK
6
CS
V-
CLOCK IN
2019-11

Using the Power Down/ 3-State Feature


V+
1
8
2
7
50Ω
EL2018/19
3
Vout
4
5
6
V-
LE/CLOCK
CS
V+
1
8
2
7
50Ω
EL2018/19
3
4
5
To more stages
6
V-
LE/CLOCK
CS
A
B
C
74LS138
2019-10

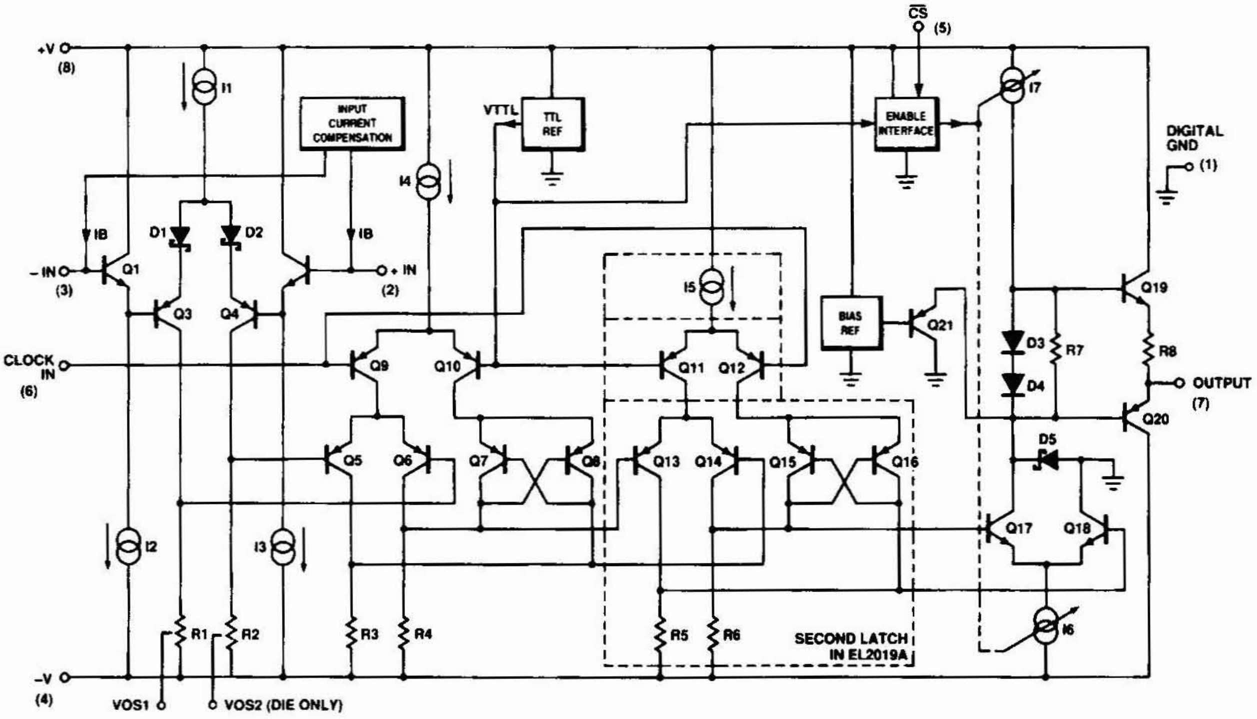
Burn-In Circuit


1
8
V+ =
+10 V
R1, 1 kΩ
2
7
C1
0.01
µF
D1
R2, 1 kΩ
3
+
−
6
4
5
CLK =
0, +5 V
@ 1kHz
V− =
−10 V
D2
C2
0.01
µF
D3

2019-12

Pin numbers are for DIP packages. All packages use the same schematic.

Equivalent Schematic


CS
(5)
+V
(8)
I1
INPUT CURRENT COMPENSATION
VTTL
TTL REF
ENABLE INTERFACE
I7
DIGITAL GND
(1)
I4
IB
D1
D2
IB
−IN
(3)
Q1
+IN
(2)
Q3
Q4
I5
BIAS REF
Q21
Q19
D3
R7
R8
CLOCK IN
(6)
Q9
Q10
Q11
Q12
D4
OUTPUT
(7)
Q20
D5
Q5
Q6
Q7
Q8
Q13
Q14
Q15
Q16
Q17
Q18
I2
I3
R1
R2
R3
R4
R5
R6
SECOND LATCH IN EL2019A
I6
−V
(4)
VOS1
VOS2 (DIE ONLY)

2019-13

EL2019 Macromodel

```
* Connections:    +input
*                 |    -input
*                 |    |    +V
*                 |    |    |    -V
*                 |    |    |    |    Cpin
*                 |    |    |    |    |    C̅S̅
*                 |    |    |    |    |    |   output
*                 |    |    |    |    |    |   |
.subckt M2019     2    3    8    4    6    5   7
*
* Input Stage
*
i1 8 10 700μA
r1 13 4 1K
r2 14 4 1K
q1 8 3 11 qn
q2 8 2 12 qn
q3 13 11 10 qp
q4 14 12 10 qp
i2 11 4 200μA
i3 12 4 200μA
*
* 2nd Stage & Flip Flop
*
*i4 8 24 700μA
i4 8 24 1mA
q9 22 6 24 qp
q10 18 17 24 qp
v1 17 0 2.5V
q5 15 14 22 qp
q6 16 13 22 qp
r3 15 4 1K
r4 16 4 1K
q7 16 15 18 qp
q8 15 16 18 qp
i5 8 40 500μA
q11 41 17 40 qp
q12 42 6 40 qp
q13 43 16 41 qp
q14 44 15 41 qp
q15 44 43 42 qp
q16 43 44 42 qp
r5 43 4 1K
r6 44 4 1K
*
* Output Stage
*
i7 8 35 2mA
s1 35 20 5 0 sw
d2 35 8 ds
i6 26 34 5mA
```

EL2019 Macromodel — Contd.

```
s2 34 4 5 0 sw
d3 34 26 ds
q19 8 20 21 qn 2
q20 4 19 7 qp 2
r8 21 7 60
r7 20 19 4K
q17 19 44 26 qn 5
q18 0 43 26 qn 5
q22 20 20 30 qn 5
q23 19 19 30 qn 8
d1 0 19 ds
q21 0 17 19 qp
*
* Power Supply Current
*
ips 8 4 4mA
*
* Models
*
.model qn npn (is=2e-15 bf=400 tf=0.05nS cje=0.3pF cjc=0.2pF ccs=0.2pF)
.model qp pnp (is=0.6e-15 bf=60 tf=0.3nS cje=0.5pF cjc=0.5pF ccs=0.4pF)
.model ds d(is=2e-12 tt=0.05nS eg=0.62V vj=0.58)
.model sw vswitch (von=0.4V voff=2.5V)
.ends
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2021C
Monolithic Pin Driver

Features

- Wide range of programmable analog output levels
- 0.5 Ampere output drive with external transistors
- Programmable Slew Rate
- Low overshoot with large capacitive loads-stable with 500 pF
- 3-state output
- Power-down capability
- Wide supply range
- Overcurrent sense

Applications

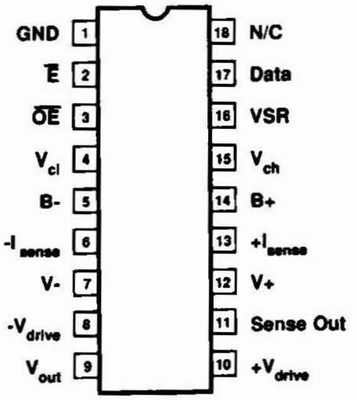
- Loaded circuit board testers
- Digital testers
- Programmable 4-quadrant power supplies

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL2021CJ	0°C to +75°C	CerDIP	MDP0031

Connection Diagram

18-Pin DIP Package


GND 1
$\overline{E}$ 2
$\overline{OE}$ 3
V_{cl} 4
B- 5
$-I_{sense}$ 6
V- 7
$-V_{drive}$ 8
V_{out} 9
18 N/C
17 Data
16 VSR
15 V_{ch}
14 B+
13 $+I_{sense}$
12 V+
11 Sense Out
10 $+V_{drive}$

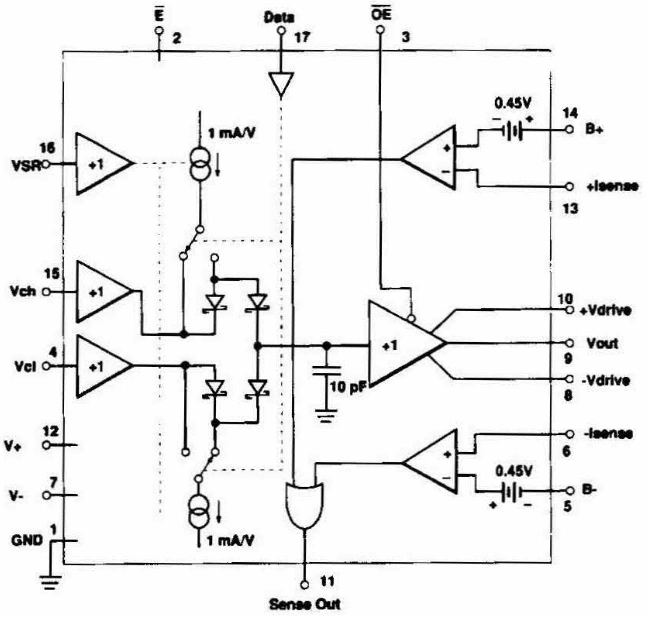
2021-1

Top View

General Description

The EL2021 is designed to drive programmed voltages into difficult loads. It has the required circuitry to be used as the pin driver electronics in board test systems. Capable of overpowering logic outputs, the part can accurately drive independently set high and low levels with programmed Slew Rates into reactive loads. It can also be placed into high impedance to monitor the load without having to disconnect. Previous board testers had multiplexing schemes to reduce the number of pin drivers required. With the small size and power consumption of the monolithic EL2021, a driver per node with little or no multiplexing becomes practical. Since only a few pins of "bed-of-nails" board testers need be active at any given time, the power-down feature saves substantial power in large systems.

Block Diagram


$\overline{E}$ 2
Data 17
$\overline{OE}$ 3
0.45V
14 B+
+Isense 13
1 mA/V
16 VSR
+1
15 Vch
4 Vcl
10 +Vdrive
Vout 9
-Vdrive 8
10 pF
-Isense 6
0.45V
B- 5
12 V+
7 V-
1 GND
1 mA/V
11 Sense Out

2021-2

Truth Table

$\overline{E}$	$\overline{OE}$	Data	V_{OUT}	Comments
0	0	0	V_{CL}	Active
0	0	1	V_{CH}	Active
0	1	X	High-Z	Third State
1	X	X	Undefined	Power-down

EL2021C

Monolithic Pin Driver

Absolute Maximum Ratings (T_A = 25°C)

V+	Supply Voltage	−0.3V to +16V	Sense Out	Output Current	−10 mA to +10 mA
V−	Supply Voltage	0.03V to −16V	V_{OUT}, Drive+, Drive−	Output Currents	−45 mA to +45 mA
B+, B−	Supply Voltages	V− to V+	T_J	Junction Temperature	150°C
Sense+	Input Voltages	(−2V + B+) to (0.3V + B+)	T_A	Operating Ambient Temperature Range	0°C to +75°C
Sense−	Input Voltages	(−0.3V + B−) to (2V + B−)	T_{ST}	Storage Temperature	−65°C to +150°C
$\overline{E}$, VSR, $\overline{OE}$, Data	Input Voltages	−0.3 to +6V	P_D	Power Dissipation (T_A = 25°C) (See Curves)	1.8W
V_{CH}, V_{CL}	Input Voltages	B− to B+ and V− to V+			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

T_A = 25°C, V+ = 15, V− = −10V, B+ = V_{CH} +3.6V, B− = V_{CL} −3.6V, No Load. Data and $\overline{OE}$ levels are: L = 2.0V and H = 3.0V (CMOS thresholds). $\overline{E}$ levels are: L = 1.5V and H = 3.5V. All tests done using 2N2222 and 2N2907 output transistors with Beta > 40 @ I_C = 400 mA and Beta > 27 @ I_C = 500 mA and V_{CE} = 3.1V. $\overline{OE}$ and $\overline{E}$ low.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
I_S	V+, -Supply Currents	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data = H or L	15	25	30	I	mA
		V_{CH} = 11V, V_{CL} = −6V, VSR = 5V, Data = H or L	21	33	45	IV	mA
		V_{CH} = −6V, V_{CL} = 11V, VSR + 2.5V, Data = H or L	15	25	30	IV	mA
I_S, disabled	V+, -Supply Currents	V_{CH} = 5V, V_{CL} = 0V, VSR = 2.5V, Data = H or L, $\overline{E}$ = H	0	0.5	2.5	I	mA
I_{VCH}	V_{CH} Input Current	V_{CH} = −1V to +7.5V, V_{CL} = 0V, VSR = 5V, Data = H or L	−20	5	20	I	μA
I_{VCL}	V_{CL} Input Current	V_{CL} = −3.5V to +3.5V, V_{CH} = 0V, VSR = 5V, Data = H or L	−20	−5	20	I	μA
I_{Data}	Data Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = 0 or 5V	−50	5	50	I	μA
I_{OE}	$\overline{OE}$ Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = L, $\overline{OE}$ = 0V or 5V	−20	5	20	I	μA
I_E	$\overline{E}$ Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = L, $\overline{E}$ = 0V or 5V	−20	2	20	I	μA
I_{VSR}	VSR Input Current	V_{CH} = 5V, V_{CL} = 0V, Data = L, VSR = 0V or 5V	−20	2	20	I	μA
$\pm I_{sense}$	Sense Input Currents	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = 0V or 5V	−20	5	20	IV	μA
I_B+, I_B-	B+, B− Input Currents	V_{CH} = 5V, V_{CL} = 0V, Data = L, VSR = 5V	−20	5	20	IV	μA

DC Electrical Characteristics

T_A = 25°C, V+ = 15, V− = −10V, B+ = V_{CH} +3.6V, B− = V_{CL} −3.6V, No Load. Data and $\overline{OE}$ levels are: L = 2.0V and H = 3.0V (CMOS thresholds). $\overline{E}$ levels are: L = 1.5V and H = 3.5V. All tests done using 2N2222 and 2N2907 output transistors with Beta > 40 @ I_C = 400 mA and Beta > 27 @ I_C = 500 mA and V_{CE} = 3.1V. $\overline{OE}$ and $\overline{E}$ low. — Contd.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage	V+ = 14.5V, V− = −9.5V					
		V_{CH} = 5V, V_{CL} = 0, VSR = 1V, Data = L,					
		Output Current = −100 mA, 0 mA, or +100 mA	−50		50	I	mV
		Output Current = −400 mA or +400 mA	−300		300	I	mV
		Output Current = −500 mA or +500 mA	−600		600	I	mV
		V_{CH} = 5V, V_{CL} = 0, VSR = 1V, Data = H					
		Output Current = −100 mA, 0 mA, or +100 mA	4.95		5.05	I	V
		Output Current = −400 mA or +400 mA	4.7		5.3	I	V
		Output Current = −500 mA or +500 mA	4.4		5.6	I	V
		V_{CH} = 11V, V_{CL} = −6V, VSR = 1V, I_{OUT} = 0, Data = L	−6.1		−5.9	I	V
		V_{CH} = 11V, V_{CL} = −6V, VSR = 1V, I_{OUT} = 0, Data = H	10.9		11.1	I	V
I_{sense+}	+I_{sense} Threshold	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, R_{sense} = 1Ω, Data = H	400	450	600	I	mA
I_{sense-}	−I_{sense} Threshold	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, R_{sense} = 1Ω, Data = L	−400	−450	−600	I	mA
$V_{O,\ sense}$	Sense Out Levels	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data L or H,					
		Output Current = −350 mA or +350 mA	0		0.6	I	V
		Output Current = −550 mA or +550 mA	3.5		5.0	I	V
$I_{OUT,TRI}$	High-Impedance Output Leakage	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data = L, $\overline{OE}$ = H, Output Voltage = −2.5V or +7.5V	−100	5	100	I	μA

AC Electrical Characteristics

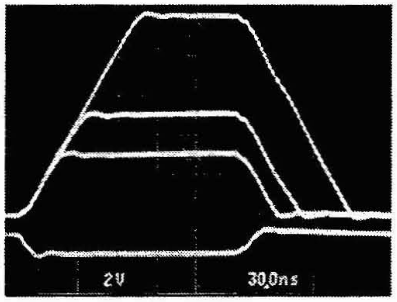
DC test conditions apply except where noted. For AC tests, R_L = 1k, C_L = 200 pF. Delay times are measured from $\overline{OE}$ or Data crossing 2.5V, V_{CH} = 5V, V_{CL} = 0.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
SR+	+Slew Rate	Data L to H, Output from 0.5V to 4.5V, VSR = 1V	80	100	120	I	V/μs
		VSR = 3V	150	240	360	I	V/μs
SR−	−Slew Rate	Data H to L, Output from 4.5V to 0.5V, VSR = 1V	−80	−100	−120	I	V/μs
		VSR = 3V	−150	−240	−360	I	V/μs
SRSYM	Slew Rate Symmetry	$\left[\frac{(SR+)-(SR-)}{(SR+)+(SR-)}\right]$ VSR = 1V	−10		10	I	%
		VSR = 2V	−20		20	IV	%
T_{pd}	Propagation Delay	Data L to H, Output to 0.2V, VSR = 2.5V	6.5	9	11.5	I	ns
		Data H to L, Output to 4.8V, VSR = 2.5V	6.5	9	11.5	I	ns
T_s	Settling Time	VSR = 5V, Data L to H, Output 4.5V to 5V ±0.2V			30	IV	ns
		VSR = 5V, Data H to L, Output 0.5V to ±0.2V			30	IV	ns
OS	Overshoot	VSR = 1V, Data L to H or H to L	−300		300	I	mV
		VSR = 1V, $\overline{OE}$ H to L, Data = L, R_L to 5V	−300		300	I	mV
		VSR = 1V, $\overline{OE}$ H to L, Data = H, R_L to 0V	−300		300	I	mV
T_{pda}	Propagation Delay, High-Z to Active	VSR = 2.5V, $\overline{OE}$ H to L, C_L = 50 pF					
		R_L to 5V, Data = L, Output to 3.5V			50	I	ns
		R_L to 0V, Data = H, Output to 1.5V			50	I	ns
T_{pdh}	Propagation Delay, Active to High-Z	VSR = 2.5V, $\overline{OE}$ L to H, C_L = 50 pF,					
		Data = L, R_L to 5V, Output to 0.5V			50	I	ns
		Data = H, R_L to 0V, Output to 4.5V			50	I	ns

Pin Description Table

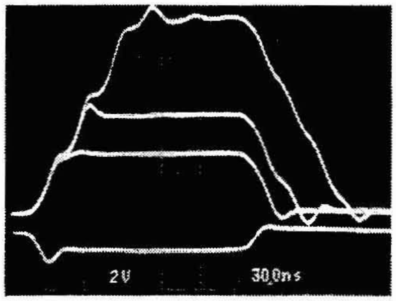
Pin #	Name	Description
1	GND	System ground.
2	$\overline{E}$	$\overline{\text{Enable}}$ control input. A logic low allows normal operation; a logic high puts the device into power down mode. No output levels are defined in powerdown nor does the output behave as a high impedance.
3	$\overline{OE}$	$\overline{\text{Output Enable}}$ input. A logic low sets the output to low-impedance driver mode; a logic high places the output into a high-impedance state.
4	V_{CL}	Lower analog control input. When Data = $\overline{OE}$ = $\overline{E}$ = L, the V_{CL} level is output as V_{OUT} (assuming $V_{CL} < V_{CH}$).
5	B−	System power supply. The EL2021 uses this pin as a negative output current monitor connection. Little current is drawn from this pin, transient or static.
6	$I_{sense}-$	Negative output current monitor input.
7	V−	Negative power supply. Because all negative output drive currents come from this pin (as much as 60 mA transiently), good bypassing is essential.
8	Drive−	Output to external pnp transistor base.
9	V_{OUT}	High-current input and output, depending on $\overline{OE}$.
10	Drive+	Output to external npn transistor base.
11	Sense Out	Logic output which signals that a high + or − output current is flowing.
12	V+	Positive power supply. Like V−, it should be well bypassed.
13	$I_{sense}+$	Positive output current monitor input.
14	B+	System power supply, similar to B−.
15	V_{CH}	Higher analog control input. When Data = H and $\overline{OE}$ = $\overline{E}$ = L, the V_{CH} level is output as V_{OUT} (assuming $V_{CH} > V_{CL}$).
16	VSR	Slew rate control input. A 1V level on this pin causes the output to slew at 100 V/µs, 0.5V causes a slew rate of 50 V/µs, etc.
17	Data	Output level control input. This pin digitally selects V_{CL} or V_{CH} as the output voltage when $\overline{OE}$ = $\overline{E}$ = L.
18	N/C	Not Connected.

Typical Performance Curves



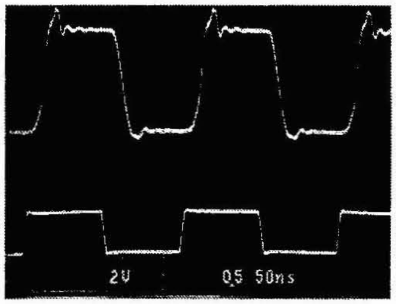
2021-3

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 50 pF, VSR = 1V.



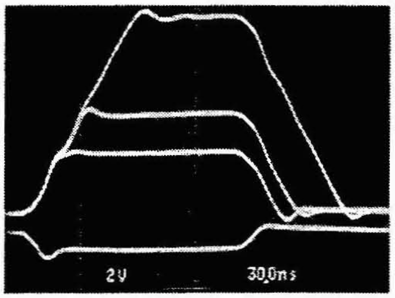
2021-4

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 200 pF, VSR = 1V.



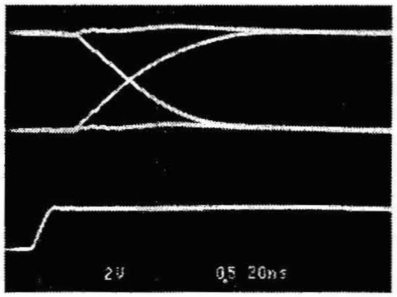
2021-5

Output waveshapes with 5 MHz data rate. C1 = 50 pF, VSR = 4V.



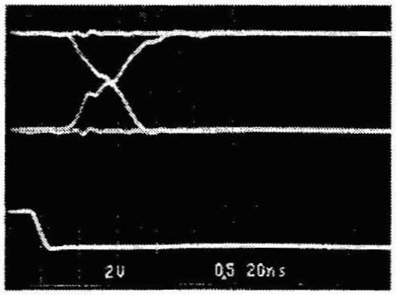
2021-6

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 200 pF, VSR = 1V, and overcompensated with 22 pF from each drive pin to ground.



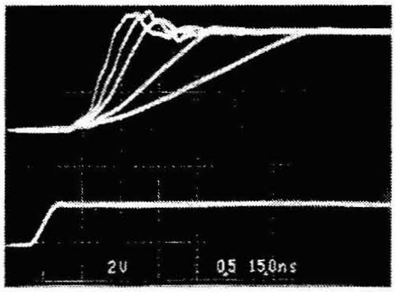
2021-7

Family of output waveshapes from active H, L to high-impedance H, L.



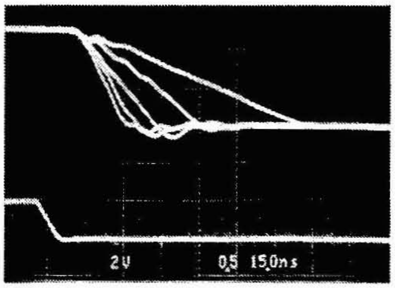
2021-8

Family of output waveshapes from high-impedance H, L to active H, L.



2021-9

Family of + output edges, 0V to 5V for VSR = 0.5V, 1V, 2V, 3V, 5V.

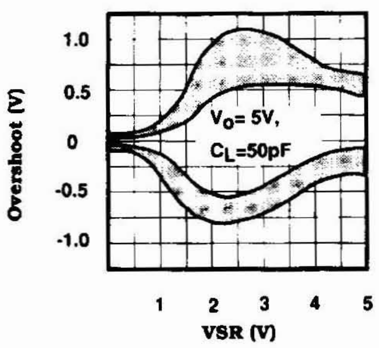


2021-10

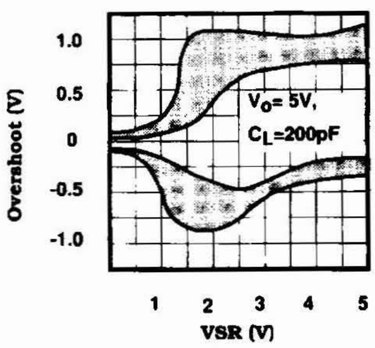
Family of—output edges, 5V to 0V or VSR = 0.5V, 1V, 2V, 3V, 5V.

Typical Performance Curves — Contd.

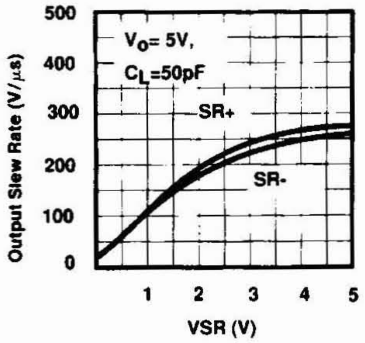
Overshoot vs VSR



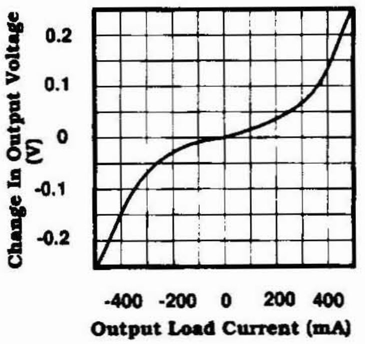
Overshoot vs VSR



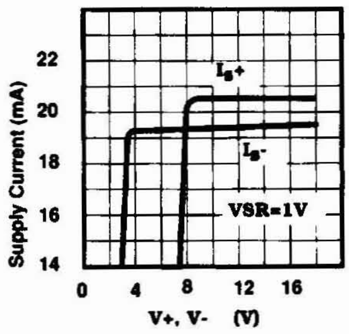
Slew Rate vs VSR



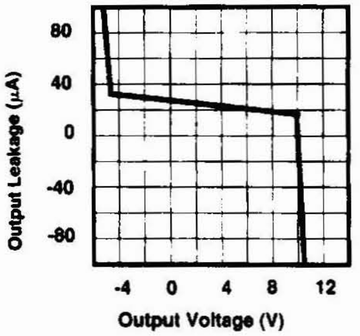
VOUT vs Load Current



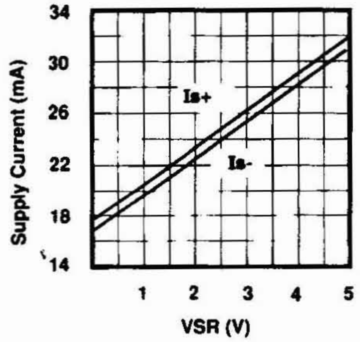
Supply Current vs Supply Voltage



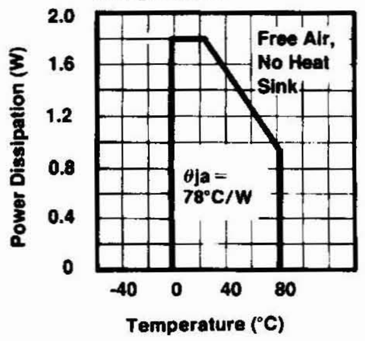
Tri-State Leakage vs Output Voltage



Supply Current vs VSR



Power Dissipation vs Temperature



2021-11

Applications Information

Output Stage

To meet the requirements of low output impedance, wide bandwidth, and large capacitive load driving capability, the EL2021 has a fairly exotic output stage. Figure 1 shows a simplified schematic of the circuit, only applicable in normal, low impedance mode. External transistors are used to handle the large load currents and peak power dissipations. Since there is no need for good AC crossover distortion performance in a pin driver, the output transistors are operated class C. That is, for small output currents, neither output transistor will conduct bias current, and when load currents do flow, one of the devices is off. This is accomplished by biasing the output transistors from Schottky diodes D1 and D2. In operation, the diode forward voltage is about 0.4V, whereas the "on" output transistor will have a V_{BE} of 0.6V. This leaves only 0.2V across the "off" transistor's base-emitter junction, not nearly enough to cause bias currents to flow in it. Schottky diodes have a temperature drift similar to silicon transistors, so the class C bias maintains over temperature. One caution is that the diodes are in the IC package and are thermally separate from the transistors, so there can exist temperature differences between packages that can cause thermal runaway. Runaway is avoided as long as the external transistors are not hotter than the EL2021 package by more than 80°C. The only way runaway has been induced as of this writing is to use "freeze spray" on the IC package while the output transistors are very hot.

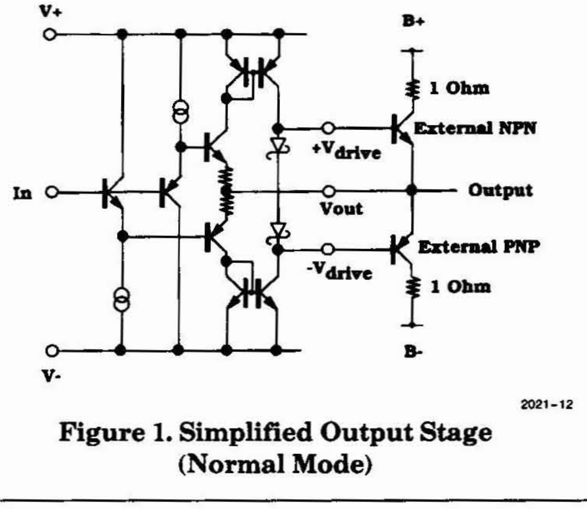


Figure 1. Simplified Output Stage (Normal Mode)

This circuit allows the external transistors to run from B+ and B− supplies that are of less voltage than V+ and V− to conserve power. Reducing B± supplies also reduces dissipations in the output devices themselves. B+ is typically made K volts more than V_{CH} and B− made K volts more negative than V_{CL}. Ideally K is made as small as possible to minimize output transistor dissipation, but two factors limit how small K can be. These factors are both related to the fact that transistors have two collector resistance numbers: "hard" and "soft" saturation resistance. As a transistor begins to saturate at high collector currents and small collector-emitter voltages, minority carriers begin to be generated from the base-collector junction. These carriers act as more collector dopant and actually reduce effective series collector resistance. At conditions of heavy saturation, the collector is flooded with minority carriers and exhibits minimum collector resistance. In this way, small geometry transistors like the 2N2222 and 2N2907 devices have excellent collector-emitter voltage drops at high currents, but are actually still in heavy saturation for 1V-2V drops. This "soft" saturation shows up as reduced beta at high currents and moderate V_{CE}'s as well as very poor AC performance. A transistor may exhibit an f_t of only 2 MHz in soft saturation when, like the 2N2222, it gives 300 MHz in non-saturated mode. The EL2021 requires the output transistors to have an f_t of at least 200 MHz to prevent degradation in overshoot, slew rate into heavy loads, and tolerance of heavy output capacitance. With a K of 3.2V and 1Ω collector resistors, almost all 2N2222 and 2N2907 devices perform well, but we have obtained devices from some vendors where the beta does indeed fall permaturely at reduced V_{CE} and high currents. It is important to characterize the external devices for the service that the EL2021 will be expected to provide.

The output stage of the EL2021 does not ring appreciably into a capacitive load in quiescent conditions, but it does ring while it slews. This is an unusual characteristic, but the output slews monotonically and the slew "ripple" does not cause problems in use. The slew ripple does cause a similar "ripple" in the overshoot-vs-VSR characteristic: the overshoot may decrease for slightly increasing VSR, then increase again for larger VSR's again. The overshoot-vs-VSR graphs

Applications Information — Contd.

presented in this data sheet thus reflect the range of overshoot rather than one particular device's wavy curve.

The typical 2N2222 and 2N2907 will deliver 750 mA into a short-circuit. This puts four watts of dissipation into the 2N2222 for $V_{CH} = 5V$. The npn can dissipate this power for a few tenths of a second as long as a metal-base TO-39 package is used. The small or non-metal-based packages have short thermal time constants and high thermal resistances, so they should withstand shorts for only a few milliseconds. The Sense Out signal should be used to control $\overline{OE}$ or reduce V_{CH} and V_{CL} to relieve the output devices from overcurrent conditions.

Transistors such as the MJE200 and MJE210 have very much improved collector resistances and high-current beta compared to the 2N2222 and 2N2907. Their f_t's are almost as good and sustain at higher currents, and high-current output accuracy will improve. They allow a K of 2V to reduce dissipations further, but short-circuit currents will be as much as two amperes! The geometries of these transistors are larger, and the added transistor capacitances will slow the maximum Slew Rates that the EL2021 can provide.

If transistors with f_t's less than 200 MHz are used, the EL2021 will need to be overcompensated. This is accomplished by connecting equal capacitors from the Drive pins to ground. These capacitors will range from 10 pF to 50 pF. The overcompensation will slow the maximum slew rate, but it will improve the overshoot and reactive load driving capability, and can be considered a useful technique.

Figure 2 shows the equivalent output stage schematic when the circuit is in high-impedance mode ($\overline{OE}$ = H). The external transistors have their base-emitter junctions each reverse-biased by a Schottky diode drop. A buffer amplifier copies the output voltage to give a bootstrapped bias for the Schottky stack. This scheme guarantees that the external transistors will be off for any output level, and the output leakage current is simply the bias current of the buffer.

The circuit works properly for AC signals up to 500 V/μs. Above this slew rate, the buffer cannot keep up and the external transistors may turn on transiently. Because of the bootstrap action, the output capacitance is less than 10 pF up to 10 MHz of small-signal bandwidth and 300 V/μs slew rate, increasing beyond these values. Adding overcompensation capacitors will degrade the slew rate that the output can withstand before current is drawn.

It is sometime necessary to provide a "snubber" network-a series R and C— to provide a local R.F. impedance for the buffer to look into. 330Ω and 56 pF should serve. Also, it is well to provide some DC path to ground (47k for instance) to bias the output stage when no actual circuit is connected to the EL2021 in high-impedance mode.

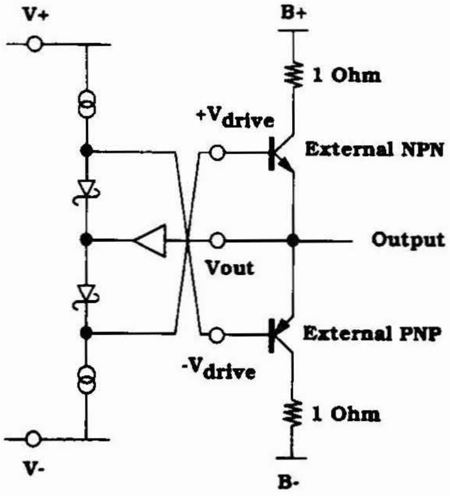


Figure 2. Simplified Output Stage (High-Impedance Mode)

Power Supplies

In typical operation, V+ and V− can be as much as ±15V and as little as V_{CH} +3V and V_{CL} −3V, respectively. When driving heavy output currents, however, it is wise to have 5V of headroom above V_{CH} and below V_{CL} to ensure no saturation of devices within the EL2021 and attendent waveshape distortions. Thus, for V_{CH} = 5V and V_{CL} = −2V, minimum operating voltages are +10, −7V. It is very important to bypass the supply terminals with low-inductance

Applications Information — Contd.

capacitors to ground, since the full base drive currents of the output transistors are derived from these supplies. Because the pulse currents can reach 60 mA, the capacitors should be at least a microfarad; 4.7 μF tantalum are ideal and require no small bypasses in parallel.

B+ and B− can be any voltage within V+ and V− and some amount previously discussed above V_{CH} and below V_{CL}. If V_{CH} or V_{CL} exceeds B+ or B−, very large internal fault currents can flow when the EL2021 attempts to bring an output transistor's base beyond the collector voltage. The bypassing care of the V± lines apply to the B± lines, as well as the fact that ampere currents can occur. Large (100 μF–500 μF) capacitors should be used to bypass perhaps every tenth EL2021.

The V_{CH}, V_{CL}, Data and $\overline{OE}$ lines should be driven locally so as to not pick up magnetic interference from the output. The inductance of interconnects to these lines can allow coupling to cause waveshape anomalies or even oscillations. If long lines are unavoidable, local 1k resistors or 50 pF–100 pF capacitors to ground can also serve the purpuse.

Data Pin

The slew rate of the input to the Data pin should be kept less than 1000 V/μs. Some feedthrough can occur for large Slew Rates which will distort the output waveshape. A 1k–2k resistor in series with the data pin will reduce feedthrough.

Current Sense

The output current is sensed by comparing the voltage dropped across the external shunt resistors to an internal 0.45V reference. The center of the trip level is adjusted for the particular output transistor betas listed in the data specifications. Transistors with less beta at high currents will cause the sense comparators to trip at slightly higher output currents. The 1Ω shunt resistors should be non-inductive. The family of wirewound resistors called "non-inductive" are too inductive for these shunts.

The response of the Sense Out can be thought of as slow attack and fast decay. A continuous overcurrent condition must last for at least 2 μs before Sense Out will go high, but will clear to low only about 200 ns after the overcurrent is withdrawn. This allows transient currents due to slewing capacitive load to not generate a flag. On the other hand, the output transistors will not be damaged with only a 2 μs system reaction time to a short-circuit.

Construction Practices

The major cautions in connecting to the EL2021 involve magnetic rather than capacitive parasitic concerns. The circuits can output as much as 100 A/μs. Even with normal Slew Rates and moderately large capacitive loads, the dI/dT can cause magnetic fields in harmless looking wires to fill adjacent lines with noise, and sometimes ringing or even sustained feedback. Thus, rules for wiring the EL2021 are:

(a) Keep leads short and large. Short wires are less inductive, as are wires with large surface area. The large surface area also reduces skin resistance at high frequencies, important at high currents (at 100 MHz, current penetrates only a few microns in metals).

(b) Use a ground plane. Due to inductance and skin effect, "ground" voltages will be different only inches apart on a copper ground plane. Individual wires do not create ground at high frequencies. The common "star" ground is a very bad idea for high-current and high-frequency circuits.

(c) Dress all wires against the ground plane. The magnetic fields that the wires would have generated will be intercepted by the ground plane and absorbed, thus reducing the wire's effective inductance. The capacitance added by this method is not important to EL2021 operation.

(d) The external transistors should have short interconnects to the EL2021, the collector shunt resistors, and the bypass capacitors. As previously stated, the shunt resistors must not be wire wound because of their inductance.

Applications Information — Contd.

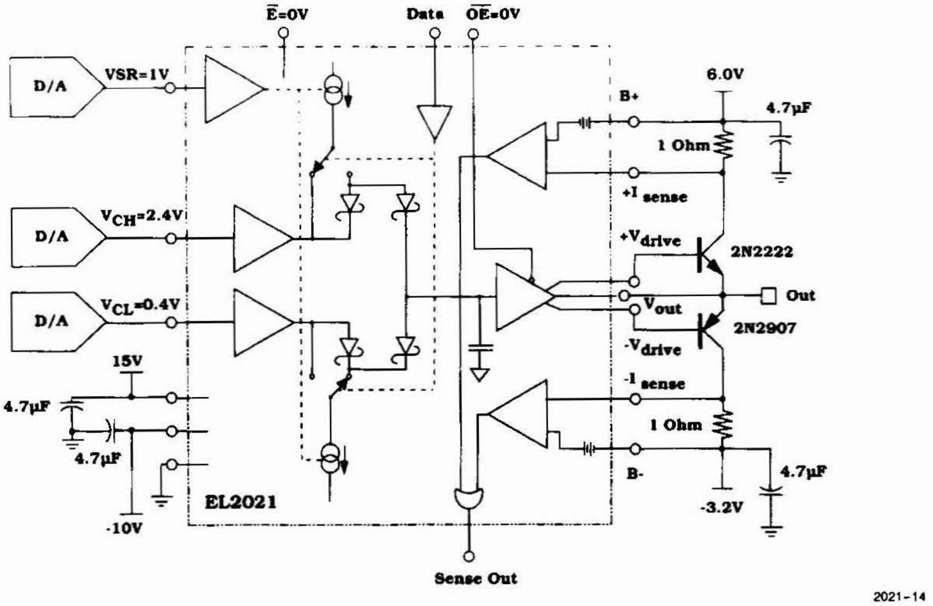
(e) The bypass capacitors should have low series resistance and inductance, but should not have a high Q. This may seem contradictory, but a 4.7 μF tantalum capacitor seems to work the best. An electrolytic capacitor should be added to help bolster the supply levels in the 0.1 μs–1 μs after a transition. No small capacitors are needed in parallel with the tantalums. The bypasses' ground returns are best connected to the area of ground inside the package outline to reduce the circulating current path length, if possible.

Using the EL2021 without External Transistors

By connecting both drive pins to the output pin, the EL2021 can be used as a stand-alone driver, not requiring the external transistors. The EL2021 is good for more than 50 mA in this mode. The output impedance rises to 12Ω, however, and the current sense and high-impedance mode are not available. The ripple seen in slew edges using the external transistors is largely absent from the standalone waveshapes; and overshoot is markedly improved at VSR > 1V, especially with large capacitive loads.

Typical Applications

100 V/μs High-Current Pin Driver Outputting TTL Levels


$\overline{E}$=0V
Data
$\overline{OE}$=0V
D/A
VSR=1V
D/A
V_{CH}=2.4V
D/A
V_{CL}=0.4V
15V
4.7μF
4.7μF
-10V
EL2021
B+
6.0V
4.7μF
1 Ohm
+I sense
+V_{drive}
2N2222
Out
V_{out}
2N2907
-V_{drive}
-I sense
1 Ohm
B-
4.7μF
-3.2V
Sense Out
2021-14

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2252C
Dual 50 MHz Comparator/Pin Receiver

Features

- Fast response—7 ns
- Inputs tolerate large overdrives with no speed nor bias current penalties
- Propagation delay is relatively constant with variations of input Slew Rate, overdrive, temperature, and supply voltage
- Output provides proper CMOS or TTL logic levels
- Hysteresis is available on-chip
- Large voltage gain—8000 V/V
- Not oscillation-prone
- Can detect 4 ns glitches
- MIL-STD-883 Rev. C compliant

Applications

- Pin receiver for automatic test equipment
- Data communications line receiver
- Frequency counter input
- Pulse squarer

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2252CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2252CM	0°C to +75°C	20-Lead SOL	MDP0027

General Description

The EL2252 dual comparator replaces the traditional input buffer + attenuator + ECL comparator + ECL to TTL translator circuit blocks used in digital equipment. The EL2252 provides a quick 7 ns propagation delay while complying with ±10V inputs. Input accuracy and propagation delay is maintained even with input signal Slew Rates as great as 4000 V/μs. The EL2252 can run on supplies as low as −5.2V and +9V and comply with ECL and CMOS inputs, or use supplies as great as ±18V for much greater input range.

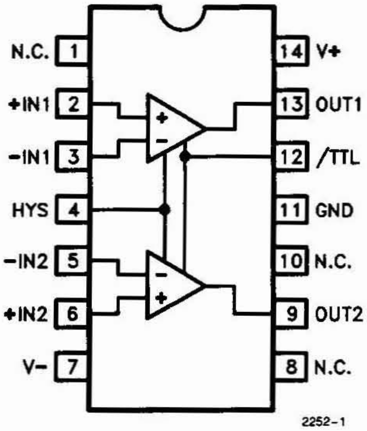
The EL2252 has a /TTL pin which, when grounded, restricts the output V_{OH} to a TTL swing to minimize propagation delay. When left open, the output V_{OH} increases to a valid CMOS level.

The comparators are well behaved and have little tendency to oscillate over a variety of input and output source and load impedances. They do not oscillate even when the inputs are held in the linear range of the device. To improve output stability in the presence of input noise, an internal 60 mV of hysteresis is available by connecting the HYS pin to V−.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1; "*Elantec's Processing, Monolithic Integrated Circuits*".

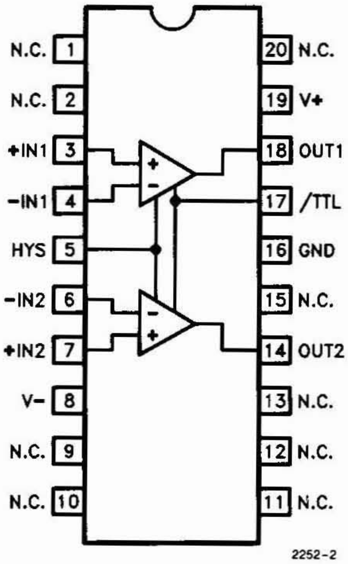
Connection Diagrams

14-Pin DIP



Top View

20-Pin SOL



Top View

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V	Internal Power Dissipation	See Curves
Voltage at V+	18V	Operating Ambient Temperature Range	−25°C to +85°C
Voltage between −IN and +IN pins	36V	Operating Junction Temperature	150°C
Output Current	12 mA	Storage Temperature Range	−65° to +150C
Current into +IN, −IN, HYS or /TTL	5 mA		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; HYS and /TTL grounded; T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level EL2252C	Units
V_{OS}	Input Offset Voltage	25°C		1	9	I	mV
		Full			13	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		7		V	µV/C
I_B	Input Bias Current at Null	25°C		6	16	I	µA
		Full			21	III	µA
I_{OS}	Input Offset Current	25°C		0.2	1	I	µA
		Full			2	III	µA
R_{IN}, diff	Input Differential Resistance	25°C		30		V	kΩ
R_{IN}, comm	Input Common-Mode Resistance	25°C		10		V	MΩ
C_{IN}	Input Capacitance	25°C		2		V	pF
$V_{CM}+$	Positive Common-Mode Input Range	Full	10	13		II	V
$V_{CM}-$	Negative Common-Mode Input Range	Full	−9	−12		II	V
A_{VOL}	Large Signal Voltage Gain V_O = 0.8V to 2.0V	25°C	4000	8000		I	V/V
		Full	3000			III	V/V

DC Electrical Characteristics

$V_S = \pm 15V$; HYS and /TTL grounded; $T_A = 25°C$ unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level EL2252C	Units
CMRR	Common-Mode Rejection Ratio (Note 1)	Full	70	95		II	dB
PSRR	Power-Supply Rejection Ratio (Note 2)	Full	70	90		II	dB
V_{HYS}	Peak-to-Peak Input Hysteresis with HYS connected to V−	25°C		60		V	mV
V_{OH}	High Level Output, CMOS Mode	Full	4.0	4.6	5.1	II	V
	TTL Mode	Full	2.4	2.7	3.2	II	V
V_{OL}	Low Level Output, I1 = 0	Full	−0.2	0.2	0.8	II	V
	I1 = 5 mA	Full	−0.2	0.4	0.8	II	V
I_S+	Positive Supply Current	Full		16	19	II	mA
I_S-	Negative Supply Current	Full		17	20	II	mA

AC Electrical Characteristics

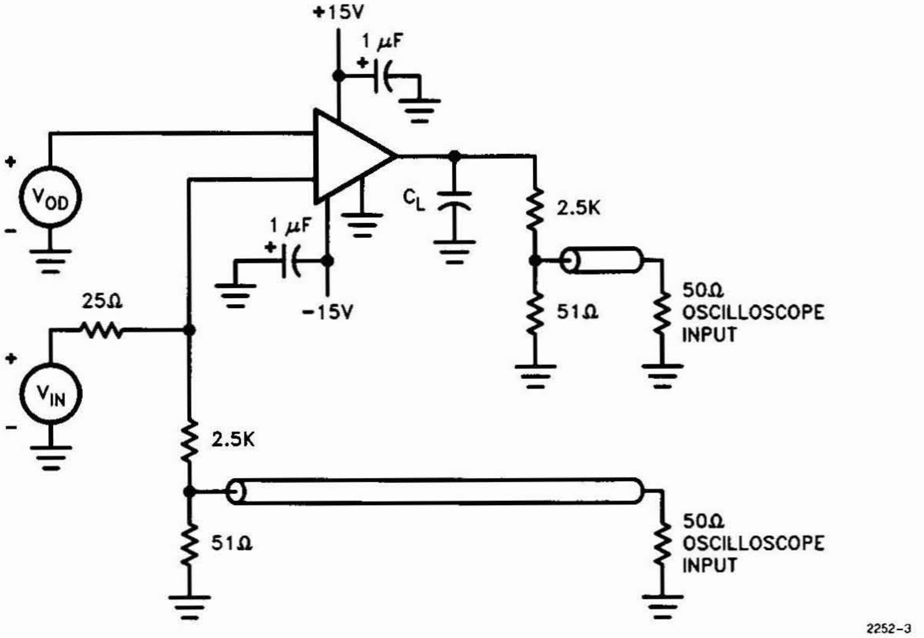
$V_S = \pm 15V$; $C_L = 10$ pF; $T_A = 25°C$; TTL output threshold is 1.4V, CMOS output threshold is 2.5V; unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level EL2252C	Units
T_{PD+}, T_{PD-}	Input to Output Propagation Delay, $0 < V_{IN} < 5V$, 500 mV Overdrive, 2000 V/µs Input Slew Rate TTL Output Swing		6	9	III	ns
	CMOS Output Swing		8		V	ns
T_{PD+}, T_{PD-}	Input to Output Propagation Delay, $-2V < V_{IN} < -1V$, 500 mV Overdrive, 2 ns Input Rise Time TTL Output Swing		5	9	III	ns
	CMOS Output Swing		9		V	ns
T_{PDSYM}	Propagation Delay Change between Positive and Negative Input Slopes		1.25		V	ns

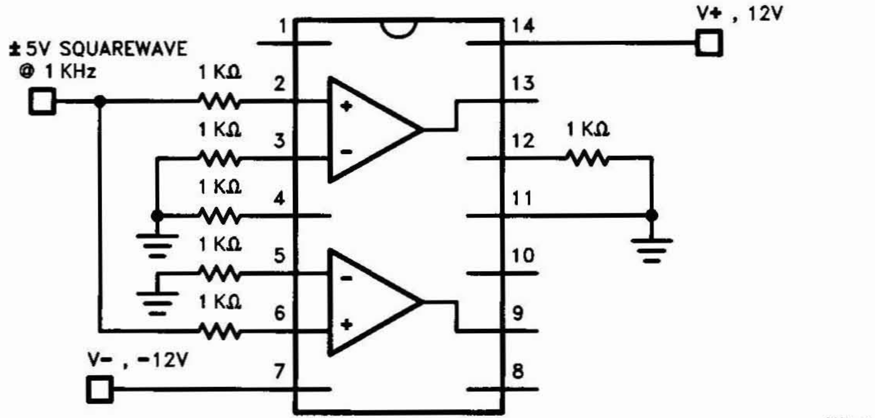
Note 1: Two tests are performed with $V_{CM} = 0V$ to $-9V$ and $V_{CM} = 0V$ to $10V$.

Note 2: Two tests are performed with V+ = 15V, V− changed from −10V to −15V;
V− = −15V, V+ changed from 10V to 15V.

AC Test Circuit

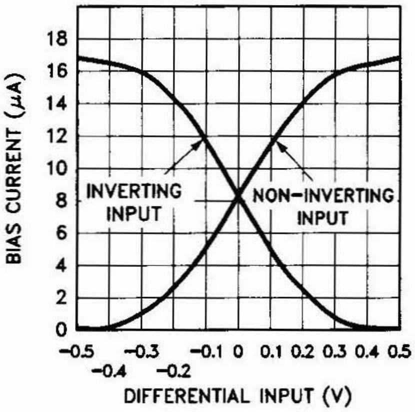

+15V
1 μF
+
+
−
VOD
CL
2.5K
1 μF
+
−15V
25Ω
51Ω
50Ω
OSCILLOSCOPE
INPUT
+
−
VIN
2.5K
51Ω
50Ω
OSCILLOSCOPE
INPUT
2252-3

Burn-In Circuit

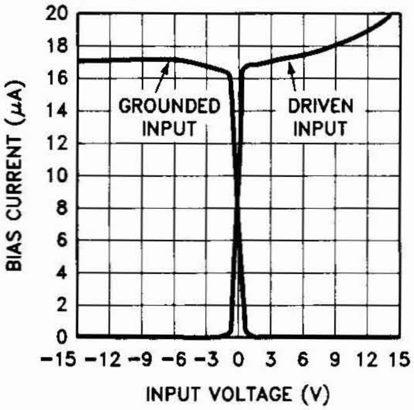

± 5V SQUAREWAVE
@ 1 KHz
1 KΩ
1 KΩ
1 KΩ
1 KΩ
1 KΩ
1
2
3
4
5
6
7
14
13
12
11
10
9
8
+
−
−
+
V+ , 12V
1 KΩ
V− , −12V
2252-4

Typical Performance Curves

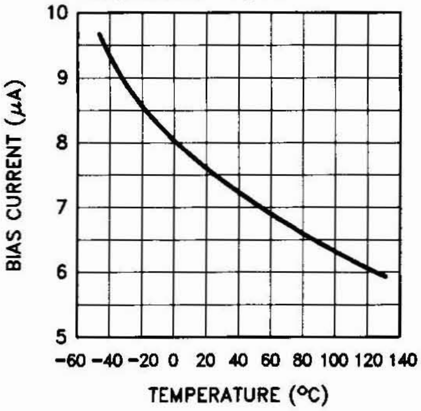
Input Bias Current vs Small Overdrives



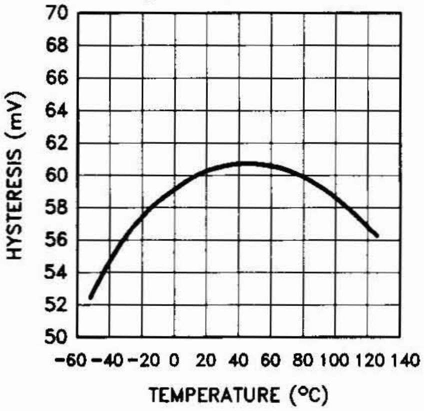
Input Bias Current vs Large Overdrives



Bias Current vs Temperature—Inputs Balanced

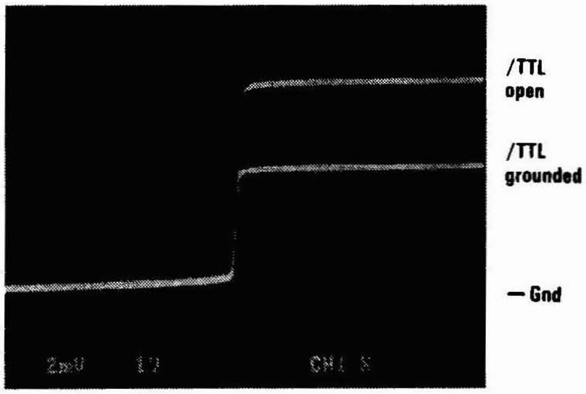


Input Hysteresis Voltage vs Temperature



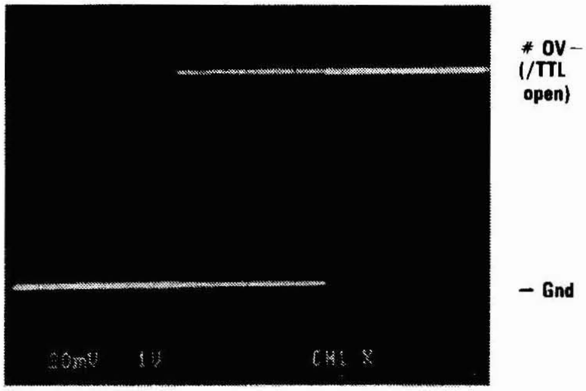
2252-5

Input/Output Transfer Function—HYS Open



2252-6

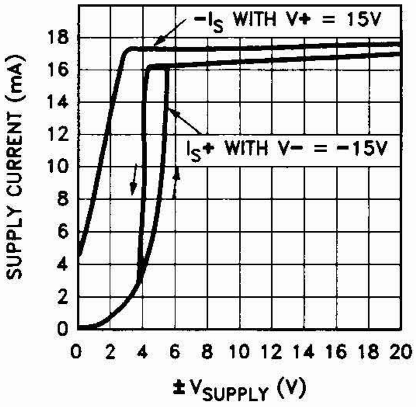
Input/Output Transfer Function—HYS Connected to V



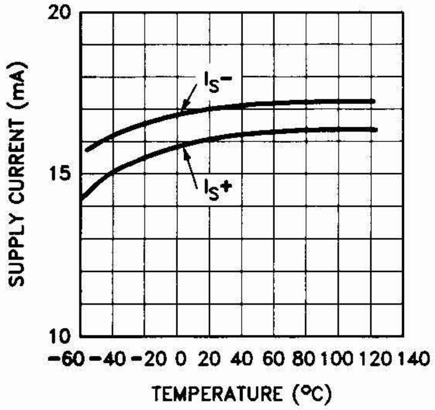
2252-7

Typical Performance Curves — Contd.

Supply Current vs Supply Voltage

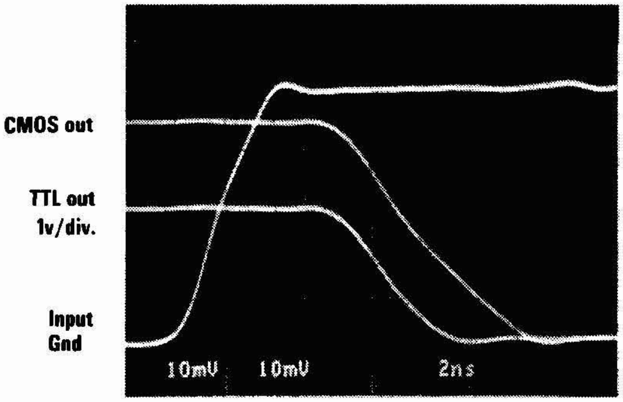


Supply Current vs Temperature (V_S = ±15V)



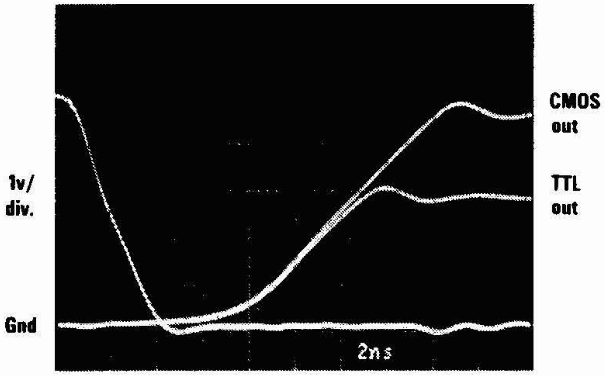
2252-8

Output Delay—0.5V Overdrive



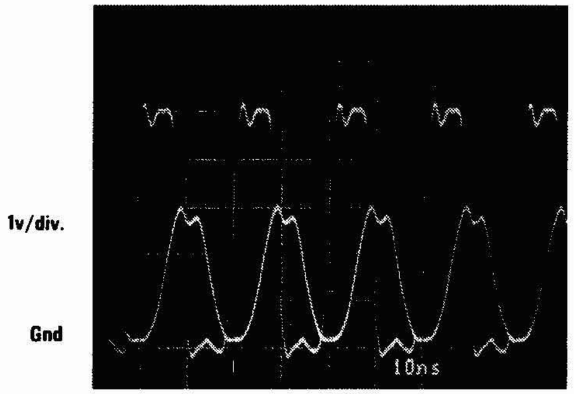
2252-9

Output Delay—0.5V Overdrive



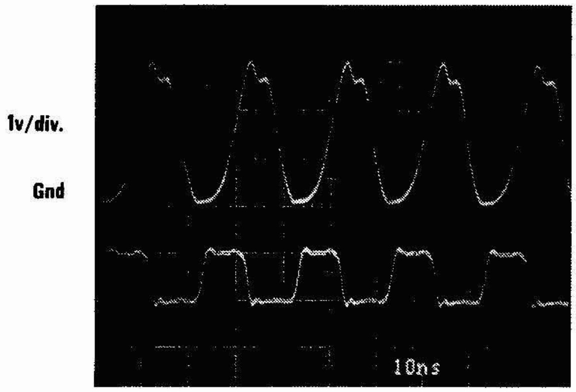
2252-10

Output with 50 MHz CMOS Input



2252-11

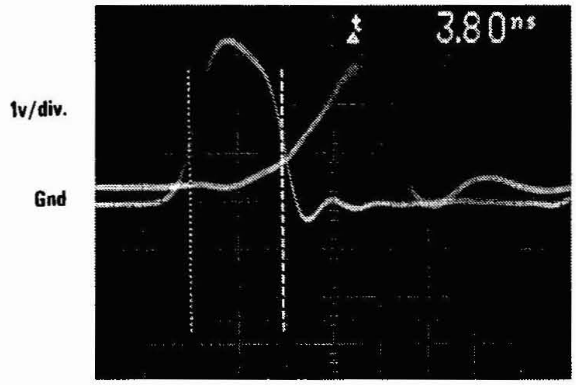
Output with 50 MHz ECL Input



2252-12

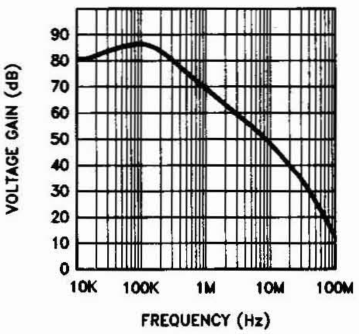
Typical Performance Curves — Contd.

4 ns TTL Glitch Detection

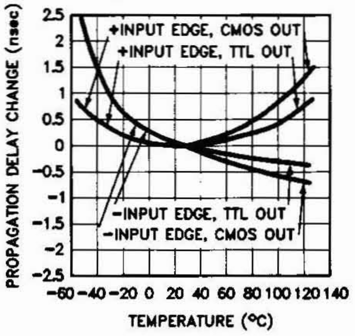


2252-13

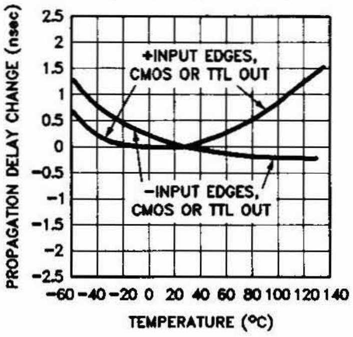
Gain vs Frequency



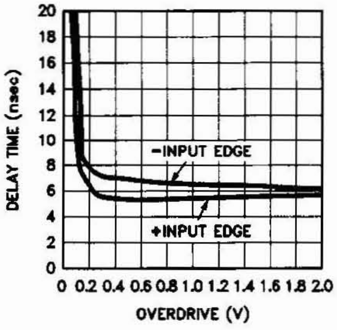
Propagation Delay vs Temperature, CMOS Input



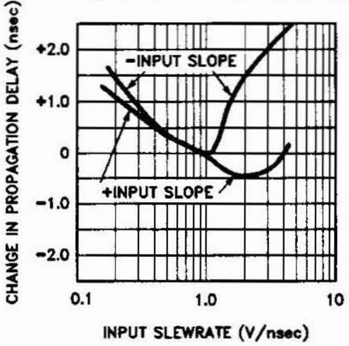
Propagation Delay vs Temperature, ECL Input



Propagation Delay vs Overdrive, CMOS Input

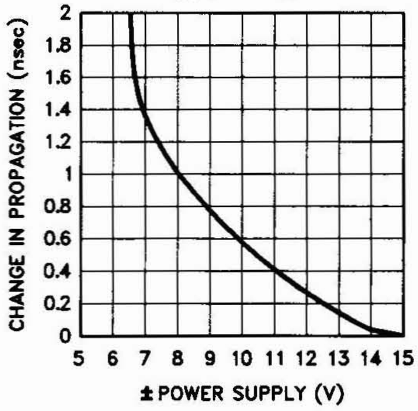


Propagation Delay vs Input Slew Rate, CMOS Input

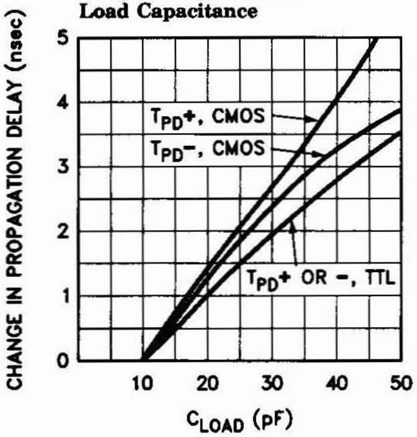


2252-14

Typical Performance Curves — Contd.

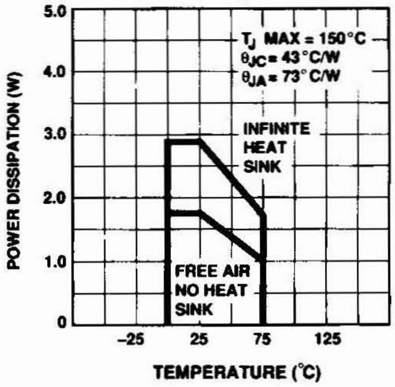


Propagation Delay vs Power Supply Voltage



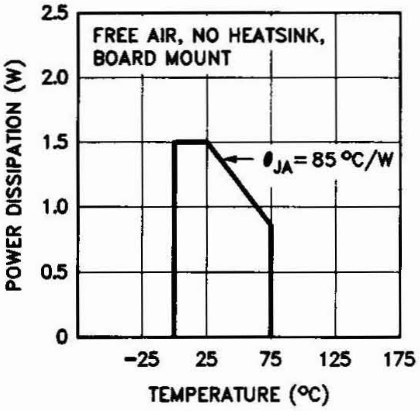
Propagation Delay vs Load Capacitance

2252-15



14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature

2252-16



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature

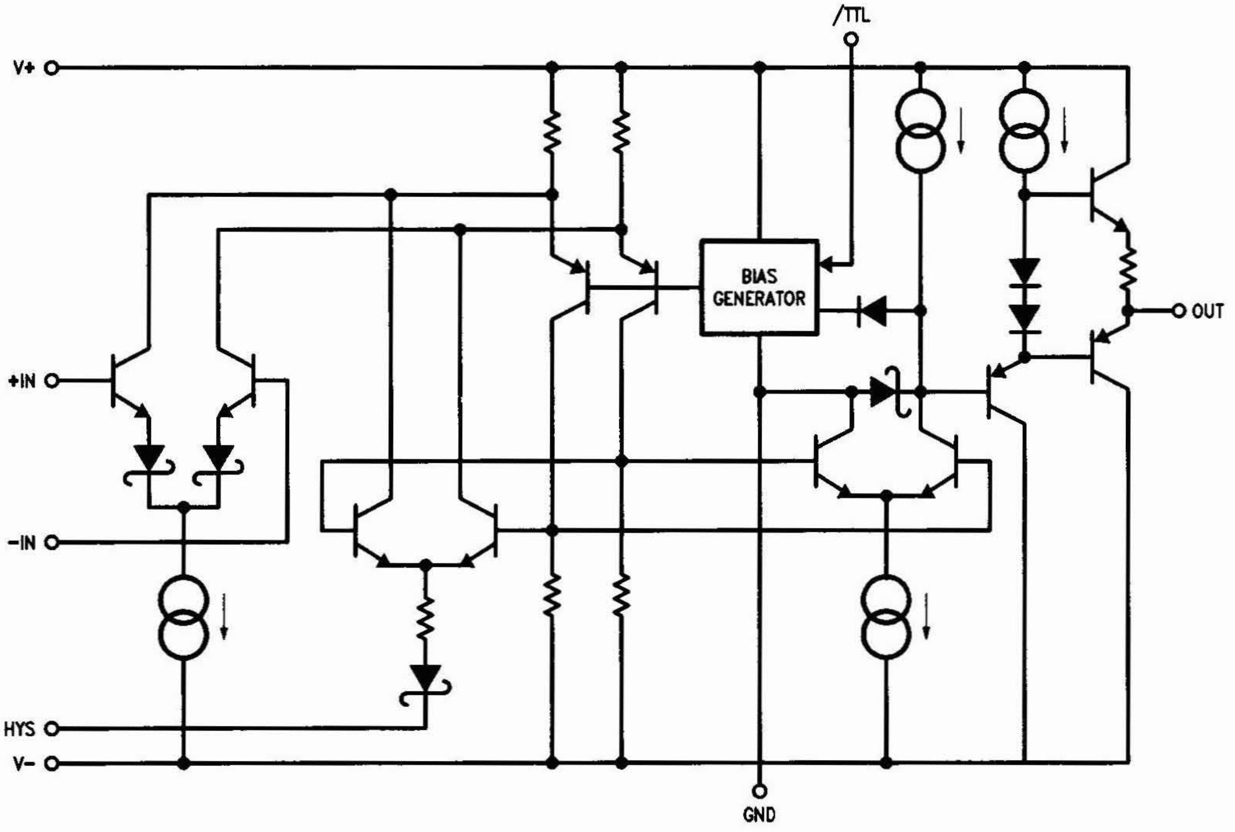
2252-18

EL2252C

Dual 50 MHz Comparator/Pin Receiver

Simplified Schematic

One Comparator



2252-19

Applications Information

The EL2252 is very easy to use and is relatively oscillation-free, but a few items must be attended. The first is that both supplies should be bypassed closely. 1 μF tantalums are very good and no additional smaller capacitors are necessary. The EL2252 requires V− to be at least 5V to preserve AC performance. V+ must be at least 6V for a TTL output swing, 8V for CMOS outputs.

The input voltage range will be referred to the more positive of the two inputs. That is, bringing an input as negative as V− will not cause problems; it's the other input's level that must be considered. The typical input range is +13/−12V when the supplies are ±15V. This range diminishes over temperature and varies with processing; it is wise to set power supplies such that V+ is 5V more positive than the most positive input signal and V− more negative than 6V below the most negative input. ±12V supplies will easily encompass all CMOS and ECL logic inputs. If the input exceeds the device's common-mode input capability, the EL2252 propagation delay and input bias current will increase. Fault currents will occur with inputs a diode below V− or above V+. No damage nor V_{OS} shift will occur even when fault currents within the absolute maximum ratings.

Applications Information — Contd.

One of the few ways in which oscillations can be induced is by connecting a high-Q reactive source impedance to the EL2252 inputs. Such sources are long wires and unterminated coaxial lines. The source impedance should be de-Q'ed. One method is to connect a series resistor to the EL2252 input of around 100Ω value. More resistance will calm the system more effectively, but at the expense of comparator response time. Another method is to install a "snubber" network from comparator input to ground. A snubber is a resistor in series with a small capacitor, around 100Ω and 33 pF. Each physical and electrical environment will require different treatments, although many need none.

The major use of the HYS pin is to suppress noise superimposed on the input signal. By shorting the HYS pin to V^- a ±30 mV hysteresis is placed around the V_{OS} of the comparator input. Leaving the pin open, or more appropriately, grounding the HYS pin removes all hysteresis. Connecting a resistor between HYS and V^- allows an adjustment of the peak-to-peak hysteresis level. Unfortunately, an external resistor cannot track the internal devices properly, so temperature and unit-to-unit variations of hysteresis are increased. The relationship between the resistor and resulting hysteresis level is not linear, but a 1.5k resistor will approximately halve the nominal value.

The time delay of the EL2252 will increase by about 0.7 ns when using full hysteresis.

The EL2252 is specifically designed to be tolerent of large inputs. It will exhibit very much increased delay times for input overdrives below 100 mV. If very small overdrives must be sensed, the EL2018 or EL2019 comparators would be good choices, although they lose accuracies with signal input Slew Rates above 400 V/μs. The EL2252 keeps its timing accuracy with input Slew Rates between 100 V/μs and 4000 V/μs of input Slew Rate.

The output stage drives tens of pF load capacitances without increased overshoot, but propagation delay increases about 1 ns per 10 pF. The output circuit is not a traditional TTL stage, and using an external pullup resistor will not change the V_{OH}. In general setting the output swing to TTL (by grounding the /TTL pin) will optimize overall propagation delay and ±swing symmetry.

EL2252C Macromodel

```
* Connections:    +input
*                 |     -input
*                 |     |     +V
*                 |     |     |     -V
*                 |     |     |     |     HYS
*                 |     |     |     |     |     TTL
*                 |     |     |     |     |     |     output
*                 |     |     |     |     |     |     |
.subckt M2252     2     3     14    7     4     5     13
*
* Application Hints:
*
* Connect pin 4 to ground through 1000 MΩ resistor to inhibit
* Hysteresis; to invoke Hysteresis, connect pin 4 to V-.
*
* Connect pin 5 to ground to invoke TTL VOH; pin 5 may left open
* for CMOS VOH.
*
* To facilitate .OP, set itl1=200, itl2=200, set node 27 to 13.8V,
* and node 30 to -12V.
*
*Input Stage
*
i1 22 7 1.7mA
r1 14 20 300
r2 14 21 300
q1 20  2 22 qn
q2 21  3 22 qn
q3 20 26 23 qn
q4 21 25 23 qn
q13 25 27 20 qp
q14 26 27 21 qp
v1 14 27 1.2V
r3 23 24 1.4k
d1 24 4 ds
r4 25 33 700
r5 26 33 700
q16 33 33 34 qn
q17 34 34 37 qn
v4 37 7 1.2V
*
* 2nd Stage
*
i2 30 7 3mA
i3 14 28 1.5mA
q7 0 35 28 qp
v2 44 0 1.2V
s1 44 35 5 0 swa
s2 45 35 5 0 swb
rsw 14 5 10k
```

EL2252C Macromodel — Contd.

```
v3 45 0 2.5V
q5 0 26 30 qn
q6 28 25 30 qn
d3 0 28 ds
*
* Output Stage
*
i4 14 38 1mA
q8 38 38 39 qn
q9 32 32 39 qp
q10 7 28 32 qp
q11 14 38 40 qn 2
q12 7 28 13 qp 2
r6 40 13 50
c1 28 0 3pF
*
* Models
*
.model qn npn (is=2e-15 bf=120 tf=0.2nS cje=0.2pF cjc=0.2pF ccs=0.2pF)
.model qp pnp (is=0.6e-15 bf=60 tf=0.2nS cje=0.5pF cjc=0.3pF ccs=0.2pF)
.model ds d(is=3e-12 tt=0.05nS eg=0.72V vj=0.58)
.model swa vswitch (von=0v voff=2.5V)
.model swb vswitch (von=2.5 voff=0V)
.ends
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7134C

High Speed, High Current, Line Driver w/3-State

Features

- 3-State output
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 4A Peak drive
- Isolated drains
- Low output impedance—2.5Ω
- Low quiescent current—5 mA
- Wide operating voltage—4.5V–16V

Applications

- Parallel bus line drivers
- EPROM and PROM programming
- Motor controls
- Charge pumps
- Sampling circuits
- Pin drivers

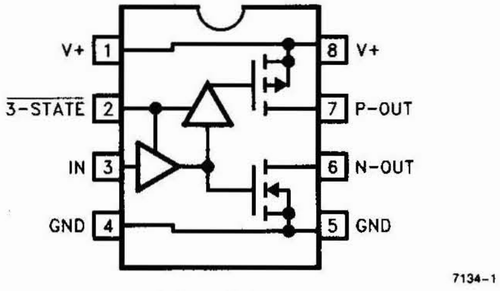
Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL7134CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7134CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL7134C 3-state driver is particularly well suited for ATE and microprocessor based applications. The low quiescent power dissipation makes this part attractive in battery applications. The 4A peak drive capability, makes the EL7134C an excellent choice when driving high speed capacitive lines.

Connection Diagram



Top View

Truth Table

3-State	Input	P-Out	N-Out
0	0	Open	Open
0	1	Open	Open
1	0	HIGH	Open
1	1	Open	LOW

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

EL7134C

High Speed, High Current Line Driver w/3-State

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Peak Output Current	4A	SOIC	570 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

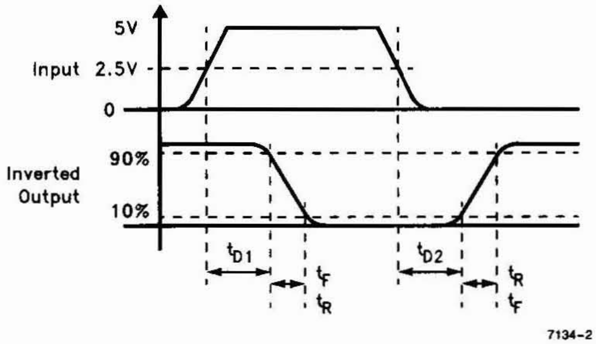
DC Electrical Characteristics $T_A = 25°C$, V+ = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	$V_{IH} = V^+$		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	$V_{IL} = 0V$		0.1	10	I	µA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	$I_{OUT} = -100$ mA		1.5	4	I	Ω
R_{OL}	Pull-Down Resistance	$I_{OUT} = +100$ mA		2	4	I	Ω
I_{OUT}	Output Leakage Current	V+/GND		0.2	10	I	µA
I_{PK}	Peak Output Current	Source Sink		4.0 4.0		V	A
I_{DC}	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I_S	Power Supply Current	Inputs = V+		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

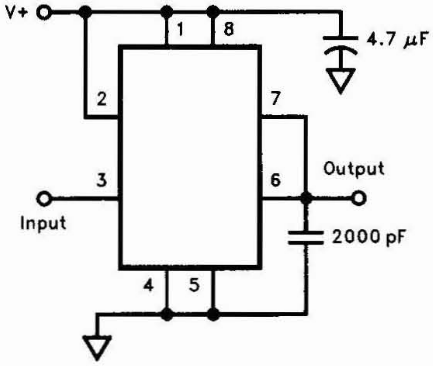
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 1000 pF C_L = 2000 pF		7.5 10	 20	IV	ns
t_F	Fall Time	C_L = 1000 pF C_L = 2000 pF		10 13	 20	IV	ns
$t_{D\text{-}ON}$	Turn-On Delay Time			18	25	IV	ns
$t_{D\text{-}OFF}$	Turn-Off Delay Time			18	25	IV	ns

Timing Table


5V
Input
2.5V
0
Inverted Output
90%
10%
t_{D1}
t_F
t_R
t_{D2}
t_R
t_F

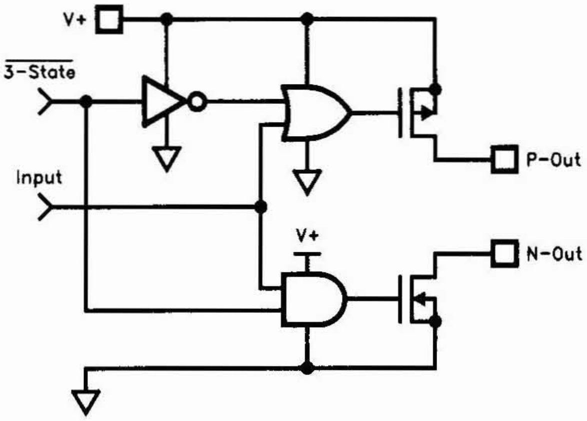
7134-2

Standard Test Configuration


V+
1
8
4.7 µF
2
7
3
6
Output
Input
2000 pF
4
5

7134-3

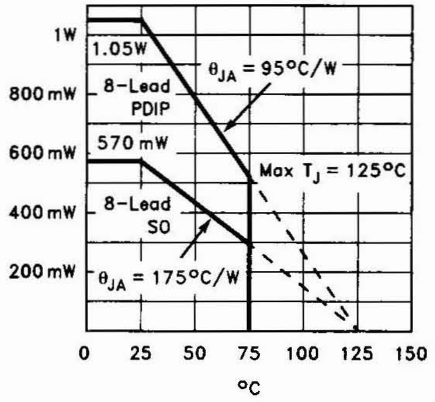
Simplified Schematic


V+
$\overline{\text{3-State}}$
Input
P-Out
V+
N-Out

7134-4

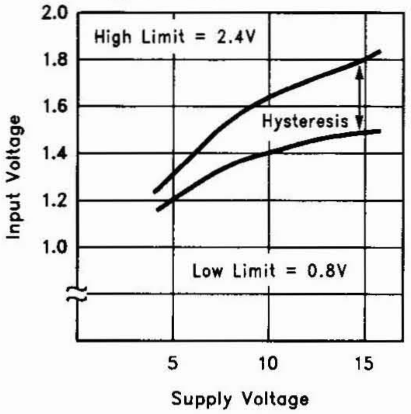
Typical Performance Curve

Max Power/Derating Curves



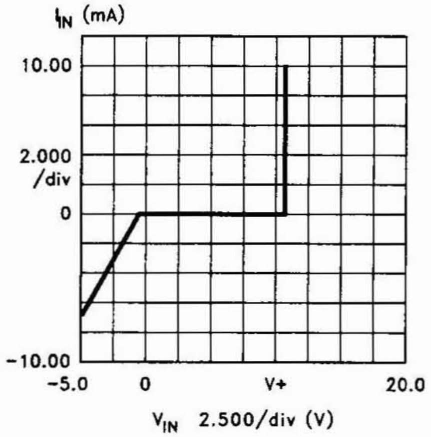
7134-5

Switch Threshold vs Supply Voltage



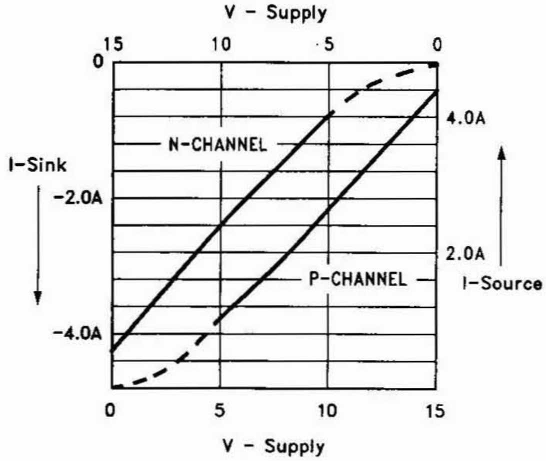
7134-6

Input Current vs Voltage



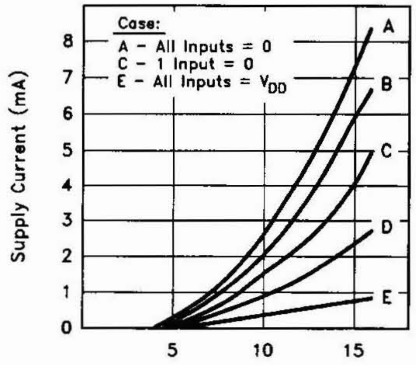
7134-7

Peak Drive vs Supply Voltage



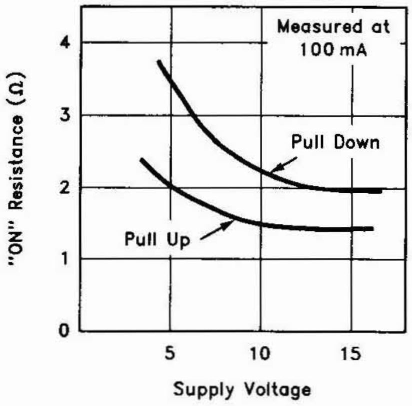
7134-8

Quiescent Supply C



7134-9

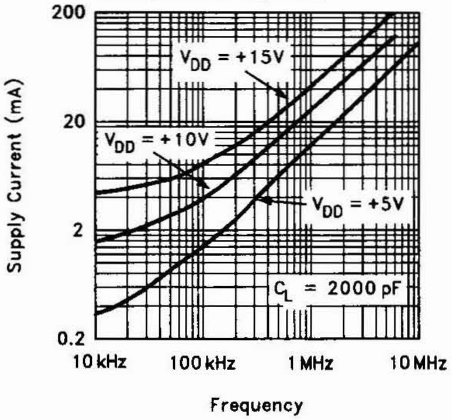
"ON" Resistance vs Supply Voltage



7134-10

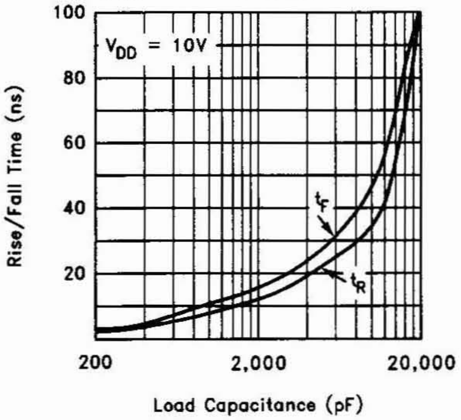
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



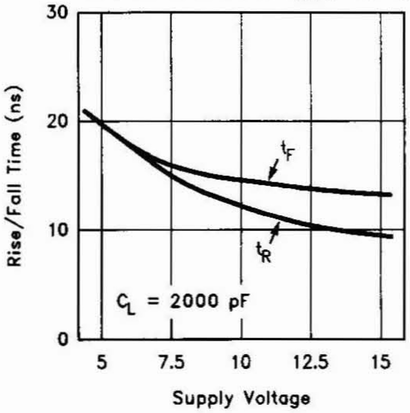
7134-11

Rise/Fall Time vs Load



7134-13

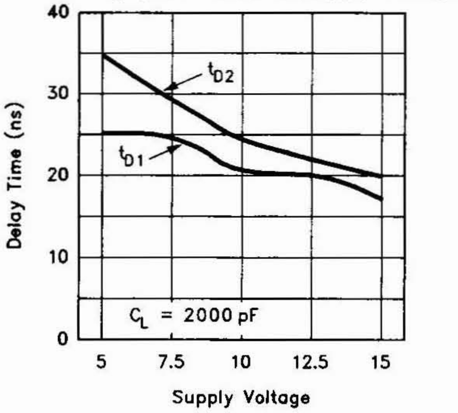
Rise/Fall Time vs Supply Voltage



7134-14

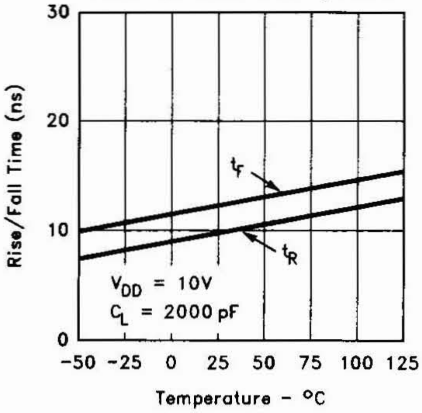
Typical Performance Curve — Contd.

Propagation Delay vs Supply Voltage



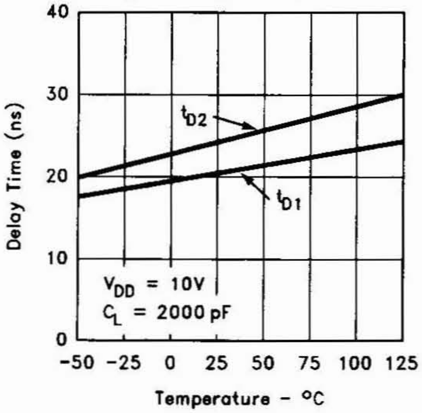
7134-15

Rise/Fall Time vs Temperature



7134-16

Delay vs Temperature



7134-17

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7154C

High Speed, Monolithic Pin Driver

Features

- Comparatively low cost
- 3-State output
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 4A Peak drive
- Isolated drains
- Low output impedance—2.5Ω
- Low quiescent current—5 mA
- Wide operating voltage—4.5V–16V
- Isolated P-channel device
- Separate ground and V_L pins

Applications

- Loaded circuit board testers
- Digital testers
- Level shifting below GND
- IGBT drivers
- CCD drivers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL7154CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7154CS	−40°C to +85°C	8-Pin SOIC	MDP0027

Nominal Operating Voltage Range

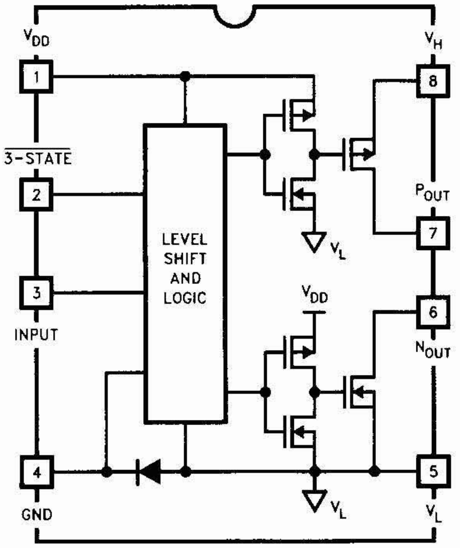
Pin	Min	Max
V_L	−3	0
$V_{DD}-V_L$	5	15
V_H-V_L	2	15
$V_{DD}-V_H$	−0.5	15
V_{DD}	5	15

General Description

The EL7154C 3-state pin driver is particularly well suited for ATE and level shifting applications. The 4A peak drive capability, makes the EL7154C an excellent choice when driving high speed capacitive lines.

The p-channel MOSFET is completely isolated from the power supply, providing a high degree of flexibility. Pin (7) can be grounded, and the output can be taken from pin (8) when a "source follower" output is desired. Then n-channel MOSFET has an isolated drain, but shares a common bus with pre-drivers and level shifter circuits. This is necessary to ensure that the n-channel device can turn off effectively when V_L goes below GND. In some power-FET and IGBT applications, negative drive is desirable to insure effective turn-off. The EL7154 can be used in these applications by returning V_L to a moderate negative potential.

Connection Diagram



7154-1

Top View

Truth Table

3-State	Input	P_{OUT}	N_{OUT}
0	0	Open	Open
0	1	Open	Open
1	0	HIGH	Open
1	1	Open	LOW

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047, #5,352,578, #5,352,389, #5,351,012, #5,374,898

January 1996 Rev B

Absolute Maximum Ratings

Supply (V_{DD} to V_L; $V_H - V_L$, V_H to GND),	
V+ to V_H	16.5V
V_L to GND	−5V
Input Pins	−0.3V below V_L to +0.3V above V_{DD}
Peak Output Current	4A
Storage Temperature Range	−65°C to +150°C

Ambient Operating Temperature	−40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	
SOIC	570 mW
PDIP	1050 mW

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

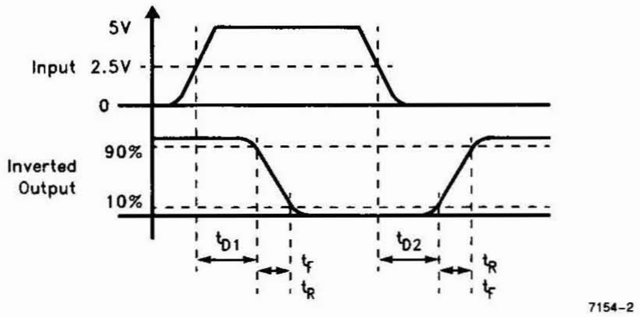
T_A = 25°C, V_{DD} = +12V, V_H = +12V, V_L = −3V, unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	$V_{IH} = V_{DD}$		0.1	10	I	μA
V_{IL}	Logic "0" Input Voltage				0.6	I	V
I_{IL}	Logic "0" Input Current	V_{IL} = 0V		0.1	10	I	μA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		1.5	4	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		2	4	I	Ω
I_{OUT}	Output Leakage Current	V_{DD}/GND		0.2	10	I	μA
I_{PK}	Peak Output Current	Source Sink		4.0 4.0		V	A
I_{DC}	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I_S	Power Supply Current	Inputs = V_{DD}		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V
I_G	Current to GND (Pin 4)			1	10	I	μA
I_H	Off Leakage at V_H	Pin 8 = 0V		1	10	I	μA

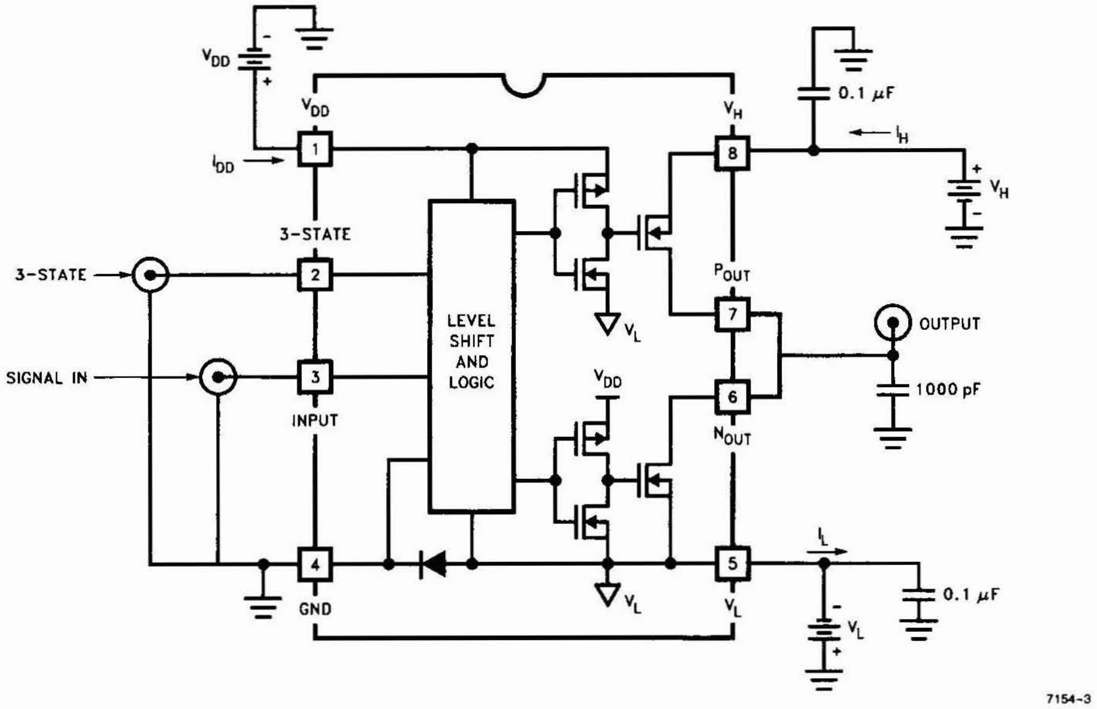
AC Electrical Characteristics $T_A = 25°C$ unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics ($V_{DD} = V_H = 12V$; $V_L = -3V$)							
t_R	Rise Time	C_L = 100 pF C_L = 2000 pF		4 20	25	IV	ns
t_F	Fall Time	C_L = 100 pF C_L = 2000 pF		4 20	25	IV	ns
$t_{D\text{-}1}$	Turn-Off Delay Time	C_L = 2000 pF		20	25	IV	ns
$t_{D\text{-}2}$	Turn-On Delay Time	C_L = 2000 pF		10	25	IV	ns
$t_{D\text{-}1}$	3-State Delay				25	IV	ns
$t_{D\text{-}2}$	3-State Delay				25	IV	ns

Timing Table

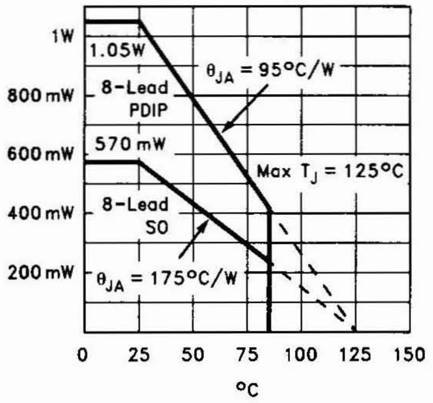

5V
Input
2.5V
0
Inverted
Output
90%
10%
tD1
tF
tR
tD2
tR
tF
7154-2

Standard Test Configuration


VDD
VDD
IDD
1
3-STATE
3-STATE
2
SIGNAL IN
3
INPUT
4
GND
LEVEL
SHIFT
AND
LOGIC
VL
VDD
VL
VH
8
0.1 µF
IH
VH
POUT
7
OUTPUT
1000 pF
6
NOUT
5
VL
IL
VL
0.1 µF
7154-3

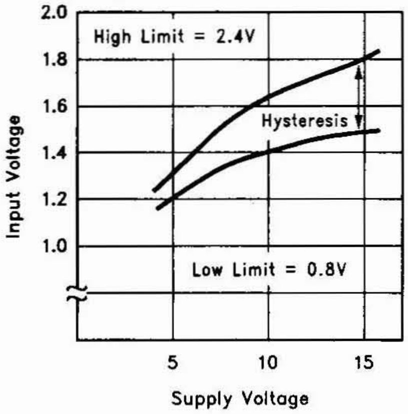
Typical Performance Curves

Max Power/Derating Curves



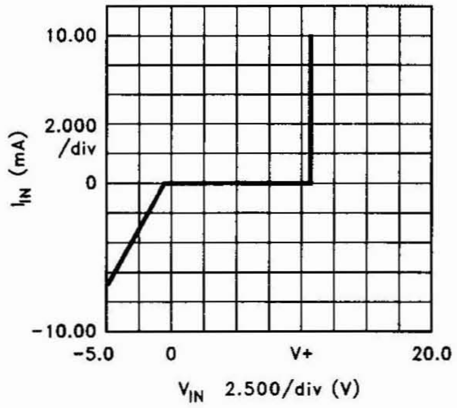
7154-9

Switch Threshold vs Supply Voltage



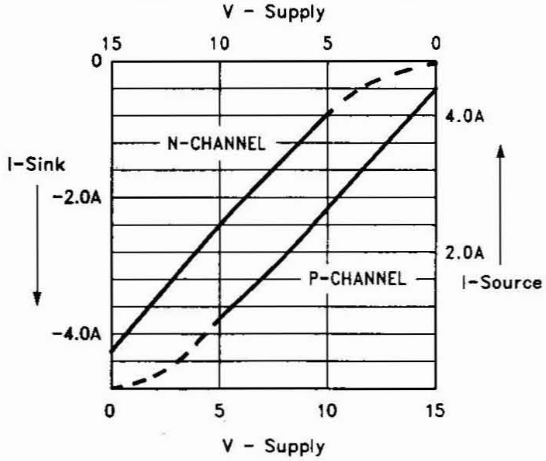
7154-10

Input Current vs Voltage



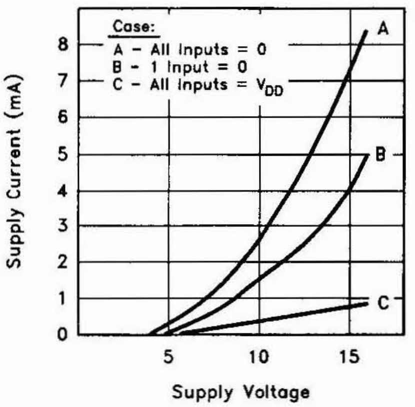
7154-11

Peak Drive vs Supply Voltage



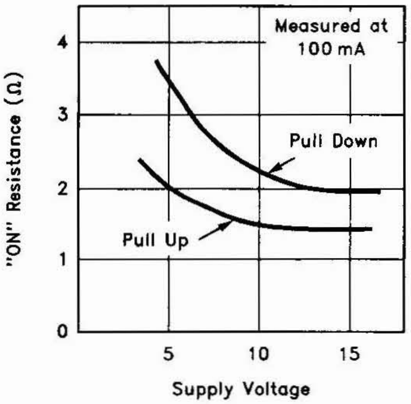
7154-12

Quiescent Supply Current



7154-13

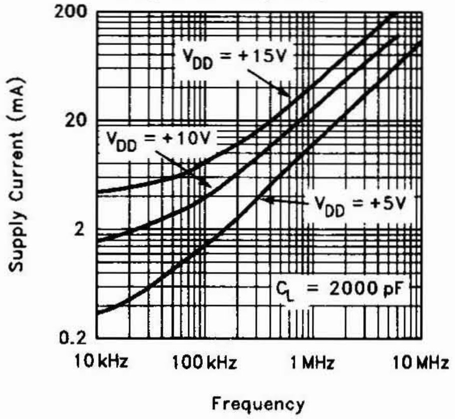
"ON" Resistance vs Supply Voltage



7154-14

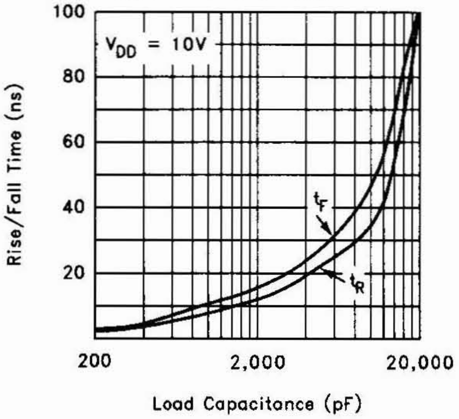
Typical Performance Curves — Contd.

Average Supply Current vs Voltage and Frequency



7154-15

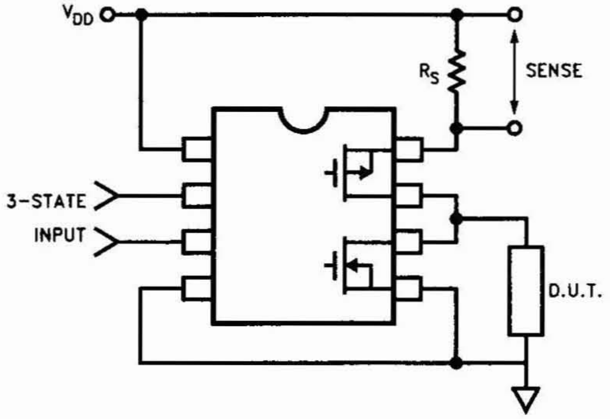
Rise/Fall Time vs Load



7154-16

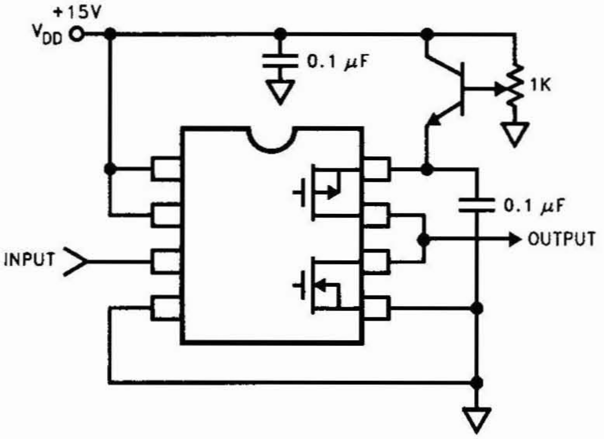
Typical Applications

Pin Driver


V_{DD}
R_S
SENSE
3-STATE
INPUT
D.U.T.

7154-4

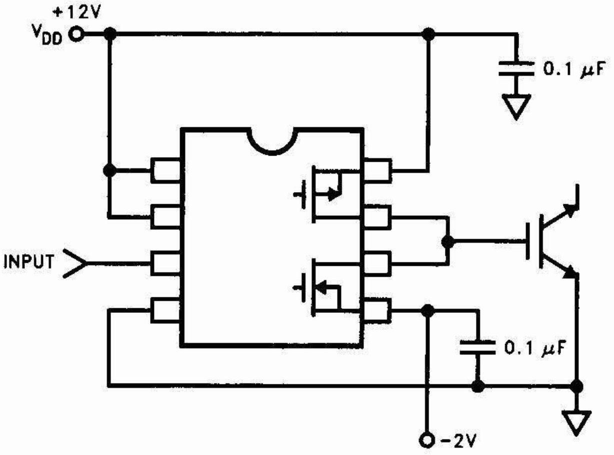
Adjustable Amplitude Pulse Generator


+15V
V_{DD}
0.1 μF
1K
0.1 μF
OUTPUT
INPUT

7154-5

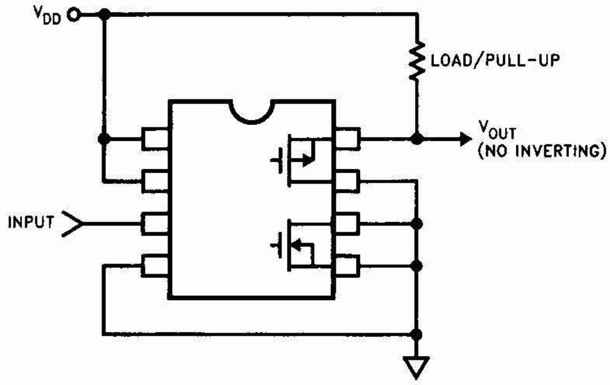
Typical Applications — Contd.

IGBT Driver (with Negative Swing)


+12V
V_{DD}
0.1 µF
INPUT
0.1 µF
-2V

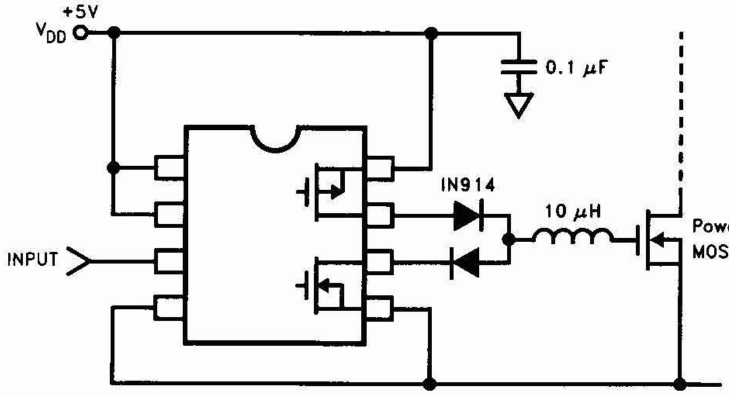
7154-6

PMOS Follower


V_{DD}
LOAD/PULL-UP
V_{OUT}
(NO INVERTING)
INPUT

7154-7

Resonant Gate Driver


+5V
V_{DD}
0.1 µF
IN914
10 µH
Power
MOSFET
INPUT

7154-8

EL7232C

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7232C

Dual Channel, High Speed, High Current Line Driver w/3-State

Features

- 3-State output
- 3V and 5V input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Low, matched output impedance—5Ω
- Low quiescent current—2.5 mA
- Wide operating voltage—4.5V--16V

Applications

- Parallel bus line drivers
- EPROM and PROM programming
- Motor controls
- Charge pumps
- Sampling circuits
- Pin drivers
- Bridge circuits

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL7232CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7232CS	−40°C to +85°C	8-Pin SO	MDP0027

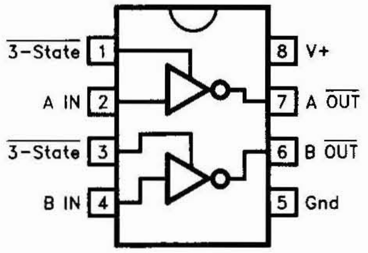
Truth Table

3-State	Input	Output
1	0	1
1	1	0
0	0	Open
0	1	Open

General Description

The EL7232C 3-state drivers are particularly well suited for ATE and microprocessor based applications. The low quiescent power dissipation makes this part attractive in battery applications. The 2A peak drive capability, makes the EL7232C an excellent choice when driving high speed capacitive lines, as well. The input circuitry provides level shifting from TTL levels to the supply rails. The EL7232C is available in 8-pin P-DIP and 8-lead SO packages.

Connection Diagram


$\overline{\text{3-State}}$ 1
A IN 2
$\overline{\text{3-State}}$ 3
B IN 4
8 V+
7 A $\overline{\text{OUT}}$
6 B $\overline{\text{OUT}}$
5 Gnd

7232-1

Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

January 1996 Rev. B

EL7232C

Dual Channel, High Speed, High Current Line Driver w/3-State

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V
Input Pins	−0.3V to +0.3V above V+
Combined Peak Output Current	4A
Storage Temperature Range	−65°C to +150°C
Ambient Operating Temperature	−40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	
SOIC	570 mW
PDIP	1050 mW

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

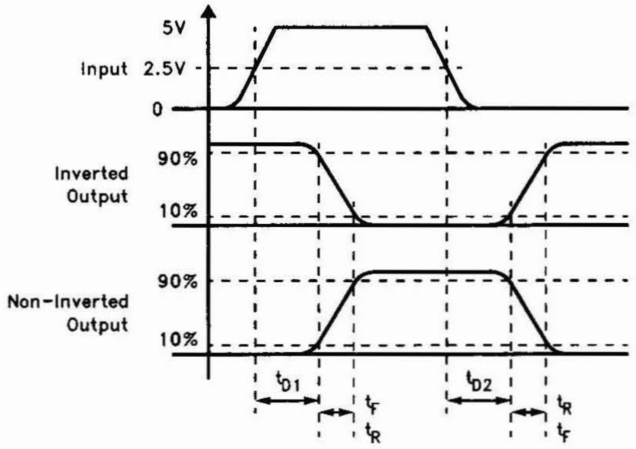
DC Electrical Characteristics $T_A = 25°C$, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	µA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	$I_{OUT} = -100$ mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	$I_{OUT} = +100$ mA		4	6	I	Ω
I_{OFF}	3-State Output Leakage	$V_{OUT} = V+$ $V_{OUT} = 0V$	0.2		10	I	µA
I_{PK}	Peak Output Current	Source Sink		2.0 2.0		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Inputs High		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

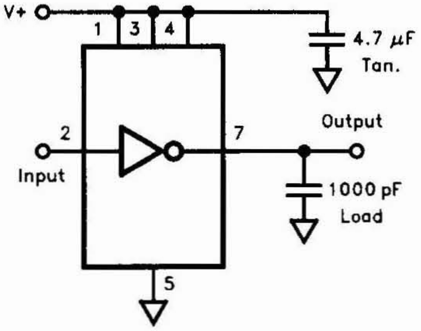
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		7.5 10		IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		10 13	 20	IV	ns
$t_{D\text{-}ON}$	Turn-On Delay Time			18	25	IV	ns
$t_{D\text{-}OFF}$	Turn-Off Delay Time			20	25	IV	ns

Timing Table



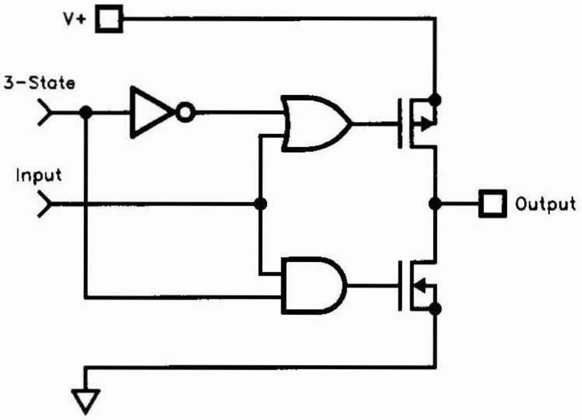
7232-2

Standard Test Configuration


V+
1
3
4
4.7 μF Tan.
2
Input
7
Output
1000 pF Load
5

7232-3

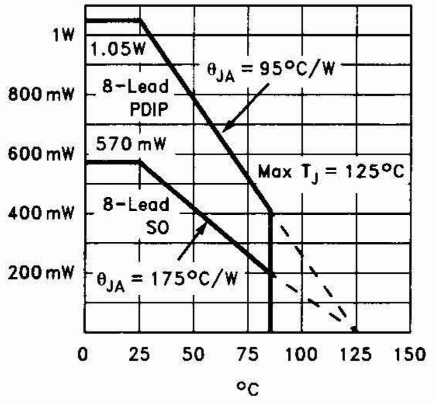
Simplified Schematic


V+
3-State
Input
Output

7232-4

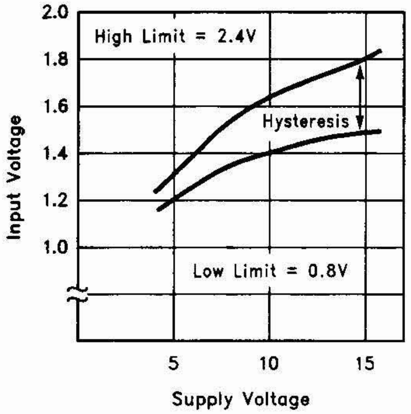
Typical Performance Curve

Max Power/Derating Curves



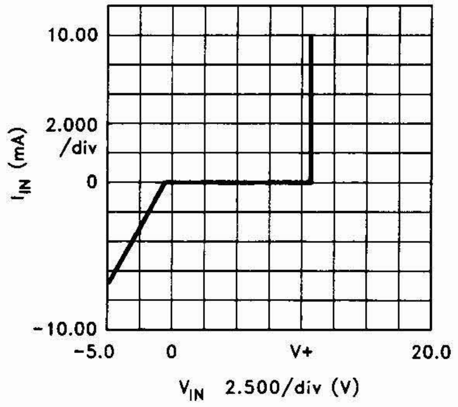
7232-6

Switch Threshold vs Supply Voltage



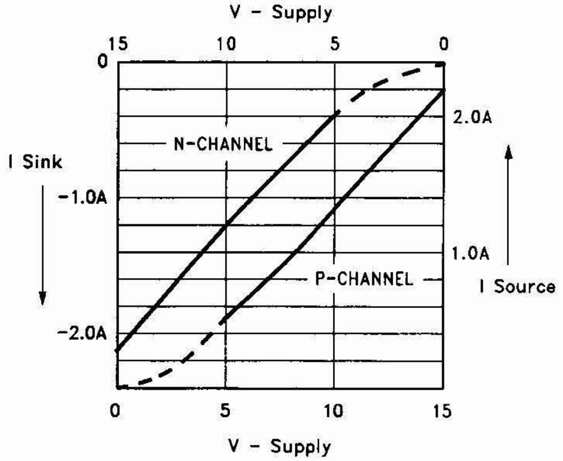
7232-7

Input Current vs Voltage



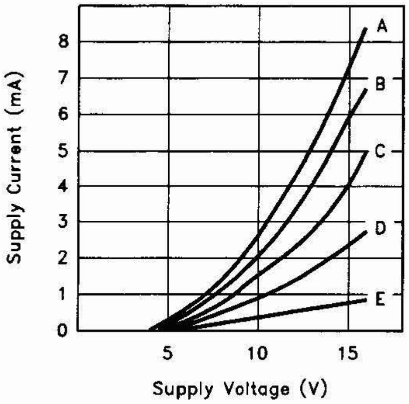
7232-8

Peak Drive vs Supply Voltage



7232-9

Quiescent Supply Current

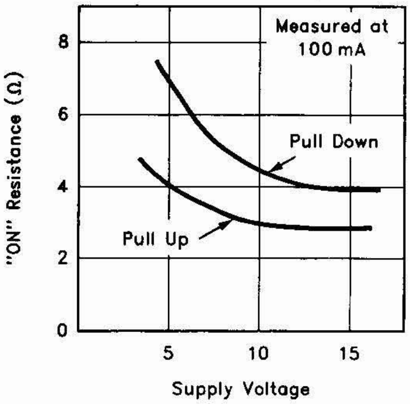


CASE:

A	ALL INPUTS GND
B	3 INPUTS GND
C	2 INPUTS GND
D	1 INPUTS GND
E	ALL INPUTS V+

7232-10

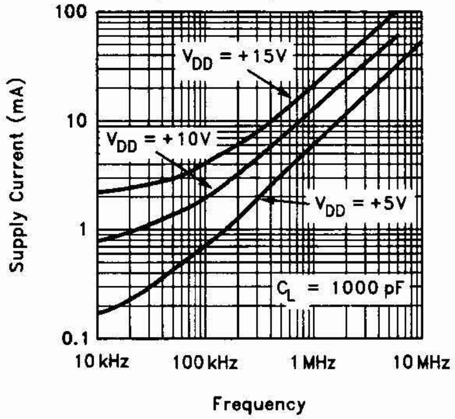
"ON" Resistance vs Supply Voltage



7232-17

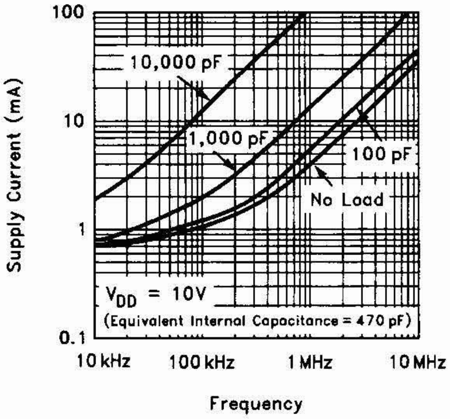
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



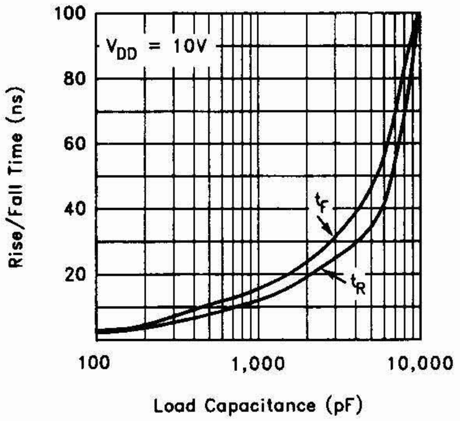
7232-11

Average Supply Current vs Capacitive Load



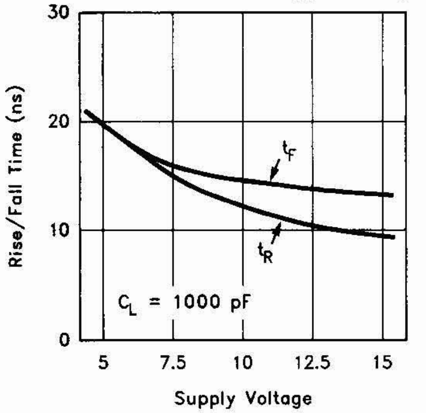
7232-12

Rise/Fall Time vs Load



7232-5

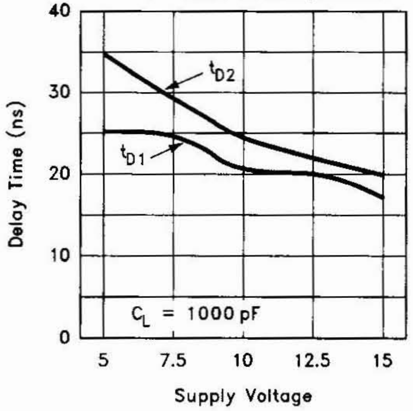
Rise/Fall Time vs Supply Voltage



7232-13

Typical Performance Curve — Contd.

Rise/Fall Time vs Temperature



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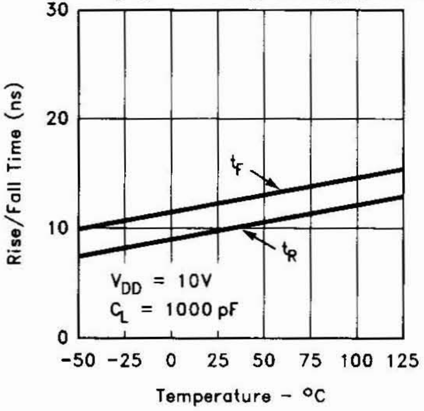
Propagation Delay vs Supply Voltage



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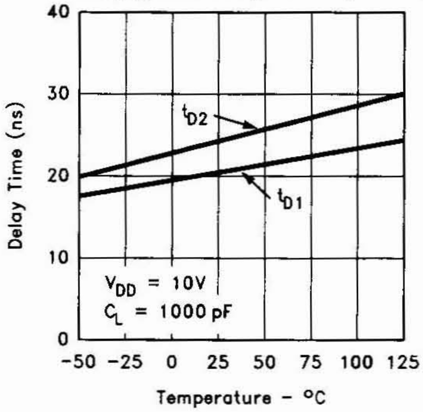
Propagation Delay vs Temperature



7232-16

Application Notes

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

A Low-Noise Variable Gain Control

A Low-Noise Variable Gain Control

by Barry Harvey

The EL2082 current-mode variable gain control IC can be connected in a way to minimize circuit noise. In the usual forward configuration, the circuit has an 80 $nV/\sqrt{Hz}$ input noise which is constant with respect to gain adjustment. The circuit to be shown has an effective input noise which reduces as adjusted gain is increased. The circuit is useful in AGC or leveling functions where a relatively constant output amplitude is required for a range of inputs.

Figure 1 shows the schematic of the configuration. The EL2082 provides an output current equal to $V_{GAIN}/1V$ times the input current. The output impedance of the EL2082 is in the megohm range and the input impedance is about 90Ω, and the part behaves as a current conveyor with adjustable gain. In essence, the EL2082 causes R_{FV} to behave as a variable feedback resistor, and in parallel with R_{FF} controls the gain of the circuit.

With $V_{GAIN} = 0$, the circuit gain is $-R_{FF}/R_{IN}$, and the noise of the EL2082 is gained to zero. In this mode, the circuit gain is maximum and input noise is determined by the op-amp alone. With $V_{GAIN} = 1V$, the circuit gain is $-(R_{FF}/R_{FV})/R_{IN}$, and EL2082 noise mixes with op-amp noise. For the maximum value of $V_{GAIN} = 2V$, the EL2082 dominates the feedback signal and gain is minimum while output noise is increased.

The op-amp must be a current-feedback type for the circuit to work. The CMF amplifier's low-input impedance prevents capacitance at the −input from causing a feedback pole and drastically limiting potential bandwidth. On the other hand, since the time delay of the EL2082 is inside the R_{FV} feedback loop, R_{FV} is a rather high value and must be adjusted to prevent excessive peaking or oscillation when $V_{GAIN} = 2V$. R_{FF} is set to control the maximum gain when $V_{GAIN} = 0$. For the values shown, the output can swing ±2V for 0.25% distortion, and the maximum swing is ±4V.

The input noise is successfully reduced by the circuit when small inputs require higher gain, as shown in Figure 2. The constancy of bandwidth and peaking and gain range are the tradeoffs. Here is a table of measured values:

V_{GAIN}	A_V	BW, −3 dB	Peaking	Input Noise
0	9.03	11 MHz	None	8.7 $nV/\sqrt{Hz}$
0.5V	5.41	26 MHz	None	19 $nV/\sqrt{Hz}$
1.0V	3.91	58 MHz	None	33 $nV/\sqrt{Hz}$
1.5V	3.11	75 MHz	2.2 dB	42 $nV/\sqrt{Hz}$
2.0V	2.62	80 MHz	5.5 dB	57 $nV/\sqrt{Hz}$

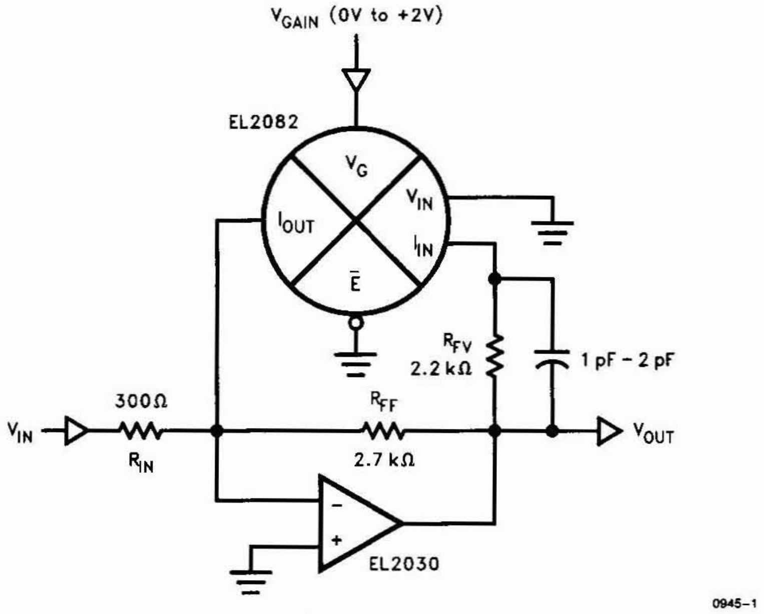
VGAIN (0V to +2V)
EL2082
VG
VIN
IOUT
IIN
Ē
RFV
2.2 kΩ
1 pF - 2 pF
300Ω
RIN
RFF
2.7 kΩ
VIN
VOUT
−
+
EL2030
0945-1

Figure 1

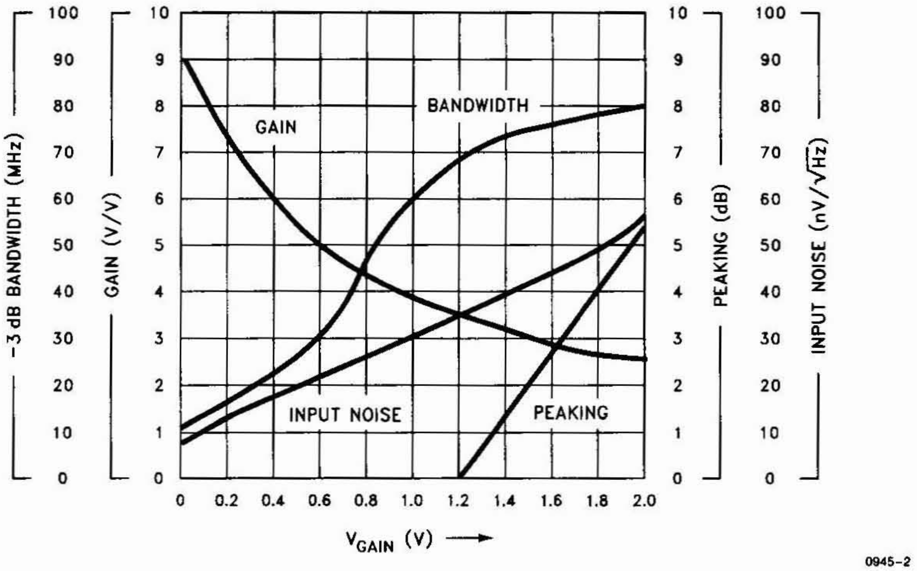

Figure 2

Thermal Considerations of the SO-8

by Barry Siegel

The world owes Phillips and Signetics a great debt in introducing the SO package. It offers a very small footprint, low cost, reliable, surface mounting package demanded by today's high density systems. However, since the thermal impedance of any package is, to the first order, inversely proportional to its area, the SO-8 imposes severe restrictions on the allowable power dissipation of the package. As pointed out in Reference (1), power dissipation raises the die junction temperature, and system reliability may be degraded. This brief sets forth a practical design method to ascertain what, if any, restrictions have to be placed on operating a linear IC in the SO package.

Analysis

Probably the best place to begin is to establish at what junction temperature a given device will be allowed to operate. Most manufacturers rate their junctions at a maximum of 150°C in plastic packages, but for reasons of reliability, a lower number may be mandated. The datasheet usually stipulates θ_{JA}, the thermal impedance from junction to ambient, and the difference between the maximum junction temperature we will allow and the maximum ambient temperature stipulates the thermal budget that we have or the junction temperature rise:

$$\mathrm{Pt} = \frac{T_J(\max) - T_A(\max)}{\theta_{JA}} \qquad (1)$$

where:

Pt = Total Power Dissipated by the Device
$T_J(\max)$ = Maximum Junction Temperature
$T_A(\max)$ = Maximum Ambient Temperature

Power dissipation is comprised of two parts—Pq, the power dissipated by the device due simply to its supply current, and Pl, the power dissipated by the chip as a consequence of driving a load. In general, Pq is independent of Pl and vice versa, so an analysis can be made of each case and the results simply added together to obtain Pt.

The analysis should start with Pq since it is straightforward, and if $T_J(\max)$ is exceeded under quiescent conditions, an alternate strategy is dictated. A word of caution, however, is in order. There are devices such as the EL2001 Unity Gain Buffer that draw a supply current of 1 mA but are capable of driving 100 mA loads. Clearly, in this case, power dissipation will be dominated by Pl. As a case in point, we might examine the EL2120 100 MHz CFA. Its quiescent supply current is specified as 20 mA. A typical video application is to use ±10V power supplies with 150Ω load driven to 8V peak-to-peak with an ambient temperature of 50°C. Under these conditions, Pq is equal to 400 mW, and using the datasheet value of 175°C/W for θ_{JA}, we obtain an average value for T_J of 120°C. What this tells us is that in order to keep the junction below 150°, the junction rise due to driving a load must be under 30°C.

Thermal Considerations of the SO-8

If we assume a steady state (sinusoidal) output voltage of 4V, the power dissipated in the EL2021's output transistor, Pl, would be:

$$Pl = (V+ \; - V_{OUT})(I_{OUT}) \qquad (2)$$

Where:

$$I_{OUT} = \frac{V_{OUT}}{R_L'}$$

$$R_L' = R_L \,||\, R_F$$

The recommended feedback resistor for the EL2120 is typically 300Ω, and for an inverter, R_F is indeed in parallel with R_L. For our particular case, Pl is equal to 240 mW, and the additional increase in junction temperature is 42°C exceeding our earlier requirement of limiting the load incurred junction rise to less than 30° and putting the junction at an average of 162°C.

In the final analysis, either the supply voltages have to be reduced or the load decreased to maintain the junction temperature below 150°. Our best advice is to approach the problem carefully, do the Pq "spot check" first, and verify the conditions with the vendor's applications department.

References

1. "Reliability and the Electronic Engineer" by Barry Siegel, paper given at the EE Times Analog conference, October, 1991
2. "A Simple Method for Characterizing Hybrid Package Thermal Impedances" by Steve Ott and Barry Siegel, *Hybrid Circuit Technology*, June, 1990

DC Restored 100 MHz Current Feedback Video Amplifier

by John Lidgey and Chris Toumazou

Summary

The EL2090 is an extremely versatile video amplifier with an integral on-board DC loop amplifier and sample-hold control circuitry. It is the first complete DC-restored monolithic video amplifier subsystem. It uses a current-feedback video amplifier with a nulling sample and hold amplifier specifically designed to stabilize video performance. This application note includes a video signal restorer with some fundamentals about DC restoration. As an application circuit of the EL2090, a x2 gain video amplifier is described together with a full evaluation circuit and double sided pc-board artwork. The EL2090 is a high-speed part, and some useful tips on layout have been included.

Although DC restoration is not a new concept, the high slew-rate, fast settling-time and low phase distortion at high frequencies provided by Elantec's family of monolithic current-feedback amplifiers, make CFAs the most attractive video amplifier choice for this application.

Video Signal Refresher

Figure 1 is a typical composite video signal which has a standard distribution level of 1V peak-to-peak into 75Ω, and comprises several sections. The video signal is the part containing the visible picture information, with a maximum amplitude between black and white of 0.7V. At the end of the picture information is the front-porch followed by a −0.3V of sync pulse, which is regenerated to provide system synchronization. The back porch is the part of the signal that represents the black or blanking level. In color NTSC systems the chroma or color burst signal is added to the back porch, normally occupying 9 cycles of 3.58 MHz subcarrier (4.43 MHz for PAL systems).

Video signals are often AC coupled to avoid DC bias interaction between different systems. The blanking level of the composite video signal needs to be restored to an externally set DC voltage, which locks the video signal to a predetermined common reference level, ensuring consistency in the picture displayed. This DC reference voltage V_R, sets and controls the picture brightness. The fundamental objective of the DC restore system is to force the DC baseline from the video amplifier to equal the externally set reference voltage V_R.

Figure 2 shows the schematic of a classical DC control servo system.

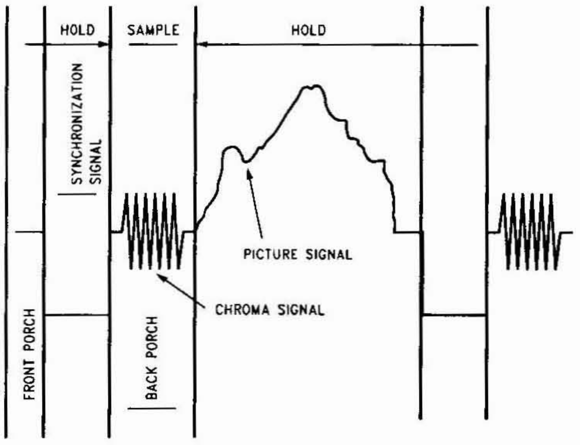

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Figure 1. Video Signal

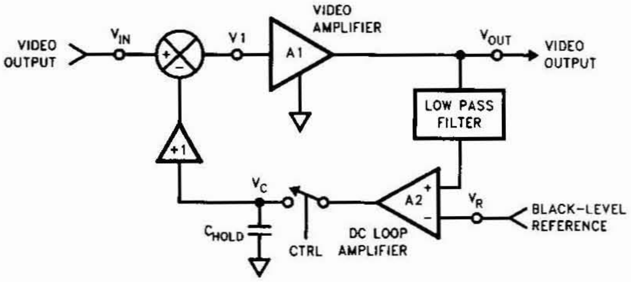

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Figure 2. Classical DC Control Servo

Video Signal Refresher — Contd.

The sync pulse is used to drive the control switch so that the DC servo loop is closed during the back porch of the video signal. The low pass filter removes the chroma burst. Operation of the DC loop is best understood by considering the voltage, V_C, across the hold capacitor, C_{HOLD}. During the back porch sample period, the switch is closed and the hold capacitor charges up. It can be shown from the loop dynamics that,

$$V_C = V_{BP} - V_{BP}/[A_1{*}A_2] - V_R/A_1$$

where V_{BP} is the average back porch voltage for the sample period.

The net result is that $V_{OUT} = V_R - V_{BP}/A_2$, which shows that the output is clamped to V_R with an offset term of $-V_{BP}/A_2$. This offset is clearly small with a high gain DC loop amplifier, A_2. The EL2090 has a DC loop amplifier gain of 15 kV/V, reducing this offset to the order of a few millivolts. During the hold period the switch is open and the stored DC value of V_C is now subtracted from the incoming video signal, making

$$V_1 = V_{IN} - V_{BP} + V_R/A_1$$

and so

$$V_{OUT} = A_1\,[V_{IN} - V_{BP}] + V_R$$

which effectively sets the back porch to V_R and the video signal is amplified by the forward amplifier with gain, A_1.

Subcircuits

The EL2090 DC restored amplifier is a 14-pin monolithic version of the circuit shown in Figure 2. The video amplifier, A_1, is a 100 MHz current feedback amplifier or CFA. These devices offer very high speed performance with excellent differential gain and phase. In many respects the CFA behaves as a conventional op-amp, but there are several key differences that must be considered by the user. In particular the two input impedances of the amplifier are different. The non-inverting input is high impedance and the inverting low impedance. However, the special feature of the CFA is that when in closed loop, the feedback current is determined by resistor, R_F, which controls the bandwidth of the amplifier independently of the gain setting resistor R_G.

The current feedback amplifier is essentially a transimpedance amplifier with an input voltage buffer to create a high input impedance non-inverting input. The transimpedance amplifier is formed by mirroring the output current of the input unity gain buffer into a high impedance internal Z-node and buffering this Z-node voltage through a low impedance output, as shown schematically in Figure 3 below.

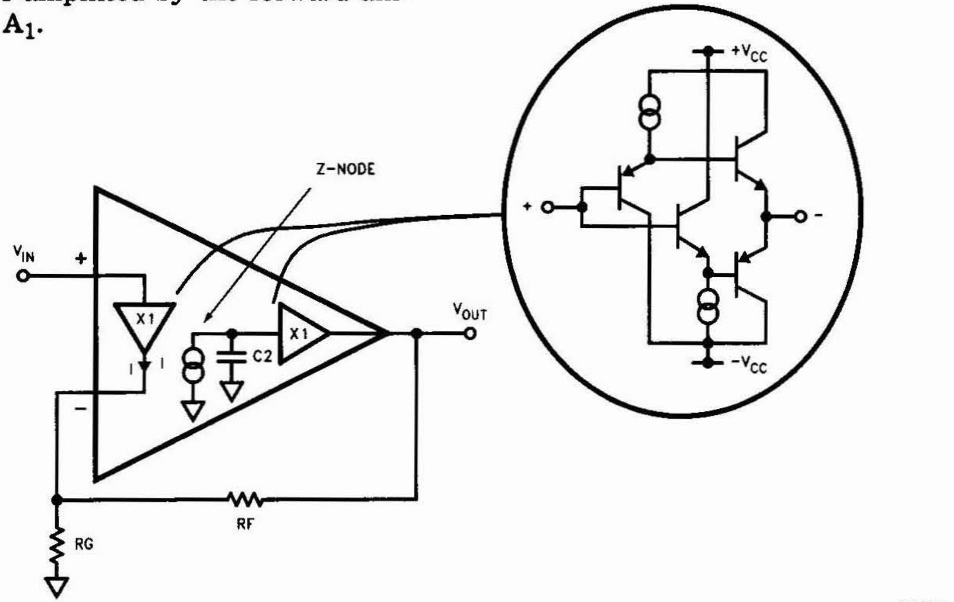

Figure 3. The Current-Feedback Amplifier

Subcircuits — Contd.

The unity gain buffers are a complementary class-AB common-collector stage, with DC current biasing. The slew-rate of the CFA is excellent due to the non-current-limiting input stage. The CFA has only one internal high impedance node (Z), so it is essentially a single pole dominant amplifier. Since the inverting input terminal is the output terminal of a voltage buffer, it is a low impedance point and the feedback signal is current. Intuitively one can see that in closed loop the feedback current through R_F supplies the current demanded by R_G and the input error current into the inverting input terminal. It is this feedback current component of R_F which is used to charge the compensation capacitance at the Z-node. Theoretically it can be shown that the −3 dB bandwidth is approximately,

$$f - 3\text{ dB} = 1/[2\pi R_F C_Z]$$

where C_Z is the compensation capacitance of the Z-node. However, as for conventional op-amps, the closed loop gain, A_1, is simply

$$A_1 = [1 + R_F/R_G],$$

and the −3 dB frequency can be controlled with R_F while the closed loop gain can be set independently with R_G.

Features of the EL2090

Elantec pioneered the development of monolithic CFAs. A first to the market with the CFA the established reputation is confirmed with the EL2090 which is the first monolithic DC restored video amplifier. The device is built with Elantec's fast proprietary complementary bipolar technology which yields NPN and PNP transistors with equivalent AC and DC performance.

The on-chip current-feedback ampifier is optimized for video performance, and since it is a current-feedback amplifier it ensures that the −3 dB bandwidth stays essentially constant for various closed-loop gains. The amplifier performs well at frequencies as high as 100 MHz when driving 75Ω. The sample and hold circuit is optimized for fast sync pulse response; the switch operates in only 40 ns. A particular feature of this sample and hold output buffer is its low output impedance which is fairly constant over frequency and load current. This provides good isolation and thus prevents the DC restore circuit from interfering with video amplifier performance through R_{AZ}.

Note that the burst output of Elantec's EL4581 and EL4583 sync separator chips can drive the Hold input of the 2090 directly.

Typical Application Circuit

Figure 4 shows a component level schematic diagram of the gain x2 DC restored video amplifier. The operation of the circuit is based upon the simple analysis given with the amplifier connected in the non-inverting mode of operation. The application circuit will restore the video DC level in ten scan lines, even if the hold pulse is as short as 2 μs long. The current-feedback resistor R_F of 300Ω will give a stable bandwidth of 115 MHz and all component values are chosen to maintain optimum speed and performance.

DC feedback resistor R_{AZ} is 2 kΩ and is sufficiently larger than R_F to provide reasonable isolation between the sample and hold circuit and video amplifier and thus avoid any video signal coupling back to the sample-hold. R_{AZ} may be (optionally) split into two 1 kΩ resistors and a 820 pF bypass capacitor to reduce unwanted transient feedthrough from the sample and hold to the video signal to less than about 1 mV seen at the amplifier's output. The circuit is designed to operate using ±15V supplies, but it can operate down to ±5V supplies by changing R_{AZ} and C_{AZ} values. Alternatively an inverting configuration video amplifier could be used with appropriate exchange of the input signals to the DC loop amplifier.

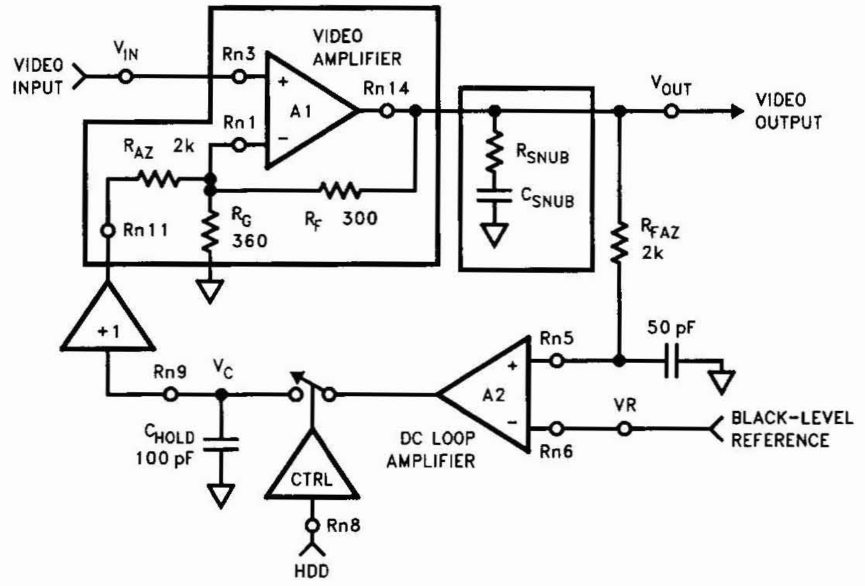

Figure 4. DC Restored Video Amplifier with $A_V = 2$

Design Procedures

1. Determining R_{AZ}

Ideally R_{AZ} should be large to provide good isolation between the sample and hold buffer and the video amplifier. This is because any video-induced current through R_{AZ} will cause changes in the buffer output impedance. A large series R_{AZ} will reduce the effect of buffer output impedance variations and thus preserve the differential gain error of the video amplifier. However, too large a value of R_{AZ} along with the output voltage compliance of the buffer will limit the maximum I_{AZ}, the DC correction current. A lower I_{AZ} will result in a lower restored reference level. Consequently, trade-offs have to be made between R_{AZ}, the maximum restored reference level, and the supply voltage which controls the output voltage compliance of the buffer. The following equations address some of the issues related to the trade-offs.

During the back-porch of the video signal, the sample and hold switch is closed. The servo loop charges C_{HOLD} to a voltage level necessary to bring the video amplifier output to the reference input level. The maximum voltage of C_{HOLD} is limited by the supply voltages.

$$V_{REF} = (V_{BP} * A_1) - V_{AZ}(R_F/R_{AZ}) \qquad (1)$$

where

V_{REF} is the new stabilized back-porch level at the output of the video amplifier.

V_{BP} is the input back-porch offset voltage at the video amplifier input

A_1 is the close loop gain of the video amplifier.

$$A_1 = R_F(1/R_{AZ} + 1/R_G) + 1 \qquad (2)$$

R_F is the feedback resistor of the current-feedback video amplifier. It is nominally 300Ω for $A_1 = +2$. In gain of $+5$ application, R_F should be decreased to 270Ω to maintain gain flatness.

V_{AZ} is the buffered C_{HOLD} voltage developed by the loop to maintain the output at the reference level.

V_{AZ} is limited to the supply rails less 2.5V.

$$-V_{SUPPLY} + 2.5V < V_{AZ} < +V_{SUPPLY} - 2.5V \qquad (3)$$

Analysis of equation (1) shows that since V_{BP}, A_1, and R_F values are established by system requirements, the maximum R_{AZ} is determined by V_{AZ} and V_{REF}. A high R_{AZ} value requires a proportionally high V_{AZ} voltage and low V_{ref}. Outside the back-porch period, the switch is opened. The DC offset is maintained.

2. Design Example

Below examples are intended to show how R_{AZ} changes under different supply voltages and reference level.

Example A.

$V_{SUPPLY} = \pm 15V$
$V_{REF} = 0V$
$A_1 = 2$
$V_{BP} = \pm 1V$
$R_F = 300\Omega$

Applying equation (3), the output voltage compliance V_{AZ} of the sample and hold buffer can be calculated,
$-12.5V \leq V_{AZ} \leq 12.5V$
Using equation (1), $R_{AZ} = 1.8\ k\Omega$ for $V_{BP} = \pm 1V$.
Once R_{AZ} is determined, equation (2) gives $R_G = 360\Omega$.

Example B.

$V_{SUPPLY} = \pm 5V$
$V_{REF} = 0V$
$A_1 = 2$
$V_{BP} = \pm 1V$

Applying equation (1), $R_{AZ} = 375\Omega$ for $V_{BP} = \pm 1V$.
Equation (2) gives $R_G = 1.5\ k\Omega$.

Example C.

$V_{SUPPLY} = \pm 15V$
$V_{REF} = 1$
$A_1 = 2$
$V_{BP} = \pm 1V$

Applying equation (3),
$-12.5V \leq V_{AZ} \leq 12.5V$
$R_F = 300\Omega$
Equation (1) gives
$R_{AZ} = 1.2\ k\Omega$ for $V_{BP} = -1V$
$R_{AZ} = 3.75\ k\Omega$ for $V_{BP} = -1V$
Therefore, $R_{AZ} = 1.2\ k\Omega$
Using equation (2), $R_G = 400\Omega$.

The above examples demonstrate the trade-off between the supply voltage, R_{AZ}, and the reference level. Examples A and B reveal that a lower supply voltage requires a lower R_{AZ}. Examples A and C show that when the supply rails are kept constant, a higher reference level requires a lower R_{AZ}.

3. Determine C_{HOLD}

Fast acquisition time is achieved with small values of C_{HOLD}, but this degrades droop performance. For video the droop needs to be better than ½ IRE in one horizontal line, or less than 3.5 mV in 45 μs for NTSC. The droop is primarily caused by C_{HOLD} voltage decaying. Since the droop of C_{HOLD} is amplified to the output by the ratio R_F/R_{AZ} then C_{HOLD} must be chosen to satisfy $dV_C/dt < 3.5\ mV/45\mu s$ multiply $R_{AZ}/R_F = 510\ V/\mu s$

$R_F = 510V/\mu s$.

Since $dVC/dt = I_{DROOP}/C_{HOLD}$, and the discharge current I_{DROOP} is a maximum of 50 nA, then

C_{HOLD} • 98 pF, or 100 pF, the nearest preferred value.

If R_{AZ} is decreased for lower supply operation, C_{AZ} is correspondingly increased to preserve droop and acquisition characteristics.

4. Acquisition Time

Based on the values shown in Figure 4 the acquisition time is approximately 20μs. Note that it will take 10 chroma-burst of 2μs each to finish settling from a Δ1.0V input signal shift.

Evaluation Printed Circuit Board

A component layout of the application circuit is shown in Figure 5(b) with some additional features.

- V_{REF} is applied externally to the grounded resistor R_{14}, which is decoupled with capacitor C_{11}.
- Optional 75Ω termination resistor has been included at the input and output.
- Built in guard ring on PCB board layout (Figure 5(b)) ensures that leakage from the hold capacitor is minimal to improve droop performance. The guard ring is connected to the S/H Out. The hold capacitor should be low leakage and so mica or mylar capacitors are recommended here.

Evaluation Printed Circuit Board

— Contd.

- Diode clamp circuit to overcome lock-up has been included on board.
- Optional AC input coupling capacitors of about 10 μF has been included.
- Optional snubber circuit has been included.
- Optional R-C low pass filter on hold input logic drive has been included should the logic signal require slowing down.

Printed Circuit Board and Layout Hints

Figure 5(a)–(d) on following pages, shows a component layout together with double sided pc-board. Ground plane is essential throughout to reduce parasitic inductance and stray pickup. Special precautions have been taken to avoid any discontinuity in ground plane since this will make the function of ground plane much less effective. Supply decoupling capacitors are kept close to the power supply pins to ensure good power supply integrity. The feedback path of the video amplifier should be kept as small as possible to avoid deterioration in high frequency gain accuracy. BNC connectors are included at the input and output.

R1 = 360Ω
R2 = 300Ω
R3 = 1 kΩ
R5 = 75Ω
R6 = 220Ω
R7 = 4.7 kΩ
R8 = 10 kΩ
R9 = 10 kΩ
R10 = 2 kΩ
R11 = 100Ω
R12 = 10 kΩ
R13 = 75Ω
R14 = 10 kΩ

C1 = 0.1 μF
C2 = 0.1 μF
C3 = 4.7 μF (Tant.)
C5 = 820 pF
C6 = 39 pF
C7 = 50 pF
C8 = 100 pF
C9 = 0.1 μF (Ceramic)
C10 = 4.7 μF (Tant., 25V)
C11 = 4.7 μF (Tant., 25V)
C12 = 30 pF
C13 = 0.1 μF (Ceramic)

POT1 = 10 kΩ
D1 = 1N914
D2 = ZN458B
D3 = ZN458B (2.45 V_{REF})

Figure 5(a). Component Values

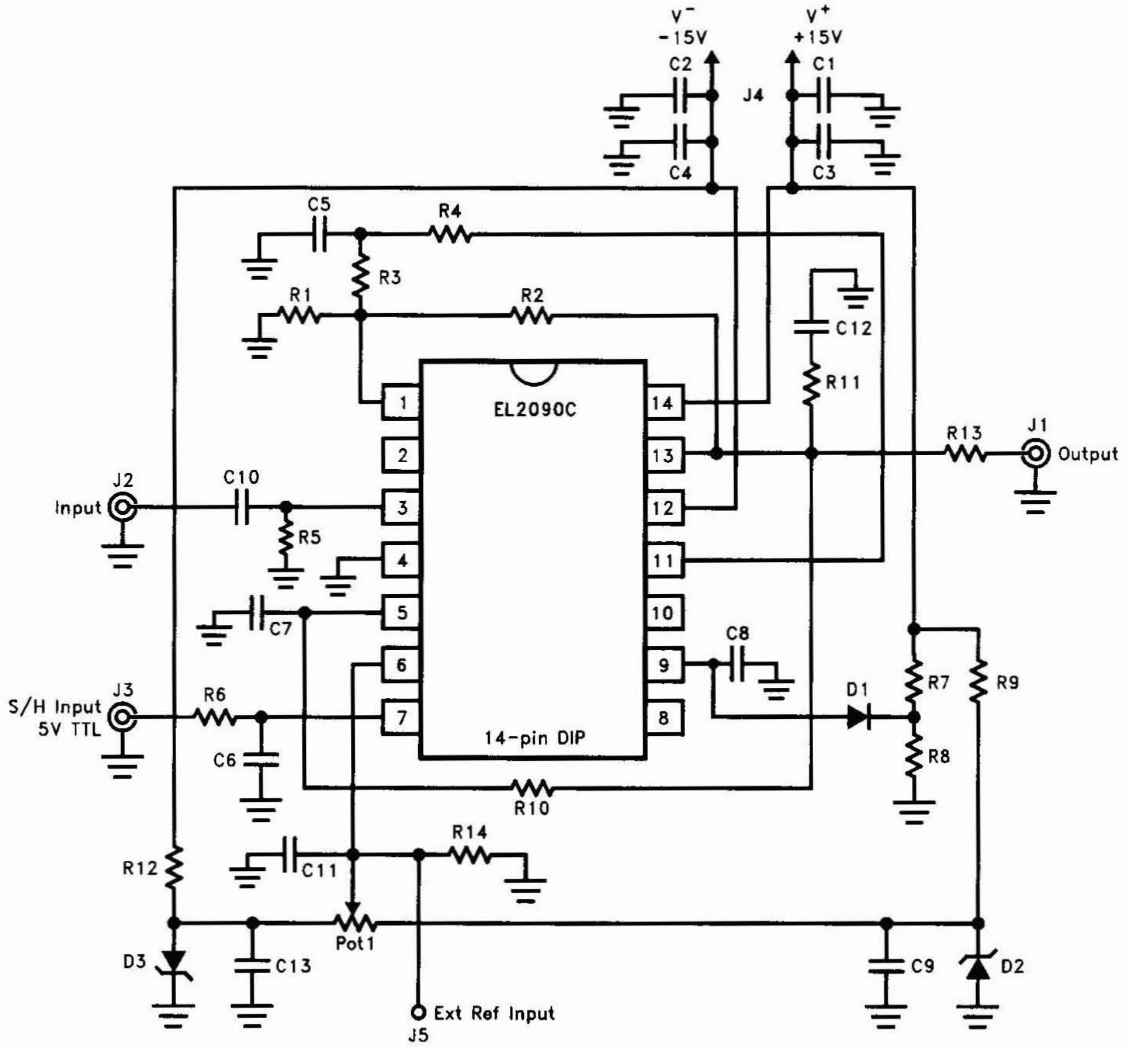
V⁻
-15V
C2
V⁺
+15V
C1
J4
C4
C3
C5
R4
R3
R1
R2
C12
R11
EL2090C
1
2
3
4
5
6
7
14
13
12
11
10
9
8
14-pin DIP
R13
J1
Output
J2
Input
C10
R5
C7
C8
D1
R7
R9
S/H Input
5V TTL
J3
R6
C6
R8
R10
R14
R12
C11
Pot1
D3
C13
C9
D2
Ext Ref Input
J5
0947-2

Figure 5(a)

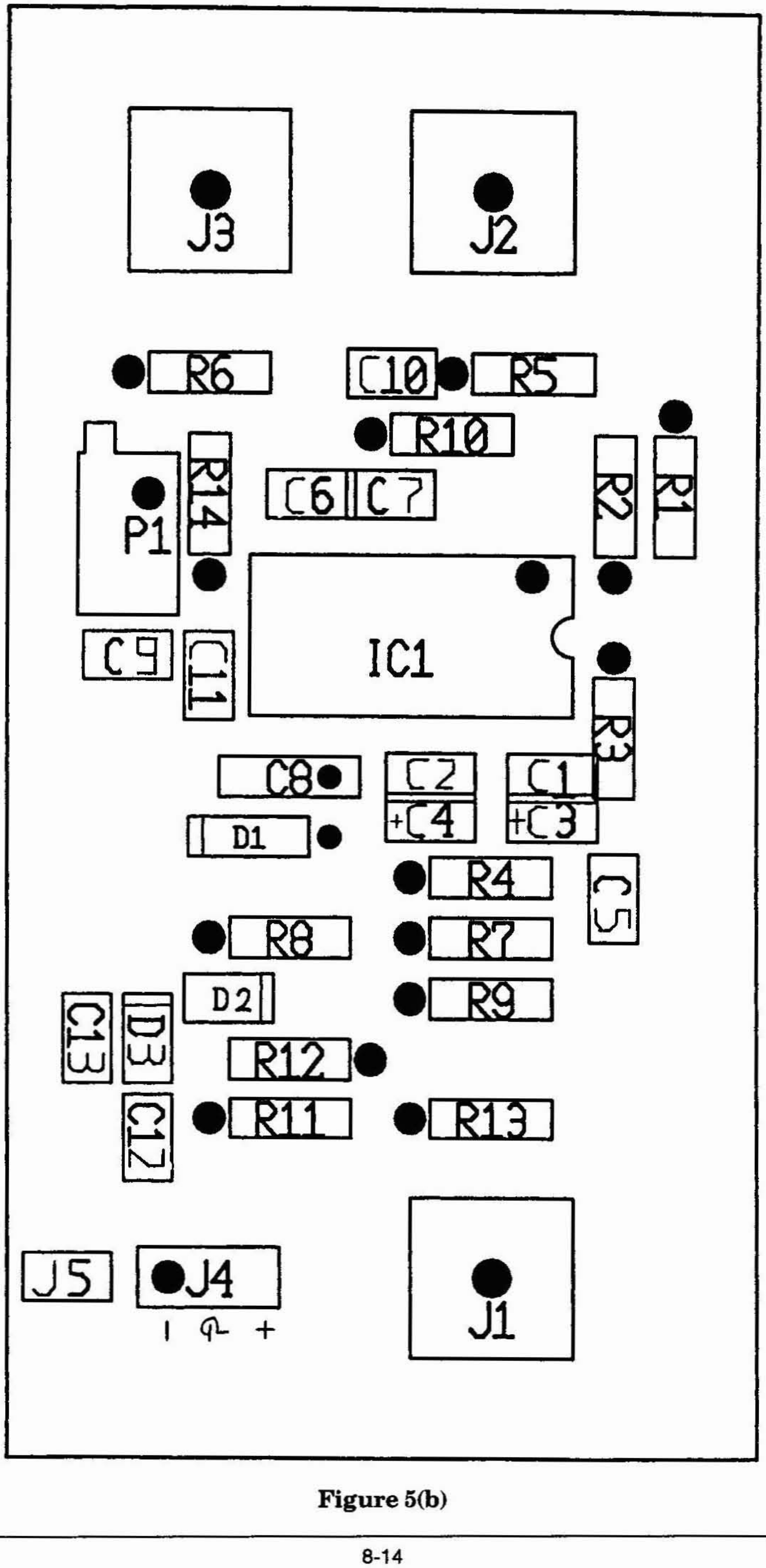
J3
J2
R6
C10
R5
R10
R14
C6
C7
R2
R1
P1
IC1
C9
C11
R3
C8
C2
C1
+C4
+C3
D1
R4
C5
R8
R7
D2
R9
C13
D3
R12
R11
R13
C12
J5
J4
J1
-
+

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Figure 5(b)

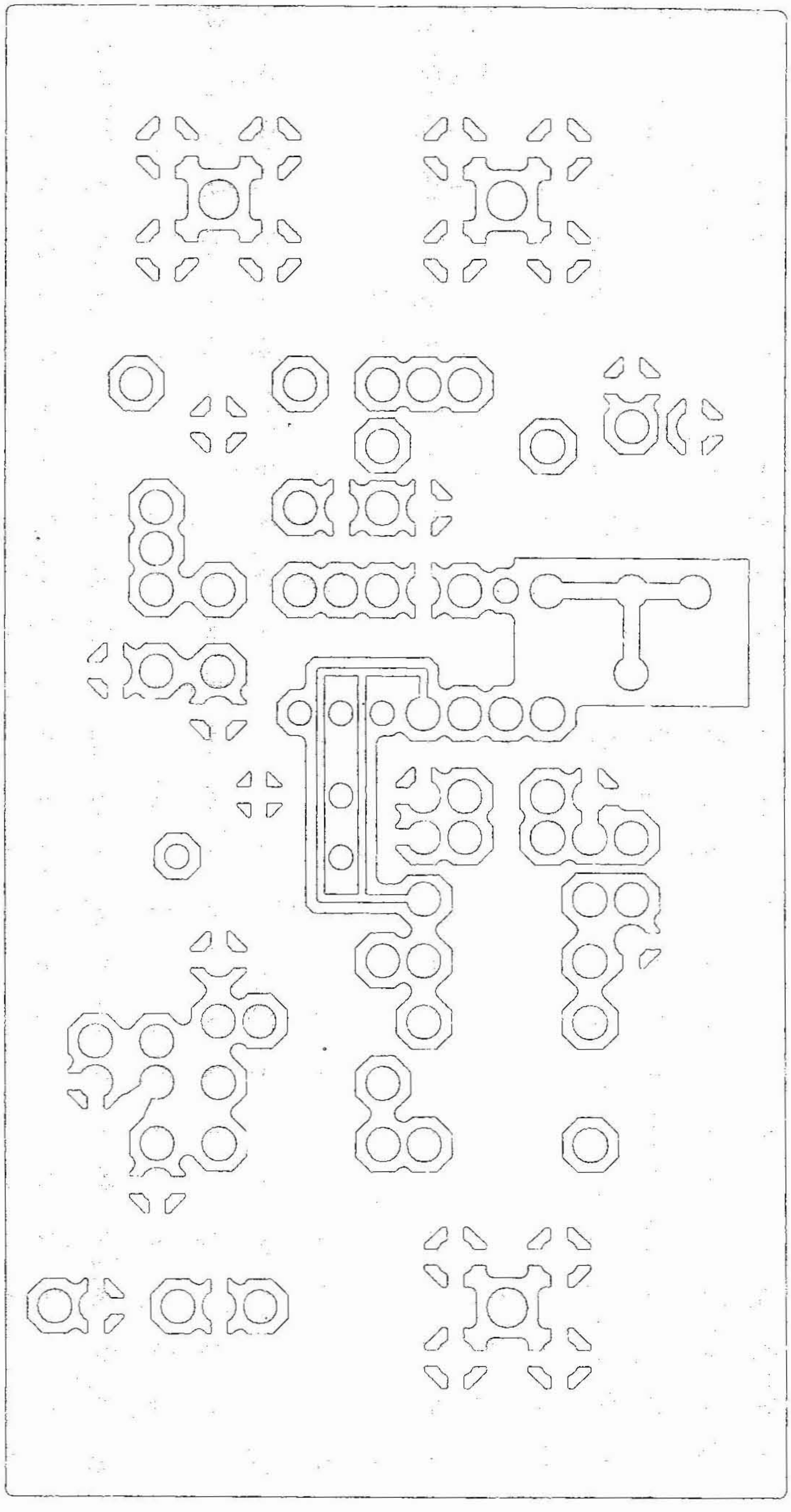


Figure 5(c)

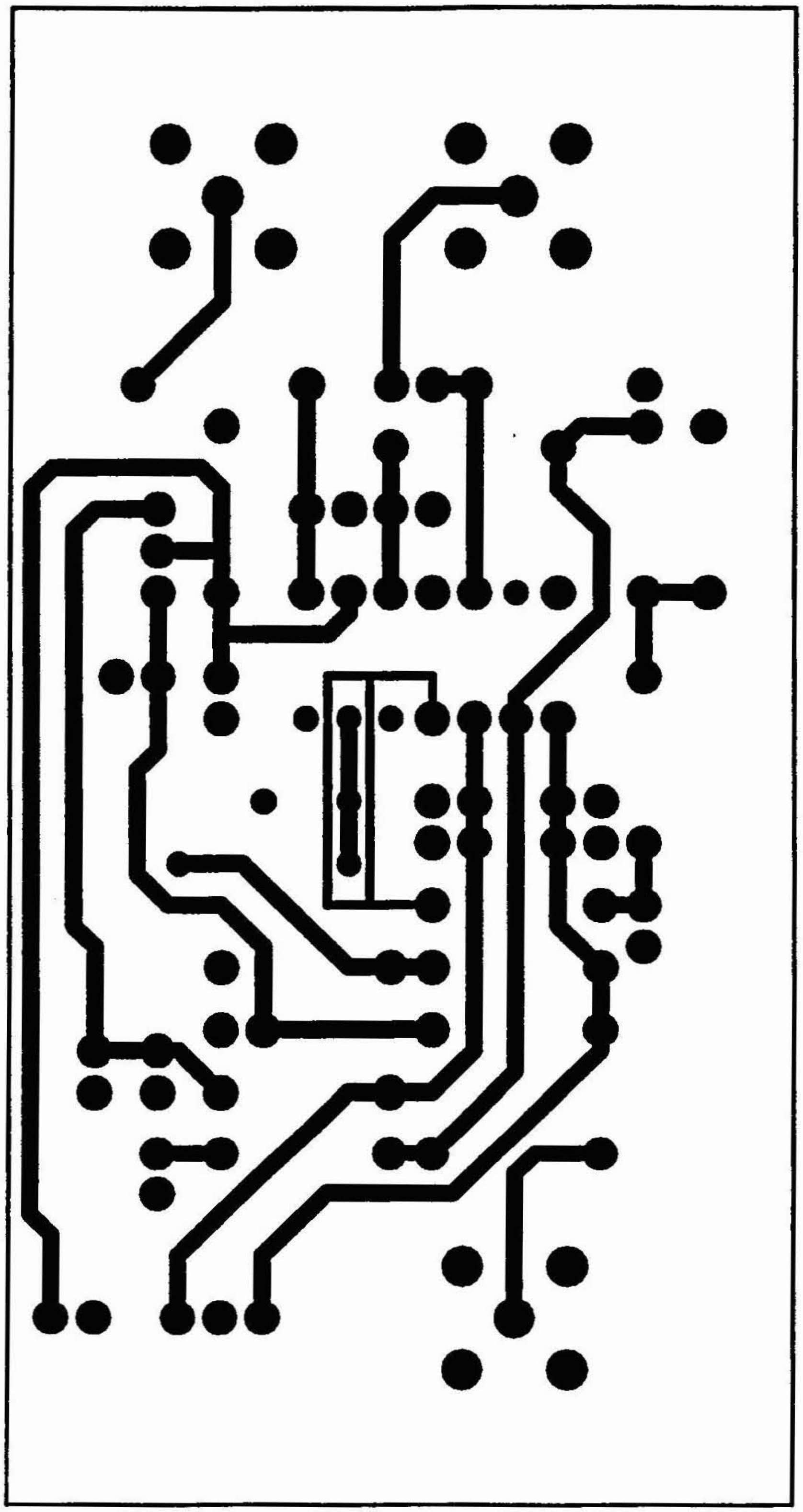


Figure 5(d)

Do's and Don'ts

General Circuit Layout

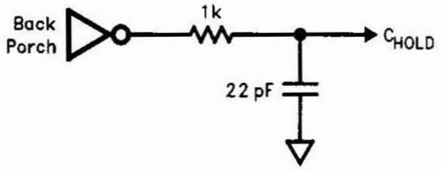
As with all high frequency devices care must be taken with printed circuit board layout. Good ground plane construction is essential and DC power supply integrity must be ensured, so the power supply pins should be bypassed to ground with ceramic capacitors as close to the supply pins of the device as possible. The video current feedback amplifier is, like all CFAs, particularly sensitive to stray capacitance at the inverting input. This capacitance combined with the inverting node input resistance generates an additional high frequency pole in the feedback loop of the CFA leading to gain peaking in the response. Consequently pc-boards should be designed to keep lead lengths as short as possible around the inverting input node, with the ground plane positioned sufficiently far away to prevent this gain peaking effect.

Load Capacitance

In general load capacitance with negative feedback amplifiers causes gain peaking. This is because the load capacitance with the non-zero output resistance of the amplifier creates an additional pole in the feedback loop. The video CFA within the EL2090 is no exception to this and it may be necessary to add a series R-C snubber network to ground to minimize peaking, as shown in the data sheet, where the appropriate components are selected for a particular value of load capacitance.

Sample and Hold Section

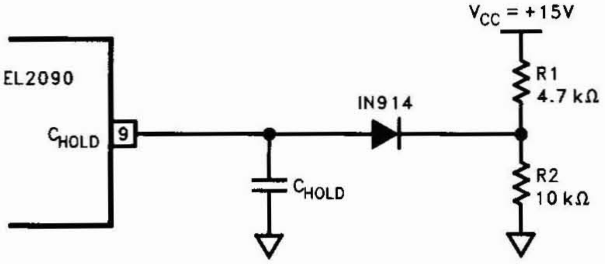
Clock-feedthrough to C_{HOLD} leads to an undesirable hold-step, effecting the DC bias level.



0947-6

Figure 6

Increasing C_{HOLD} is the most direct way of reducing this effect. Under normal operation the loop amplifier only deals with a small correction to V_C and although increasing C_{HOLD} will compromise the slew-rate of the sample-hold section, this is not a practical limitation. However with $C_{HOLD} > 1$ nF and the sampling interval $t_S < 2$ ms then on power up the device may lock-up if V_C approaches V_{CC}, causing the output transistors of the sample-hold amplifier to be taken out of their active region. The net result is that the lock-up does not self recover. Limiting V_C to $V_{CC} - 3V$ using the external clamp circuit shown in Figure 4 prevents this lock-up condition from occuring.



0947-7

Figure 7

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

A Low Distortion Tuneable Sine Wave Oscillator

A Low Distortion Tuneable Sine Wave Oscillator

Summary of Performance Characteristics

One can make a low distortion tuneable oscillator by incorporating an active filter inside an AGC loop. With a control voltage V_G of 0.1 to 2V, one can obtain over a decade of tuning range, with oscillation frequencies from 200 kHz to 3 MHz in this particular design. Total Harmonic Distortion (THD) is -64.5 dB at $V_G = 1V$, and is kept below -57 dB over most of the tuning range. Modulation sidebands due to loop jitter are at least 50 dB down over the entire tuning range, with suppression approaching 56 dB for higher V_G. Linearity error for f_{OSC} vs. V_G is below 4%.

Theory of Operation

The active filter employed in this design is a state variable configuration with the EL2082 in the integrator path providing the frequency control; a circuit diagram of this filter is shown in Figure 1. The EL2082 is a current mode multiplier with low input impedance (95Ω nom) and current source output. It takes the current through the integrator resistor R_{IN}, scales it by a gain determined by V_G, then outputs the scaled signal current to the integrator capacitor C_F. In effect, we can modify the integrator time constants by adjusting V_G; the filter cutoff frequency is then given by

$$f_O = \frac{V_G}{1V} \frac{1}{2\pi\,(R_{IN} + 95\Omega)\,C_F}$$

This filter serves as the feedback network for the oscillator, a block diagram of which is shown in Figure 2. At frequency f_O, the filter phase is 0°, and if the feedback gain is ≥ 1, sustained oscillation will occur. To ensure startup, many oscillator designs have feedback gain >1, but then oscillation amplitude grows until nonlinearity sets in and reduces the loop gain down to 1, thus making it difficult to generate a pure sine wave. In this design, Automatic Gain Control (AGC) is used to maintain unity gain and stable oscillation amplitude. The AGC circuit consists of a 4-quadrant multiplier, which multiplies the output sine wave with itself to generate a DC and double frequency term. The high frequency term is filtered and the remaining DC voltage, which provides a measure of the output amplitude, is used to control the variable gain amplifier. This gain is continually adjusted to provide unity gain around the feedback loop.

Figure 3 shows a circuit diagram of this oscillator. The top part of the diagram is the tuneable active filter implemented using two EL2082s and a EL2444 quad op amp package. The output of this filter is fed back to its input via a unity gain buffer, obtained by connecting pins 11 and 14 of the EL4451 together. To compensate for filter losses, this output is also fed through the resistive divider R_1/R_2 into the variable gain amplifier of the EL4451. By setting the gain to just the right amount, we have unity gain in the feedback path and the necessary conditions for stable oscillation.

This adjustment is provided by an AGC, which consists of the EL4450 four quadrant multiplier and a filter to act as a RMS to DC converter. If the oscillation amplitude increases, the DC control voltage also increases to lower the gain of the EL4451 amplifier. The inverse can be said for oscillation amplitude that is too small. The loop will servo itself until the mean-square of the oscillation amplitude equals the reference voltage on pin 10 of the EL4450. This reference voltage can be changed by adjusting the potentiometer VR1.

Design Notes

Several issues were raised in this design, the first of which is the speed and stability of the AGC loop. A loop that is too slow, as was found early on, is not able to track the oscillation amplitudes; what results is a backlash phenonmenon where the loop is constantly over-correcting and never finds a stable operating point. On the other hand, a loop with too much bandwidth would allow excessive feedthrough, again destabilizing itself and distorting the output. A loop bandwidth of ~16 kHz has been found to be adequate for this design.

Referring to Figure 3, we see that the EL4450 provides a "pseudo" integrator in its output path; it is termed pseudo since it provides rolloff only until ~16 kHz, after which it becomes a unity gain element. To continue the rolloff after 16 kHz, we need an additional lowpass filter with a pole at the above frequency. Although this seems sound, we encountered loop instabilities with this implementation. By moving the pole of the lowpass filter above the "integrator zero", the loop is stabilized.

The residual loop jitter causes another problem: modulation noise. Small variations in the loop voltage that reach the GAIN− pin of the EL4451 modulates the gain and creates Amplitude Modulation (AM) in the output waveform. Although this modulation is small, it is observable on the spectrum analyzer as sidebands around the fundamental. To reduce these sidebands we lowered the feedback into the multiplier, set by R_1 and R_2. Since the loop voltage directly modulates this feedback, by lowering the feedback we also lower the modulated components.

Another problem is the limited Q provided by the active filter network. As opposed to a crystal or LC tuned circuits, we are limited to painfully low Q's in this filter. Since $Q \neq 1$ unbalances the gain between filter stages, there is a practical limit to Q before the 2nd integrator is overdriven. Ideally we would like a high Q to reduce phase noise and to reduce the loop jitter. Unfortunately in this implementation, while $Q > 1$ does reduce modulation effects, it also increases the THD due to the gain unbalance mentioned earlier. In addition, a $Q > 1$ also introduces clipping problems in that during startup, the oscillator can swing to large amplitudes and clip, and the AGC has no hope of recovering from such an unhappy beginning. Hence, a $Q = 1$ was chosen for this design to provide reliable startup and lower THD.

As the frequency of operation increases, we see peaking in the active filter due to increased phase shifts through the op amp stages. Once the peaking causes the filter gain to exceed 0 dB at 0° filter phase, the AGC is no longer able to keep the feedback gain to 1, and clipping occurs in the oscillator output. For this reason it is recommended that the oscillation frequency be kept under 3.5 MHz. The range of operation in this design thus lies quite close to the upper limit. For those desiring lower frequencies of operation some recommended component values are given below:

Tuning Range	R_{in}	C_F	R_1	R_2	C_1	C_2
20 kHz–300 kHz	3k	330 pF	330	240	10 nF	10 nF
200 kHz–3 MHz	3k	33 pF	330	120	1 nF	1 nF

The current design runs on a supply of ±5V. It is possible to push the upper frequency limit to about 4 MHz by operating on ±12V supplies, provided that the current limiting resistor R_Z for the LM337 is raised to 2 kΩ.

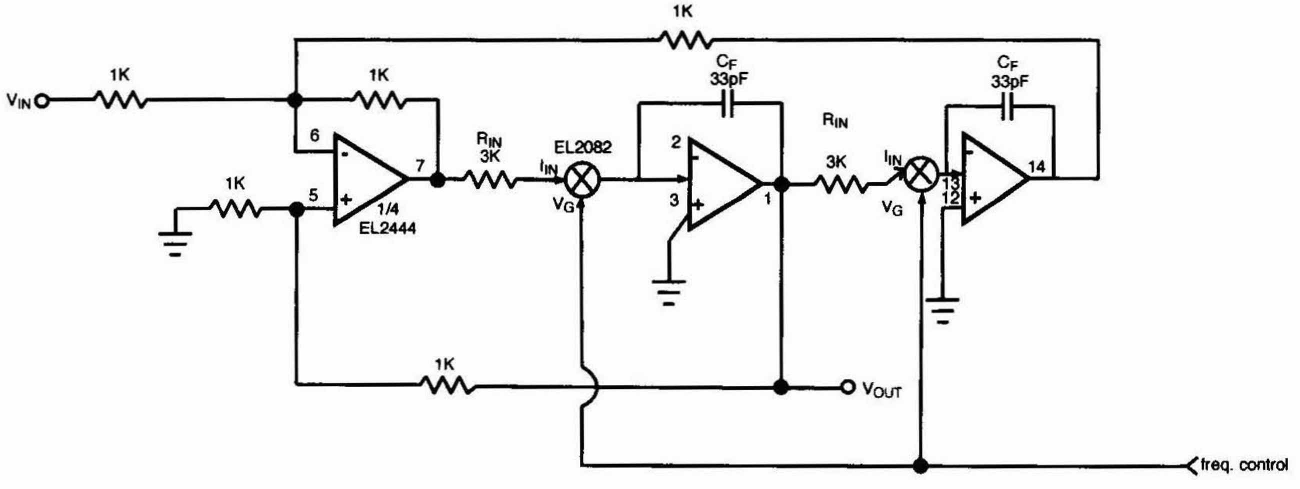


Figure 1

A Low Distortion Tuneable Sine Wave Oscillator

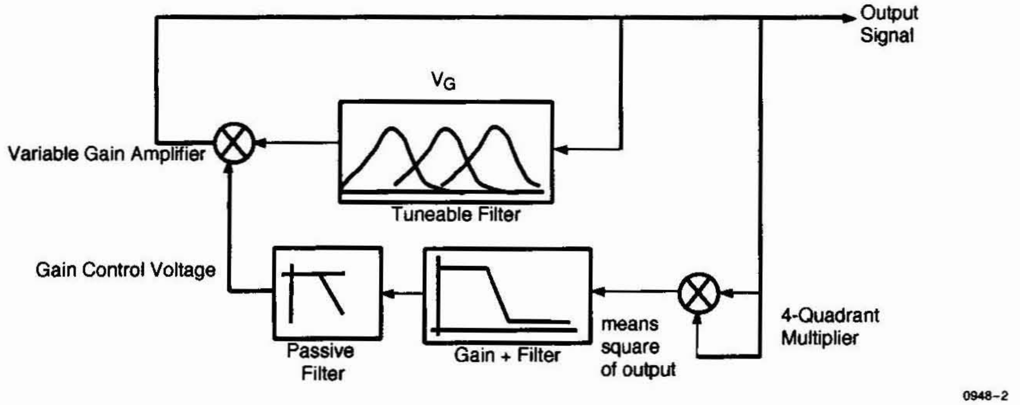

Output Signal
V_G
Variable Gain Amplifier
Tuneable Filter
Gain Control Voltage
Passive Filter
Gain + Filter
means square of output
4-Quadrant Multiplier
0948-2

Figure 2

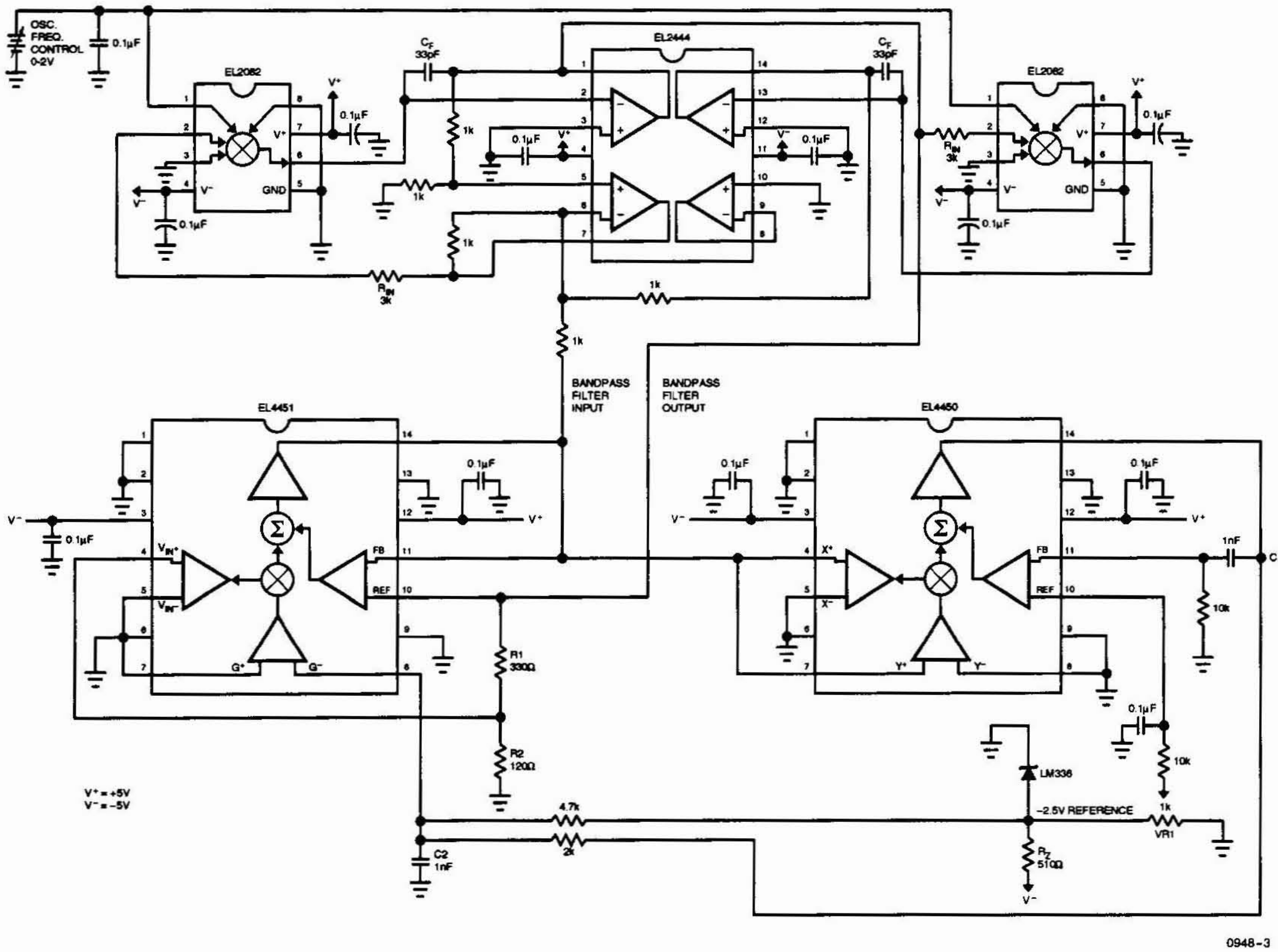
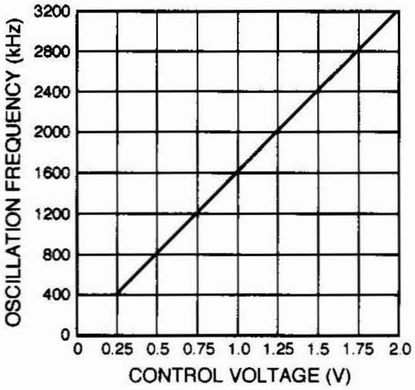
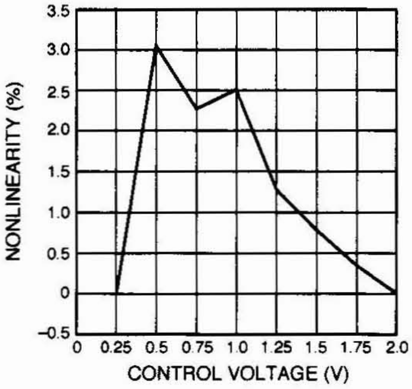

OSC. FREQ. CONTROL 0-2V
0.1µF
EL2082
V⁺
V⁻
GND
C_F 33pF
1k
R_{IN} 3k
EL2444
BANDPASS FILTER INPUT
BANDPASS FILTER OUTPUT
EL4451
V_{IN^+}
V_{IN^-}
FB
REF
G⁺
G⁻
R1 330Ω
R2 120Ω
V⁺ = +5V
V⁻ = −5V
4.7k
2k
C2 1nF
EL4450
X⁺
X⁻
Y⁺
Y⁻
1nF
C_1
10k
LM336
−2.5V REFERENCE
1k VR1
R_Z 510Ω
0948-3

Figure 3

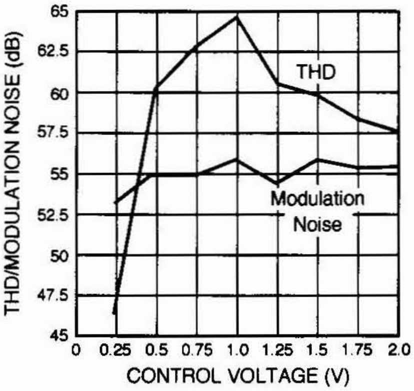
Typical Performance Curves



0948-4



0948-5



0948-6

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

High-Purity Sinewave Oscillators with Amplitude Stabilization

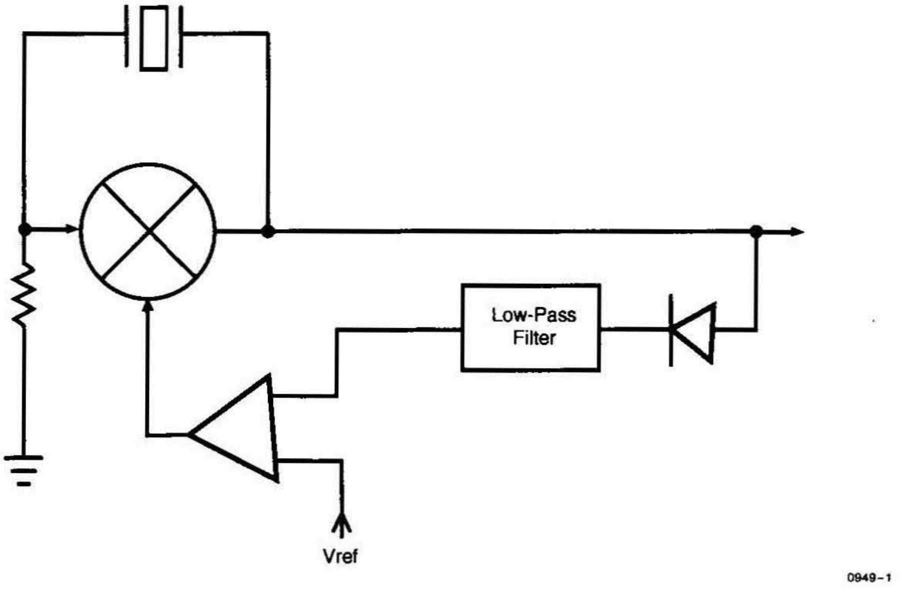
High-Purity Sinewave Oscillators With Amplitude Stabilization

by Barry Harvey

While a wide variety of circuits and components are used to generate sinewaves, it has always been a challenge to produce spectrally pure and regulated sines in circuits that require no tuning nor adjustments. This article shows a practical method of achieving these goals. The classic system architecture is shown below.

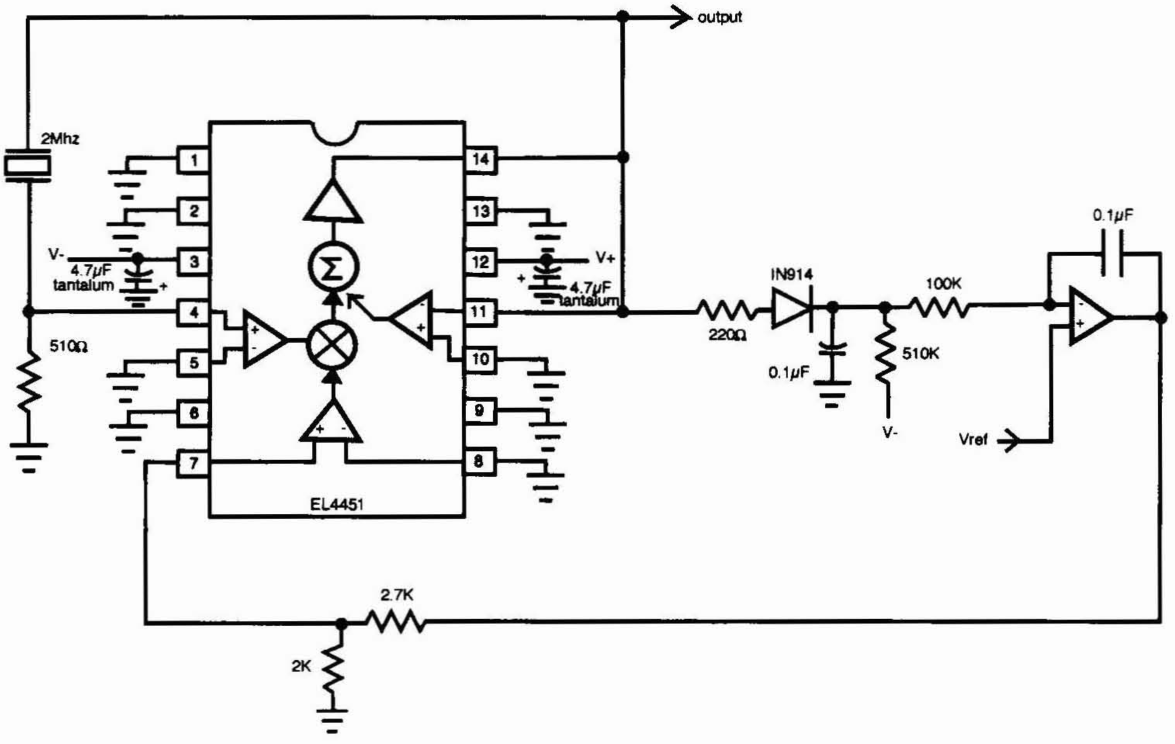
The crystal (or other frequency-selective network) provides the oscillation path around the multiplier or variable-gain amplifier. The multiplier's output is sampled by some amplitude detector, shown here as a rectifier diode. The DC output of the rectifier is filtered by a low-pass filter, and the output of that is compared to a DC reference voltage by the servo amplifier. The gained-up error is then used as the multiplier's gain-control input. The amplitude-control loop serves to set the oscillation path gain to just unity, so that the multiplier's output doesn't grow nor decay, and the loop also maintains oscillation amplitude within the linear range of all components. This gain-controlled oscillator is more complicated than simple overdriven circuits, but it produces very pure sinewaves and has no start-up problems.

Basic Stabilized Oscillator Loop



Here is a realization using common components:

Basic Oscillator with Amplitude Stabilization Loop



0949-2

The EL4451 is a two-quadrant multiplier, whose gain-control input voltage of 0 → +2V produces a voltage gain of 0 to 2. The signal input receives a portion of the output signal passed through a series crystal. At resonance, the crystals impedance phase passes through 0° and positive feedback occurs around the multiplier. The crystal has a series resistance of about 100Ω, so with the crystals 510Ω load the multiplier will need to have a gain of 1.2 to sustain oscillation.

The output is rectified by a simple diode detector and compared to a reference voltage by an integrating op-amp. The integrators output is attenuated by the 2 kΩ and 2.7 kΩ resistors so it cannot overdrive the EL4451 gain-control input and cause nonlinear oscillations. The diode detector has a 220W resistor in series so as to not cause output distortions due to charging pulses. A pull-down current flows through the 510k resistor to allow proper rectification.

Any crystal, up to about 50 MHz fundamental mode resonance, can be used. Overtone crystals will require an added series-tuned circuit to force harmonic oscillation modes. The crystal and 510W resistor can be exchanged to put the crystal at ground, using the parallel resonance mode of the crystal.

This circuit generates −53 dBc harmonic distortion at 2 MHz with ±5V supplies and 1 Vrms output into 500Ω. This is mostly due to the output stage nonlinearities of the EL4451, and it drops to −60 dBc at ±12V supplies. Reducing the output amplitude further improves distortion levels, although the simple diode detector requires a minimum 0.5 Vrms level. Sideband noise is excellent, spanning only 14 Hz at −90 dBc, the resolution of the spectrum analyzer used.

A series-tuned LC filter can be substituted for the crystal. As long as the loaded Q is greater than about 5, the output distortion will be as good as with the crystal. Sideband noise is worse than with the crystal, however.

This circuit generates very low distortion levels:

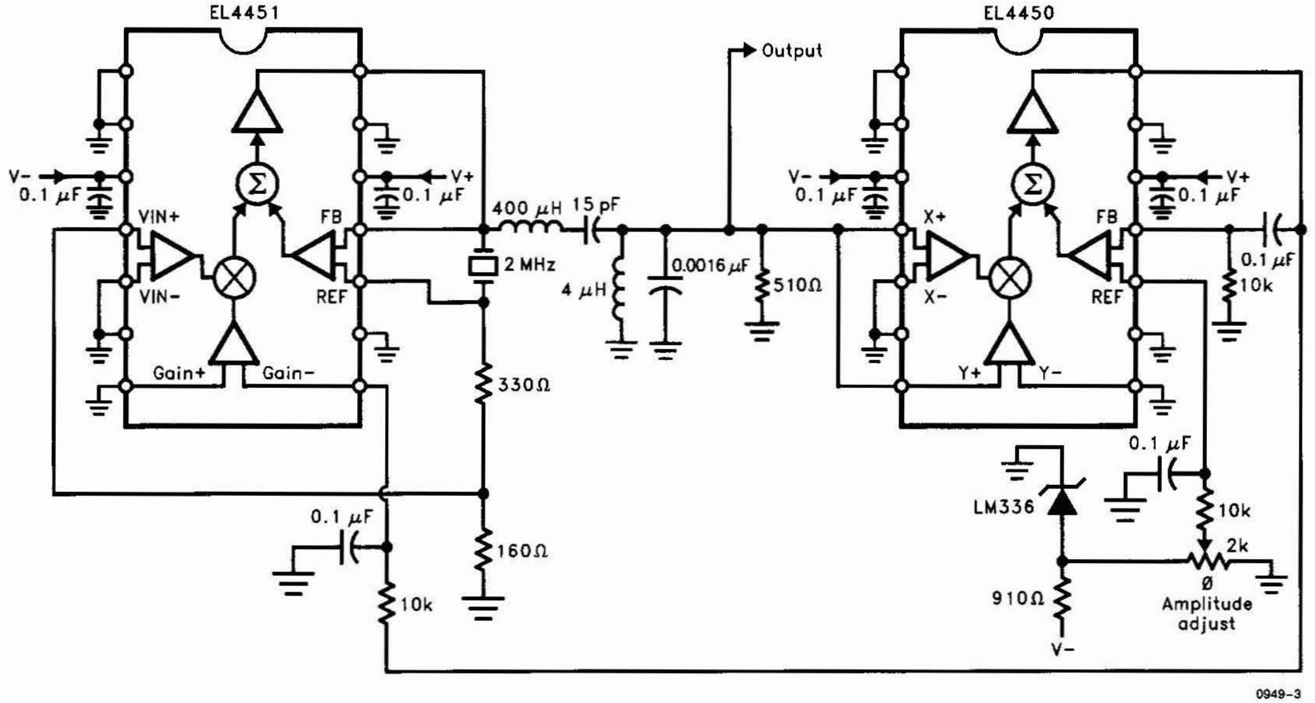


Figure 2. Very Low-Distortion Oscillator

The EL4451 is connected in a slightly different way; the majority of crystal feedback is delivered to the REF input of the feedback amplifier, and a smaller amount of signal routed through the variable-gain input port. In this way, most of the signal runs through a simple voltage-follower path with minimal distortion. The total gain of the EL4451 in this connection is 1 + (Vgain/2V) (160W/(160W + 330W)), which needs to be servoed to about 1.2 for stable oscillation.

The output of the EL4451 is passed through a simple filter to additionally reduce harmonics, then used as the output. For my measurements, I loaded the output with an additional 500Ω, bringing the total load to 250Ω. The EL4451 can drive lower impedances, but the output distortion will rise. Note that no active amplifier nor buffer can be used to drive the output with distortion levels anywhere near that of the passive filter.

Rather than load the filter with a highly nonlinear diode detector, this circuit uses the high-impedance inputs of the EL4450 to sense output amplitude. This is a four-quadrant multiplier, and is used as a mean-square amplitude detector. The advantages include much more precise initial calibration, easier ripple filtering since its at twice the oscillator frequency, and a built-in amplifier which can be used as the servo error amplifier. The X- and Y- inputs of the EL4450 are wired together to produce an internal output^2 quantity at the Σ point. Added to this is a static level from the LM336 reference that has a polarity that subtracts from the mean-square quantity. The FB terminal, normally used for DC feedback, is connected as something like an integrator using the 0.1 μF capacitor. Thus, the output amplifier of the EL4450 is both the low-pass filter and error amplifier for the servo loop, and attempts to maintain the output mean-squared voltage equal to that of the reference.

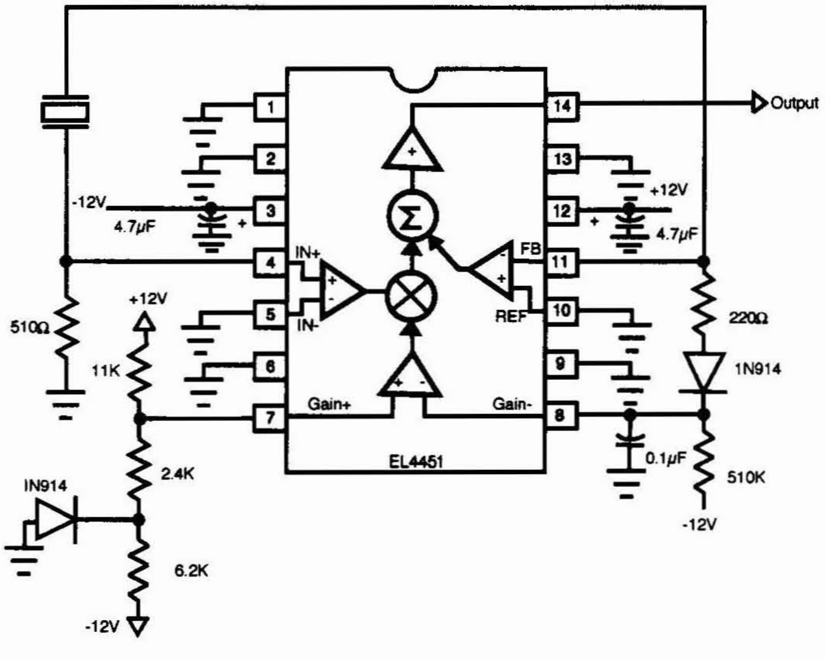
Harmonic distortion is −74 dB with the circuit running on ±5V supplies, and −80 dB with ±12V. As before, reducing the output amplitude improves distortion further.

The error amplifier is not actually required for amplitude stabilization. Since even a miniscule amount of oscillation loop gain more than unity results in a continuously growing amplitude, or a tad less than unity gain creates an ever-shrinking level, we could say that the gain-control input of the oscillating EL4451 already has infinite gain. This circuit makes use of this fact:

This circuit is very simple and still has the low distortion levels of the previous oscillators, but the output level is not well calibrated, despite the diode forward voltage compensation network connected to the Gain + terminal. Variations in crystal series resistance will vary output amplitude.

In summary, we see that recent multiplier ICs can be employed in simple circuits to generate highly pure sinewaves over wide frequency ranges. The particular devices shown are low-cost, yet well calibrated and flexible.

Simple Linear Oscillator


Output
1
2
3
4
5
6
7
14
13
12
11
10
9
8
-12V
4.7μF
+
+12V
4.7μF
+
IN+
IN-
FB
REF
Gain+
Gain-
EL4451
Σ
510Ω
+12V
11K
2.4K
6.2K
IN914
-12V
220Ω
1N914
0.1μF
510K
-12V
0949-4

Application Note #6

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4089 and EL4390
DC Restored Video Amplifier

EL4089 and EL4390 DC Restored Video Amplifier

by John Lidgey, Chris Toumazou and Mike Wong

1. Introduction

The EL4089 is a complete monolithic video amplifier sub-system in a single 8-pin package. It comprises a high quality video amplifier and a nulling, sample-and-hold amplifier specifically designed to stabilize video performance. The part is a derivative of Elantec's high performance video DC restoration amplifier, the EL2090, but has been optimized for lower system cost by reducing the pin count and the number of external components. For R_{GB} and YUV applications the EL4390 provides three channel in a single 16-pin package.

This application note provides background information on DC restoration. Typical applications circuits and design hints are given to assist in the development of cost effective systems based on the EL4089 and EL4390.

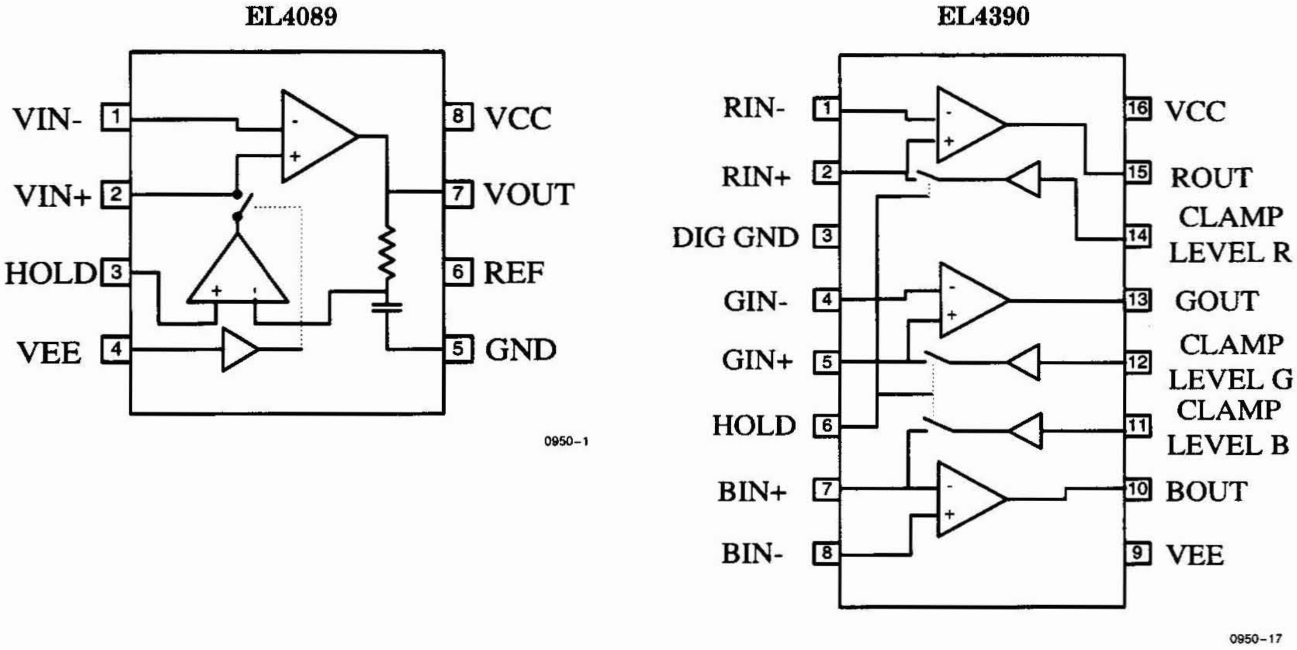

EL4089
VIN-
1
VIN+
2
HOLD
3
VEE
4
8
VCC
7
VOUT
6
REF
5
GND
-
+
+
-
0950-1
EL4390
RIN-
1
RIN+
2
DIG GND
3
GIN-
4
GIN+
5
HOLD
6
BIN+
7
BIN-
8
16
VCC
15
ROUT
14
CLAMP LEVEL R
13
GOUT
12
CLAMP LEVEL G
11
CLAMP LEVEL B
10
BOUT
9
VEE
0950-17

Figure 1. EL4089 and EL4093 Package Outlines

2. Video Signal Refresher

2.1 Composite Video Signal

The figure shown below represents a typical composite video signal, which has a standard distribution level of 1 $V_{P\text{-}P}$ into a 75Ω load, and comprises several sections. The video signal is the part containing the visible picture information, with a maximum amplitude between black and white of 0.7V. At the end of the picture information is the front-porch, followed by a sync pulse, which is regenerated to provide system synchronization. The back-porch is the part of the signal that represents the black or blanking level. In NTSC color systems, the chroma or color burst signal is added to the back-porch and normally occupies 9 cycles of the 3.58 MHz subcarrier.

2.2 DC Restoration—The Classical Approach

Video signals are often AC coupled to avoid DC bias interaction between different systems. The blanking level of the composite video signal therefore needs to be restored to an externally defined DC voltage, which locks the video signal to a predetermined common reference level, ensuring consistency in the displayed picture. This DC reference voltage, VR, sets and controls the picture brightness. The fundamental objective of the DC restore system is to force the DC output from the video amplifier to be equal to an externally defined reference voltage VR. Figure 3 shows a classical approach to DC restoration in video systems.

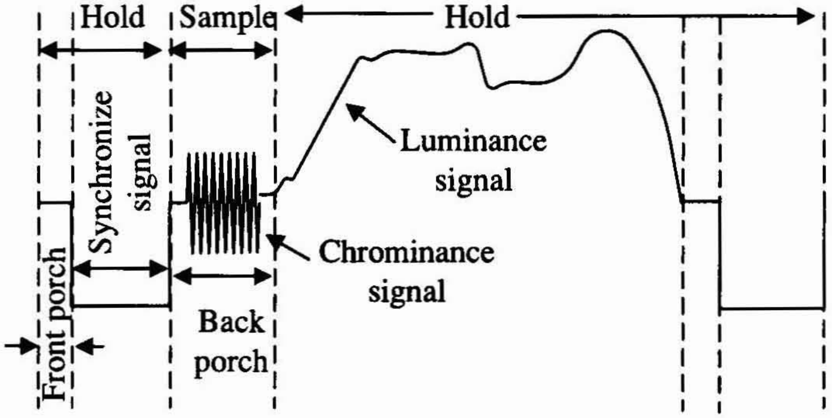


Figure 2. Typical Composite Video Signal

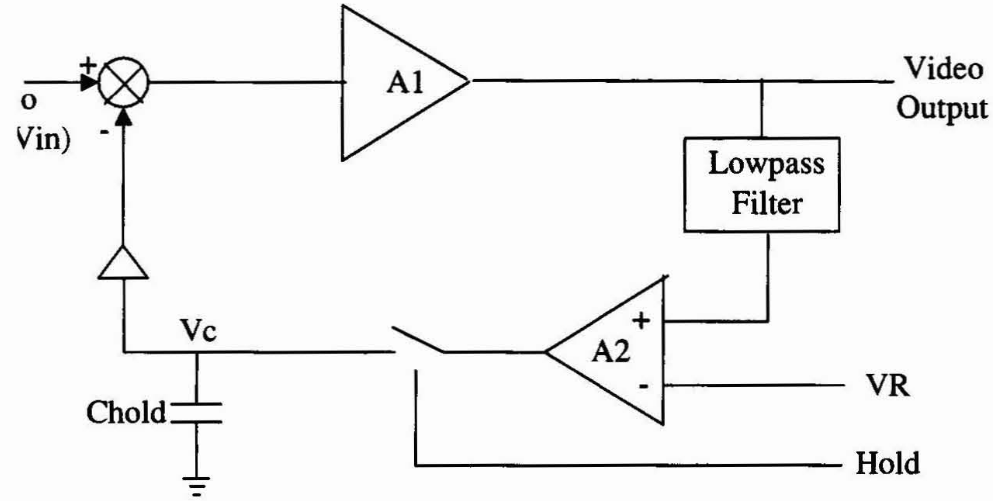


Figure 3. Classical DC Restoration Control Servo Loop

2. Video Signal Refresher — Contd.

The Sync pulse is used to drive the control switch to the sample-and-hold, so that the DC servo loop is closed during the back-porch of the video signal. The lowpass filter is used to remove the chroma burst. The operation of the DC loop is perhaps best understood by considering the voltage appearing across the hold capacitor, C_{HOLD}. During the back-porch sampling period, the switch is closed and the hold capacitor charges up. It can be shown from the loop dynamics that

$$V_C = V_{IN} - \frac{VR}{A1} \qquad (1)$$

where V_{IN} = VBP (the average back-porch voltage of the incoming video signal). Equation (1) can be reconfigured,

$$V_C = VBP - \frac{VR}{A1}$$

The net result is that

$$V_{OUT} \approx VR + \frac{VBP}{A2} \qquad (2)$$

which shows that the output is clamped to VR with an offset term of VBP/A2. This offset is clearly small for a high gain DC loop amplifier, A2. During the hold period, the switch is open and the stored DC value of V_C is now subtracted from the incoming video signal, which effectively sets the back-porch to VR and the video signal is amplified by the forward amplifier with gain, A1, giving

$$V_{OUT} = (V_{IN} - V_C)A1$$
$$= A1\left(V_{IN} - VBP + \frac{VR}{A1}\right)$$

$$V_{OUT} = A1(V_{IN} - VBP) + VR \qquad (3)$$

2.3 DC Restoration—The EL4089 Approach

A simplified scheme of the EL4089 as a feedback system is shown in Figure 4. Unlike Figure 3, the input difference symbol is not shown because the error/correction voltage is stored across the coupling capacitor C_{HOLD} which is outside the control loop.

The operation of the EL4089 is simple, but very subtle. In sample mode, the amplifier's dynamics are such that the output is set to a predetermined reference voltage VR, which may be at ground potential. The correction voltage required at the input of amplifier A1 to maintain V_{OUT} at VR is simply stored across capacitor C_{HOLD}.

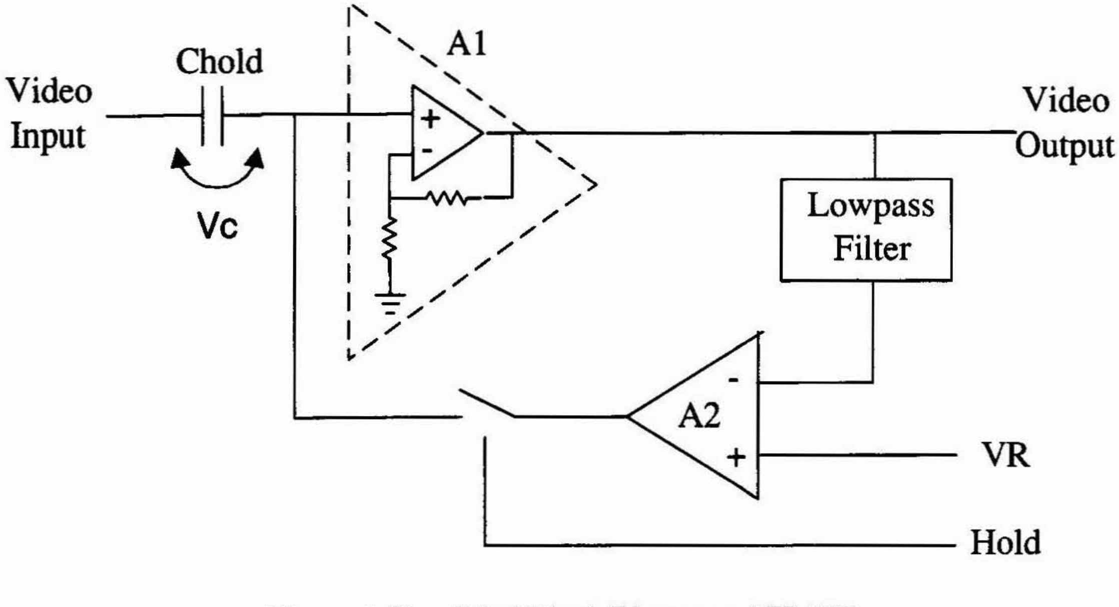


Figure 4. Simplified Block Diagram of EL4089

2. Video Signal Refresher — Contd.

Consider the following analysis. With the switch closed, the input voltage of amplifier A1 is $(VR - V_{OUT})A2$ giving $V_{OUT} = (VR - V_{OUT})A1A2$ and thus

$$V_{OUT} = VR\left\{\frac{A1A2}{1 + A1A2}\right\} \approx VR \tag{4}$$

Assuming that the loop gain A1A2 is very high.

The correction voltage stored across capacitor C_{HOLD} is simply

$$VC = V_{IN} - (VR - V_{OUT})A2 \tag{5}$$

Assuming in this instance that $V_{IN} = VBP$, which is the average back-porch reference of the incoming signal, and substituting for V_{OUT} from Equations (4) and (5) gives

$$VC = VBP - \frac{VR}{A1} \tag{6}$$

Notice that the correction voltage VC is stored across that coupling capacitor C_{HOLD}, which is external to the loop amplifier. Unlike the classical system of Figure 3, it is this unique feature of the EL4089 which obviates the need for a classical sample-and-hold buffer amplifier in the feedback path; thus allowing a very economical 8-pin solution to be realized. Furthermore, the coupling capacitor has two functions, namely to avoid DC bias interaction between different systems and to hold the correction voltage as described above.

During the hold period, the video input signal (V_{IN}) is amplified in the classical way by the *2 video amplifier A1, but in this case the correction voltage held by C_{HOLD} is subtracted from the input to give

$$V_{OUT} = VR + (V_{IN} - VBP)A1 \tag{7}$$

Summary of Operation

1. When the HOLD logic input is set to TTL/CMOS logic 0, the sample-and-hold amplifier can be used to null the DC offset of the video amplifier.
2. When the HOLD input goes to a TTL/CMOS logic 1, the correcting voltage is stored on the video amplifiers input coupling capacitor. The correction voltage can be further corrected as need be, on each video line.
3. The video amplifier is optimized for video performance and low power. Its current-feedback design allows the user to maintain essentially the same bandwidth over a given gain range of nearly 10:1. The amplifier drives back-terminated 75Ω lines.

Subcircuits

The EL4089 DC restored amplifier is an 8-pin monolithic version of the circuit shown in Figure 4. The video amplifier, A1, is a 60 MHz current feedback amplifier or CFA. These devices offer very high speed performance with excellent differential gain and phase. In many respects the CFA behaves as a conventional op-amp, but there are several key differences that must be considered by the user. In particular the two input impedances of the amplifier are different. The non-inverting input impedance is high and the inverting a low impedance. However, the special feature of the CFA is that when in a closed loop configuration, the feedback current is determined by the resistor, R_F, which controls that bandwidth of the amplifier independently of the gain setting resistor R_G.

2. Video Signal Refresher — Contd.

The current feedback amplifier is essentially a transimpedance amplifier with an input voltage buffer to create a high input impedance non-inverting input. The transimpedance amplifier is formed by mirroring the output current of the input unity gain buffer into a high impedance internal Z-node and buffering this Z-node voltage through to a low impedance output, as shown schematically in Figure 5 below.

The unity gain buffers are a complementary class-AB common-collector stage, with DC current biasing. The slew-rate of the CFA is excellent due to the non-current limiting input stage. The CFA has only one internal high impedance node (Z), so it is essentially a single pole dominant amplifier. Since the inverting input terminal is the output terminal of a voltage buffer, it is a low impedance point and the feedback signal is current. Intuitively one can see that in closed loop the feedback current through R_F supplies the current demanded by R_G and the input error current into the inverting input terminal. It is this feedback current component of R_F which is used to charge the compensation capacitance at the Z-node. Theoretically it can be shown that the -3 dB bandwidth is approximately,

$$f_{-3\,\mathrm{dB}} = \frac{1}{2pRFCZ} \qquad (8)$$

where CZ is the compensation capacitance of the Z-node. However, as for conventional op-amps, the closed loop gain, A1, is simply

$$A1 = 1 + \frac{R_F}{R_G} \qquad (9)$$

and the -3 dB frequency can be controlled with R_F while the closed loop gain can be set independently with R_G.

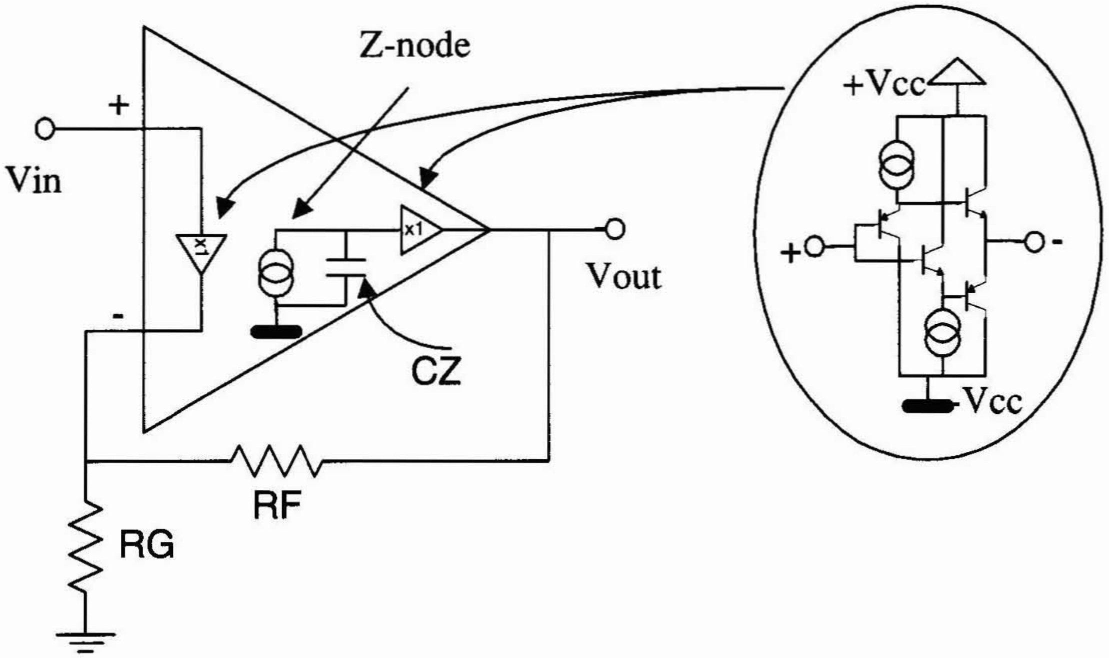


Figure 5. The Current-Feedback Op-Amp

2. Video Signal Refresher — Contd.

The EL4390 Approach

The EL4390 is three high performance current feed-back amplifiers with DC restore function. A simplified schematic diagram of one of the channels in a DC restore configuration is shown in Figure 6. Its basic approach is very similar to the EL4089 in that the error/correction voltage is stored across the coupling capacitor C_{HOLD} from the video input to the positive input of the amplifier. Different from the EL4089, when the sample and hold switch is close, an internal buffer amplifier is enabled to force the non-inverting input of the video amplifier to be equal to the reference input level. When the switch is open, an error voltage is stored on the input coupling capacitor C_{HOLD} to maintain the offset at the output. The following details the mathematical relationships between the inputs and output.

When the sample and hold switch is close,

$$V_{OUT} = A1 * VR \tag{11}$$

where A1 is the close-loop gain of the amplifier.

The voltage across the hold capacitor is

$$VC = V_{IN} - VR \tag{12}$$

In many NTSC video applications, the back-porch of the video signal is clamped. Thus, V_{IN} is the input back-porch level, VBP.

$$VC = VBP - VR \tag{13}$$

When the sample and hold switch is open, the voltage across the hold capacitor maintains the proper offset.

$$\begin{aligned} V_{OUT} &= A1(V_{IN} - VC) \\ &= A1\,(V_{IN} - VBP + VR) \end{aligned} \tag{14}$$

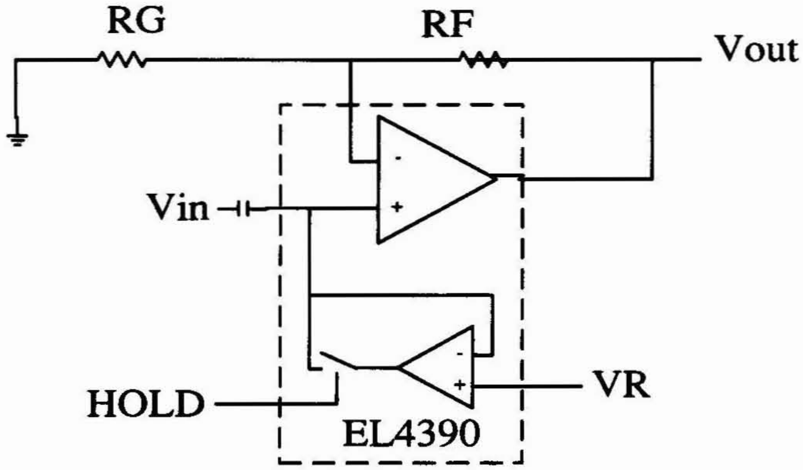


Figure 6. Simplified Connection Diagram of EL4390

3. Features of the EL4089C

Elantec pioneered the development of monolithic CFAs. As first to the market with the CFA our established reputation is confirmed with the EL4089 which is the first 8-pin monolithic DC restored video amplifier. A connection diagram for the EL4089 configured as a DC restoring amplifier with a gain of 2 restoring to ground (pin 3—zero voltage reference) is shown in Figure 7.

The EL4089C is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL4089C is specified for operation over the 0°C to + 75°C temperature range.

The on-chip current-feedback amplifier of EL4089 and EL4390 is optimized for video performance. Since it is a current-feedback amplifier, the −3 dB bandwidth stays essentially constant for various closed-loop gains. The amplifier performs well at frequencies as high as 60 MHz for the EL4089 and 80 MHz for the EL4390 when driving 75Ω. The sample and hold circuit is optimized for fast sync pulse response.

4. Typical Application Circuits

The EL4089 and EL4390 are designed to DC-restore a video waveform (Figure 2). A typical application circuit of the EL4089 is illustrated in Figure 8. The following analysis also applies to the EL4390. This circuit forces the cable driving video amplifier's output to pin 3 reference voltage level when the HOLD pin is at a logic low. In the case of EL4390, when HOLD pin is logic low, the output of the video amplifier is driven to the reference voltage multiply by the close loop gain of the video amplifier. In Figure 8, pin 3 is grounded and HOLD pin is low during backporch of the video signal, consequently, the backporch is clamped to the ground voltage level.

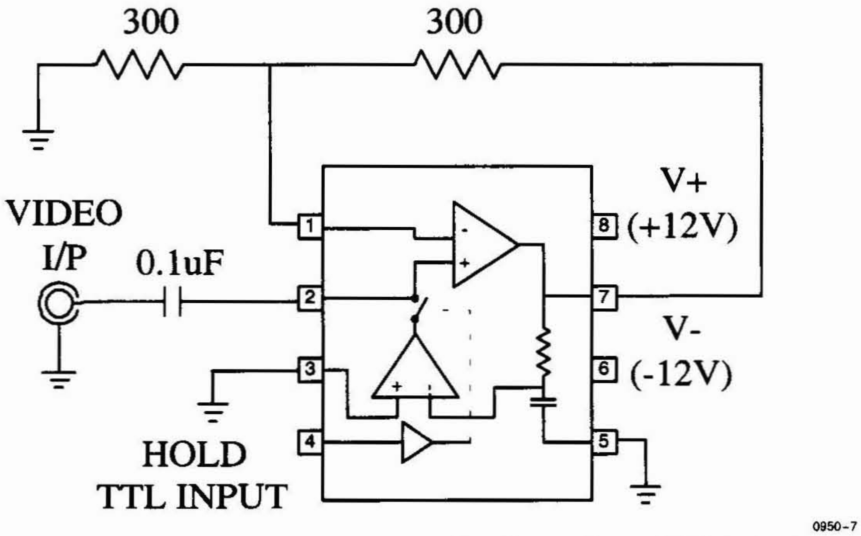


Figure 7. EL4089 Connection Diagram (Configured as a DC Restoring Amplifier with a Gain of 2, Restoring to Ground)

4. Typical Application Circuits — Contd.

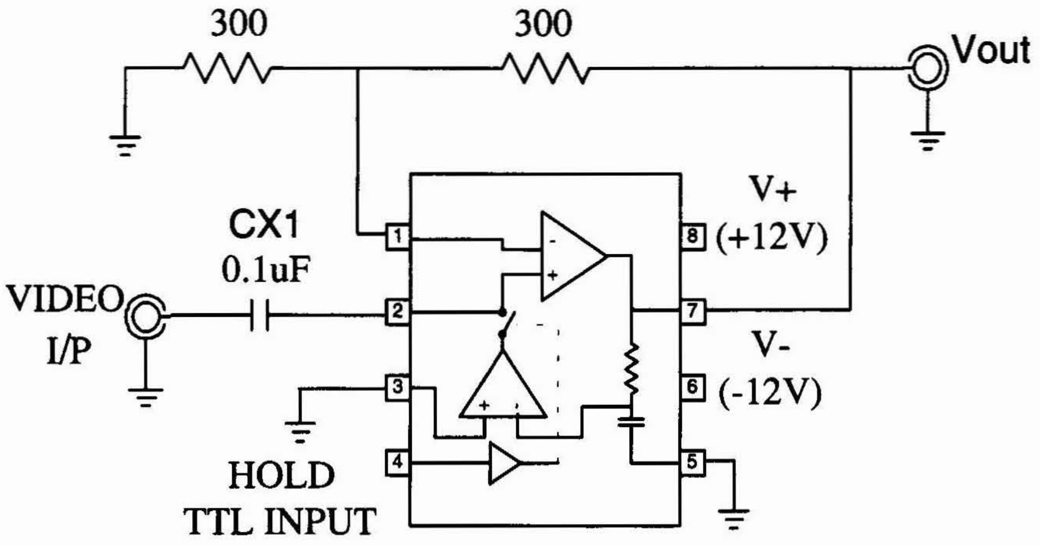


Figure 8

CX1 Determination

The correction voltage is stored across the capacitor CX1, an external ceramic capacitor connecting from the video signal input to the non-inverting input of the video amplifier. The following demonstrates how the CX1 capacitor should be chosen to satisfy the system droop voltage and sampling requirements.

Ideally the input impedance of the video amplifier should be infinite during the hold period to avoid any discharging effects on the CX1 capacitor. However, due to the inherent nature of the bipolar transistors, a bias current is always present. This bias current discharges CX1 during the hold time and as a result causes the correction voltage across CX1 to drift. Equation (15) gives the basic relationship between correction droop voltage and the CX1 value.

$$V(\text{droop}) = \frac{(I_B+)(T_{LINE} - T_{SAMPLE})}{CX1} \qquad (15)$$

Where:

V(droop) is the voltage change across CX1 during hold period.

I_B+ is the amplifier's non-inverting input bias current.

T_{LINE} is the single video line duration.

T_{SAMPLE} is the sampling time during which the S/H switch is closed.

The output voltage change due to voltage drooping is simply,

$$V_{OUT}(\text{droop}) = V(\text{droop}) * A1$$

Where:

A1 is the close loop gain of the video amplifier.

In the Figure 8 design example, a typical input bias current of the video amplifier is 1 µA, so for a 62 µs hold time and 0.01 µF capacitor, the correction voltage droops 6.2 mV; consequently, the output voltage drifts by 12.4 mV in one video line.

4. Typical Application Circuits
— Contd.

The CX1 value and sampling time also determinate the amount of time required by the EL4089 to reach within its DC-restored voltage range.

$$V(\text{charge}) = I_{OUT}\frac{T_{SAMPLE}}{CX1} \quad (16)$$

Where:

I_{OUT} is the sample and hold amplifier output current.

The sample and hold amplifier can typically provide a current of 300 μA to charge CX1, so with 1.2 μs sampling time, the output can be corrected by 36 mV in each line.

Equations (15) and (16) demonstrate the tradeoffs between CX1, sampling time, DC off-set droop voltage, and speed of the DC-restore function. Using a smaller value of CX1 increases both the voltages that can be corrected each line and the drift while being held, likewise, using a larger value of CX1 reduces those voltages.

In Figure 9, a resistor is connected from the noninverting input of the amplifier to the negative supply to compensate for the non-inverting input bias current. To obtain the optimum performance, the compensation resistor R1 should be adjusted to give 0 mV droop voltage at 50% field.

The restore current generated by the sample and hold amplifier decreases as the output voltage approaches the reference voltage. This effect combines with the 7 mV of offset voltage error in the sample and hold amplifier can result in a 22 mV of total error from the output to the reference voltage input during clamping. A method of correcting this problem is depicted in Figure 10. A voltage divider is used to compensate for the sample and hold amplifier offsets.

A complete DC-restore circuit with the EL4581 sync separator is shown in Figure 11. An optional RC low pass filter on HOLD input pin is included should the logic signal require slowing down. This RC network can also serve to prevent feetthrough from the falling and rising edges of the back-porch sync timing signal to the video amplifier output. The video DC restore output and EL4581 back-porch timing waveforms are illustrated in Figure 12. During the back-porch interval, the EL4581 pulls the hold pin of the EL4089 low and the EL4089 servo loop forces the output to the reference voltage level. In the photo, the input back-porch voltage level is 0.5V and the output back porch voltage level is restored to 0V, the reference voltage level.

4. Typical Application Circuits — Contd.

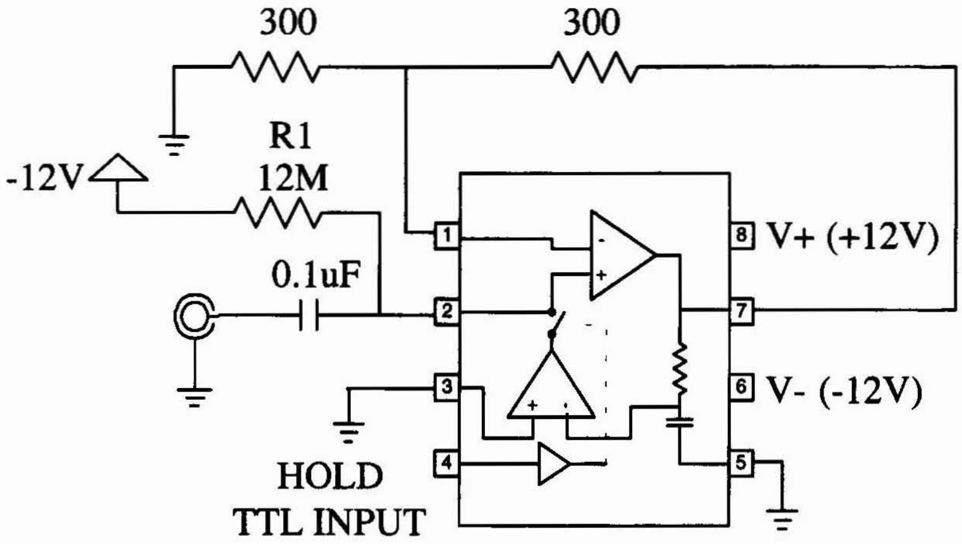

300
300
R1
12M
-12V
0.1uF
1
2
3
4
8
7
6
5
V+ (+12V)
V- (-12V)
HOLD
TTL INPUT
0950-9

Figure 9. I_B+ Bias Current Correction

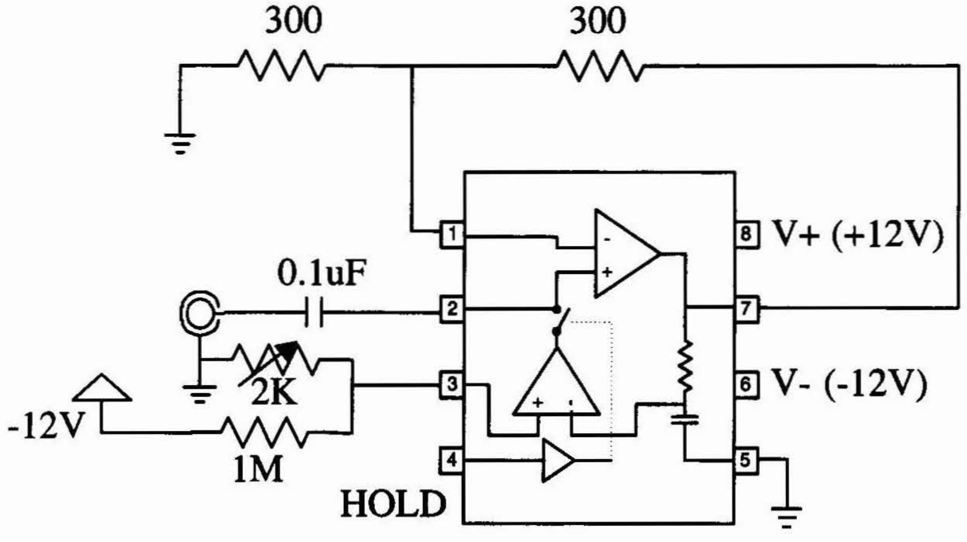

300
300
0.1uF
2K
-12V
1M
HOLD
1
2
3
4
8
7
6
5
V+ (+12V)
V- (-12V)
0950-10

Figure 10. Sample and Hold Off-Set Error Compensation

4. Typical Application Circuits — Contd.

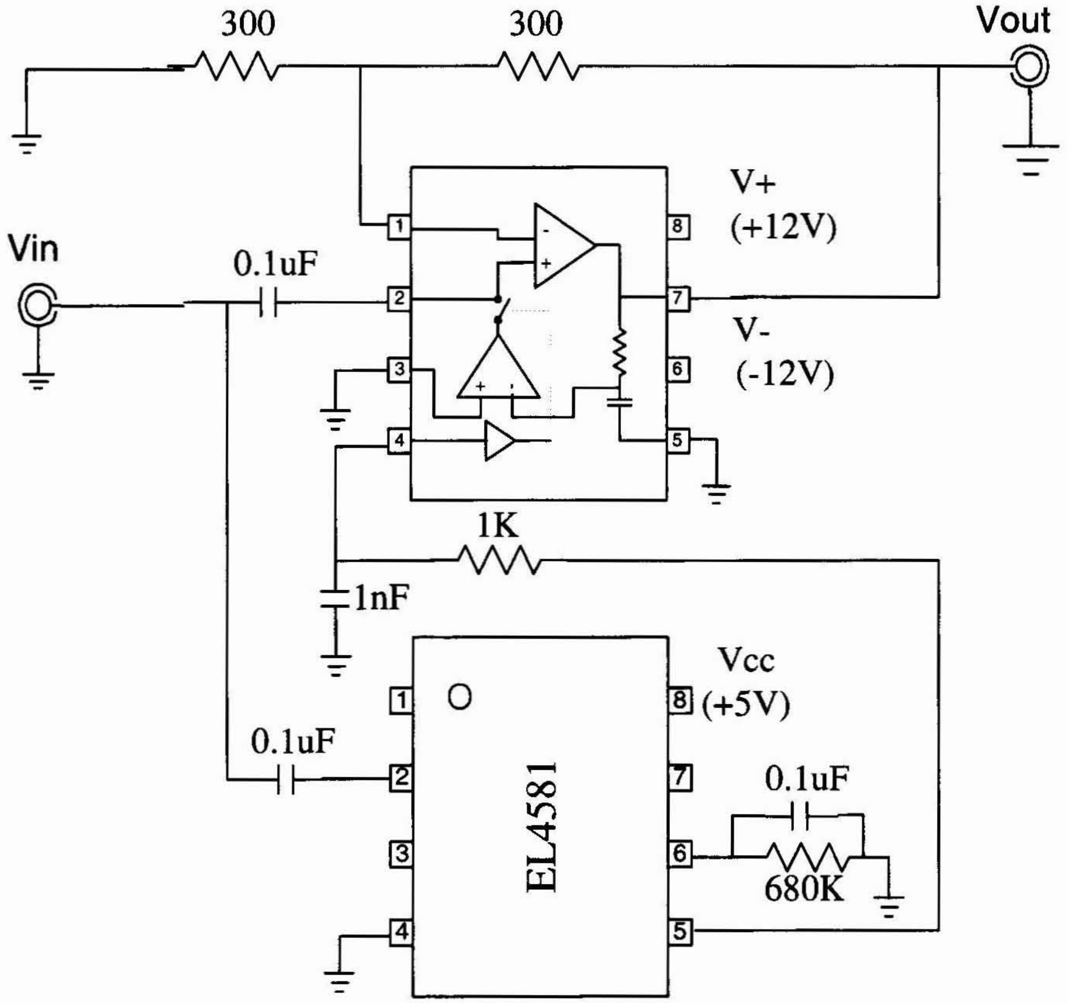

300
300
Vout
Vin
0.1uF
V+
(+12V)
V-
(-12V)
1K
1nF
Vcc
(+5V)
0.1uF
EL4581
0.1uF
680K
1
2
3
4
5
6
7
8
0950-11

Figure 11. EL4581 and EL4089 Restore Amplifier and Sync Separator

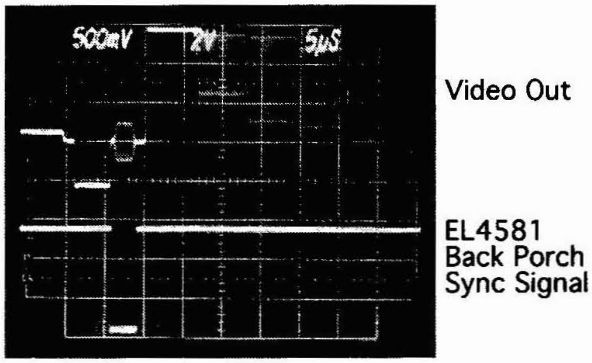
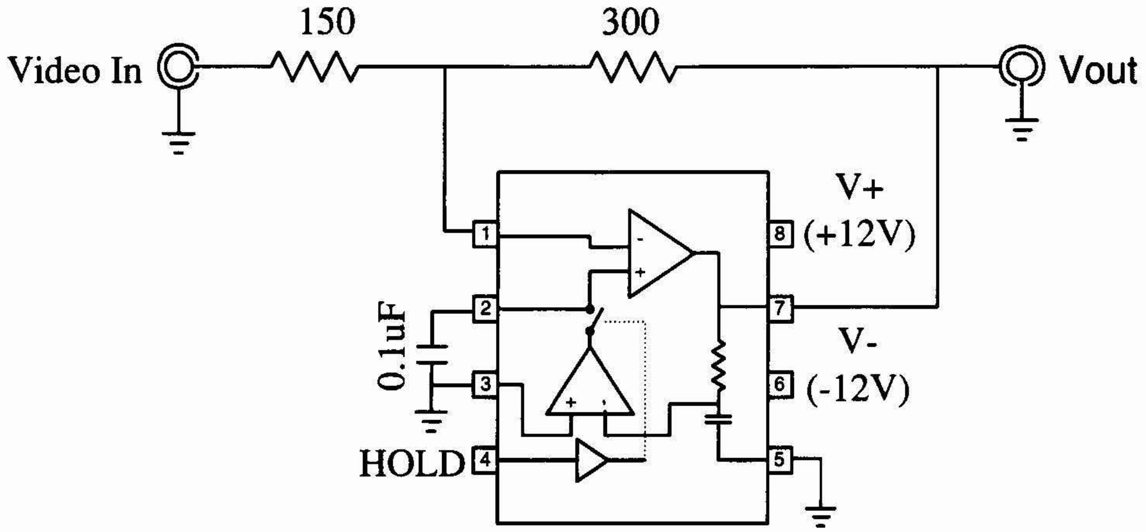


Figure 12. Video Output and EL4581 Back-Porch Sync Signal

4. Typical Application Circuits — Contd.

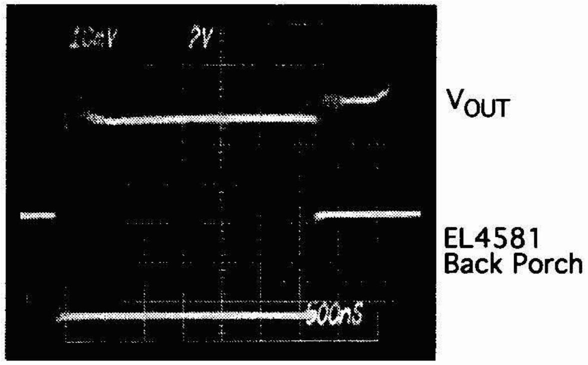


0950-13

Figure 13. EL4089 DC-Restore Amplifier in −2 Gain Configuration

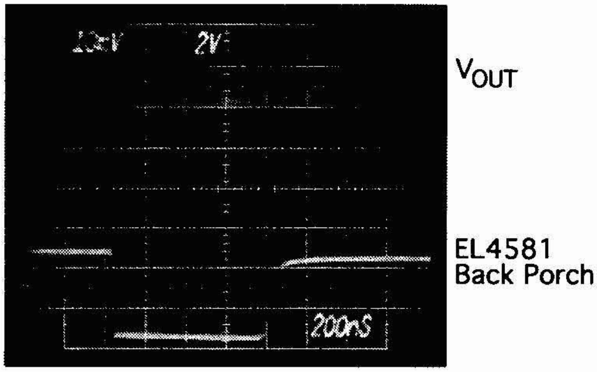
EL4089 in Inverting Gain Configuration

Placing the hold capacitor in the signal path leads to sync signal feed-through and phase distortion of the burst signal. Rearranging the EL4089 in the inverting configuration as shown in Figure 13 provides significant improvements. Figure 14 indicates a 15 mV of voltage spike in amplifier output during the sampling interval and coincides with the falling and rising edge of the HOLD signal. The output voltage spike is caused by the charging current injecting out of the output of S/H amplifier during the back-porch interval. One way to minimize the sync feed-through is to feed the video input signal directly into the inverting input of the video amplifier and short the DC restore capacitor to ground. As a result, the video input signal is not affected by output current of the S/H amplifier. The voltage spike is also reduced by an addition of a simple RC network from the output of the EL4581 to the HOLD input of the EL4089. Figure 15 test result shows no voltage spikes and only a 4 mV of voltage dip during the sampling period. In the inverting configuration, the video signal goes directly into a purely resistive component, thus, no phase shift occurs.



0950-14

Figure 14. Back-Porch Sync Edge Feed-Through



0950-15

Figure 15. EL4089 Inverting Amplifier Output Waveform

4. Typical Application Circuits
— Contd.

EL4581 Interface

The hold input of the EL4089 is designed to interface directly to Elantec's existing suite of sync separators, namely the EL4581 and the EL4583. The connection diagram of the EL4581 is shown in Figure 16.

The EL4581 extracts timing information including composite sync, vertical sync, burst/back-porch timing and odd/even field information from standard negative going sync NTSC, PAL, and SECAM video signals. The EL4581 detects video signals from 0.5 to 2 $V_{P\text{-}P}$. The 50% slicing feature provides precise sync edge detection even in the presence of noise and variable signal amplitudes. A built-in linear phase, third order, color burst filter minimizes spurious timing information and reduces the number of external components. The integrated circuit is also capable of providing sync separation for non-standard, faster, horizontal rate video signals by changing an external horizontal scan rate setting resistor. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default output is produced after an internally generated time delay, in the event of missing serration pulses, for example, in the case of a non-standard video signal. All outputs are active low.

5. Printed Circuit Board Layout Hints

The feedback path of the video amplifier should be kept as small as possible to avoid deterioration of high frequency gain accuracy.

The board layout should have a ground plane underneath the EL4089, with the ground plane cut away from the vicinity of the $V_{IN}-$ pin (pin 1) to minimize the stray capacitance between pin 1 and ground.

Power supply bypassing is important and a 0.1 μF ceramic capacitor, from each power pin to ground, placed very close to the power pins, together with a 4.7 μF tantalum bead capacitor, is recommended.

When both digital and analog grounds are on the same board, the EL4089 should be on the analog ground. The digital ground can be connected to the analog ground through a 100Ω–300Ω resistor near the EL4089. This allows the digital signal a return path while preventing the digital noise from corrupting the analog ground.

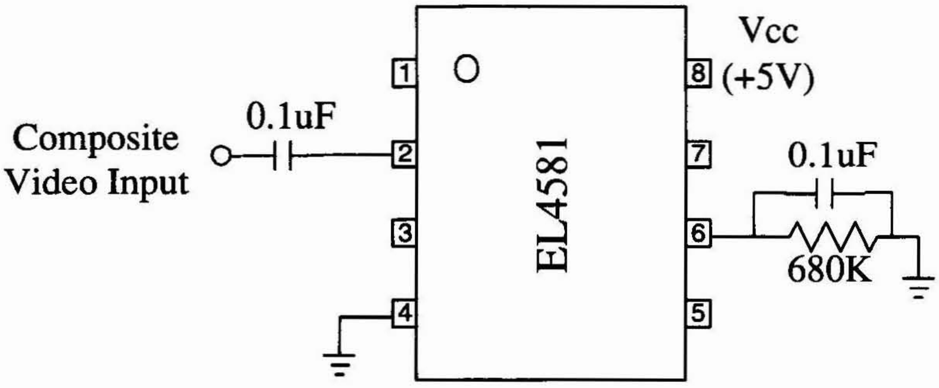


Figure 16. EL4581 Connection Diagram

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Real Time Power Measurement of a Transistor

Real Time Power Measurement of a Transistor

Introduction

It is quite typical to monitor the current through a component or a voltage on a node to regulate an input. Some applications may find it more useful, however, to monitor the power through a transistor. One such occasion would be in charging a battery. When the voltage is low, the designer may want more current charging, but as the voltage increases, the current could decrease, ultimately saving charging time and power.

Circuit Description

The circuit in Figure 1 utilizes an EL4452, a wideband variable gain amplifier compensated for a gain of 10. Circuit operation is very straightforward. Add a small resistor (Re) in shunt with the emitter and apply the differential voltage across it to the differential input of the EL4452. The voltage at this input will be:

$$V_{IN1} = Ie * Re$$

Secondly, attach a simple voltage divider between the collector and emitter and apply this voltage to the gain input of the EL4452. The voltage at the gain input will be:

$$V_{IN2} = V_C * R_{c_2}/(R_{c_1} + R_{c_2})$$

The voltage divider, R1 and R2, is necessary to ensure linearity if the collector will swing beyond ±2V.

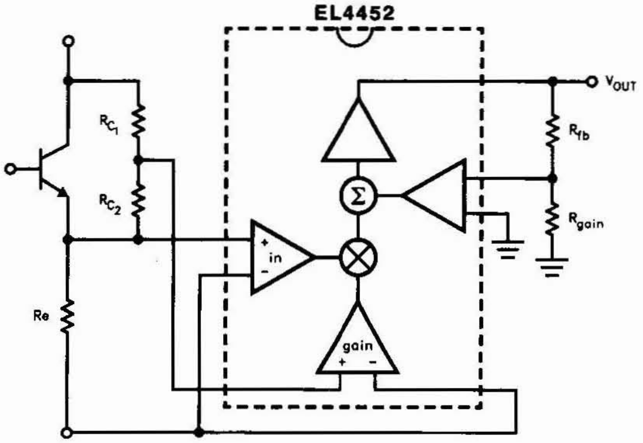
Simply choosing R_{fb} and R_{gain} to give a gain of ten ($R_{fb} = 9 * R_{gain}$), the output will be a real-time, scaled measurement of power:

$$V_{OUT} = k * Ie * V_c$$
$$\text{where } k = [Re * R_{c_2} * 10/(R_{c_1} + R_{c_2})]$$

The EL4452 is internally compensated for a feedback gain of 10. It is not guaranteed stable for smaller values of gain. Also, since it is a high frequency part, the feedback resistors should be on the order of hunderds of ohms so that the pole created by the feedback resistors and the parasitic capacitances does not limit the performance. If there are instability problems with parasitics, small capacitors can be placed across R_{fb} and R_{gain} to dominate these parasitics, increase the compensation, and allow for higher divider resistances.

Conclusion

A circuit capable of providing real time power measurements has been presented. This circuit has a functional bandwidth of 50 MHz (with R_{fb} and R_{gain} chosen for a gain of 10.) The gain bandwidth product holds, so if more gain is needed, it is a proportional tradeoff with bandwidth.



0951-5

Figure 1

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Measuring the Thermal Resistance of Power Surface-Mount Packages

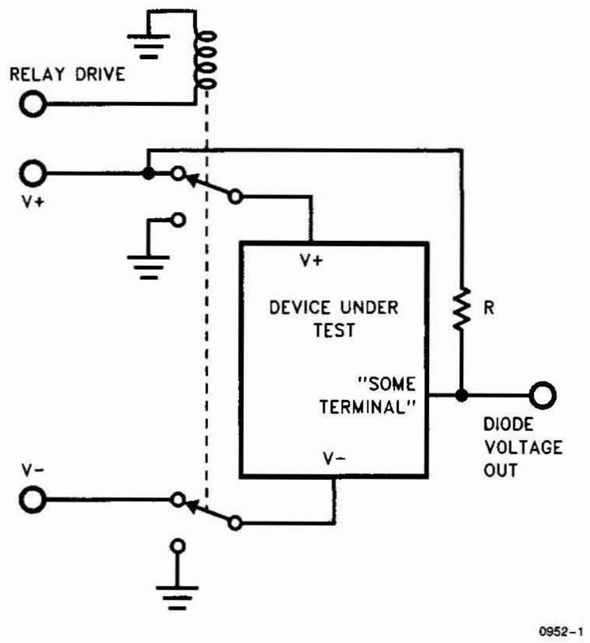
Measuring the Thermal Resistance of Power Surface-Mount Packages

by B. Harvey

Modern miniature IC packages have allowed great space savings in products, but frustrate the designer by concentrating the heat generated by circuits into smaller volumes. Increasing IC speeds and complexities over the years have also demanded greater power dissipation. Higher internal operating temperatures will shorten the life of an IC; elevated but safe temperatures often reduce the quality of performance in circuits, for instance degrading frequency response or distortion.

To cope with the problem, a variety of heat management packages have been introduced which conduct heat from the IC die through the package leads to the circuit board. The board becomes the major heatsink, and the onus of thermal design passes from the IC manufacturer to the board designer. This article is intended to assist the board designer in measuring thermal resistance of mounted IC devices efficiently.

Traditional parameters θ_{JA} (thermal resistance of a device not connected to anything) and θ_{JC} (infinite heatsink connected to the part) are not useful with mounted devices. Circuit boards are neither insignificant nor infinite heat sinks. We will use the parameter θ_{JM} as the mounted thermal resistance of an IC, and it will vary with die size, package type, and circuit board features. The θ_{JM} can be estimated by thermal simulation of the part and its mounting environment, but seldom is there concrete data on the thermal structure of the IC, and correctly modeling the board environment is difficult. A good way to estimate θ_{JM} is to solder the IC to an area of circuit board that has been suitably sculpted with a Dremel tool to emulate a final board pattern in the region of the test device (or a finished board itself) and use the following circuit to measure θ_{JM}:

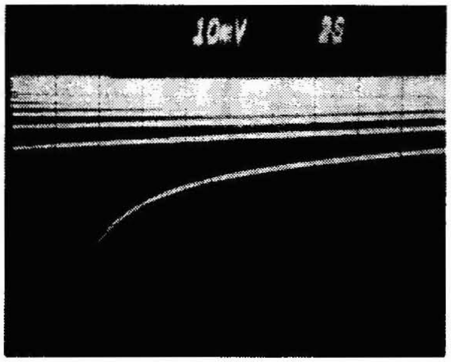


"Some terminal" is any pin that is connected to an internal parasitic diode whose other connection is either power supply pin. The IC manufacturer's technical support people can help select the right pin and drive polarity. We will use the forward voltage as a measure of internal die temperature. When the relay grounds the supply pins, R provides a current from a supply to bias the diode. Depending on the internal diode connection, V+ or V− will be connected to R. R should supply a current low enough to create minimal resistive drop in series with the diode. 50 µA is a good guess for the current, or any current that sets up about 600 mV of forward diode voltage at room temperature. The general equation for diode tempco (it generally need not be measured directly) is:
$\Delta V/\Delta T = -(1.12V - V_{be}\ (25°C))/300°K$. Thus a 600 mV junction at room temperature has a −1.7 mV/°C temperature coefficient.

Using a storage or digitizing oscilloscope measuring the forward diode voltage, we will observe the thermal relaxation of the die after a steady power dissipation is terminated. The dissipation is the part's own supply current, applied through the relay. The relay's drive is also the oscilloscope trigger. Because the temperature change may only cause tens of millivolts of diode voltage variation against the background of 600 mV, a stable differential-amplifier with adjustable offset will be used for the oscilloscope input. Alternately, the ground of the above circuit may be shifted with a third supply before being connected to the oscilloscope.

This is the test sequence:

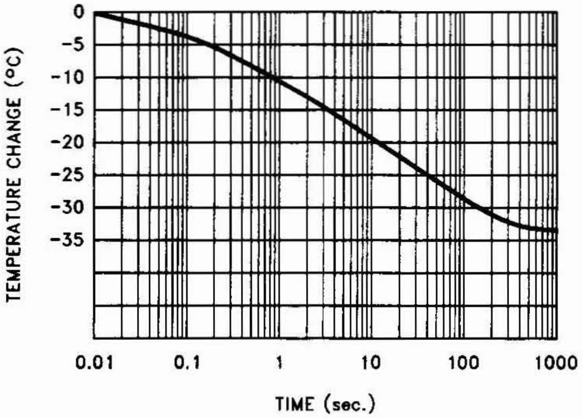
1. Connect everything with the device powered down. Set the oscilloscope sweep to the slowest setting, continuously sweeping.
2. Adjust the offset against the diode voltage to center the oscilloscope trace. The 10 mV/div. sensitivity is a good start.
3. Apply power to the device via the relay. The oscilloscope trace will be off-screen. Allow the part at least ten minutes to warm up its mounting.
4. Clear any stored trace. Turn off power to the device. The following trace should be seen on the oscilloscope:



0952-2

Oscilloscope Display of Diode Voltage Relaxation During Cooling

We see an initial rapid cooling followed by very slow settling back toward room temperature. The cooling rate is not a simple exponential decay, but has a wide range of time dynamics. Here is the decay behavior of an EL1501 mounted on a large heat spreader:



0952-3

Thermal Relaxation vs. Time of a Mounted Power SO-20 Package

For the first ten milliseconds little die temperature change occurs. Then the heat makes its way through the die and flows out through the leadframe, which occurs in around ten seconds. The last event is the settling of the heat-sinking board, which resolves in ten minutes. Clearly, thermal measurements require patience and time.

The thermal resistance θ_{JM} is then the temperture variation (long-term) divided by the power dissipated, so:

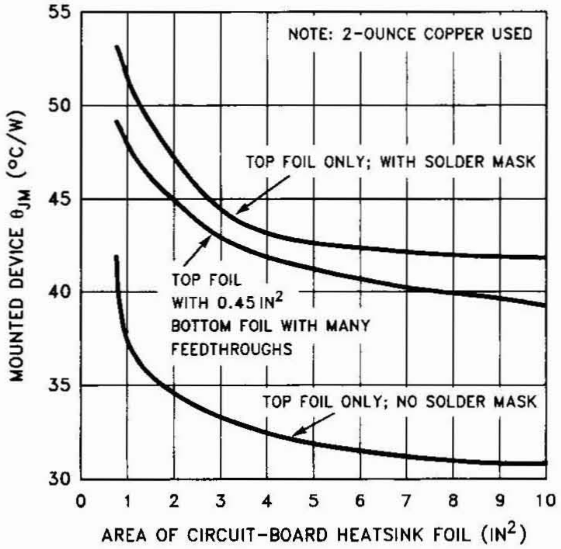
$$\theta_{JM} = \Delta T_{diode}/P_{diss,\ quiescent}$$

$$= \frac{\Delta Vdiode * 300°K}{P_{diss,\ quiescent} * (1.12V - V_{BE}\ (25°C)}$$

Measuring the Thermal Resistance of Power Surface-Mount Packages

Using this technique, the thermal resistance of the SOL-20 fused-lead package was measured. This package houses the EL1501 and has four center leads on each side fused to the IC's mounting header. Thus, heat flows directly through these pins from the IC and spreads through the ground plane on top of the circuit board. A nearly continuous ground plane is hand-drawn. Several variations of the board were tested. The first was the most straightforward: just the top foil is a heatsink. By cutting away board material, a variable area was implemented and thermal resistance measured. Then the measurements are repeated on an identical board with no solder mask to add to thermal resistance. Another variation was to create another heatsink area on the back of the board, thermally connected to the top foil by a multitude of feedthroughs. Finally, a copper sheet-metal heatsink was soldered to the top foil near the IC's heat-spreading pins.

The results are shown in this graph:



Thermal Resistance of Dual-4-Fused-Lead SOL-20 Package

The SO-20 standard package has a θ_{JA} of 80°C/W. With 4in^2 of circuit board heatsink copper with solder maskcutout, the thermal resistance drops to 32°C/W. Given a quiescent dissipation of 1.25W, the die temperature rise of the mounted EL1501 is 40°C. With a maximum ambient temperature of 85°C, we have a worst-case die temperature of 125°C, safely within the 150°C package limit.

Some observations:

1. 4in^2 of copper area is sufficient in that more doesn't help much.
2. The bottom foil did not greatly help.
3. Removing the solder mask over the heat spreading area, if appropriate, reduces θ_{JM} nicely.

Finally, a large metal heatsink mounted close to the heat-spreading pins produced a θ_{JC} of 30°C/W.

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Driving Reactive Loads with High Frequency Op-Amps

Driving Reactive Loads with High Frequency Op-Amps

by Barry Harvey and Chris Siu

As the bandwidth of op-amps today pushes past 100 MHz towards the GHz region, increasing attention must be paid to the components, loads, and circuit traces which surround the op-amp. Not only is this necessary to optimize performance, but neglecting to do so may throw the amplifier into oscillation. This application note discusses the effect of loads, especially capacitive ones, on the behaviour of a high speed op-amp.

1.0 Real World Loads

To start, one needs to question whether there are any pure capacitive loads at high frequencies. To connect any load we need some wires or metal interconnect, and associated with these wires are resistance and self-inductance. In the following sections we will examine some possible loads and their behaviour over frequency.

Coaxial Cables

Coaxial cables must be terminated in the proper impedance to look like a resistive load to the driving source. A common myth is that an unterminated cable looks capacitive. While this may be true for short cables at low frequencies, it certainly does not hold at higher frequencies. An unterminated cable presents a varying impedance to the source over frequency, and it can look capacitive or inductive depending on the length of the cable and the frequency. This behaviour can be explained by viewing the coaxial cable as a lossless transmission line. The input impedance Z_i of a transmission line with characteristic impedance Z_o and length L, terminated in a load Z_L, is given by:

$$Z_i = Z_o \frac{Z_L + jZ_o \bullet \tan \beta L}{Z_o + jZ_L \bullet \tan \beta L}$$

where $\beta = 2\pi/\lambda$, and λ is the size of one wavelength on the line. As an example, consider the standard RG58C/U 50Ω coaxial cable. If we terminate the cable with a 50Ω load, then by the above equation $Z_i = Z_o$ and the cable should look perfectly resistive over frequency. Figure 1.1 shows an actual measurement done on a 5′ long cable terminated in a 50Ω load. Except for minor impedance variations due to mismatch and line loss, the cable does look like 50Ω over a wide range of frequency. If the cable was terminated improperly, with a 75Ω load for example, the impedance then varies with frequency as shown in Figure 1.2. Note that even though we have terminated the cable with a resistive load, the cable impedance phase varies between ±23°. In the extreme, if the cable is unterminated, then $Z_L = \infty$ and the equation reduces to $Z_i = -jZ_o/(\tan \beta L)$. Figure 1.3 shows the input impedance of an unterminated 50Ω cable, and we see the phase skipping between −90° (capacitive) to +90° (inductive) at regular intervals. In fact, for frequencies at which the line length is an odd multiple of a quarter wavelength, Z_i becomes zero. Conversely, for frequencies at which the line is a multiple of a half wavelength, Z_i becomes infinite.

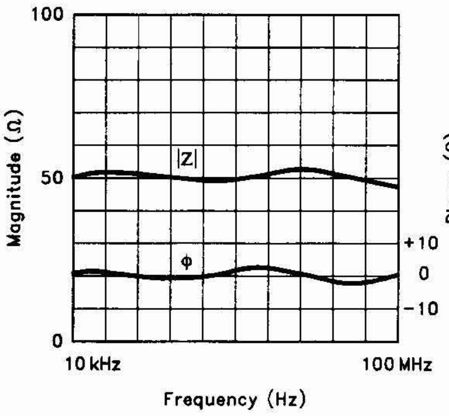


Figure 1.1. Impedance of a 50Ω Cable Terminated in 50Ω

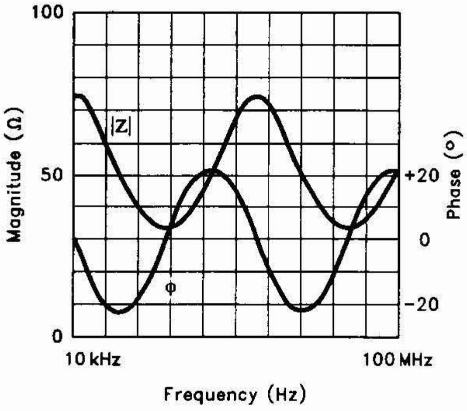


Figure 1.2. Impedance of a 50Ω Cable Terminated in 75Ω

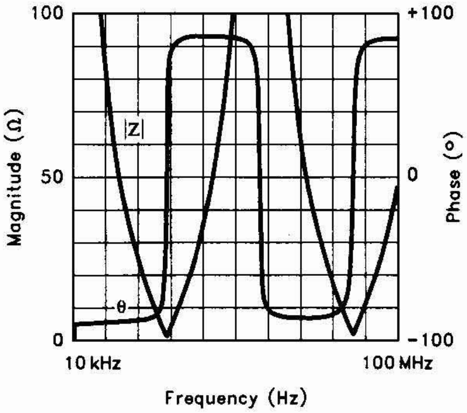


Figure 1.3. Impedance of an Unterminated in 50Ω Cable

The moral of the story is that you must terminate your cable with the correct load at high frequencies. Otherwise, the driving source will see a wildly changing load with frequency, and this may cause the amplifier to oscillate.

Discrete Capacitors

At high frequencies, another parasitic which becomes dominant is the inductance of a leaded capacitor. We can treat the capacitor as a series RLC circuit, with L modelling the lead inductance and R modelling the losses due to the electrodes, leads, and dielectric. The capacitor will thus self-resonate at a frequency given by:

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

As an example, the impedance of a 10 nF leaded ceramic capacitor was measured, yielding the equivalent series RLC values of 0.66Ω, 36 nH, and 8.6 nF respectively. Figure 1.4 shows the impedance of this capacitor over frequency, and we see that it self-resonates at 9.1 MHz, behaving as an inductor for frequencies above that. For this measurement the leads of the capacitor were kept as short as possible. If we were a bit sloppy and left 1″ leads on the capacitor, the inductance would increase to about 60 nH, lowering the resonance down to 7 MHz. Generally, an inch of slender wire has about 20 nH of inductance per inch, which is why it is so important in high frequency work to minimize lead length.

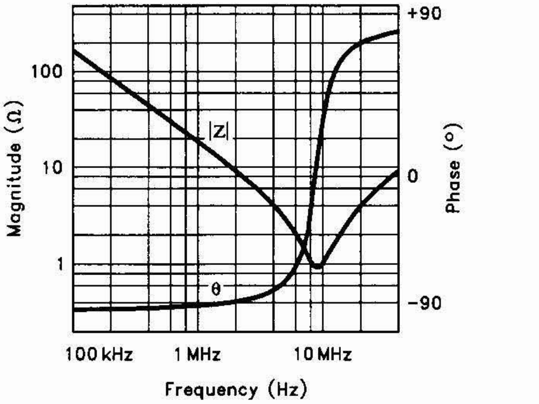
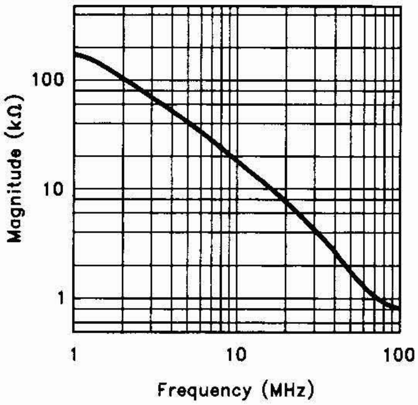


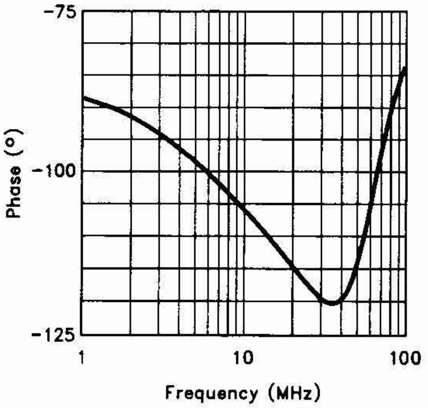
Figure 1.4. Impedance of a Leader 10 nF Capacitor

Inputs of Active Devices

Besides driving cables or passive loads, an amplifier could also be driving the input of another active device. At first, one might think that the input of an op-amp can be modeled by some high-value resistance in parallel with a capacitance. While this model is correct to some extent, some measurements quickly reveal that the input capacitance is not all that "pure". Figure 1.5 shows the input impedance of the EL2044 connected as an unity gain buffer. While the impedance does decrease with frequency, it does not do so at −6 dB/octave; rather, the impedance is decreasing at a greater rate. The phase of the input impedance also reveals the "impurity" of this input capacitance.



(a) Magnitude 0954-5



(b) Phase 0954-6

Figure 1.5. Input Impedance of a Unity Gain Follower Using The EL2044

Other Capacitive Loads

As the examples above may suggest, strictly capacitive loads are difficult to find at high frequencies. The only load we know of that is capacitive at high frequencies is a Liquid Crystal Display (LCD). In this instance, the intersection of the row and column lines causes many capacitances to be distributed along the line, and because of numerous parallel lines the inductance tends to be low, giving loads upwards of 1000 pF without large amounts of inductance.

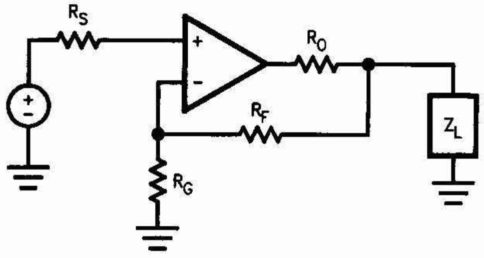
Although pure capacitive loads are rare at high frequencies, this does not mean that we can ignore them. Capacitive reactance can exist over narrow frequency ranges, and we must ensure that our amplifier does not oscillate in these ranges.

2.0 Capacitive Loads are Hard

Generally, an op-amp has no problem driving resistive or inductive loads. Of course, this statement needs to be qualified as to the size of the load, but the point is that both kinds of loads do not degrade the phase margin of the amplifier. Capacitive loads, on the other hand, do reduce an amplifier's phase margin, and in severe cases can cause the op-amp to oscillate.

Op-Amp Output Resistance

To see how various loads affect the phase margin, we can model the open-loop output impedance of an op-amp as the resistance R_O. Shown in Figure 2.1, R_O forms a divider with the load Z_L, and the output V_O goes to the feedback network R_F and R_G. If the phase lag of V_O increased due to the $R_O Z_L$ divider, the phase margin around the loop diminishes and peaking, even oscillation, will occur.



0954-7

Figure 2.1. Open Loop Output Resistance of an Op-Amp

First, if Z_L is resistive, then there is no phase lag and the phase margin is preserved. If Z_L is inductive, then V_O gets a phase lead and the phase margin is increased! Finally, if Z_L is capacitive then we do get a phase lag and the amplifier will peak due to this load. The severity of this problem increases with high speed op-amps, as the example below illustrates.

Suppose that we have a 100 MHz amplifier with 45° of phase margin. Let $R_O = 50\Omega$ and $Z_L = 15$ pF, then this network has a cutoff frequency f_c of 212 MHz. At 100 MHz, this network provides 25° of phase lag and thus reduces the phase margin to 20°. Severe peaking will result in the frequency response. The loss of phase margin due to a capacitive load is given by:

$$\Delta PM = TAN^{-1}\frac{f_u}{f_c}$$

8

where f_u is the op-amp's unity gain frequency, and f_c is the cutoff frequency of the R_oC_L network. Thus we see that for high frequency op-amps, even a small capacitive load can cause a large reduction in the phase margin.

Op-Amp Output Inductance

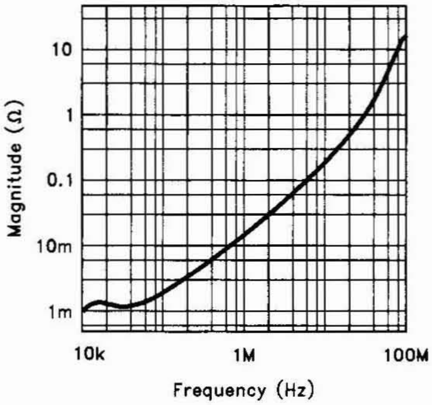
Another way to understand an op-amp's sensitivity to capacitive loads is to look at its closed-loop output impedance more closely. As an example, consider the output impedance vs frequency curve of the EL2044, reproduced in Figure 2.2. We see that beyond about 200 kHz, the output impedance actually looks inductive, and this would resonate with a capacitive load! To see why an op-amp's output impedance looks inductive, consider the circuit in Figure 2.3, where we have an op-amp with open loop gain A(s) and some general feedback network with gain β. The transfer function of this circuit is given by:

$$H(s) = \frac{A(s)}{1 + A(s)\beta}$$

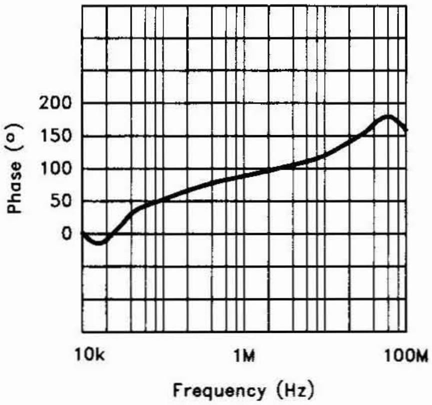
If the loop transmission $A(s)\beta$ is large, then $H(s) \cong 1/\beta$, and we arrive at one of the important results of negative feedback: the system's gain depends largely on the feedback network and not on the op-amp itself. Similarly, the system's output impedance is given by:

$$Z_{OUT} = \frac{R_o}{1 + A(s)\beta}$$

where R_o is the op-amp's open loop output resistance. Thus for large values of loop transmission, negative feedback drives the output impedance to some low value. As frequency increases, however, the magnitude of A(s) rolls off, reducing the loop transmission and raising Z_{OUT}. Eventually, at frequencies where $A(s)\beta << 1$, Z_{OUT} asymtotes to the output impedance of the op-amp output stage.



(a) Magnitude



(b) Phase

Figure 2.2. Closed Loop Output Impedance of EL2044

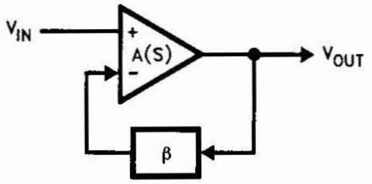
Output Stage Superinductance

Beyond the system level explanations given above, we can gain understanding into the problem by looking at the op-amp at the transistor level. In any op-amp we have an output stage that buffers the gain stage from the external load. The emitter follower is often used for this purpose, so we will consider the follower's output impedance under different conditions. Figure 2.4 shows the general circuit. At low frequencies we can find the output impedance using the reflection rule:

$$R_{OUT} = \frac{R}{\beta + 1}$$

At higher frequencies, however, we cannot neglect the frequency dependence of β. If we model β as a single-pole system with DC gain β_o and unity gain crossing w_u, then the output impedance becomes the following:

$$Z_{OUT} \cong \frac{R}{\left(\dfrac{B_0}{1 + j\dfrac{f\beta_0}{f_T}}\right)} = \frac{R}{\beta_0}\left(1 + \frac{f\beta_0}{f_T}\right) = \frac{R}{\beta_0} + jf\frac{R}{f_T}$$



0954-8

Figure 2.3. Block Diagram of General Feedback System

then we get the transformations shown in Figure 2.4. In the first case where the source is resistive, the output impedance is resistive and inductive. This is intuitively similar to the op-amp example presented earlier; since β decreases with frequency, R_{OUT} rises and thus appears inductive. Hence we see that even a simple emitter follower can resonate into a capacitive load. As an example, a transistor with an internal base resistance of 200Ω and a f_T of 300 MHz has an output inductance of 100 nH. If this was used to drive a 50 pF load, its resonant frequency would be at 70 MHz, well within the range of today's high speed op-amps.

The next transformation is for a capacitive source, which results in a resistive and capacitive output impedance.

Finally, when the source is inductive, the output impedance has a negative real component. This negative impedance has no reactive phase, but its magnitude increases as the frequency squared; we will name this component a "super-inductor". If the sum of series resistance in a network is negative and all the reactances cancel, then the network will oscillate. Thus the seemingly benign emitter follower really misbehaves if we drive it with an inductive source!

So where do we get an inductive source from within an op-amp? The Darlington connection is one possibility. In this configuration, an emitter follower drives another emitter follower. The first follower transforms its base resistance into an output inductance, and the second follower transforms this inductance into an output super-inductance. The effect is the same for a NPN follower driving a PNP, or vice versa. Since base resistance tends to be larger for IC transistors than for discrete transistors, super-inductance is very much an issue for monolithic amplifiers. An output stage with this topology is shown in Figure 2.5, first used in the LH0002 buffer amplifier. Most integrated amplifiers built with a complementary bipolar process also use this output stage, and so a real amplifier's output impedance is the sum of resistive, inductive, and super-inductive components. If a capacitive load resonates with the inductance at a frequency where the super-inductance is greater than the real resistance, oscillations will occur in the output stage independent of loop characteristics.

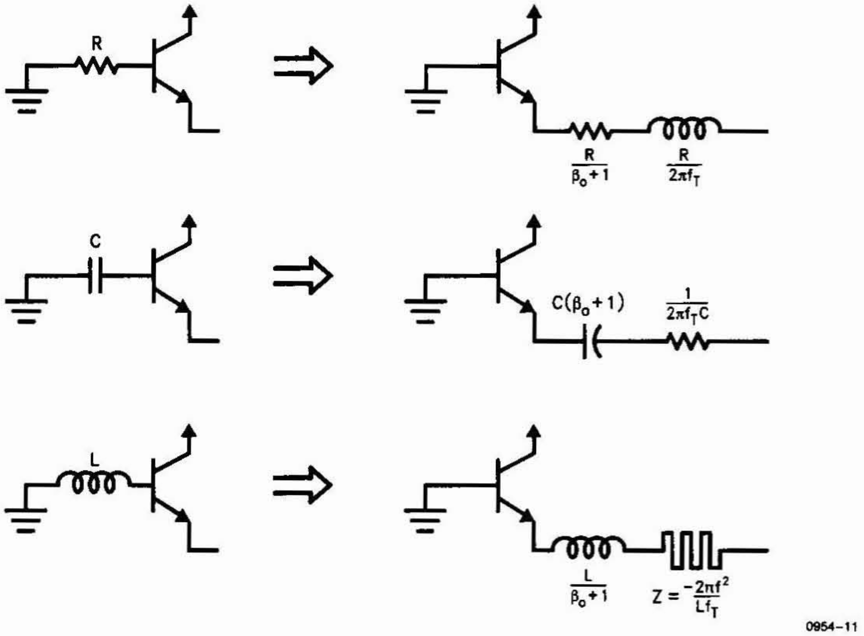

R
$\frac{R}{\beta_o+1}$
$\frac{R}{2\pi f_T}$
C
$C(\beta_o+1)$
$\frac{1}{2\pi f_T C}$
L
$\frac{L}{\beta_o+1}$
$Z = \frac{-2\pi f^2}{L f_T}$
0954-11

Figure 2.4. Impedance Transformations for an Emitter Follower with Various Source Impedances

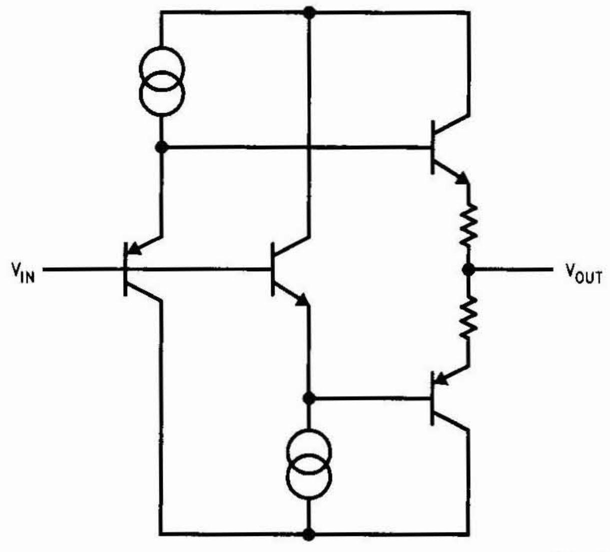


Figure 2.5. LH0002 Output Stage Topology

3.0 Possible Solutions

Like death and taxes, it is inevitable that we will have to drive some form of capacitance. Unlike death and taxes, techniques exist to deal with capacitive loads to some degree. We will present some of these techniques in the following sections.

Internal Compensation

As we saw earlier, heavy capacitive loads can reduce the phase margin of an amplifier, and thus cause the amplifier response to peak. However, if we can lower the dominant pole of the amplifier such that the phase margin is restored, then the overall amplifier response should not peak, although the bandwidth will also be reduced. Is there such a way of sensing the amount of capacitive load and adjusting the dominant pole appropriately? The answer is yes, and the solution can be seen in Figure 3.1, where a capacitor C_c has been connected between the gain stage and output of an op-amp.

First, consider a light load on the output (high R_L, low C_L). Driving this load, the two voltages V_{OUT} and V_{HIZ} should track each other closely, and no current will flow thru the R_cC_c combination. The compensation network does no work in this case, and we get the normal amplifier response as given by Curve A in Figure 3.2. Now suppose we raise C_L to some high value. The voltage V_{OUT} will not follow V_{HIZ} as closely, and current begins to flow in the R_cC_c network.

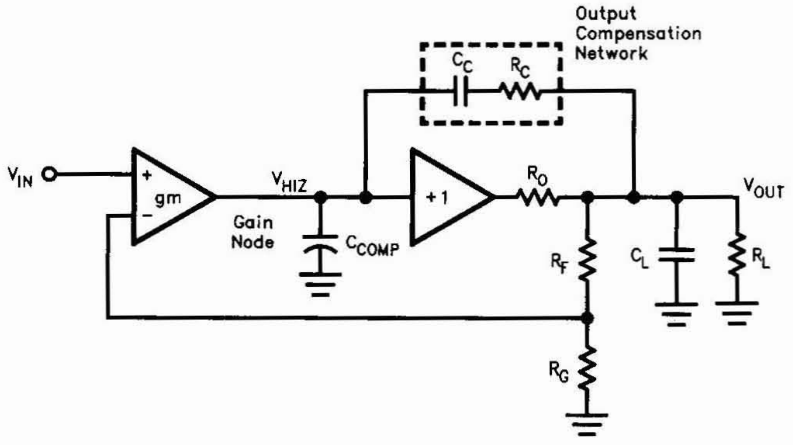


Figure 3.1. Compensation Scheme To Make Op-Amps More Tolerant of Capacitive Loads

This in effect puts part of C_c on the gain node, thus lowering the bandwidth of the amplifier. Curve B in Figure 3.2 shows what the response may look like in this case. On the other hand, Curve C shows what will happen if we did not use the compensation network to drive a large C_L; although we retain the bandwidth, severe peaking occurs.

This technique does have its drawback: the bandwidth reduces for heavy loads in general. Thus, the bandwidth lowers for heavy resistive loading as well, which is an undesirable trait. In addition, this technique degrades the RF linearity of the amplifier, ruining such performance parameters as differential gain and phase.

External Compensation—Series Resistor

To avoid sacrificing performance, most of Elantec's op-amps are not heavily compensated for capacitive loads. The use of external compensation networks may be required to optimize certain applications. Figure 3.3 shows one such network, where we have inserted a series resistor with the op-amp's output. The stabilizing effect of this resistor can be thought of in two ways. One is that R_{SERIES} serves to isolate the op-amp output and feedback network from the capacitive load. The other way to think about it is to recall the super-inductor concept introduced earlier. Since the output stage presents a negative resistance over certain frequencies, adding enough series resistance would cancel this negative resistance and prevent oscillation.

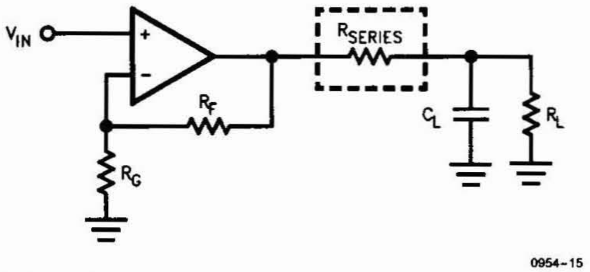


Figure 3.3. Series Resistor Compensation To Stabilize an Op-Amp Driving Capacitive Loads

The required amount of series resistance depends on the part used, but values of 5Ω to 15Ω is usually sufficient to prevent local resonances. The disadvantage of this technique is a reduction in gain accuracy, and extra distortion when driving nonlinear loads.

External Compensation—The Snubber

Another way to stabilize an op-amp driving a capacitive load is the use of a snubber, as shown in Figure 3.4. To see how a snubber can reduce peaking, consider the 300 MHz f_T transistor presented in Section 2. For that example, the output inductance of the emitter follower was shown to be 100 nH. With a light resistive load $R_L = 1\ k\Omega$ and moderate capacitive load $C_L = 50\ pF$, the circuit resonates at 70 MHz with a Q given by:

$$Q = \frac{R_L}{\sqrt{\frac{L}{C_L}}}$$

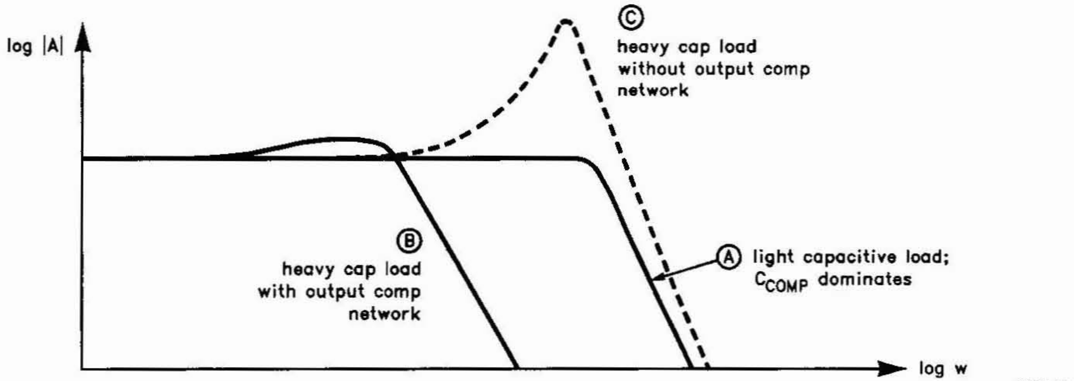


Figure 3.2. Effects of Compensation Scheme Shown in Figure 3.1

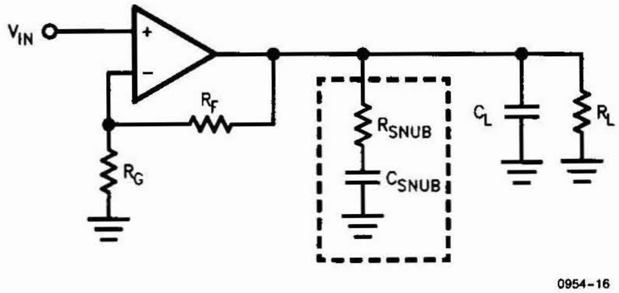


Figure 3.4. The Snubber

In this case, Q works out to be about 22, giving us severe peaking in the frequency response. However, with a load of 150Ω, the Q reduces to 3. Thus the extra stabillty gained with a heavy load resistor is desirable, but we may be wasting DC load current with this approach. A way around this is to insert a capacitor in series with the resistor, resulting in a snubber.

There are various ways to determine appropriate values for R_{SNUB} and C_{SNUB}, one of which is presented in [2]. We will describe an alternative method here. First, operate the amplifier as in the intended application and look at its frequency response on a network analyzer. Find the frequency at which the peak occurs, and denote that as f_p. Next, try loading the amplifier with different load resistances until the peaking reduces to a satisfactory level; this value will be R_{SNUB}. Finally, we need a capacitor that will make the snubber look resistive at the frequency of the peak. A rough guideline is to make the snubber zero frequency 3 times lower than f_p, resulting in the following design equation:

$$C_{SNUB} = \frac{3}{2\pi \bullet f_p \bullet R_{SNUB}}$$

Note that as opposed to the series resistor method, the use of a snubber does not degrade the gain accuracy or cause extra distortion when driving a nonlinear load.

Unterminated Coaxial Lines

As we may have hinted earlier, unterminated coaxial lines mean trouble. The simple remedy for this is to terminate the line in its characteristic impedance, and the cable will look like a stable resistive load to the driving amplifier.

In certain cases the cable termination may be unknown, or it may not be under our control at all times. A good example of this is in ATE systems, where an amplifier drives a signal through a coaxial cable to a test pin. However, when a device under test is not plugged in, the test pin is left unterminated, and so the amplifier is driving into an open cable. Figure 3.5 shows how we can use back-matching to solve this problem. In back-matching, we insert a resistor R_{BM} equal to the cable's characteristic impedance between the amplifier and the cable. R_{BM} serves to isolate the amplifier from the cable, the impedance of which could wildly vary with frequency. Also, since R_{BM} terminates the cable at the source end, reflected signals are absorbed in R_{BM}, preventing multiple reflections from occurring.

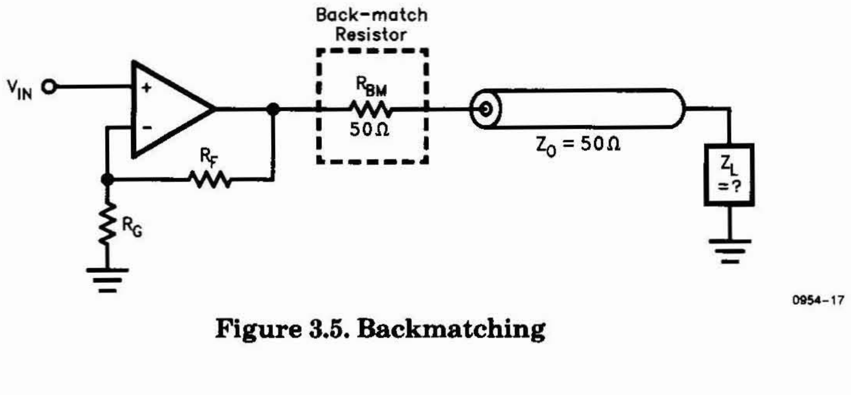


Figure 3.5. Backmatching

4.0 Summary

High frequency op-amps are sensitive to capacitive loads due to the loss of phase margin in driving these loads. In addition, the op-amp output stage can introduce its own resonance, further complicating the stability issue. These problems can introduce severe peaking in the frequency response or excessive ringing in the transient response. Some recent op-amp designs have incorporated an internal compensation network for capacitive loads. Such op-amps, however, sacrifice bandwidth and RF linearity in return for foolproof usage. For the best performance, amplifiers without the internal compensation network should be used in conjunction with a snubber when necessary. Proper bypassing and board layout have not been stressed in this application note, but they are equally important to the well-being of a high speed op-amp.

References

1. Cheng, David K., *Field and Wave Electromagnetics*, Addison-Wesley: New York, 1989.
2. Siegel, Barry. "High Frequency Amplifier Instability". Elantec, October 1992.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Current Boosted and DC Stabilized Half Bridge Driver

Current Boosted and DC Stabilized Half Bridge Driver

by Les Mills

Following are two applications notes for the EL7661 half bridge driver.

1. The current boosted half bridge driver offers the control functions of the EL7661 with enhanced drive capability. For example an application with $V_S = 16V$, a 25 ns turn on time and a 3000 pF load would require $I_{PK} = (V_S + V_{GS}) * C/T_{ON} = (16 + 10) * 3000$ pF/25 ns = 3.12A peak current from the driver. Since the EL7761 specifies $I_{PK} = 1A$ typical, the output requires current boosting to achieve the desired turn on time. This circuit is also useful in applications where the switching time is less stringent or the load is lighter but the output is required to swing over a greater range due to higher supplies voltages.

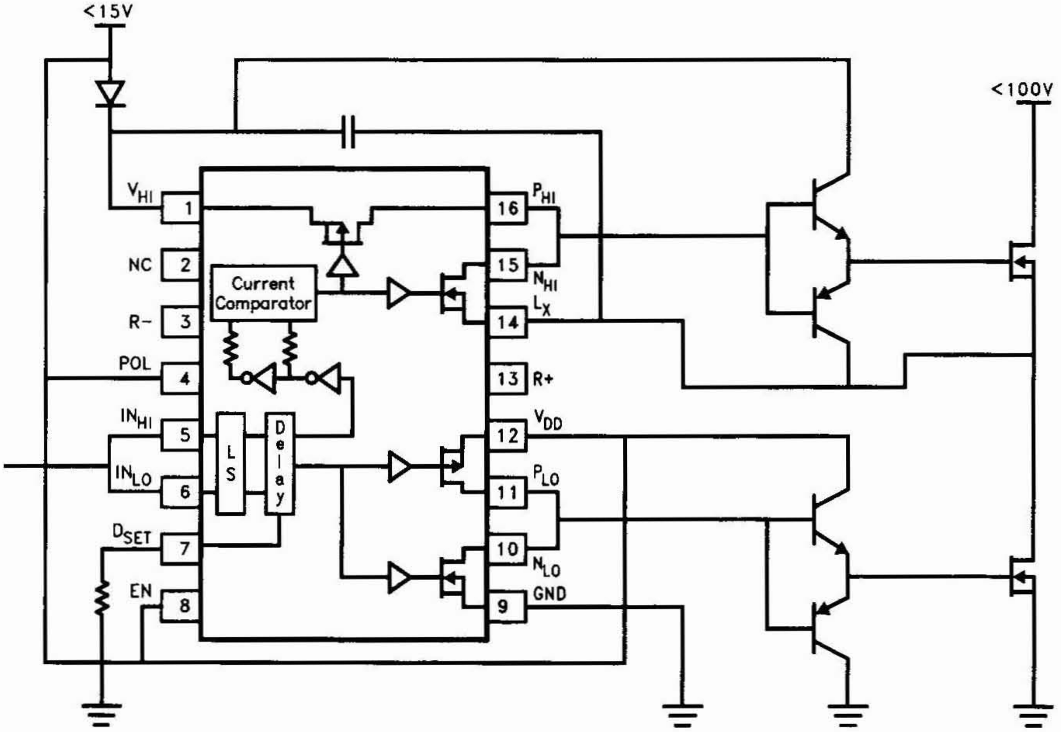

<15V
<100V
V_HI
1
NC
2
R−
3
POL
4
IN_HI
5
IN_LO
6
D_SET
7
EN
8
16
P_HI
15
N_HI
L_X
14
13
R+
12
V_DD
11
P_LO
10
N_LO
9
GND
Current Comparator
LS
Delay
0955-1

Figure 1. EL7661 Half Bridge Driver with Output Current Boost

2. DC stabilization of the half bridge driver is achieved by charge pumping the high side supply storage capacitor while the output is in the high state. This keeps the top half of the circuit (V_{DD} to L_X) biased at 12V when a 12V Zener is used as shown. The Zener should be 15V or less. The EL7232 was selected for the oscillator since its output must swing between GND and the 16V supply and provide a minimum of 10 mA, the supply current of the EL7761. The EL7232 is capable of 1.5A peak. Any driver providing 30 mA, swinging between GND and the 16V supply would also be suitable.

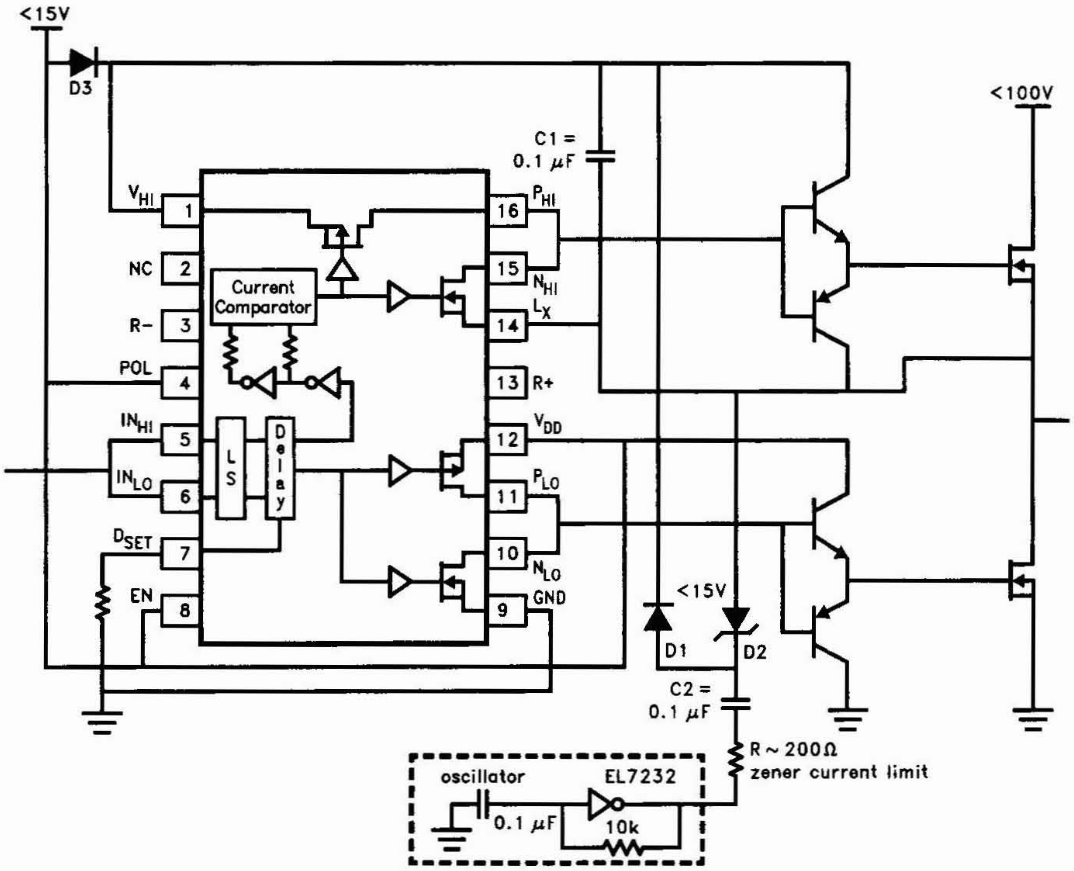

<15V
D3
C1 =
0.1 µF
<100V
VHI
1
NC
2
R-
3
POL
4
INHI
5
INLO
6
DSET
7
EN
8
16
PHI
15
NHI
14
LX
13
R+
12
VDD
11
PLO
10
NLO
9
GND
Current Comparator
L S
Delay
<15V
D1
D2
C2 =
0.1 µF
R ~ 200Ω
zener current limit
oscillator
EL7232
0.1 µF
10k
0955-2

Figure 2. EL7661 Half Bridge Driver DC Stabilized with Output Current Boost

25 kHz Electronic Ballast Using The EL7981 Delay Driver

by Bruce Rosenthal

Introduction

Electronic ballasts are rapidly gaining market acceptance, as ballast prices drop, electrical rates increase, and performance improves. Their primary advantages are: (1) the elimination of flicker, and noise (hum), (2) increased efficiency resulting in a cost advantage, and (3) reduces size and weight. The EL7981 is particularly well suited for this application by using the programmable delay and high current drive features.

System Operation

The ballast, in many respects, resembles an OFF-LINE Switch-Mode Power Supply. The 120 VAC line is rectified and doubled, developing ≅ 300 VDC rail-to-rail. When the intensity switch is set to "Low", the doubler is eliminated, and 150 VDC is produced. A "half bridge" configuration, using (2) Power MOSFET's drives an LC resonant circuit, with sufficient "Q" to develop the necessary starting voltage. The resulting current and voltage to the lamp are sinusoidal. Isolated drive to the FET's is provided with a transformer coupled from EL7981 Dual Delay Driver. The delay function allows for the "Recovery Time" of the parasitic diodes in the Power Mosfet's. A 555 timer generates the desired clock frequency. The clock can be tuned to the resonant frequency of the series L-C network. For tutorial reasons, auxillary power for the clock and driver were supplied externally, however, in practice a simple charge-pump can be used to develop the 10V supply.

Lamp

The "F40" 40 watt, 48″ flourescent lamp was selected for its popularity, and low cost. Above 20 kHz, these flourescent lamps behave like a 300Ω resistor because the plasma is maintained. The "striking" voltage for a cold tube is around 400V, however, this can be reduced by supplying current to the starter filament. Additional lamps can be added, but require separate L-C networks. 25 kHz operation was chosen, because it's above the audible range, yet not so high, that switching losses would be of concern. Increased lamp life has been reported by operating at these frequencies compared to 50 Hz–60 Hz.

EL7981

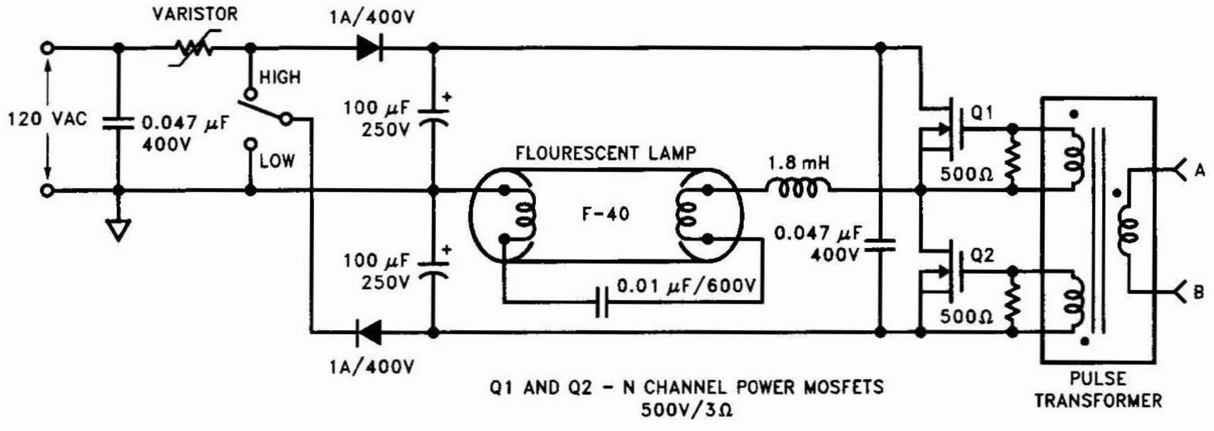
The EL7981 Dual Delay Driver generates a programmable delay to the rising edge of the output waveforms. Each output has a nominal "ON" resistance of 5Ω, and can source and sink 1A. With R_{SET} = 300 kΩ, the delay is about 1.5 μs, which provides sufficient time for the parasitic diodes in the FET's to recover. The strong output devices are suitable for driving the "Gate" transformer directly. The resulting gate drive waveform has (3) distinct levels: −10V, 0V, +10V.

Magnetics

The two magnetic components of the Ballast are (1) the gate transformer, and (2) the output resonating inductor. The output inductor is rated at 1.8 mH (Magnetic Circuit Elements Inc. #OC25BL25). The gate transformer is wound 1:1:1 and is tightly coupled to provide fast switching. (Magnetic Circuit Elements Inc. #0-1853T1). For further information on these components, contact John Conklin at Magnetic Circuit Elements (408) 757-8752.

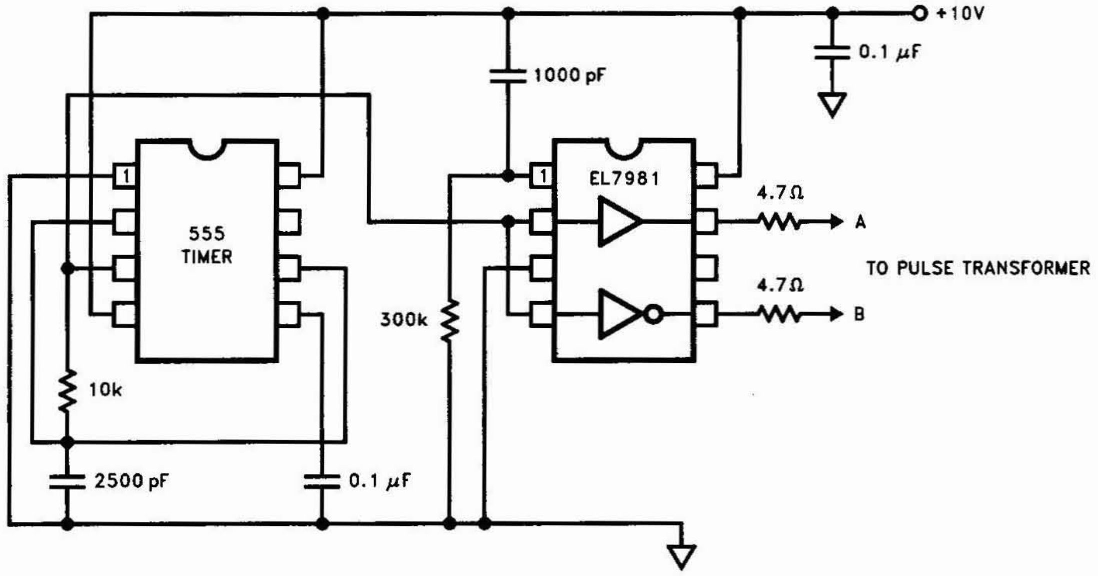
25 kHz Electronic Ballast Using The EL7981 Delay Driver

Electronic Ballast (Power Mesh)


VARISTOR
1A/400V
HIGH
LOW
120 VAC
0.047 µF
400V
100 µF
250V
FLOURESCENT LAMP
F-40
1.8 mH
0.047 µF
400V
0.01 µF/600V
100 µF
250V
1A/400V
Q1
Q2
500Ω
500Ω
A
B
PULSE
TRANSFORMER
Q1 AND Q2 - N CHANNEL POWER MOSFETS
500V/3Ω

0956-1

Electronic Ballast (Gate Drive Circuit)


+10V
0.1 µF
1000 pF
1
555
TIMER
1
EL7981
4.7Ω
A
4.7Ω
B
TO PULSE TRANSFORMER
300k
10k
2500 pF
0.1 µF

0956-2

Temperature Compensation for the EL4581C and EL4583C

by Chris Siu

The EL4581C and EL4583C are sync separators with on-board filters. It has been found that over temperature, the propagation delay of composite sync varies due to this filter. For example, in the 25°C to 85°C range, the delay varies by about 20 ns. The reason for this is that as temperature increases, the g_m of transistors in the filter stage drops, causing the filter bandwidth and delay to change. A solution for this is to introduce a PTAT (Proportional To Absolute Temperature) bias current for this stage, thus maintaining a constant g_m as temperature increases.

For the EL4581C, the filter bias current is set by the resistor R_{SET} on pin 6. We replace this with a resistor and two diodes in series as shown in Figure 1 below. Since the diode voltage has a negative temperature coefficient, this would increase the bias current thru R_{SET} as temperature rises. Shown in Table 1 below are the propagation delays over temperature with and without compensation. With compensation, we achieved a threefold improvement over the uncompensated case.

Table 1. Propagation Delays for the EL4581C

Temperature (°C)	Delay w/o Comp (ns)	Delay with Comp (ns)
25	233	232
50	240	228
85	253	226

Note: Propagation delay is defined as the time from the rising edge of the input horizontal sync to the rising edge of the CSYNC output.

If we look more closely at the above results, however, we see that the circuit is over-compensating, causing the delay to decrease with temperature. The two diodes actually provided too much of a PTAT current, whereas a single diode does not create enough PTAT current. Thus, the ideal compensation would provide about one and a half diodes of temperature coefficient.

Shown in Figure 2 below is a circuit which does the job; it is a V_{BE} multiplier with a multiplication factor of about 1.6. Measured on the scope, there is no perceivable delay variations in the 25°C to 85°C temperature range. Since the measurement accuracy is limited by the waveform jitter, the delay may have actually changed by 1 ns to 2 ns, but this should not present a problem for most applications.

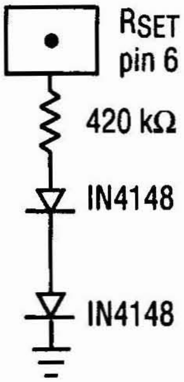


Figure 1. EL4581C Compensation Network

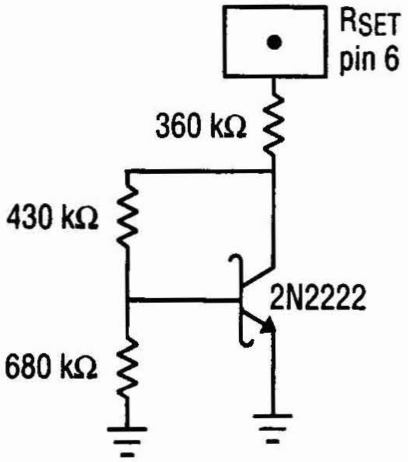


Figure 2. Improved Compensation Network

For the EL4583C, however, the filter bias current is not controlled by R_{SET}, but by the Filter Cutoff resistor RF on pin 1. Moreover, since there is only about 0.5V on this pin at room temperature, putting a diode in series with RF would not work in this case. A compensation network which circumvents this problem is shown in Figure 3 below. At room temperature, the voltage at node A would be about 0.7V due to the diode, and since node A is higher than node B, R_2 would inject a current into RF, thus requiring a smaller current from pin 1 than would otherwise. As temperature rises, the voltage at node A would decrease, such that R_2 would take current away from RF and requiring pin 1 to supply more current. We have thus achieved the desired PTAT effect on pin 1 with this arrangement, and the results using this network is shown in Table 2.

Table 2. Propagation Delays for EL4583C

Temperature (°C)	Delay w/o Comp (ns)	Delay with Comp (ns)
25	243	247
50	250	244
85	261	246

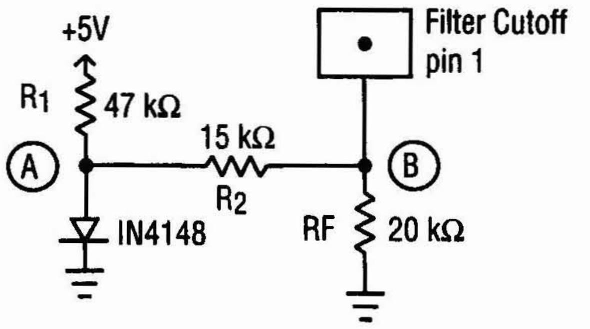


Figure 3. EL4583C Compensation Network

We can see that with these compensation schemes, we obtained a drastic reduction in propagation delay drifts over temperature. For comparison the delay drift of the LM1881 is also shown.

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EL75XX Thermal Design Considerations

Thermal Design Considerations—EL75XX

by Vijay Soman

1.0 Introduction

Elantec's EL7560C/EL7561C/EL7556C series of voltage regulators are highly integrated, simple to use and the most effective switching mode designs to power microprocessors such as Intel Corporation's *Pentium® Pro, and *Pentium. The EL7560C/EL7561C is designed for classes of processors such as the Pentium Pro. EL7556C is designed primarily for Pentium class desktop models.

These devices are packaged in a 28-pin power SO package (28 PSOP 2) developed by Amkor Corporation. The 28 PSOP 2 is a 28-lead surface mount package with 50 mil lead centers. It includes a specially designed copper slug on which the die is attached. The copper slug provides the excellent power dissipation capability required for these devices. Two versions, "Slug up" and "Slug down", are available for various board mounting and heatsink options. This application note describes the various package and heatsink combinations, which can be used with the EL75XX series.

2.0 Typical Applications Power Requirement

The typical power applications requirement for microprocessors is either a VRM (Voltage Regulator Module) or a direct mother board solution, both options operate under certain power dissipation, environmental, physical, and, of course, cost constraints. Table 1, below, summarizes the majority of typical applications requirements.

Several other variations in ambient temperature and airflow conditions may exist in practice, depending upon the user's board layout and system configurations.

3.0 Structure and Characteristics of the 28 PSOP 2

Figure 1 illustrates the structure of the Amkor PSOP 2 package. The copper slug is 535 x 170 mils in dimension and its thickness is optimized in order to arrive at a good compromise between biggest size possible for maximum thermal performance and the smallest foot print for the package. The die can either be soft soldered to the slug or attached using a thermally conductive epoxy.

Table 1

Application	Thermal Requirement	Typical Environment	Thermal Resistance Required
VRM-Pentium Pro	Pdiss = 3.4W, T_J = 105°C	T_A = 60°C, 100 LFM	θ_{JX} = 13°C/W
VRM-Pentium P54/55	Pdiss = 2.4W, T_J = 105°C	T_A = 50°C, 100 LFM	θ_{JX} = 23°C/W
Laptop-Pentium P54	Pdiss = 1.6W, T_J = 105°C	T_A = 50°C, No Airflow	θ_{JX} = 34.3 C/W

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*Pentium® Pro and Pentium are registered trademarks of Intel Corporation.

The slug provides low thermal resistance from the die to the external heatsink and also through the leads. At the same time, it provides a large thermal capacitance to absorb power peaks during switching. Thermal resistance (θ_{JC}—junction to case) for a typical 100 x 100 mil die is 4–5° C/W. The electrical lead resistance is in the range (5) mmhos; inductance is typically (2 nH) per lead and capacitance is about 1 pF. The package comes in two different lead stand-offs: normal stand-off is 9 mils and low stand-off is 2 mils. The two board mounting options are shown in Figure 2.

4.0 Components of Thermal Resistance and Heat Dissipation

Long term reliability of the semiconductor device is enhanced by keeping the junction temperature (T_J) as low as possible consistent with the given application. (See Elantec "Reliability and the Electronic Engineer" Tutorial #1.)

T_J—Junction temperature is a function of the amount of heat dissipated, the thermal resistance between the junction and the ambient air, and the ambient air temperature.

PSOP 2—Exposed Slug with Coupled Leads

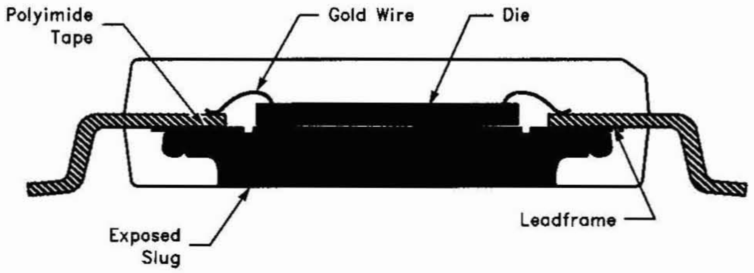

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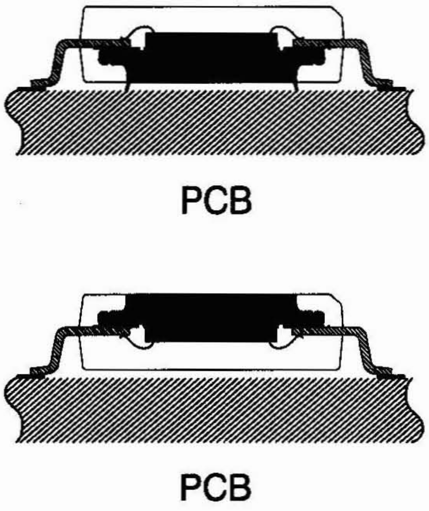
Figure 1. 28 PSOP 2 Structure



- PowerSOP2:
—Direct slug solder to PCB
—Low stand-off (4 mils)

- PowerSOP2:
—Die down
—Slug exposed to ambient

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Figure 2. 28 PSOP 2 Board Mounting Options

Integrated thermal resistance (θ_{IT}) is the sum of the following individual thermal resistances.

θ_{JC}—Thermal resistance from junction to case (die size, d/a, package dependent).

θ_{CH}—Thermal resistance from case to heatsink (interface—package to heatsink dependent).

θ_{HA}—Thermal resistance from heatsink to ambient (heatsink dependent).

Thus,

$$\theta_{IT} = \theta_{JC} + \theta_{CH} + \theta_{HA} \ (^\circ C/W)$$

As stated above in section 2, the thermal resistance required is the total integrated thermal resistance θ_{IT} under the "In Situ" applications condition.

θ_{JC}—Thermal resistance from junction to case depends on the die size, Cu slug size, the die attach material and the lead frame. In the case of PSOP 2 package, almost all the heat from the die is conducted through the Cu slug and very little through the leads.

Figure 4 shows the relationship between θ_{JC} and die size for a given package and die attach material.

θ_{CH}—Thermal resistance from case to heatsink is dependent upon the thermal properties of the interface used to attach the heatsink to the copper slug of the package. Various types of heat conducting pads, thermal greases and thermal epoxy bonding materials are available from several manufacturers. Table 2 shows estimated values of θ_{CH} for several types of epoxy bonding materials.

θ_{HA}—Thermal resistance from heatsink to ambient is a function of the conduction through heatsink material to the dissipating surface area; convection (natural or forced); and radiation from the heatsink surface area. Different designs of the sizes of heatsinks are available to achieve maximum conduction and convection. Forced air can be used to improve convection and black anodizing can improve heat dissipation through radiation.

5.0 Thermal Resistance—28 PSOP 2

The 28POSP 2 is available in two versions—the "Slug down" in a low stand-off version (2 mils) and a "Slug up" version with a standard stand-off of 9 mils. The slug down version is suitable for direct mounting onto the PCB by using surface mount solder technique. The heat dissipating copper area on the circuit board can be configured in various shapes and sizes depending upon the particular application. Figure 3 shows a typical configuration for heat dissipating copper clad. Thermal resistance measurements for the slug down version are listed in Table 3. Medium power dissipations of up to 2W are easily obtainable in practice with this configuration. The slug up version offers more heat sinking options. One of the most beneficial options is to epoxy bond a suitable heatsink to the package slug as shown in Figure 5 and Figure 6.

Another heat sinking option is to use a mounting clip to secure the heatsink to the PCB, as shown in Figure 7 adding mechanical strength against shock and vibration. Heatsink arrangements shown in Figure 5 and Figure 6 offer very effective heat dissipation under forced air condition of 100 LFM–200 LFM in a typical PC system application. (See Figure 8 for effect of forced air convection on thermal resistance.) The methods shown in Figure 5 and Figure 6 allow power dissipations in the 2W–9W range, as shown in Table 3. Figure 9 graphically summarizes the power dissipation capability of the 28 PSOP 2.

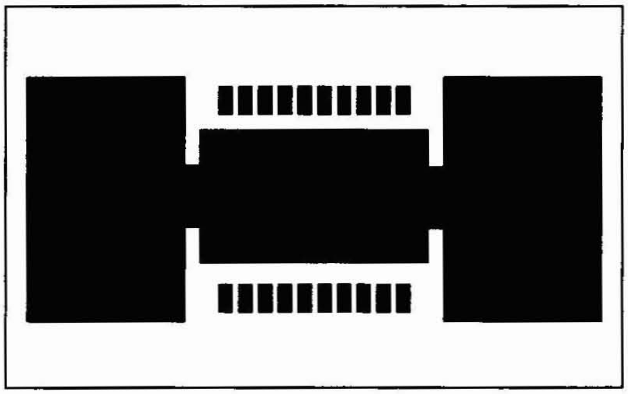

Figure 3. Typical Footprint for a Heat Dissipating Copper Clad

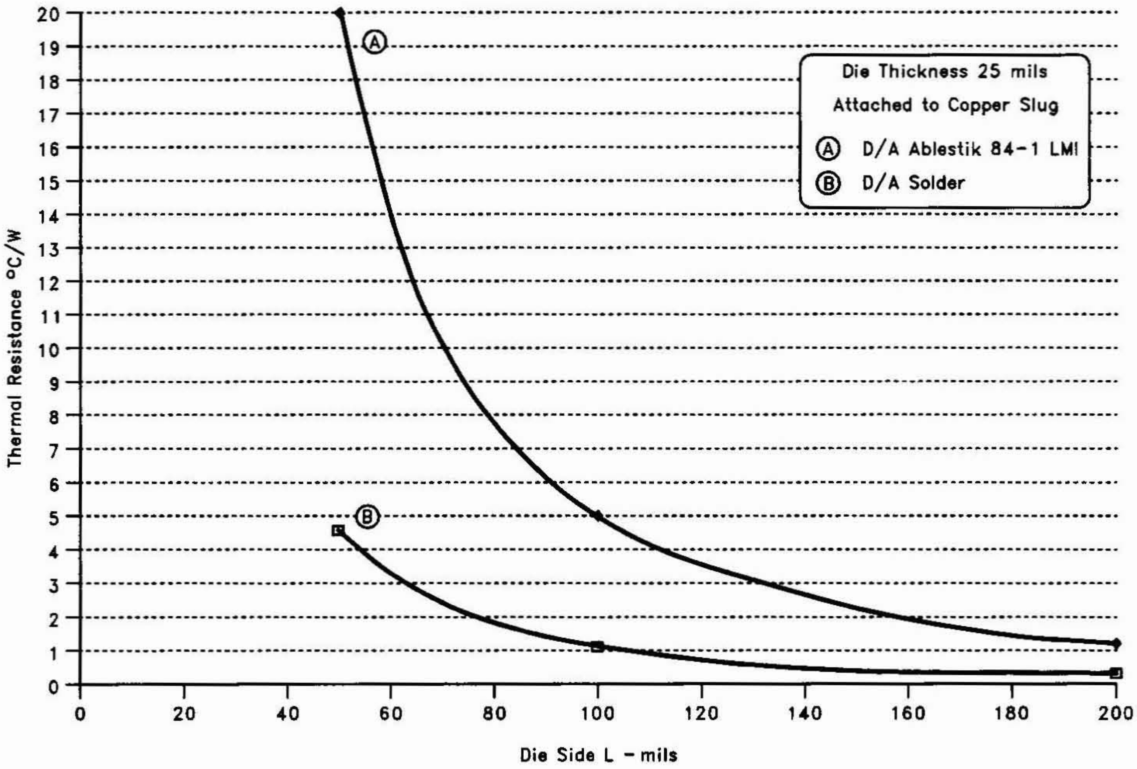

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Figure 4. Thermal Resistance—θ_{JC} 28PSOP 2

Table 2. Thermally Conductive Bonding Materials

Manufacturer	Type	Thermal Conductivity	Strength Mechanical (Bond Shear)	Thickness Applied	θ_{CH}-°C/W Thermal Resistance
Ablestik	84-1LMIT	4.3 w/mk	6000 psi	2 mils	0.2
Wakefield	120	0.74 w/mk	—	2 mils	1.1
Thermagon (Elastomer)	T-pill 210	6 w/mk	—	10 mils	0.14
Wakefield Deltabond	152-B4	0.9 w/mk	2300 psi	2 mils	0.95

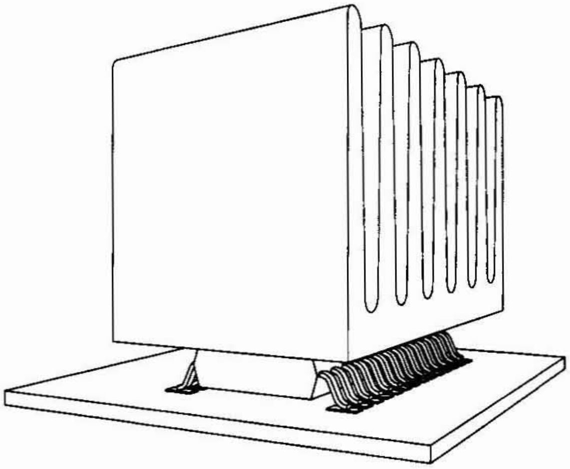

Figure 5. PSOP 2 with Wakefield # 8052-60 Heatsink

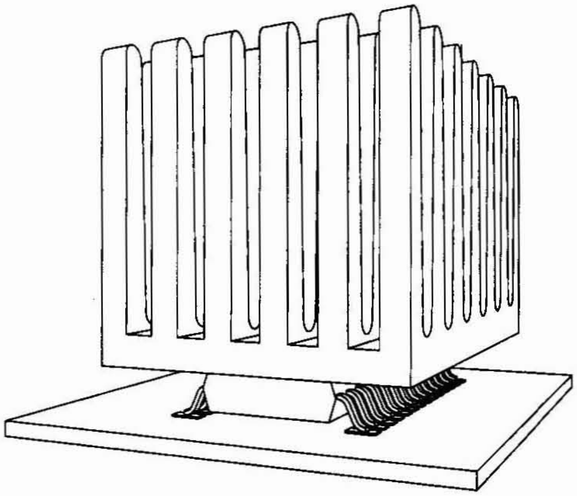

Figure 6. PSOP 2 with Wakefield Penguin # 658-60A Heatsink

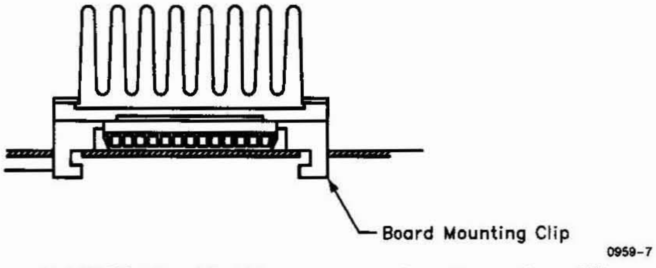
Board Mounting Clip
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Figure 7. PSOP 2 with Heatsink and a Mounting Clip

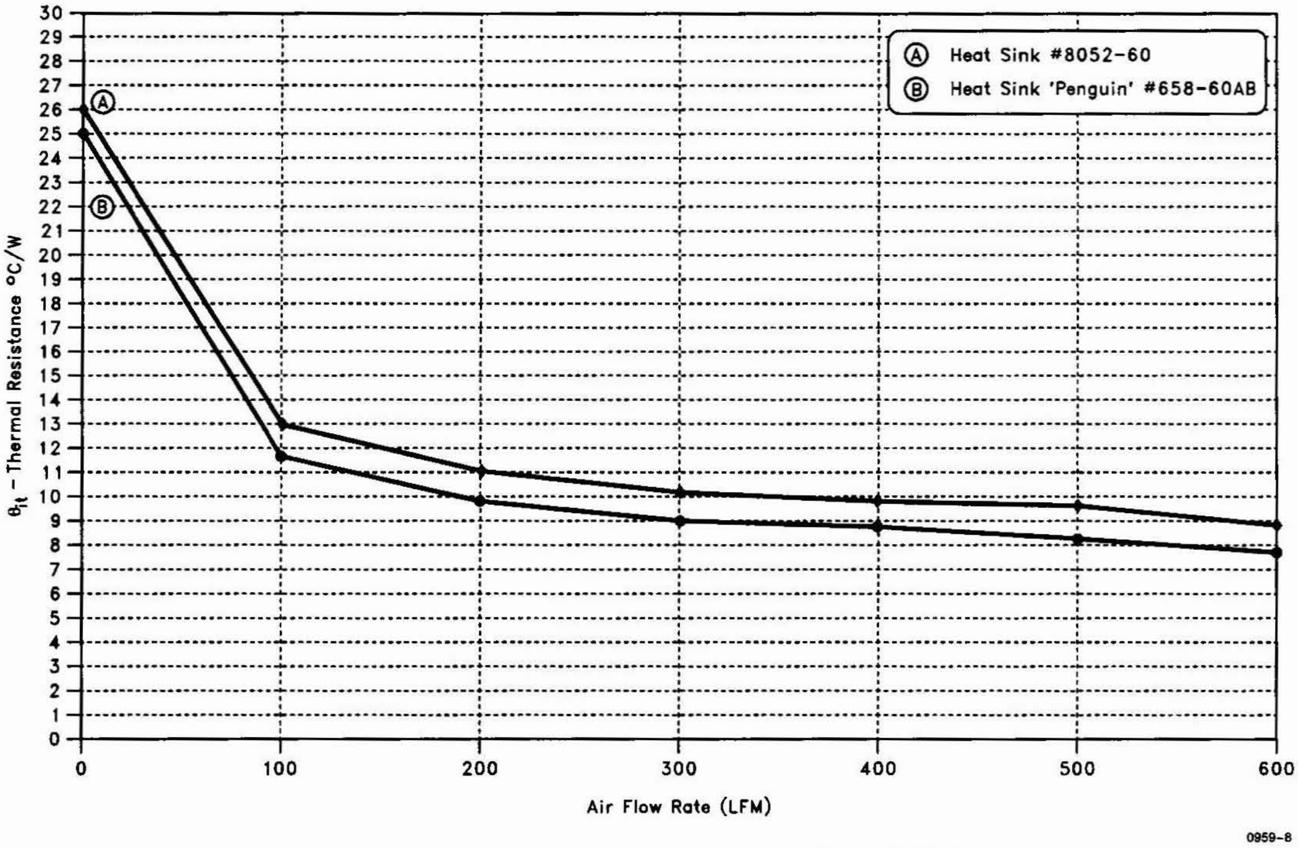

Figure 8. Thermal Resistance vs Air Flow—LFM

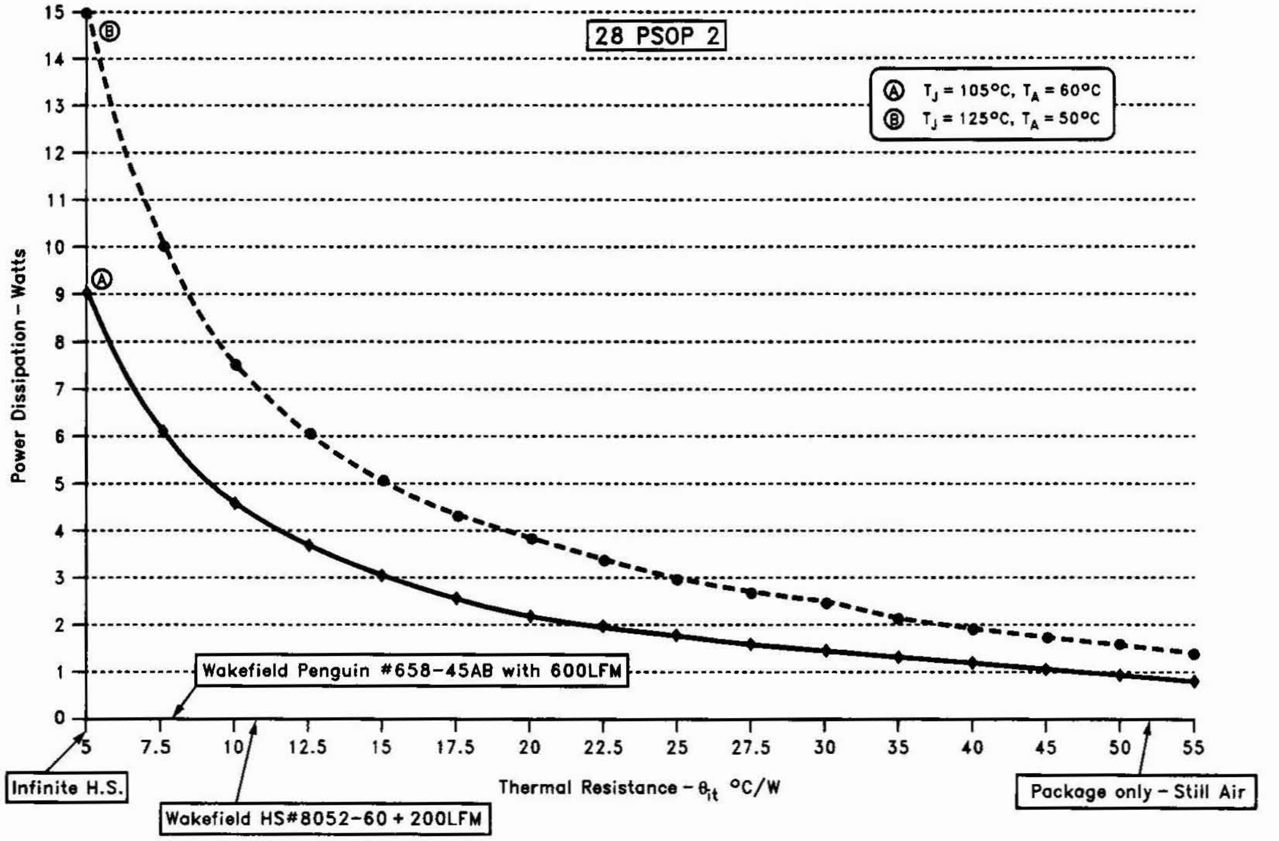

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Figure 9. Power Dissipation vs Thermal Resistance

Table 3. Power Dissipation Capability of 28 PSOP 2

Mounting Condition	Ambient Condition	Thermal Resistance °C/W	Power Dissipation-Watts			
			ΔT 45°C A	ΔT 55°C B	ΔT 60°C C	ΔT 75°C D
I. Slug Up						
Package Only	Still Air	52	0.87	1.05	1.15	1.44
Package + Wakefield H.S. #8052-60	Still Air	25	1.8	2.2	2.4	3
Package + Wakefield H.S. #8052-60	Air Flow 100 LFM	12.9	3.5	4.3	4.65	5.8
Package + Wakefield H.S. #8052-60	Air Flow 200 LFM	11	4	5	5.45	6.8
Package + Wakefield H.S. Penguin #658-60AB	Air Flow 600 LFM	7.7	5.8	7.2	7.8	9.8
II. Slug Down						
Package Soldered to 3″ sq Cu PCB	Still Air	33.4	1.3	1.65	1.8	2.2
Package Soldered to 3″ sq Cu PCB	Air Flow 100 LFM	30	1.5	1.8	2	2.5

Notes: A—$T_J = 105°C, T_A = 60°C$
B—$T_J = 105°C, T_A = 50°C$
C—$T_J = 110°C, T_A = 50°C$
D—$T_J = 125°C, T_A = 50°C$

All thermal resistance measurements were done with a thermal die size of 100 x 100 mils. The actual die size of the EL7560/61 is larger than the thermal die therefore, the thermal resistance of the EL7560/61 will be 1-3°C/W lower than the numbers in the table.

Conclusions

Powering of the *Pentium® Pro and *Pentium microprocessors presents a challenge in thermal management. It has been demonstrated that by utilizing special power dissipating capability of the 28 PSOP2 package and an appropriate heatsink, the EL7560C/EL7561C and the EL7556C DC regulators will successfully power Pentium and Pentium® Pro microprocessors. Power dissipations from 2W to 6W can easily be achieved, while keeping the junction temperature as low as 105°C.

Acknowledgments

The Author wishes to thank Ratnaji Arumilli for his work on thermal modeling, Mas Kobashi and Dave Mabrey for their efforts in thermal resistance measurements and also Amkor Ltd for their support in supplying thermal die packaged in PSOP2 packages.

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2. Simple Method of Characterizing Hybrid Package Thermal Impedance—Steve Ott and Barry Siegel, Hybrid Circuits Technology, June 1990
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An Improved Peak Detector

by Tamara I. Ahrens

Diodes have long served as adequate rectifiers despite necessarily large input voltages and poor accuracy. The most common configuration for a simple diode peak detector (Figure 1) provides a mediocre 10% error for very large input voltages (Figure 2). If the diode is linearized, the necessary input voltage is only reduced to 1V peak for the same 10% error (Figure 2). However, development of high frequency op amps allows feedback circuitry to provide better accuracy and more sensitivity at the input. With feedback (Figure 3), peak detection is feasible at input voltages as small as 50 mVrms.

Function of Feedback Diode Circuitry

The input stage consists of a high frequency op amp whose output is fed into both a diode (D1), which functions similar to the diode of a simple peak detector, and a clamping network, which limits the negative output swing of the forward op amp. The output of the diode (D1) is connected to the storage capacitor and is also fed back to the input through a buffer. A storage capacitor of 0.1 μF is recommended for peak detection at audio frequencies. A small resistance is shown in series with the storage capacitor to isolate it from the feedback loop. The smallest functional value is recommended for minimal peaking and maximum bandwidth; 10Ω is suggested. A bleed current is necessary to allow the output to relax for a smaller input or in the absence of an input. 20 μA, small enough to avoid deteriorating the output value substantially, but large enough to dominate the bias current of the feedback buffer, was chosen. The output of the buffer is fed back to the negative input of the forward op amp through a resistor. This resistor buffers the emitter of the pnp transistor of the clamping network from the low impedance at the output of the buffer. Please note: a compensation capacitor on the forward op amp may be a necessary addition to ensure stability and the output of the entire peak detection circuit must be buffered to prevent a disturbance in performance.

Clamping Network

The diode (D2) of the clamping network is always held on by the current source. For voltage signals greater than the peak held at the output, the forward, rectifying diode (D1) is conducting, the output voltage is raised to match the input voltage, the buffer feeds that voltage back around to the negative input of the forward op amp, and the emitter of the pnp transistor is held at the same voltage as its base, keeping it off and eliminating the second feedback loop.

For voltage signals less than the peak held at the output, the rectifying diode (D1) is off. The emitter of the pnp transistor is set as high as the output voltage by the buffer through the 1 kΩ resistor while the base is pulled down by the output of the forward op amp through the feedback diode (D2). The 270Ω resistor adds a 0.3V bias to the base of the transistor producing a charge-discharge current ratio of 10,000:1. When the transistor turns on, a crude unity gain feedback loop is completed through the clamping network (from the output voltage, down a diode drop and up the base-emitter diode of the transistor, to the input voltage) and a voltage drop builds across the 1 kΩ resistor. This clamping action minimizes the recovery time of the circuit. Since the clamping network works like a unity gain buffer for inputs less than the peak voltage, the output needs to slew less than one diode drop to turn on the rectifying diode (D1) for inputs greater than the peak voltage. In this manner, the clamping network prevents the forward op amp from exhibiting open loop behavior and railing negative for inputs less than the peak voltage. This greatly reduces the slew rate necessary to achieve a desired bandwidth.

Amplitude Considerations

This circuit has the ability to function with amplitudes 30 times smaller than a simple diode peak detector. The EL2244C has an open loop gain of 60 dB, raising smaller input signals enough to be detectable by the diode. The smallest amplitudes recoverable will be determined by the noise amplified within the circuit. For the given circuit, this limit is approximately 30 mVrms input voltage. The largest amplitudes allowable will be determined by the input constraints of the op amp. For the EL2244C at ±5V supplies, the maximum input range is approximately ±3.5V.

Frequency Considerations

If 5% errors can be tolerated, this circuit has a bandwidth of 100 kHz (Figure 4), making it ideal for audio applications. A great deal of small signal bandwidth and large slew rates are necessary to swing quickly through the dead zone at the output of the first op amp and these quantities limit circuit performance.

Thus, for a handful of inexpensive parts, a drastic improvement can be made in the performance of a peak detector over that of a simple diode. With the utilization of modern, high-speed op amps, the feedback diode peak detector offers almost two decades of input voltage range improvement while maintaining functionality into the megahertz range.

Note: Reprinted from Electronic Design, June 26, 1995.

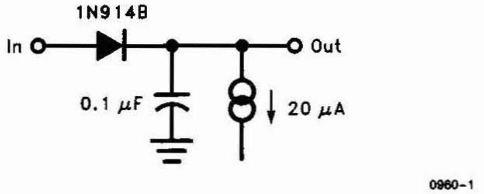

Figure 1. Simple Diode Peak Detector

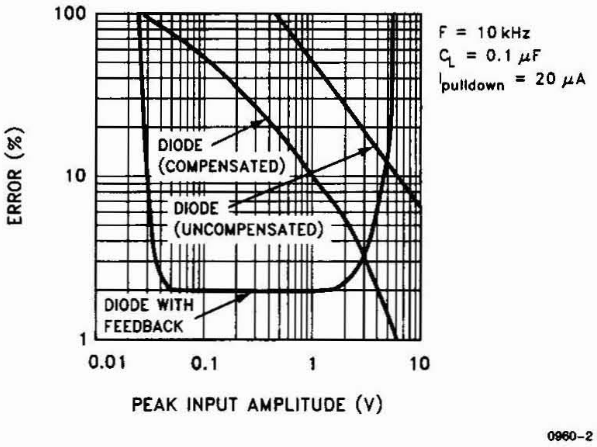

Figure 2. Error vs Amplitude

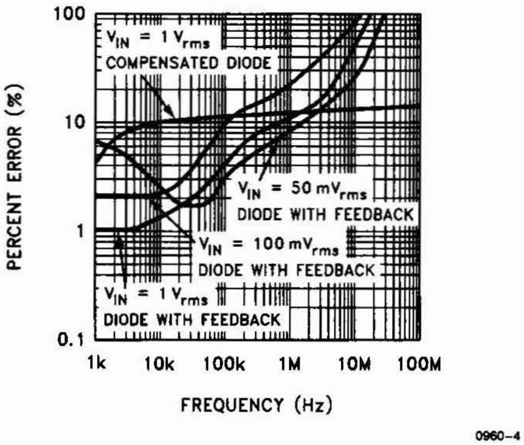

Figure 4. Error vs Frequency

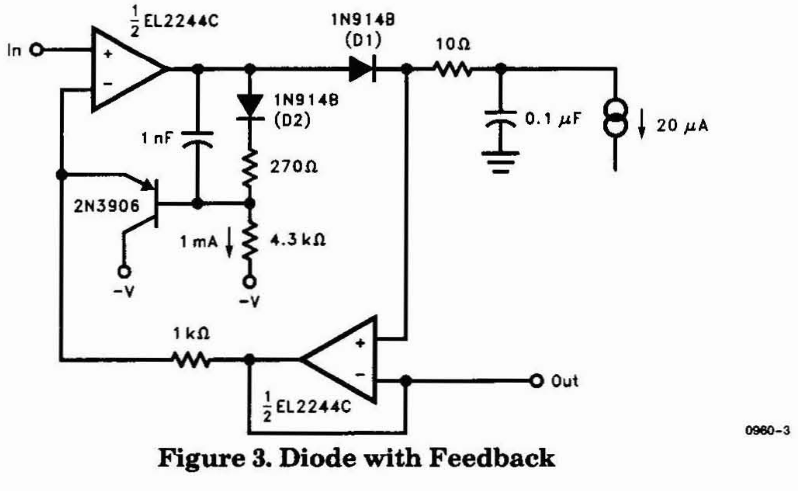

Figure 3. Diode with Feedback

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
Fine Harmonic Distortion
Measurements in the Megahertz Range

Fine Harmonic Distortion Measurements in the Megahertz Range

by Barry Harvey

Harmonic distortion measurements of amplifiers is easily accomplished using a commercial test set which includes a low-distortion oscillator. These units work only up to 100 kHz or less; at higher frequencies, a low-distortion oscillator and spectrum analyzer are employed. Unfortunately, commercial sinewave oscillators have no better than −56 dBc harmonic content (0.16%), and spectrum analyzers offer no better than −72 dBc (0.025%) internal distortion levels. This author had to test amplifier IC's to −80 dBc (0.01%) levels at 2 MHz, and couldn't buy general-purpose lab equipment to do the job at any price. This article shows the circuits made to do the job.

Referring to Figure 1, we will make a clean sinewave source to drive the Device Under Test (DUT). Its output will pass through a fundamental reject filter so that the harmonics may be amplified without overload from the high-amplitude fundamental. Having stripped most of the fundamental away, the reject filter's output may be viewed on a spectrum analyzer or passed on to individual harmonic measurement sections for fast automated testing.

The sinewave applied to the DUT must have less than −80 dBc distortion. This is pretty hard to accomplish, since we will generate it with active semiconductors whose distortion levels are too high. About the best unfiltered output distortion level we can obtain from transistor amplifiers is −60 dBc (ref. 1). We cannot use an active filter to clean up the harmonics further, because again no amplifiers can be used that will not add more distortion. A simple passive filter is used to bring distortion below −80 dBc.

Figure 2 shows the oscillator schematic. It produces 1 VMRS into a 500Ω load. Note that the simple passive network is not a fancy N-th-order filter of some precise characteristic; it is simply a series tuned circuit and a parallel trap at the output, both resonant at the oscillator frequency. The Q's of the circuits are intentionally low, around 10 with the 500Ω load, to make them non-critical with respect to tuning. Two ranks of tuned circuit give a harmonic rejection of roughly Q^2, more than enough to achieve the desired output distortion level. The loss of the filter does not effect the output level; it is actively stabilized, even if a 50Ω load is used.

The EL4451C in Figure 2 is a variable-gain amplifier. It has two inputs: REF, which has a low distortion gain of 1 to the output; and V_{IN}, which is a variable-gain input controlled by the Gain inputs. A crystal is connected from the output back to the REF input, loaded by 330Ω + 160Ω. The crystal has about 150Ω series impedance at resonance, so the voltage division through the crystal prevents sustained oscillation. The extra gain required for oscillation comes from the V_{IN} path, and if the Gain input level is sufficient the EL4451C will oscillate.

This oscillation will grow uncontrollably until clipping occurs, so an EL4450C is used as an amplitude stabilizer. The EL4450C is a four-quadrant multiplier, and its X- and Y-inputs are wired to the filtered oscillator output. In the EL4450C's multiplier is developed a level proportional to V_{OUT}^2, and this is compared to a reference level at the REF input. The FB terminal is connected to DC ground, but it also is connected to C3 to form a pseudo-integrator with the output amplifier. Thus, the output is approximately the integral of the RMS of the oscillator output level minus the DC reference. If the oscillator output is greater than the reference, the EL4450C output ramps positive and reduces the EL4451C gain via its Gain-terminal. If the oscillator output is less than the reference, the integrator output ramps negative and raises the EL4451C gain. Thus the EL4450C acts as a level detector and servo loop integrator. Amplitude modulation noise is extremely low with this servo.

The pseudo-integrator in the EL4450C output circuit includes a zero between C3 and its 10K resistor. This is cancelled with an additional pole from C4 and the parallel of its 20K resistors.

The crystal can be replaced by a series LC circuit. It is very difficult to make this circuit provide widely variable output frequency, but it can easily be switched with rotary switches and multiple crystals and output filters. Both input and output terminals of the filter must be switched. Other load impedances can be driven, but the output filter must be redesigned. Generally, at resonance $X_{L1} = X_{C1} = R_L * Q$ and $X_{L2} = X_{C2} = R_L/Q$.

Figure 3 shows the fundamental reject circuitry. Because in the author's test setup the DUT produces a 9 VRMS fundamental amplitude, the L3-C3-L4-C4 filter attenuates it immediately so that the first amplifier is not overloaded. The EL2074C is a very low distortion wideband amplifier, but we still have to control the levels. The amplifiers provide a total gain of 100 for the harmonics to the spectrum analyzer or harmonic select sections, and each stage includes a fundamental-reject filter.

The output of the first amplifier still has an attenuated fundamental level of around 900 mVRMS, so the second filter knocks the fundamental down further to around 9 mVRMS. The final output has a fundamental down by about 80 dB, and harmonics up by 40 dB, easily viewed on a spectrum analyzer. Calibration is simple: just provide an input at some frequency greater than the fundamental and find the gain with an oscilloscope, or better yet use a network analyzer to measure gain over frequency. Set amplitudes so that no more than 1 VRMS is outputted.

SW1 is used to select high or low gain for the harmonic select and measure sections, due to their restricted dynamic ranges. A switch can be used, but the author used a relay. To preserve distortion and noise quality, semiconductor analog switches or multiplexed-amplifiers should not be used.

The EL2120C amplifier buffers the final filter and provides a gain of +2 to compensate for the loss of the back-matched 50Ω load termination.

Figure 4 shows a harmonic select channel. The output from SW1 routes through the L9-C9-L10-C10 network which passes the desired harmonic frequency. The EL2074C amplifies this harmonic and drives another filter also tuned to the desired harmonic. This highly selected harmonic is passed a fast comparator and then to the EL4450C four-quadrant multiplier. The multiplier's input signals are the harmonic and a clipped version of the harmonic. This clipped signal is the same as the sign of the harmonic, so the multiplier output is the harmonic times its own sign, or the absolute value of the harmonic. A simple RC filter passes the DC component, which is a linear measure of the selected harmonic. The 180Ω–10 pF components provide a simple time delay equal to that of the comparator to balance the phase of the multiplier inputs, improving accuracy at higher frequencies.

The design of L's and C's in the harmonic select section is similar to that of the other sections, where at the harmonic frequency $X_{L9} = X_{C9} = X_{L11} = X_{C11} = 250\Omega * Q$ and $X_{L10} = X_{C10} = X_{L12} = X_{C12} = 250\Omega/Q$.

Unless 5% L's and C's are used and parasitic capacitances are kept to less than 2 pF, the networks will have to be tuned. The author used a network analyzer, measuring the output of an amplifier following a tuned circuit so as not to load and de-tune it. Either the inductor or the capacitor can be adjusted; if the capacitance value is less than 100 pF a variable trimmer can be used in parallel with a fixed capacitor, otherwise a slug-tuned variable inductor can be used. It seems archaic to have to adjust LC circuits in this era of IC's, but they do allow the lowest distortion measurements.

It is completely practical to use multiple-pole rotary switches to allow different operating frequencies, seven poles being adequate for the oscillator and fundamental reject section. A pole can be saved by wiring all crystals together at the EL4451C output. The filters should be kept as physically separate as possible.

This project provided a lab test device better than commercial units. It does require assembly and adjustment, but it produces solid results.

References.

1. Harvey, Barry, "Oscillators Blend Low Noise and Stable Amplitude", Microwaves and RF, Oct. 27, 1994, pp125–129.

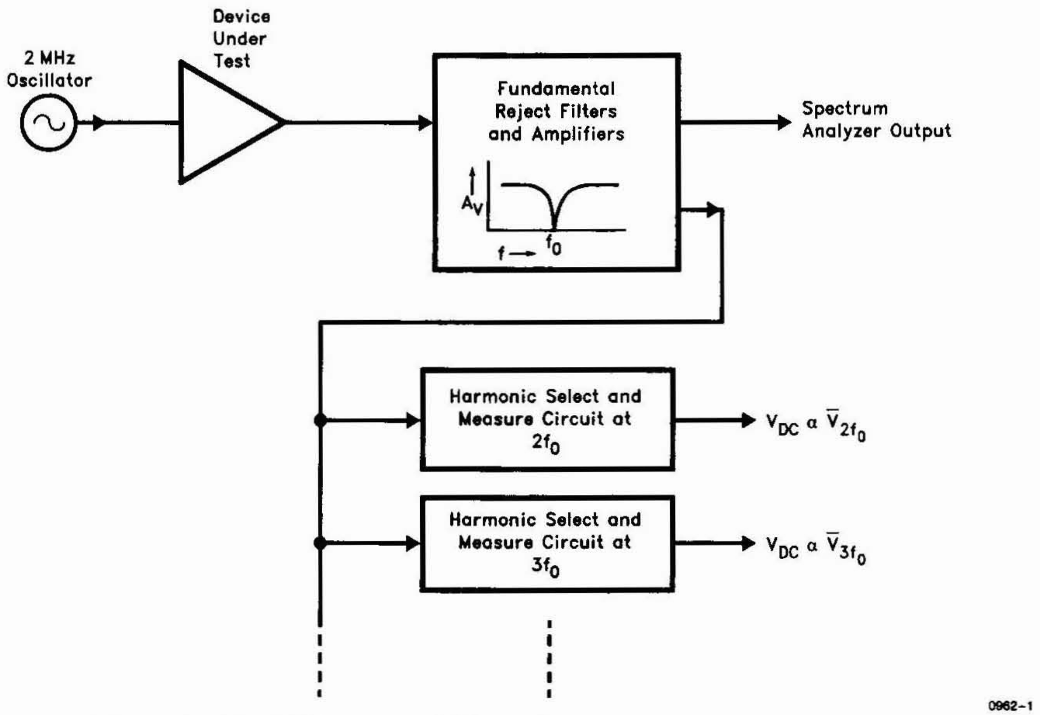

2 MHz
Oscillator
Device
Under
Test
Fundamental
Reject Filters
and Amplifiers
A_V
f →
f_0
Spectrum
Analyzer Output
Harmonic Select and
Measure Circuit at
$2f_0$
$V_{DC} \propto \overline{V}_{2f_0}$
Harmonic Select and
Measure Circuit at
$3f_0$
$V_{DC} \propto \overline{V}_{3f_0}$
0962-1

Figure 1. Block Diagram of Distortion Measurement System

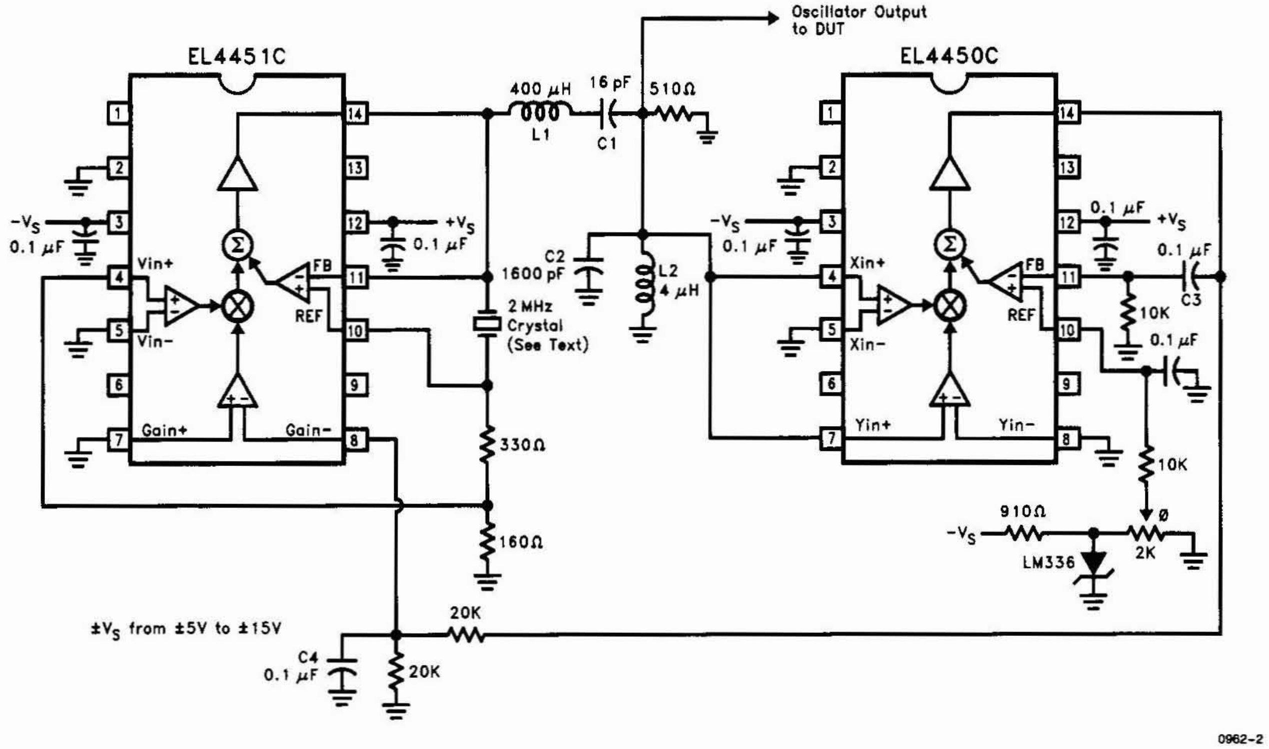

Oscillator Output to DUT
EL4451C
EL4450C
400 µH
L1
16 pF
C1
510Ω
$-V_S$
0.1 µF
$+V_S$
0.1 µF
Vin+
Vin−
FB
REF
Gain+
Gain−
C2
1600 pF
2 MHz Crystal (See Text)
L2
4 µH
330Ω
160Ω
±V_S from ±5V to ±15V
C4
0.1 µF
20K
20K
$-V_S$
0.1 µF
Xin+
Xin−
Yin+
Yin−
FB
REF
0.1 µF
$+V_S$
0.1 µF
C3
10K
0.1 µF
10K
Ø
910Ω
$-V_S$
LM336
2K
0962-2

Figure 2. Low-Distortion Oscillator

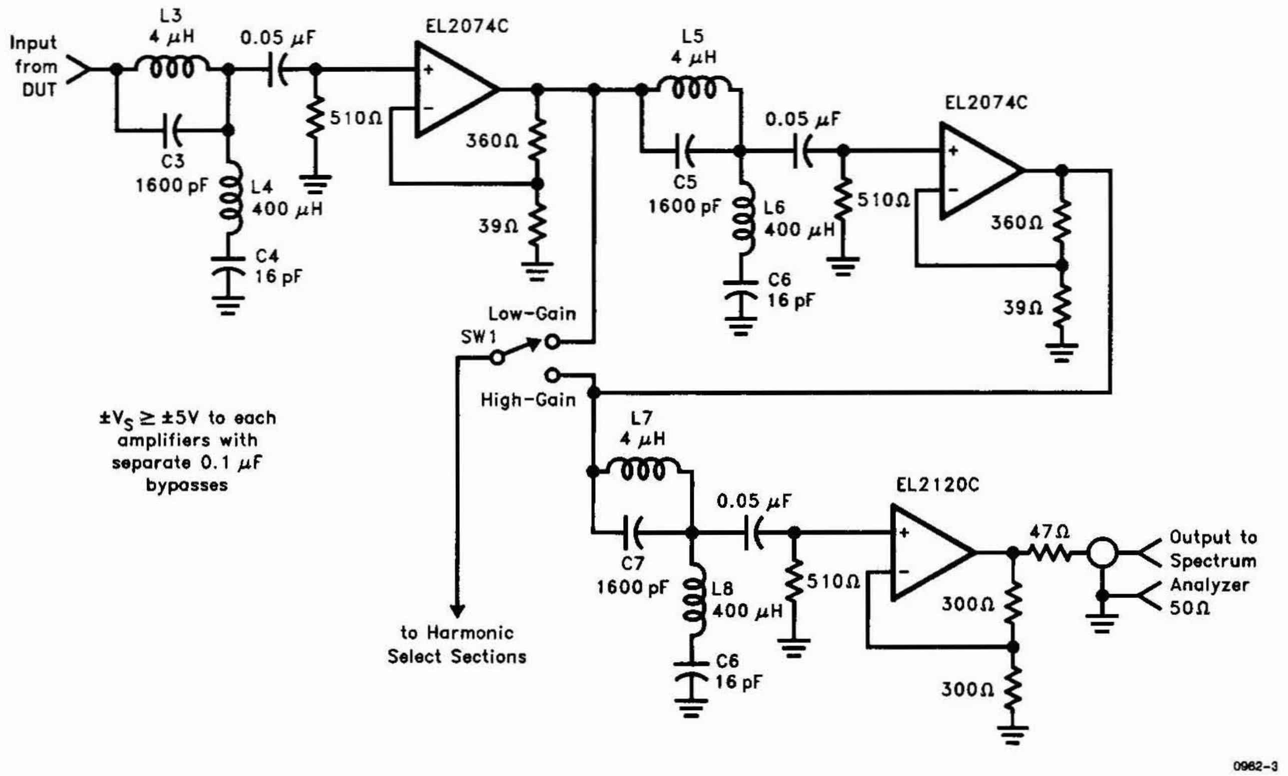

Input from DUT
L3
4 µH
C3
1600 pF
L4
400 µH
C4
16 pF
0.05 µF
510Ω
EL2074C
360Ω
39Ω
L5
4 µH
C5
1600 pF
L6
400 µH
C6
16 pF
0.05 µF
510Ω
EL2074C
360Ω
39Ω
Low-Gain
SW1
High-Gain
±V_S ≥ ±5V to each amplifiers with separate 0.1 µF bypasses
L7
4 µH
C7
1600 pF
L8
400 µH
C6
16 pF
0.05 µF
510Ω
EL2120C
47Ω
300Ω
300Ω
Output to Spectrum Analyzer 50Ω
to Harmonic Select Sections
0962-3

Figure 3. Fundamental Reject Filters and Amplifiers

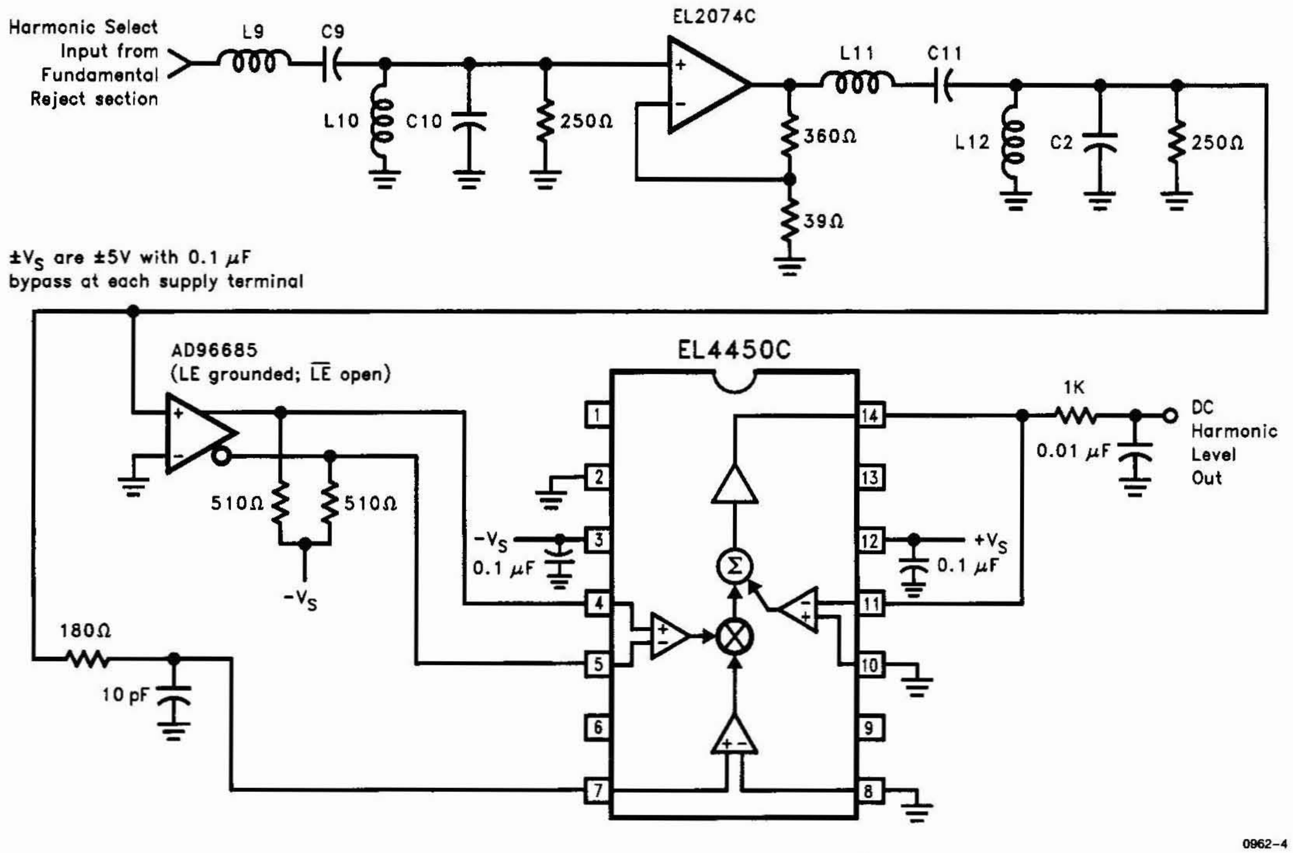

Harmonic Select Input from Fundamental Reject section
L9
C9
L10
C10
250Ω
EL2074C
+
−
L11
C11
360Ω
39Ω
L12
C2
250Ω
±V_S are ±5V with 0.1 μF bypass at each supply terminal
AD96685
(LE grounded; $\overline{LE}$ open)
+
−
510Ω
510Ω
$-V_S$
EL4450C
1
2
3
4
5
6
7
8
9
10
11
12
13
14
$-V_S$
0.1 μF
$+V_S$
0.1 μF
Σ
1K
0.01 μF
DC Harmonic Level Out
180Ω
10 pF
0962-4

Figure 4. Harmonic Select and Measure Section

A Simple Circuit Removes Sync

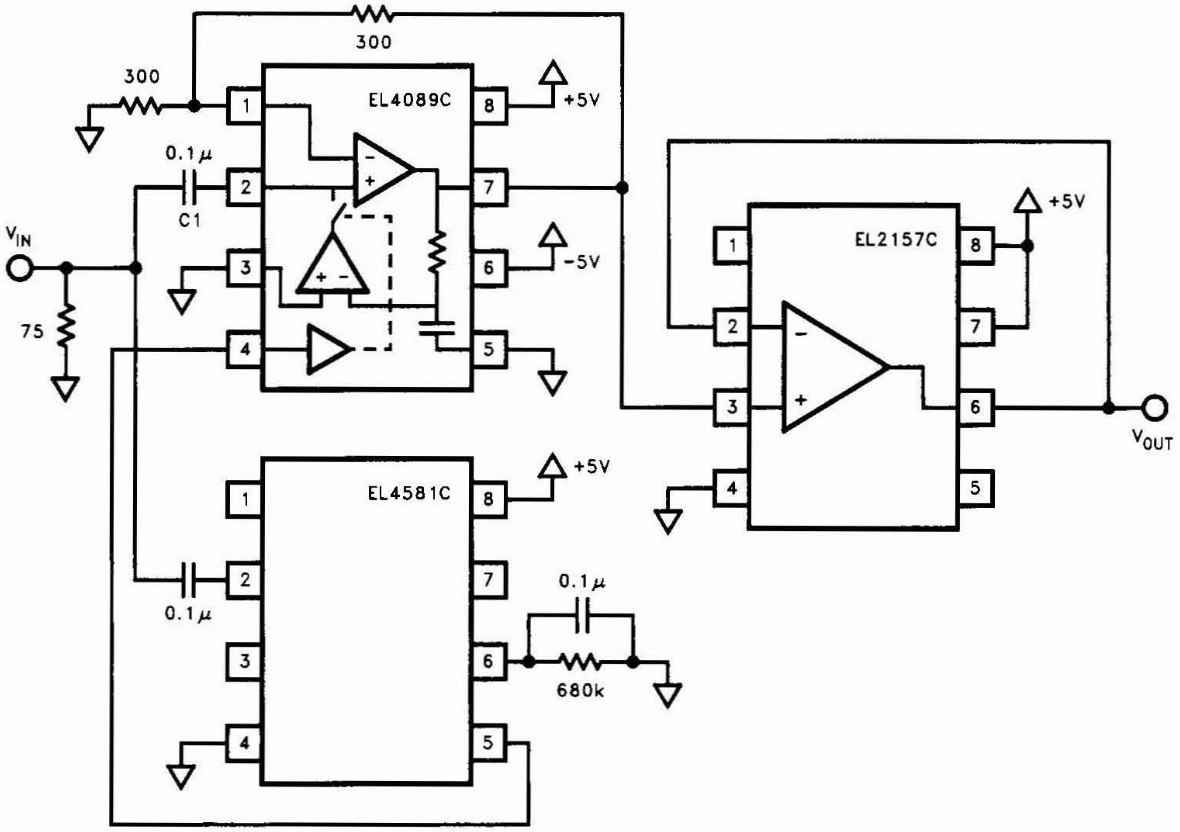
by Mike Wong

As the digital world encroaches into analog territory, signal conditioning circuits are required to prepare analog signals for digital processing. The standard composite video signal is an analog signal and generally AC coupled in video systems to prevent circulating DC currents. The following circuit demonstrates a method of conditioning a composite video signal for an analog to digital converter. The design example as depicted in Figure 1 consists of two main sections, a DC restore amplifier and a clamping amplifier. The DC restore amplifier clamps the back-porch of the video signal to a fixed reference and the clamping amplifier removes the sync portion of the video signal.

The video signal first goes into a sync separator, the EL4581C, and at the same time into a DC restore amplifier, the EL4089C. The EL4581C outputs a CMOS logic low signal into hold control input of the EL4089C during the back-porch section of the video signal. When the hold control input is low, the servo loop in the DC-restore amplifier forces its output to the reference level. A necessary offset voltage is placed across the sample and hold capacitor to create the proper input to output voltage shift. In the design example, C1, the AC coupling capacitor doubles as a sample and hold capacitor. Photo 1 shows the analog video input and the sync separator back-porch output waveforms. The back-porch output is used as the control signal for the sample and hold clamp signal. The combination of the EL4581C and EL4089C clamps the back-porch of the video signal to the ground level. Note that the sync tip of the video signal remains untouched.

All CMOS ADCs have a parasitic latch-up problem when subjected to negative input voltage levels. Since sync tip contains no useful video information and it is a negative going pulse, we can chop it off. The EL2157C stage limits the negative excursion to the ground level. The input and output range of the EL2157C is 0V to 3.5V. Its fast 7 ns of negative over-drive recovery makes it ideal for clamping applications. Photo 2 shows the incoming video signal whose back-porch is clamped to the ground level and the amplifier output signal with negative going portion of the sync tip chopped off.

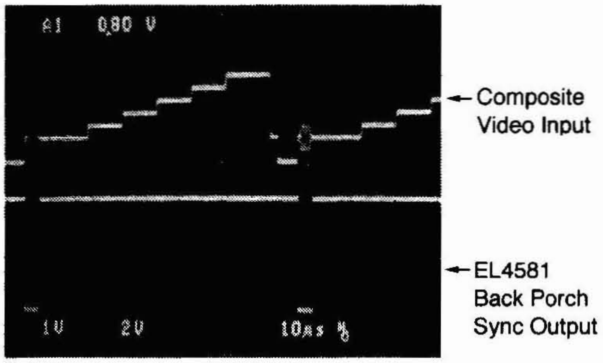
A Simple Circuit Removes Sync


300
300
EL4089C
1
2
3
4
8
7
6
5
+5V
-5V
0.1µ
C1
VIN
75
EL2157C
+5V
VOUT
EL4581C
+5V
0.1µ
0.1µ
680k

0961-1

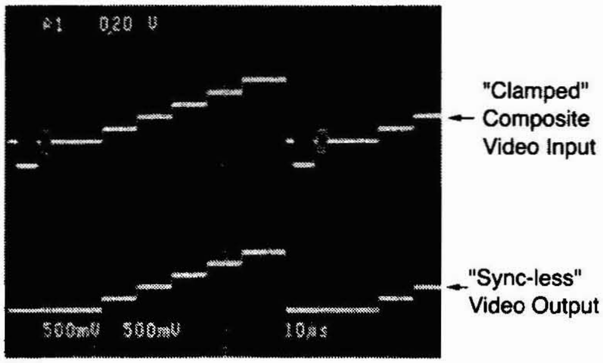
Figure 1. DC-Restore Sync Remover

Photo 1. DC Restore



0961-2

Photo 2. "Sync-Less" Video Signal



0961-3

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Simple CMOS Driver Circuits Generate Bipolar Outputs

Simple CMOS Driver Circuits Generate Bipolar Outputs

by Mike Wong

There are many applications such as IGBT, CCD, and transducer drivers where high peak current and bipolar output voltage swings are often required. This applications brief discusses two implementations of generating bipolar output using the EL7182 and EL7501 CMOS drivers.

Figure 1 shows the traditional scheme. The EL7182 is powered with a +5V and −7V supplies. The input comparator threshold is referenced to the ground pin which is connected to the negative supply so proper input voltage level shifting is necessary to operate the input comparator. The Zener diode in series from the TTL output to the input of the EL7182 provides the voltage level shift. Figure 2 depicts the inputs and the output waveforms. When TTL input is 0V, the voltage at the EL7182 input is shifted to −7V. When TTL input is 3V, the voltage at the EL7182 input is shifted to −4V which is 3V above the −7V on the ground pin. However, this implementation has a couple of drawbacks, in addition to the extra components required for input level shifting, the series Zener diode and resistor can also load down the TTL signal. When TTL input signal is high, bias current must flow across the Zener diode through the resistor to ground. This pulls the EL7182 input pin high with reference to the −7V supply.

Figure 2 uses the EL7501 to escape the input loading problem. The inputs of the EL7501 are differential where a 1V differential voltage across its input pins guarantees the output voltage to switch state. The input can be modeled as a series 180 kΩ resistor tied to a DC voltage 1V below the V_{DD} supply. The series 50 kΩ resistor puts a 1.1 voltage at pin 4, as a result, when the TTL input at pin 1 is switching between 0V to 3V, the current comparator internal to the EL7501 senses current changes through the input resistors and changes the state of its output FETs. The ground and input pins are isolated and their breakdown voltage is over 100V. There are a couple of drawbacks with this circuit solution, 1) the maximum frequency is limited to 2.5 MHz, 2) input to output delay is higher than the EL7182. Figure 4 shows the input and output waveforms.

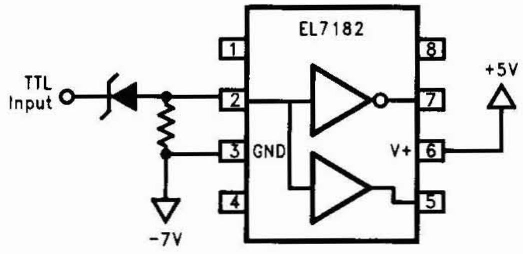


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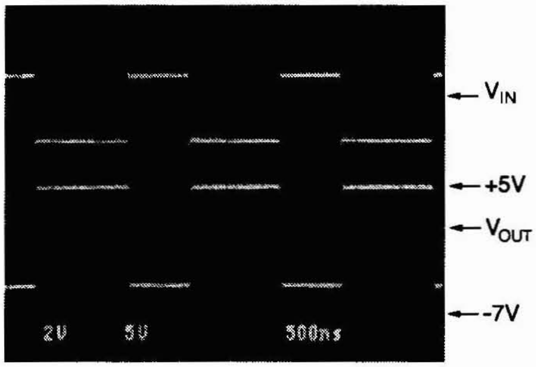
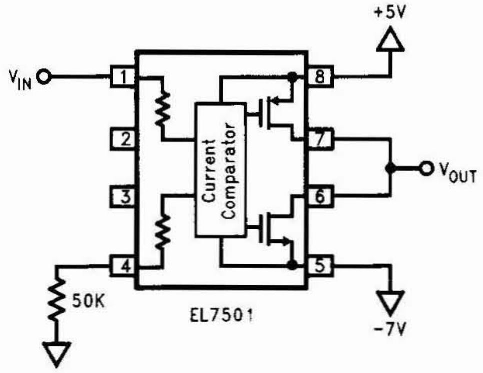
Figure 1



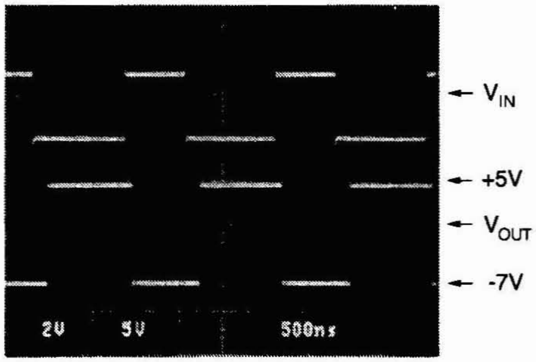
0963-2

Figure 2


+5V
V_{IN}
1
2
3
4
8
7
6
5
Current Comparator
V_{OUT}
50K
EL7501
-7V

0963-3

Figure 3



0963-4

Figure 4

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Designing a High Efficiency DC-DC Converter with the EL75XX

Application Note #18

8

Designing a High Efficiency DC-DC Converter with the EL75XX

by Mike Wong

Preface

Since the beginning of the digital revolution, the speed of a microprocessor has been governed by Moore's law postulated in 1968 by Intel's co-founder Gorden Moore. Moore suggested that the speed of a microprocessor would double in every 18 months. However, the principle of conservation of energy, more scientific in nature, will eventually dominate and limit the rate at which the speed of a microprocessor is increasing. The equation $P = CV^2F$, a derivative of the principle of conservation of energy, dictates that the power dissipated in a device is linearly proportional to its clock frequency and distributed capacitance. Microprocessor manufacturers have made great advances in reducing the amount of power dissipation in the device. The popular Pentium microprocessor, for example, employs a combination of heat-sink/fan to extract heat from the package. To further combat the power dissipation problem, a new generation of low voltage CMOS fabrication processes have been developed. The low voltage processes have a smaller transistor geometry that results in lower parasitic capacitance, reducing C in the above equation. Smaller transistor size also allows for a increase in the number of transistors in a given die area, and as a result, the lifetime of Moore's law is extended. However, technical problems are being passed onto the shoulders of power supply designers. Lower microprocessor supply voltages and higher supply currents mean that the linear DC-DC regulator is no longer a viable solution. Power supply designers are forced into using switching regulator techniques. Lower output voltage, higher output current, and smaller output voltage ripple requirements have greatly increased the difficulty of the power supply design. To further burden the problem, power saving "stop-clock" modes have demanded faster and more stable transient response from the DC-DC converter.

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Slope Compensation
PWM Comparator
Output Inductor
Output Capacitor and Load Transient Analysis
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Input Current Transient Analysis
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Efficiency Calculations
Heat Sinking Requirements
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Charge Pump Design
Remote Sense
Bill of Materials

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B. Core and Inductor Manufacturers
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D. Heat Sink Manufacturers

Designing a High Efficiency DC-DC Converter with the EL75XX

Introduction

The purpose of this Application Note is to demonstrate the operation of the EL7560 in an 12.4A output current mode DC-DC converter module for powering Intel's latest microprocessor, the Pentium-Pro. The EL7560 is the world's simplest, most integrated, and most cost effective switcher. It incorporates the PWM functions, current sense resistor, high current synchronous FETs, precision DAC for output voltage programming, and over-voltage and over current protection features. In addition, the advanced control loop design controls the load regulation of the DC-DC converter to meet the P6 DC-DC converter output load transient specification with low cost and readily available Aluminum Electrolytic capacitors.

Lower output current versions of the device are also available. The EL7560 requires an external reference. This gives the application more flexibility and accuracy. A precision ±½% reference is incorporated in the EL7561 to reduce component count. The EL7556 is the 6A output current version. The power supply design considerations presented in this Application Note are applicable to all devices in the EL75XX family.

In the component selection sections, all calculations are based on the worst case specification limits in the Intel P6 DC-DC Converter Design Specifications.

EL7560 Theory of Operations

The EL7560 is a current mode switcher which means that the power switch duty cycle is determined by comparing the output inductor current and the error amplifier output voltage. Current mode control offers a number of advantages over the traditional voltage mode control. First, because the inductor current ramp is proportional to the input voltage level the converter can respond quickly to line variations. Second, it greatly simplifies the over-all loop design. The pole introduced by the output inductor is taken out of the loop and replaced by a high output impedance current source which is regulated by an inner current control loop. Lastly, it allows automatic pulse by pulse current limiting which protects the power switches when the output is overloaded or shorted.

The negative input of the error amplifier is brought out to sense the output voltage. The output of the error amplifier is compared with the current ramp from the current sense amplifier. (The current ramp is modified by slope compensation circuitry in order to prevent noise and oscillation problems.) The output of the comparator then resets a flip-flop which terminates the "on" time of an internal power NMOS FET. The error amplifier reference voltage is programmed by a 4-bit DAC with 100 mV resolution.

The EL7560 also includes a number of house keeping functions. In the case of overheating, the power switches can be shut off by properly configuring Otbar, pin 13/OT. When the output voltage is within regulation, the power good signal pin will go high. The device can be disabled by pulling output enable (pin 14) low, putting the device in a lower power state. During start-up, the switching duty cycle is limited by the internal soft-start circuit to generate a smooth power converter output response.

The oscillator frequency can be easily set by an external capacitor. The oscillator is designed to operate up to 1 MHz switching frequency. External adjustable slope compensation is provided to obtain the best system performance.

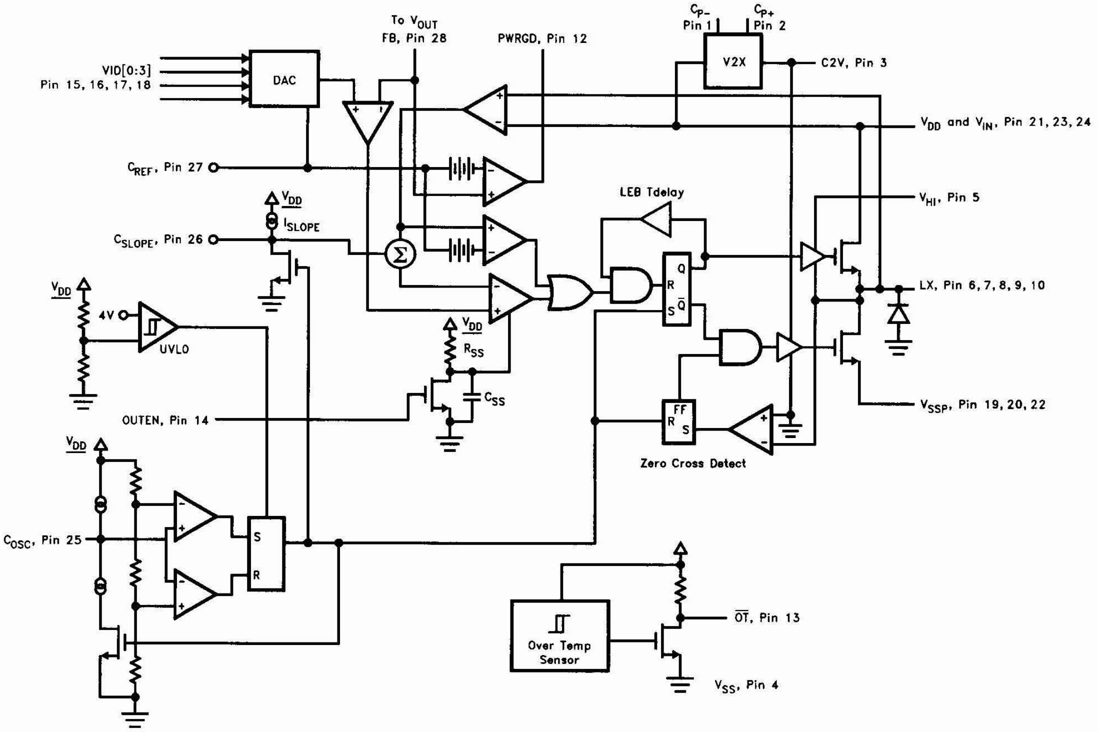

To V_{OUT} FB, Pin 28
PWRGD, Pin 12
C_{P-} Pin 1
C_{P+} Pin 2
V2X
C2V, Pin 3
VID[0:3] Pin 15, 16, 17, 18
DAC
V_{DD} and V_{IN}, Pin 21, 23, 24
C_{REF}, Pin 27
V_{DD}
I_{SLOPE}
C_{SLOPE}, Pin 26
Σ
LEB Tdelay
V_{HI}, Pin 5
Q
R
S
$\overline{Q}$
LX, Pin 6, 7, 8, 9, 10
V_{DD}
4V
UVLO
V_{DD}
R_{SS}
C_{SS}
OUTEN, Pin 14
FF
R
S
Zero Cross Detect
V_{SSP}, Pin 19, 20, 22
V_{DD}
C_{OSC}, Pin 25
S
R
Over Temp Sensor
$\overline{OT}$, Pin 13
V_{SS}, Pin 4
0965-1

Figure 1. EL7560 Functional Block Diagram

Pin Descriptions

Pin #	Description
1, C−	Negative terminal for the charge pump bootstrap capacitor. This pin oscillates from V_{DD} to V_{SS} at one half the clock frequency.
2, C+	Positive input for the charge pump bootstrap capacitor. This pin oscillates from V_{DD} to twice V_{DD} at one half the clock frequency.
3, C2V	Voltage doubler input. A 100Ω resistor is used to limit current into this pin. A 1 μF capacitor is also needed to sustain the voltage doubler output. The 1 μF capacitor should be returned to the power ground node. The voltage on this pin will be 8V–10V depending on the load.
4, V_{SS}	This pin is the ground input for the control circuitry. It must be separated from the high current power ground. This pin should be connected directly to the ground point of the output capacitors.
5, V_{HI}	This pin is the positive supply for the high side driver. It is bootstrapped from the LX pin with a 0.1 μF capacitor.
6, 7, 8, 9, and 10, LX	This is the halfway point between the two large internal FETs. It drives the inductor of the buck regulator circuit. High switching current is seen at this pin.
11, TEST	This pin is used to test the internal power FETs during the final test at the factory. It must be connected to any convenient ground in the application.
12, PWRGD	This pin outputs a high signal (Logical "1") to signify power good when the FB pin is within 7% of its programmed value.
13, OTbar	This pin pulls low (Logic "0") when the die temperature exceeds 135°C. It is normally a high impedance output. It has 15°C of hysteresis. To turn off the FETs in the event of an over-temperature condition, simply connect this pin to the OUTEN pin and a 10 kΩ resistor to V_{DD}.
14, OUTEN	A high input signal applied to this pin enables the switching regulator. The reference, oscillator, and voltage doubler operate whenever the power supply is above its UVLO threshold regardless of the state of this pin.
15, 16, 17, and 18 $V_{ID3, 2, 1, \text{and } 0}$	These are the DAC input pins used to program the output voltage.
19, 20, and 22, V_{SSP}	These pins are the ground returns to the buck regulator. They are internally connected to the source of the low side synchronous NMOS FET.
21 and 23, V_{IN}	These pins are the positive power supply input to the buck regulator. They are internally connected to the drain of the high side synchronous NMOS FET.
24, V_{DD}	This pin supplies power to the internal control circuitry. It typically draws 30 mA when operating.
25, C_{OSC}	A capacitor connected from this pin to ground sets the frequency of the PWM oscillator. The oscillator frequency is approximately $F_{OSC} = 0.001/C_{OSC}$. The maximum duty cycle is fixed at 96%.
26, C_{SLOPE}	A capacitor connected from this pin to ground sets the amount of slope compensation. A 30 μA current flows out of this pin. The voltage at this pin is reset to the reference voltage whenever the high side NMOS FET is off.
27, C_{REF}	This is the external reference input pin. A minimum of 1.0 μF to ground is recommended.
28, FB	This is the voltage feedback input pin for the buck regulator. It is internally connected to a resistor divider.

P6 DC-DC Converter Schematic

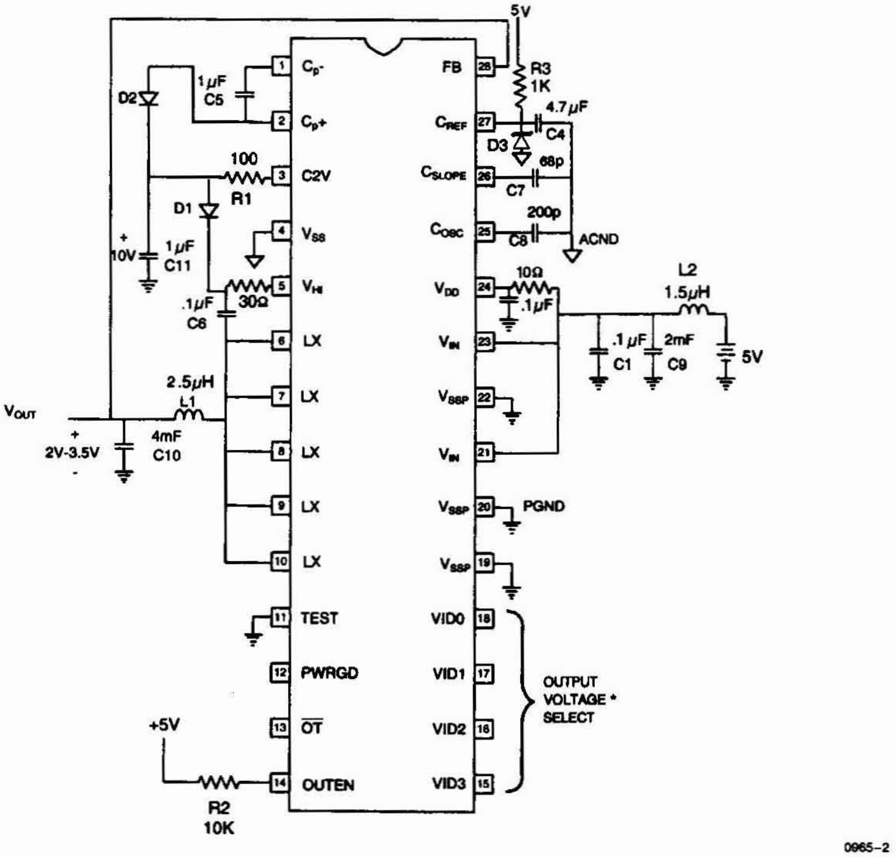

5V
Cp-
Cp+
C2V
VSS
VHI
LX
TEST
PWRGD
OT
OUTEN
FB
CREF
CSLOPE
COSC
VDD
VIN
VSSP
VID0
VID1
VID2
VID3
R3
1K
4.7μF
C4
D3
68p
C7
200p
C8
ACND
10Ω
.1μF
L2
1.5μH
.1μF
C1
2mF
C9
5V
PGND
OUTPUT
VOLTAGE *
SELECT
1μF
C5
D2
100
R1
D1
10V
1μF
C11
.1μF
C6
30Ω
2.5μH
L1
VOUT
2V-3.5V
4mF
C10
+5V
R2
10K
0965-2

Figure 2. P6 DC-DC Converter Circuit

Designing a High Efficiency DC-DC Converter with the EL75XX

Basic Buck Regulator Topology

Figure 3 shows the basic buck regulator topology. When Q1 turns on the voltage across L1 is $V_{IN} - V_{OUT}$ and current flows from V_{IN} to V_{OUT}. When Q1 turns off, the inductor current continues to flow, and as a result the cathode of D1 gets pulled below ground by the back EMF of the output inductor, L1, and starts to conduct. The voltage across L1 is $-V_{OUT}$ and output current flows through D1 and L1 to V_{OUT}. Under steady-state conditions, the voltage across L1 must average to zero. If T1 is the time Q1 is closed, and T2 is the time Q1 is open, then the relationship between V_{IN} and V_{OUT} is:

$$(V_{IN} - V_{OUT})T1 - (0 - V_{OUT})T2 = 0 \qquad (1)$$

Equation (1) can be simplified to

$$V_{OUT} = V_{IN} \bullet D \qquad (2)$$

Where D is the duty cycle, $D = T1/(T1 + T2)$

Equation (2) tells us a great deal about switching mode converters. First, it suggests that the output voltage is solely a function of V_{IN} and the duty cycle of the switch. Secondly, it is not a function of the output inductor, capacitor or switching frequency. Lastly, it is not a function of the magnitude of the output load current.

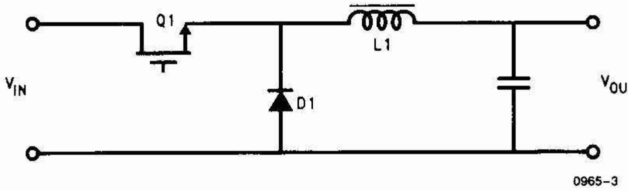


Figure 3. Basic Buck Converter Topology

Synchronized Rectification

The diode in Figure 3 may be replaced by a switch to further improve efficiency. As an example, if I_{OUT} is 12.4A and the forward bias voltage of the diode is 0.6V, and the duty cycle is 60%, the total power dissipation of the diode is 0.6V • 12.4A •(1 − 0.6) = 2.97W. This represents 8% of the efficiency loss in a 3V output converter. If the diode is replaced with a low "on" resistance power FET(Q2) as depicted in Figure 4, the power loss is determined by the "on" resistance of Q2. The "on" resistance of the power FETs in the EL7560 is typically 20 mΩ, at 12.4A and 60% duty cycle the power loss is 12.4A • 12.4A • 20 mΩ • (1 −0.6) = 1.23W which is a 1.69W efficiency improvement over the diode configuration. A Schottky doide, D3 in the PC DC-DC coverter schematic, in parallel with drain-source terminals of Q2 is often required to provide the inductor current path during the transient when both Q1 and Q2 are turned off. With this Schottky diode, the body diode of Q2 will never forward bias, thereby improving the reliability of the converter.

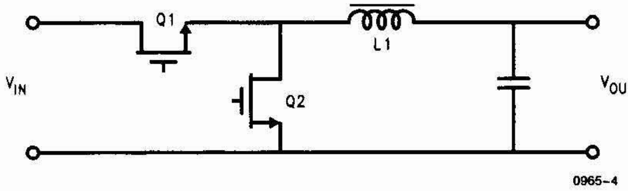


Figure 4. Buck Converter with Synchronized Switches

Continuous Mode Operation

The preceding discussion describes the situation where the inductor current never reaches zero. This form of operation is called "continuous" mode. Figure 5 depicts Q1 and Q2 gate drive waveforms, Q1 drain and Q2 source current waveforms, and the output inductor currents.

During T1, Q1 is turned "on" and Q2 is turned "off", inductor current IL1 and $I_{SOURCE1}$ increase from the initial value which is not zero. The slope of the current ramp is dictated by

$$\frac{\Delta ID\,(Q1)}{\Delta T} = \frac{V_{IN} - V_{OUT}}{L1} \qquad (3)$$

In this cycle, energy is stored in the inductor for use during the off cycle and current flows from input to the output.

During T2, Q1 is turned "off" and Q2 is turned "on", inductor current IL1 continues to flow to the output via Q2. Inductor current declines to the initial value and gives up energy to the output.

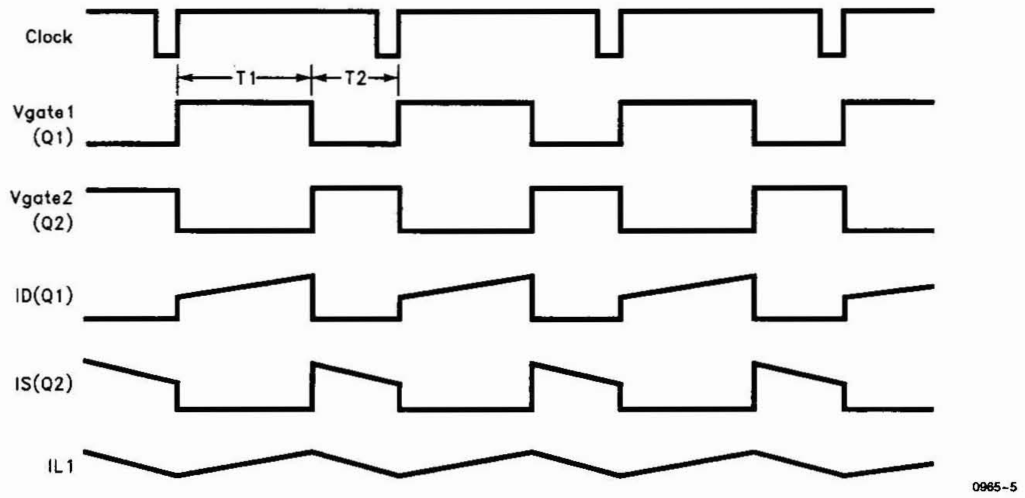


Figure 5. Gate Drive and Current Waveforms under Continuous Mode

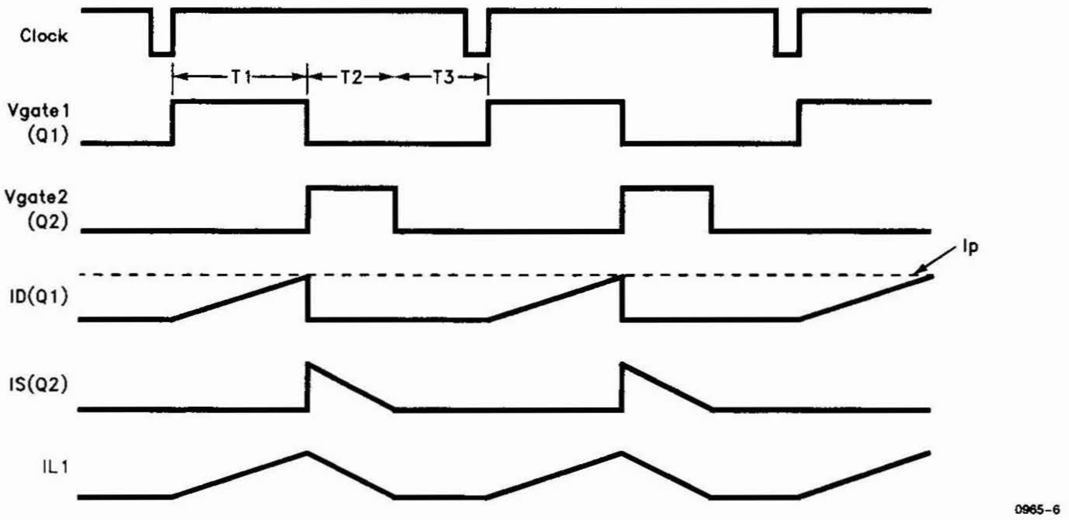


Figure 6. Gate Drive and Current Waveforms under Discontinuous Mode

Discontinuous Mode Operation

Normally, a converter designed for the continuous mode operation stays in continuous current mode under all load conditions. However, the converter can go into discontinuous current mode momentarily when the output load is changed from its maximum to minimum level. The mode of operation where the inductor current falls to zero is called discontinuous operation. The waveforms in Figure 6 are synchronized gate drive waveforms, power FET source current and output inductor current waveforms. During T1, Q1 turns "on" and Q2 turns "off", the inductor current starts from zero and rises to the peak value I_P. Energy, $P = LI^2/2$, is stored in the inductor. During T2, Q1 turns "off" and Q2 turns "on", inductor voltage reverses and its stored energy is delivered to the output. The inductor current decreases linearly to zero. When the inductor current reaches zero, Q2 must turn "off" to prevent inductor current flow from the storage capacitor to ground. Thus, during T3, both Q1 and Q2 are turned "off".

Current Mode Control

The advantages of current mode control were discussed in an earlier section. It basic block diagram is shown in Figure 7. The duty cycles of the power FETs are generated by comparing the error amplifier output voltage with a sawtooth ramp. This sawtooth ramp is provided directly from the power switching circuit inductor current waveform through a current sense resistor, R_{SENSE}. The fact that the slope of the current ramp is a function of V_{IN}, V_{OUT}, and the output choke inductance, $V_{IN} - V_{OUT} = L\ \Delta I/\Delta T$, suggests an inherent voltage feed forward characteristic with instantaneous open loop response to any input voltage changes. The output inductor pole is included in the current loop, and as a result, it is eliminated from the outside voltage loop. This reduces the output filter from a two pole network to a simple single pole. The outer loop is a voltage loop where the output voltage, V_{OUT}, is compared with a reference voltage, V_{REF}, and produces an error voltage output for the PWM comparator. An interesting aspect of the current mode control scheme is that the error amplifier output voltage programs the inductor current which causes the output voltage to rise or fall and the error amplifier output voltage is derived from comparing V_{OUT} with V_{REF}. The result is that the PWM duty cycle maintains the inductor current such that V_{OUT} is equal to V_{REF}.

Slope Compensation

While current mode control has a number of desirable characteristics, it also carries a flaw which, if not treated properly, can cause severe output oscillation. As described in the previous sections, current mode control regulates the peak inductor current via the inner current loop. However, in a buck converter, the output current is the average inductor current. Figure 8 graphically represents the output inductor current using two different input voltages. When in regulation, the error amplifier output voltage, V_E, should not change. A constant V_E (V_E sets the peak output inductor current level) implies that the average output current for the higher input voltage level (duty cycle = D1) is slightly higher than the output current associated with the lower

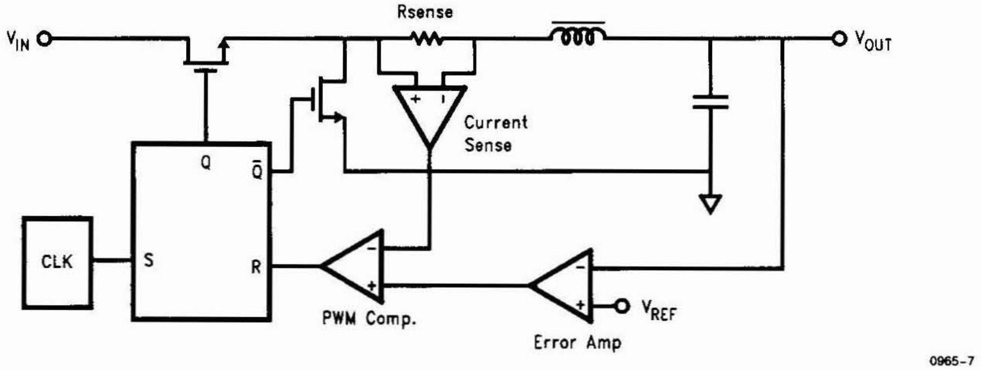


Figure 7. Current Mode Control

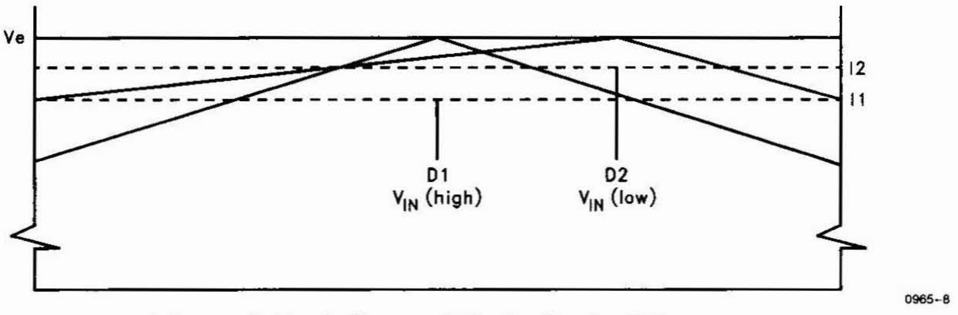


Figure 8. Peak Current Mode Control Error

input voltage (duty cycle = D2). This will result in a higher output voltage which the voltage loop will correct by changing V_E, which in turn will result in a different duty cycle, which results in different average current levels. This effect has been dubbed sub-harmonic oscillation and can be evidenced by output voltage oscillation at one half the switching frequency.

One method of maintaining constant output current is to add a voltage ramp on the current sense output as depicted in Figure 9. This has the effect of lowering the error amplifier voltage as a function of T_{ON}.

Slope compensation also improves noise immunity. Figure 10 demonstrates how a small perturbation in the inductor current can result in an unstable condition. For a duty cycle less than 50%, the perturbation is suppressed quickly each cycle (dI'1 ≪ dI1). For greater than 50% duty cycle, a small perturbation is amplified (dI'2 ≫ dI2) each cycle and causes an unstable condition.

Figure 11 shows the inductor current perturbation problem being corrected with slope compensation. With slope compensation, inductor current perturbation is attenuated each cycle at all times even when the duty cycle is greater than 50%.

In the EL7560, a slope compensation ramp is created with a 30 µA current source charging an external capacitor, C_{SLOPE}. The voltage on C_{SLOPE} is reset to the reference voltage whenever the internal high side NMOS FET is off.

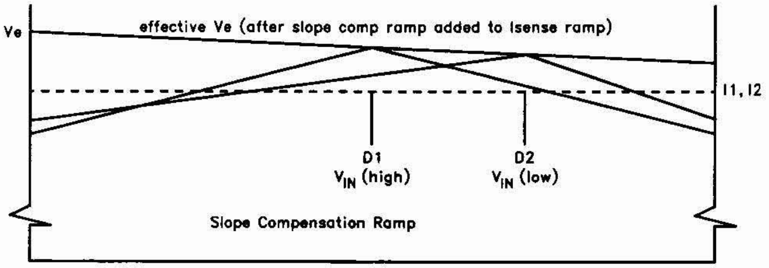

Ve
effective Ve (after slope comp ramp added to Isense ramp)
I1, I2
D1
V_{IN} (high)
D2
V_{IN} (low)
Slope Compensation Ramp
0965-9

Figure 9. Constant Average Output Current

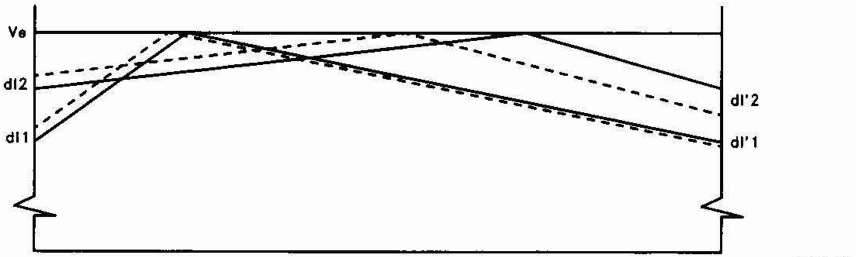

Ve
dI2
dI1
dI'2
dI'1
0965-10

Figure 10. Inductor Current Error

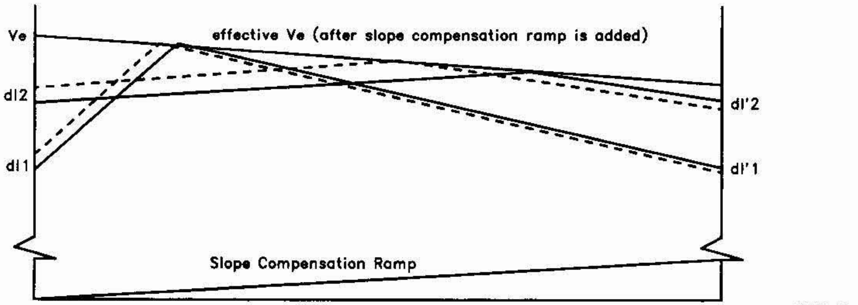
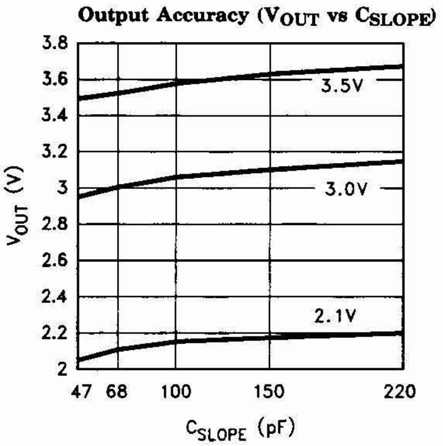

Ve
effective Ve (after slope compensation ramp is added)
dI2
dI1
dI'2
dI'1
Slope Compensation Ramp
0965-11

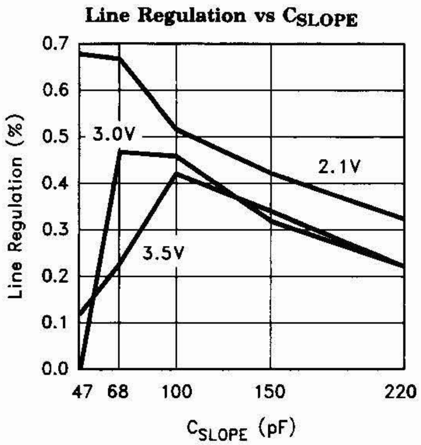
Figure 11. Inductor Current Ramps with Slope Compensation

Note 1: Figure 12 shows the experimental test results of the effects of the amount of slope compensation on the output voltage accuracy, output load regulation, and line regulation. The fact that slope compensation limits the duty cycle becomes apparent in Figure 12a. A C_{SLOPE} is decreased, the slope of the current ramp increases as a result the duty cycle is decreased and thus the decrease in output voltage.



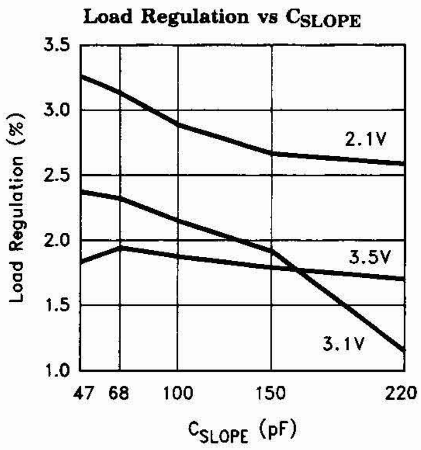
0965-25

Figure 12a



0965-26

Figure 12b



0965-27

Figure 12c

PWM Comparator

In the heart of the EL7560 PWM section is a direct summing comparator. The regulator output is first compared with a reference (DEC output) voltage. The resultant error voltage is then compared with current sense signal and slope compensation ramp. PWM duty cycle is then adjusted according to the summing comparator output. The direct-summing scheme enables cycle by cycle control of the output voltage. This scheme also eliminates the traditional feedback compensation integrator. The dominant pole is set by the output capacitor and the equivalent output resistive loading.

Output Inductor, L1

The output inductor serves two purposes, it stores energy and filters output ripple current. Trade-offs often have to be made between the physical size of the inductor and the maximum energy storage. The primary criterion for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode operation under all line and load conditions. To maintain the conditions of continuous mode operation under the minimum load and maximum line condition (duty cycle is at its minimum) at 500 KHz switching frequency, the minimum inductance can be calculated with the following equation:

$V = L \bullet \Delta I/\Delta T$

where

V is the voltage across the inductor,
$V = 5.25-3.07 = 2.13V$
(The Worst case P6 DC-DC converter specifications are used in all calculations.)
L is the inductance required to maintain continuous mode operation
ΔI is the peak ripple current,
$\Delta I = 2 \bullet I_{OUT(min)} = 0.6A$
ΔT is the duration at which the current is ramping up in the inductor, or the "on" time of the PWM,
$\Delta T = (3.07/5.25)/500\ KHz = 1.17e\text{-}6$

$L = V \bullet \Delta T/\Delta I = 2.13 \bullet 1.17e\text{-}6/0.6 = 4.15\ \mu H$

One inductor which meets this criterion is the Pulse Engineering PE-53681. Its inductance is 4.2 μH at minimum output current. The saturation effect of the magnetic core causes the inductance to decrease. At the maximum output current of 11.4A, the inductance of the PE-53681 decreases to 2.5 μH. As a result the ripple current will increase at high output current,

$\Delta I = V \bullet \Delta T/L = 2.13 \bullet 1.17e\text{-}6/2.5e\text{-}6 = 1A.$

When selecting the output filter capacitor, the worst case 1A ripple current must be used when calculating the output ripple voltage.

There are two important criteria in selecting an output inductor:

1. The minimum inductance at zero DC current must be greater than the inductance required to maintain continuous mode operation.
2. The core size and wire gauge must be sufficient to handle the maximum output DC current.

Output Capacitor, C10

The output capacitor filters the output inductor ripple current; thus, it must be low ESR type electrolytic capacitor. One must carefully decide between cost, size, and quality (ESR) of different types of capacitors. Names of capacitor manufacturers are listed at the end of this Application Note. The calculations shown below are done with the low cost United Chemi-Con LXF series Aluminum Electrolytic capacitors. The module layout available in the appendices of this document can accommodate both the high quality OS-Con capacitors or the inexpensive United Chem-Con capacitors.

As stated previously, the output capacitors must be low ESR type for two reasons: 1) to ensure lower ripple voltage 2) to meet the load transient specifications.

Designing a High Efficiency DC-DC Converter with the EL75XX

1. The Intel P6 DC-DC converter specification calls out for a maximum of ±1% output voltage ripple. For a 3V output that corresponds to 60 mV peak to peak. The previous inductor calculation section shows the ripple current to be 1A at the maximum load, thus, the maximum ESR allowed is 60 mΩ. For this example we have chosen 6 pieces of 680 μF United Chemi-Con series LXF aluminum electrolytic capacitors (part # LXF16VB681M10X12FT). The total capacitance is 4 mF and their combined ESR is 10.33 mΩ. The resultant peak to peak ripple voltage under full load condition is 10.33 mV.
2. When the output is stepped from minimum to the maximum level, the full output current load step will initially be supplied from the output capacitor C_O (I_C), as shown below,

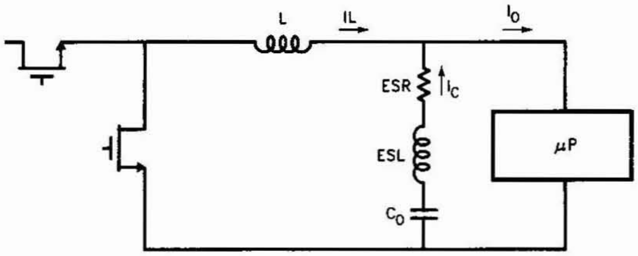


Figure 13. Output Current Path during Transient

The initial voltage droop will be:

$$\Delta V_{OUT} = ESR \bullet I_{TRANSIENT} + ESL \frac{\Delta I}{\Delta T} \quad (4)$$

Cylindrical aluminum electrolytic capacitor typically has 5 nH of ESL. The combined effective equivalent series inductance is ⅚ nH. The change in output voltage due to ESR and ESL during the initial output current transient is

$$\Delta V_{OUT} = 10.33\ m\Omega \bullet (12.4-0.3) + \tfrac{5}{6}\ nH \bullet 30A/\mu s = 153\ mV$$

Immediately after load transient, C_O will continue to supply current to the output load until the inductor current ramps to the maximum 12.4A output current level. The internal FET will be switching at 96% duty cycle until the output voltage gets back to within regulation. The amount of time for the inductor to ramp up to 12.4A is,

$$\Delta T = \frac{L \bullet \Delta I}{V_{IN} - V_{OUT}} = \frac{2.5\ \mu H \bullet 12.1A}{2.1} = 14.4\ \mu s$$

Taking the 96% duty cycle into account:

$$\Delta T = 14.4\ \mu s/0.96 = 15\ \mu s$$

In 15 μs the output voltage drops to:

$$dV = [1/C_o \bullet \int_0^{15\ \mu s} (12.4A - 0.3A - \frac{dI}{dt} t)dt] + (12.4A - 0.3A) \bullet ESR$$

$$dI/dt = (V_{IN}-V_{OUT})/L = (5-2.9)/2.5\ \mu H = 0.84A/\mu s$$

Plugging in the numbers to equation (4) yields:

$$dV = 146.7\ mV$$

The output drop caused by the output capacitor discharging is less than voltage drop due to ESR and ESL of the output capacitor.

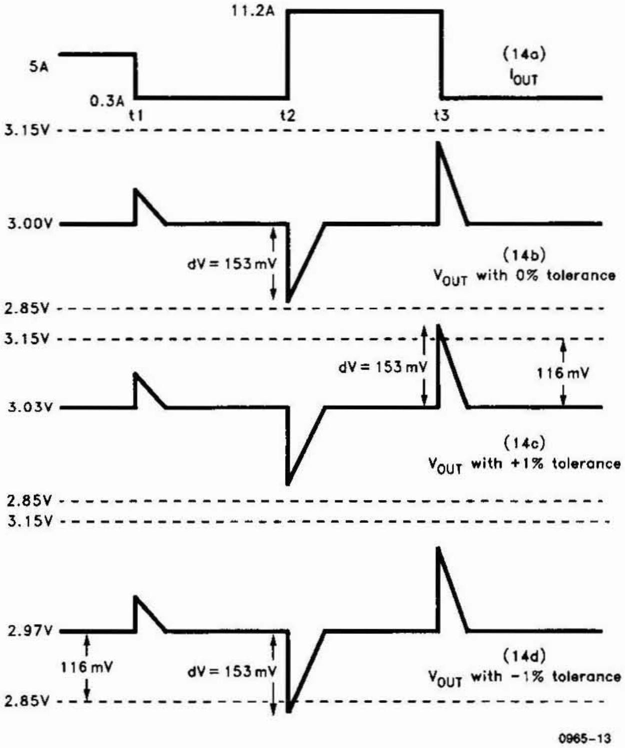


Figure 14. Output Voltage Variation with Traditional Control Scheme

The total ΔV_{OUT} transient allowed by the Intel spec is ±5%. If we subtract 1% for the tolerance of the EL7560 reference we end up with only 4% of the 2.9V which is 116 mV which is less than the 153 mV that we calculated. However, the unique loop compensation of the EL7560 degrades the load regulation by ±2% so that at maximum load the output voltage is 2% lower than nominal and at minimum load the output voltage is 2% higher than nominal. The result is 58 mV of additional output voltage head room to move around during load transient.

The timing diagrams in Figure 14 show how the output voltage changes in a converter with the traditional control scheme. The converter output current, waveform 14a, is changed from the nominal level (5A) to the minimum (0.3A) then to the maximum (12.4A) then back to 0.3A again.

Figure 14b depicts the output voltage response for a control IC with infinite open loop gain and the error amplifier reference voltage is exactly at 3.00V. The infinite open loop gain gives us the perfect load regulation, i.e., the output voltage always settles to 3.00V under all conditions. dV = 153 mV is a result of ESR and ESL of the output capacitor. Equation (4) is the equation and derivation.

Figure (14c) and (14d) show output transient effects with ±1% tolerance on the error amplifier, 153 mV of voltage change at the output gets out of the ±5% output voltage limit called out in the Intel P6 DC-DC converter design specification.

The EL7560 utilizes a unique error amplifier compensation technique to control the load regulation. The Intel spec allows a 4% total output change with loading. The load regulation is set such that at minimum output load (0.3A) the output voltage is 2% higher than nominal (5A) and at maximum load (12.4A) the output voltage is 2% lower. The result is an additional 2% (60 mV) of head room for transient load response. Figure 15 shows the transient response waveforms.

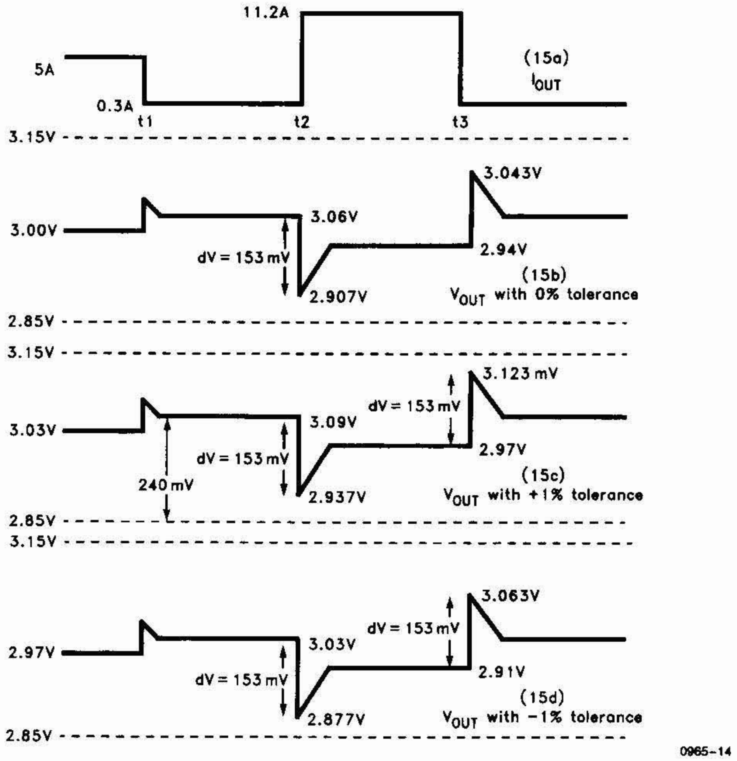


Figure 15. EL7560 Transient Output Voltage Response

In summary, if the load regulation is properly controlled, i.e., at minimum load the output voltage is 2% (60 mV) higher than nominal load (5A) and at maximum load the output voltage is 2% (60 mV) lower than nominal load, we can fit the output transient response curves within Intel's ±5% window under any conditions.

Input Filter/Input Current Transient Analysis

A 1 μH inductor in series with the input capacitor is required to meet the Intel "Load Transient Effects" specification which states that, "During this step response (the output load is switching from 0.3A to 12.4A) the input current di/dt shall not exceed 0.1A/μs." The input filter inductor is absolutely necessary in the standard buck topology. The simulation results of input transient current during output load changes are shown in Figure 16. As the input inductance increases, the slope of the input transient current decreases.

In the Elantec module reference design, a custom inductor is used. The core of the inductor is Micrometals T30-26 and the wire gauge is AWG#20 with 7 turns. The inductance value is 1.6 μH. For users who want to use an off the shelf inductor we sugest the Pulse engineering PE53188. Its inductance spec is 2.2 μH at 6.4A.

Figure 16 shows the simulated input current response for various combinations of the input inductor and capacitor. The simulation result shows that a 1.5 μH inductor and a 2 mF capacitor combination suffice to meet the Intel input transient specification.

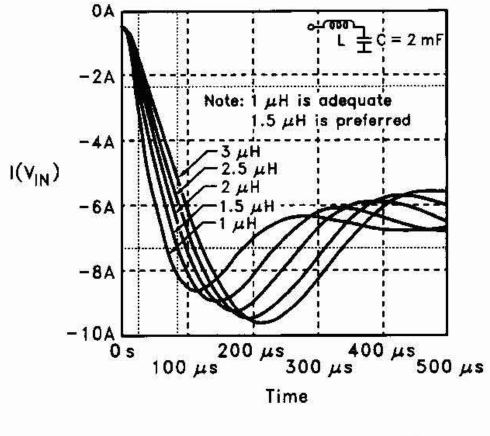


Figure 16. Input Filter Transient Response

Over-Voltage Protection

The over-voltage condition is defined by Intel as the situation when the output voltage goes 10% higher than the programmed level. Upon detection of an over-voltage fault, the internal high side FET is turned off. A clamping diode D4 from the LX pin back to the input is recommended to keep the LX pin a diode voltage drop above the input. The switcher recovers automatically when the over-voltage fault is removed.

Over-Current Protection

The EL7560 has a built-in over-current protection feature. When an over-current fault occurs, the high side FET automatically turns off. The switcher recovers automatically when the over-current fault is removed.

Efficiency Calculations

Most of the power dissipated in the EL7560 is due to the "on" resistance of the power FETs. Each power FET exhibits a typical 30 mΩ "on" resistance; therefore, the power loss is $P = I^2R = 12.4 \bullet 12.4 \bullet 0.030 = 4.61W$ (at rated maximum load).

Efficiency curves of the typical VRM demo module is depicted in Figure 17. The curves show low efficiency at both ends of the output loading. At the low output current end, switching losses of the switcher is high relative to the output power. At the high output current end, the on-resistance of the power mosfet dominates.

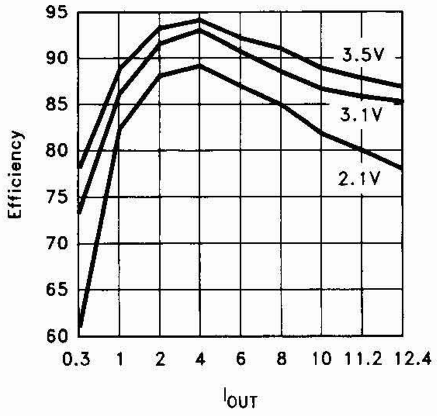


Figure 17. VRM Efficiency

Heat Sinking Requirements

For reliability reasons, the Intel spec requires that the junction temperature of the EL7560 be kept below 115°C with the ambient temperature at 50°C and 100 LFM air flow. The minimum θ_{JA} required is:

$$\theta_{JA} = (115-50)/4.61\text{W} = 14.1°\text{C/W}$$

The θ_{JA} for the 28-pin PSOP2 without a heat sink is 52°C/W, and the θ_{JC} is 5°C/W. The θ_{JC} of the device combined with the thermal resistance of the heat sink must be less than 17°C/W. Thermal analysis has been done with Wakefield 8052-60 mounted on top of the package with Ablebond 84-1 LMIT epoxy adhesive which has 0.2°C/W thermal resistance. With a board size of 1.5″ x 3″ and an air flow of 100LFM, measurements made by Elantec yield a θ_{JX} is 12.9°C/W.

Board Layout Considerations

Grounding Issues

Figure 18 is the simplified circuit of the power system.

When the high side FET is turned on, Figure 19 shows current flow directly from the AC/DC power supply and the input capacitor through the high side FETs to the load. The ground return current splits into two directions: 1) from the load directly to the AC/DC power supply 2) from the load into the DC-DC module and to the ground of the input capacitor.

When the low side FET is turned on, most of the output load current flows through the low side FET. Current from the AC/DC power supply continues to flow into the input capacitor, whose magnitude (around 8A at maximum output load) is the same as the ground return current from the load. The 12.4A of output current is a combination of current from the input capacitor and the ground input of the DC-DC module.

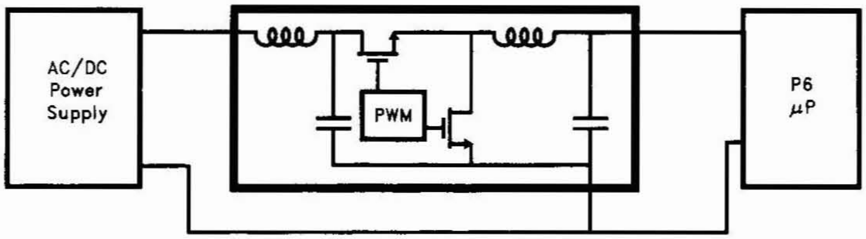

P6 DC-DC Module
AC/DC
Power
Supply
PWM
P6
μP
0965-16

Figure 18. A Simplified Power System Block Diagram

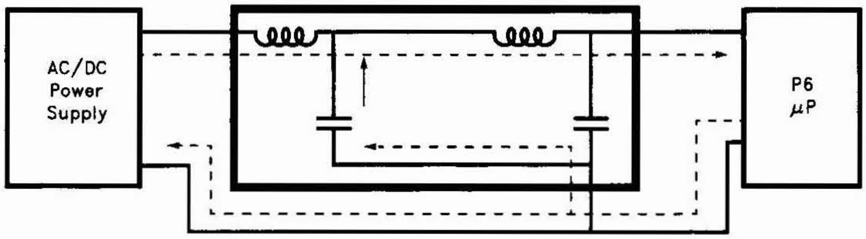

P6 DC-DC Module
AC/DC
Power
Supply
P6
μP
0965-17

Figure 19. Current Flow Path when High Side Switch is ON

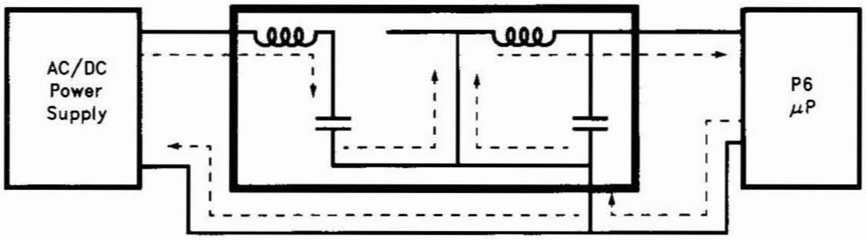

P6 DC-DC Module
AC/DC
Power
Supply
P6
μP
0965-18

Figure 20. Current Flow Path when Low Side Switch is ON

Figure 21 summarizes the magnitudes and directions of currents at various nodes in the DC to DC converter under the maximum output loading condition. The DC-DC module input and output current, and AC/DC power supply ground return current, and load return current are constant under steady state conditions.

The current path in the above figures show that the power ground pin, V_{SSP}, V_{IN}, and LX pins, which are switching at 500 KHz, are thus extremely noisy. They should be isolated from the logic control and reference of the PWM controller. The ground pin of the output capacitor, C10, is the quietest point in the converter. We recommended splitting the signal ground and power ground at the ground pin of the output capacitor.

The V_{SS} pin and ground connection for C4, C7 and C8 should all be connected to the signal ground.

A 12.4A DC-DC converter reference layout is included in the appendices section of this application note. Proper grounding and layout techniques discussed above are demonstrated in this design.

Charge Pump Design

The EL7560 has an internal voltage doubler and a bootstrap charge pump to generate the high voltage required to switch on the internal high side N-channel FETs. C5, the 1 μF capacitor from pin 1 to 2, is the voltage doubler pump capacitor. It charges C11 through D2. A ceramic capacitor is adequate for C5. D1 and C6 are the bootstrap diode and capacitor. When the low side FET is turned on, capacitor C6 is charged to 10V, when the high side FET switch on the V_{HI} pin is bootstrapped to 15V. Capacitor C11 holds the voltage doubler output voltage and the 100Ω resistor R1 limits the current into the low side FET drivers inside the chip. A 1N914 type diode suffices for both D1 and D2. The most critical specification for selecting this diode is its reverse breakdown voltage which should be greater than 15V. In addition, a low forward voltage drop is desired to generate a higher voltage level for the high side drive. If a 12V supply is available, then the charge pump diode and voltage doubler capacitor can be eliminated. Figure 22 shows the circuit implementation.

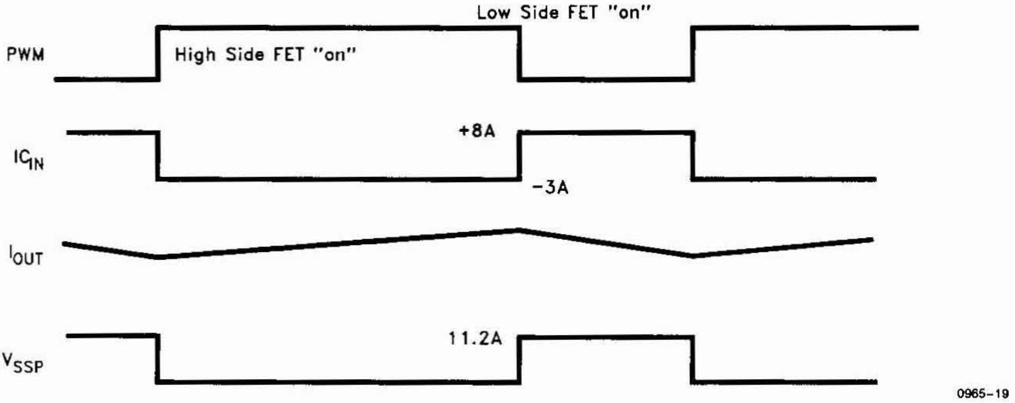


Figure 21

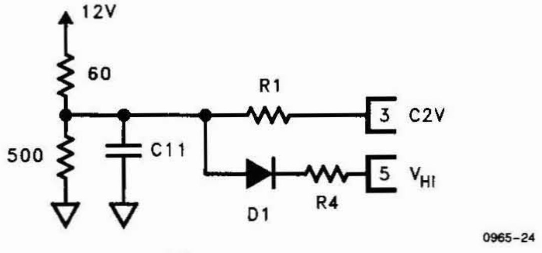
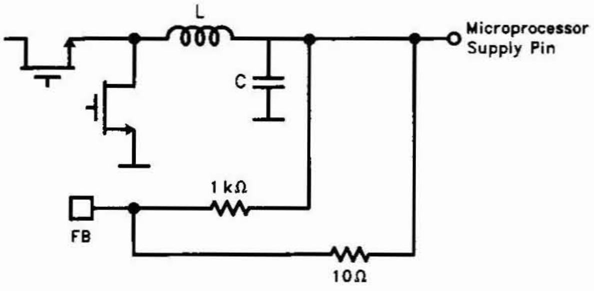


Figure 22

Remote Sense

Although it is not specified in Intel P6 DC-DC converter design guide, remote sensing is often desired in many applications. In the case of a 200 MHz P6 microprocessor, the supply current can reach over 12.4A. A 10 mΩ of trace resistance results in a 124 mV of voltage drop from the converter output to the microprocessor supply pin. A simple method of implementing remote sensing is depicted in Figure 23.



0965-23

Figure 23.

The 1 kΩ resistor is connected directly to the converter output and the 10Ω remote sense resistor should be tied directly to the load or the microprocessor supply input pin.

Bill of Materials

C10, United Chemi-Con, LXF16VB681M10X20LL, 680 μF	6 pcs
C9, United Chemi-Con, LXF16VB681M10X20LL, 680 μF	3 pcs
L1, Pulse Engineering, Inductor, PE-53681, 2.5 μH	1 pc
C4, C6, Chip Capacitors, 0.1 μF	2 pcs
C7, Chip Capacitors, 400 pF	1 pc
C8, Chip Capacitors, 200 pF	1 pc
C5, C11, Chip Capacitors, 1 μF	2 pcs
D1, D2 SMT Diode, 1N914	2 pcs
L2, Inductor, 1.5 μH, Micrometals T30–26, 7T AWG#20	1 pc
R1, 100Ω	1 pc
R2, 10 KΩ	1 pc
R3, 1K	1 pc
R4, 30Ω	1 pc
AS1004, 1.235V Reference Diode	1 pc
Heat Sink—Wakefield Engineering, 8052-60	1 pc

Appendices

Package outline

Core and Inductor Manufacturers
Magnetic Cores
Micrometals
1190 N. Hawk Circle
Anaheim, CA 92807
Phone 800-365-5977

Inductors
Pulse Engineering
P.O. Box 12235
San Diego, CA 92112
Phone 619-672-8100

Inductors
Pan Technology Ltd.
Unit 11, 6/F Proficient Industrial Center (Block A)
6 Wang Kwun Road
Kowloon Bay, Hong Kong
Phone 852-2758-5759
Fax 852-2758-5761

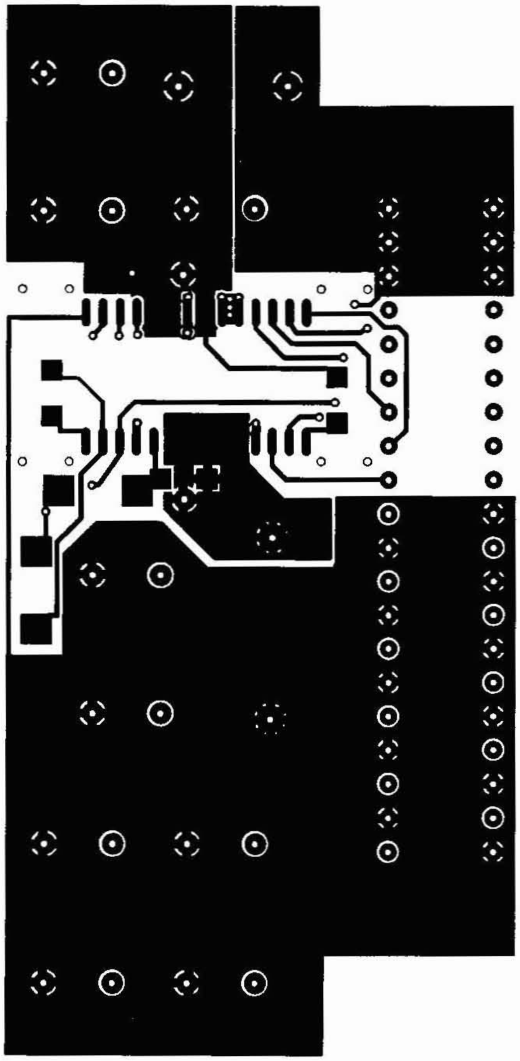
Capacitor Manufacturers
Aluminum Electrolytic Capacitors
United Chemi-Con
9801 West Higgins Road
Rosemont, IL 60018
Phone 708-696-2000

Solid Tantalum Chip Capacitors/OS-Con
Solid Aluminum Capacitors
Sprague
678 Main Street
Sanford, ME 04073
Phone 2070324-7223

Heat Sink Manufacturers
Heat Sink and Mounting Clip
Pan Technology Ltd.
Unit 11, 6/F Proficient Industrial Center (Block A)
6 Wang Kwun Road
Kowloon Bay, Hong Kong
Phone 852-2758-5759
Fax 852-2758-5761

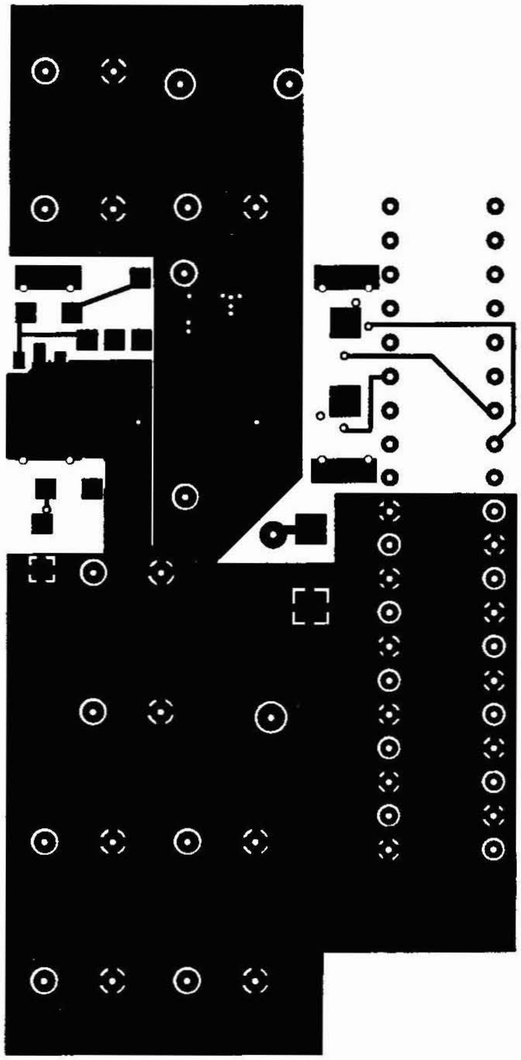
Heat Sink
Wakefield Engineering

Top Layer

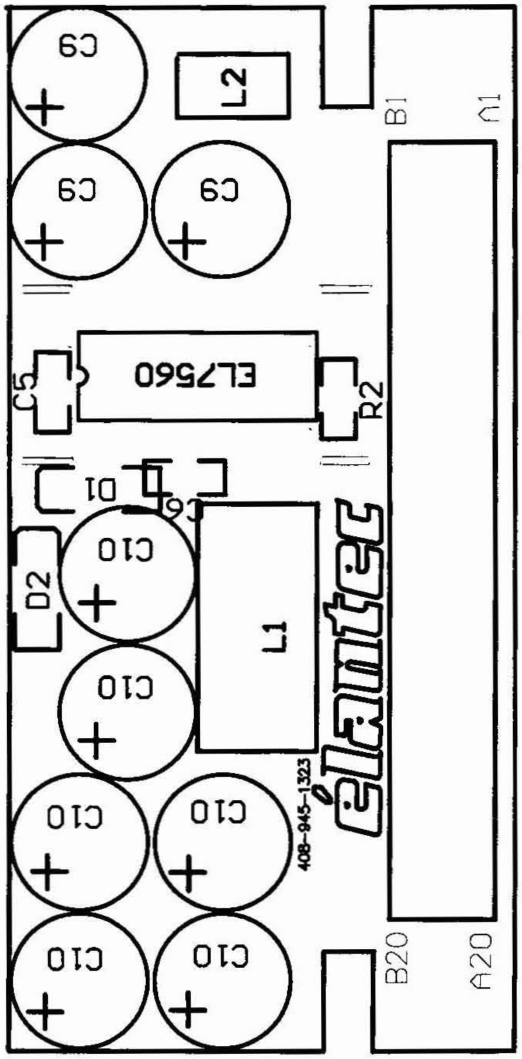


0965-20

Bottom Layer



Top Layer Silkscreen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B1
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C9
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R2
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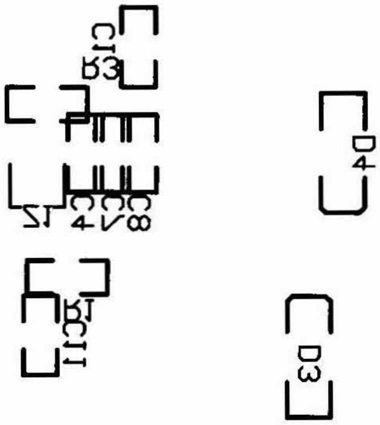
Bottom Layer Silkscreen


C12
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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

The Care, Feeding, and Application of Unity Gain Buffers

Introduction

Unity gain buffers have been available in integrated form since the introduction of the LH0002 by National Semiconductor several years ago. The "ideal" buffer would exhibit a gain identically equal to one, an input impedance of infinity, an output impedance of 0Ω, infinite bandwidth and zero phase shift, infinite slew rate, large but limited to a safe level output current, and an output offset voltage and input bias current of zero. These devices are usually implemented with fairly simple circuit topologies which makes them very cost effective in applications requiring large output currents, isolation from reactive loads, input to output isolation, and in some instances thermal isolation in circuits requiring precision gain and offset. The buffers simplicity imply obvious applications in a circuit. After all, what could go wrong with a unity gain buffer? This note is intended to discuss this very subject.

Circuit Topologies

When you get down to it, there are only two types of circuits: open and closed loop. The latter are specially designed operational amplifiers optimized for operation at unity gain which typically exhibit less bandwidth, more phase shift, and usually more expensive than the open loop variety. On the other hand, they exhibit better offset voltage and gain linearity. The former is essentially a glorified compound emitter follower offering cost, increased bandwidth, and in general poorer DC characteristics.

Open Loop Buffers

Shown in Figure 1 is the classic "0002" topology. It is comprised of compound emitter followers Q1 and Q3 which provide current gain for positive going signals and their mirror image of Q2 and Q4 for negative signals. Bias is set up with current sources I1 and I2. In some realizations of the circuit, I1 and I2 are replaced by resistors. If we assume for simplicity that I1 = I2, inspection of the circuit reveals that the Vbe's of Q1 and Q2 are impressed across the base emitter junctions of Q3 and Q4; hence, the emitter currents of Q3 and Q4 are almost equal to I1 or I2 (ignoring the effects of R1 and R2). In real circuits, R1 and R2 are used to prevent thermal runaway of the output stage. Since Q3 and Q4 will sink or source many milliamps, their Vbe's will decrease as they heat up, but the "bias" voltage across them, $Vbe_{(Q1)} + Vbe_{(Q2)}$ remains substantially the same, there is a real possibility of reaching a thermal runaway point. R1 and R2 provide "positive" feedback to the output transistors increasing their effective Vbe as the output current increases.

One of the nice things about the 0002 topology is that it exhibits very low crossover distortion (typically under 0.1% with an output power of 0.5W @ 10 MHz). As the output current in Q3 increases, its Vbe increases while Q4's emitter current and Vbe decrease while the bias of $Vbe_{(Q1)} + Vbe_{(Q2)}$ remains essentially constant. Q4's emitter current never quite goes to zero thus minimizing crossover distortion.

The output current will limit or the output voltage will "clip" when all the current provided by I1 (or I2) is demanded as base current to Q3 (or Q4) which obviously occurs when: $I1 = I_{OUT}/\beta$ or when I1 saturates. The output offset voltage is simply the difference between Vbe_{Q1} and Vbe_{Q3} or Vbe_{Q2} and Vbe_{Q4} whichever is lower. To the first order then:

$$V_{OS} = Vbe_{Q1} - Vbe_{Q3} \text{ or } Vbe_{Q2} - Vbe_{Q4} \qquad (1)$$

$$Ibias = I1\,(\beta 1 - \beta 2)/(\beta 1)(\beta 2) \qquad (2)$$

$$A_V \cong R_L/(R_L + R_{OUT}) \qquad (3)$$

$$R_{OUT} \cong [R1 + re_{Q4} + Rs/(\beta 4 * \beta 1)]/2 \qquad (4)$$

$$R_{IN} \cong (\beta 1)(\beta 2)(R_L) \qquad (5)$$

$$I_{SUPPLY} \cong 3\ I1$$

Myth Number 1: Input Impedance

Earlier we said that one of the attributes of an ideal buffer was infinite input impedance. Illustrated in Figure 2 is a plot of the input impedance of the EL2002, 180 MHz Unity Gain Buffer. Clearly, at low frequencies, the input impedance is above 1 MΩ; however, as the frequency increases the β decreases and the input impedance drops accordingly per equation (5). In fact there is a doublet in the vicinity of 50 MHz where the input capacitance of the EL2002 and the source resistance create the additional pole. This behaviour is typical of all 0002 type buffers and whereas it is not fatal, the user should be aware of the issue.

Myth Number 2: Output Impedance

The ideal buffer should exhibit zero output impedance. Illustrated in Figure 3 is the DC output impedance of the EL2002 as a function of output current. As the load current increases, R_{OUT} asymptotically approaches the value of R1 or R2 (depending on which half of the circuit is working). In other words, the r_e term approaches zero as the emitter current increases per equation (4) above. Furthermore, Figure 4 illustrates the small signal output impedance of the EL2002 as a function of frequency. In this instance any impedances which exist at the base of Q3 (or Q4) is divided by the product of $\beta 1 * \beta 4$, but as the frequency goes up, the β goes down, and the R_{OUT} increases. The dip in the output impedance above 100 MHz is due to capacitance of the package and on the die.

The foregoing discussion would have consequences in applications where the buffer was used "open loop" for example as a video distribution amplifier. Since R_{OUT} is both a function of output current and frequency, the gain of the circuit would vary destroying the backmatch to the coax cable thereby creating distortion.

Booby Trap Number 1: Closed Loop Operation Oscillation

Clearly, a straight forward way of avoiding the problem in the previous section is to put the buffer in a loop with an op amp or CFA as illustrated in Figure 5. Indeed, this is a classical application for a buffer when the op amp does not have enough output current to drive the desired load. What could go wrong? In some instances, depending on the bandwidth and phase margin of the amplifier and the phase shift through the buffer, the composite loop can and will oscillate. For example, the phase shift of the EL2002 is illustrated in Figure 6. At about 100 MHz, it exhibits a phase lag of about 70°. When placed in a loop with an EL2044 which exhibits a nominal 60 MHz bandwidth with 45° phase margin and connected for unity gain, the circuit peaks 12 dB (or if you prefer **oscillates**) as shown in Figure 7. The caveat of this story is that one might expect 45° of phase lag at the -3 dB bandwidth of the buffer which in the case of the EL2002 is 180 MHz, but you would be wrong. Obviously, in the circuit of Figure 5, the phase margin of the EL2044 is eradicated by the phase shift of the buffer and the circuit oscillates. The moral of the story is to select an amplifier and buffer whose phase characteristics are compatible.

Another distinct possibility that can cause oscillation is the pole created by R3 and the input capacitance to A2. R3 isolates C_{IN} from the output of the op amp, but if R3 $*$ C_{IN} is in the same order of magnitude as the unity gain crossing frequency as the op amp, you get oscillation. In this case, get the value for C_{IN} from the datasheet, and keep the value of R3 as small as possible.

Finally, given that the buffers are no more than compound emitter followers, their ability to buffer reactive loads is no better (or worse) than a conventional op amp. See Elantec Application Notes Numbers 9 and 22 for details.

Booby Trap Number 2: Closed Loop Operation

Virtually all monolithic buffers offer some sort of short circuit protection. Although not shown explicitly in Figure 5, the typical scheme senses current in R1 and R2 and limits the base drive to Q3 and Q4. Yet in some applications in spite of the manufacturer's claims of being short circuit proof, the buffer dies in the circuit. In this instance, envision a 0Ω short from the output of A2 to ground. The loop goes open and the output of A1 saturates toward the positive or negative rail. Clearly, the bases of Q3 and Q4 are "clamped" by the short to one Vbe above (or below) ground. If the base emitter breakdown voltage of Q1 or Q2 is less than the saturation voltage of A1 less a Vbe, these transitors can and will avalanche leading to self destruction.

To preclude this possibility, Elantec places a chain of back-to-back diodes (usually about 4) from input to output. This clamps the input to 4 Vbe's several volts below the rated breakdown voltage of Q1 and Q2. The moral of this story is to check with the vendor on the details of the short circuit method.

Closed Loop Buffers

Most of the pitfalls of the preceding sections can be avoided by choosing a "closed loop" buffer. One of our favorites is the EL2099 whose primary mission was intended as a video distribution amplifier. Nevertheless, it is a 50 MHz Current Feedback Amplifier with output current capability of 800 mA. It has all of the virtues of Figure 5 with none of the booby traps.

Conclusion

Some of the basic issues in using unity gain buffers has been presented, and armed with these details the wary and informed circuit designer can make excellent use of buffers in real and demanding applications.

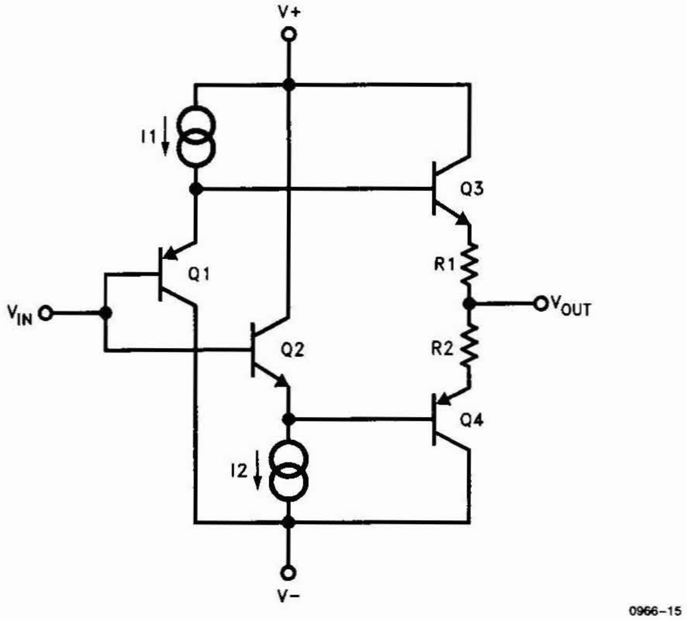

Figure 1. "0002" Topology

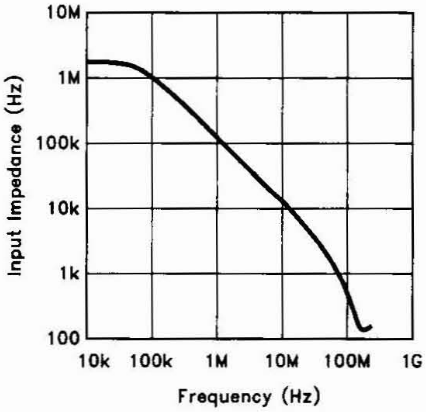

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Figure 2. EL2002 Input Impedance

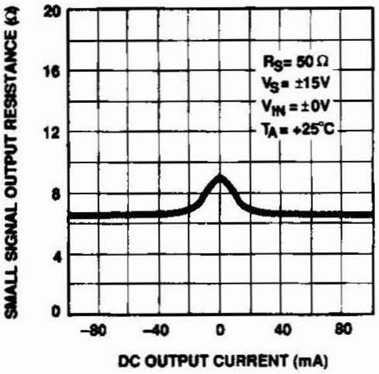

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Figure 3. EL2002 DC Output Impedance

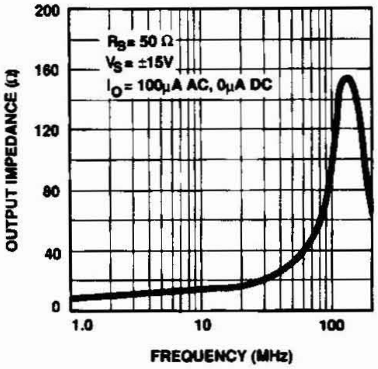

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Figure 4. Output Impedance vs Frequency

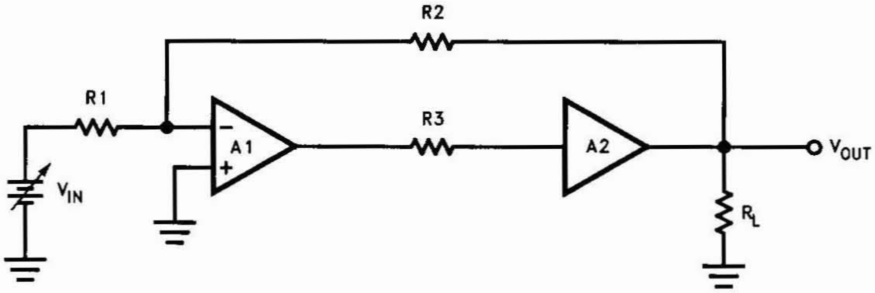

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Figure 5. Buffer in a Closed Loop with an Op Amp

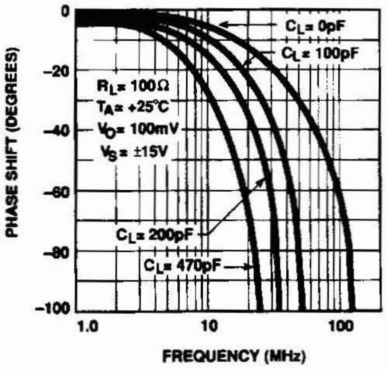

Figure 6. Phase Shift vs Frequency for Various Capacitive Loads

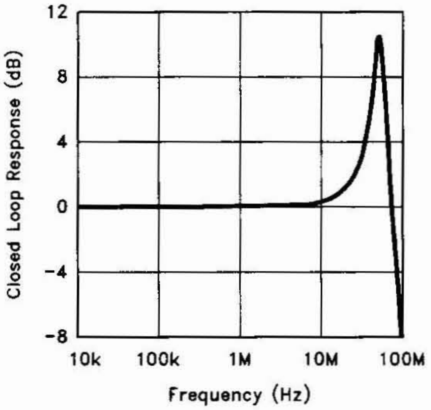

Figure 7. 2044 in Loop with 2002

Using Single-Supply High-Frequency Amplifiers

by Barry Harvey and Mike Wong

The trend toward lower power supply voltages has recently inspired the design of integrated single-supply high-frequency amplifiers. The greatest use of these circuits is in passing video signals, although there are many other applications. Unity-gain bandwidths of the new offerings are in the 90 MHz–160 MHz range.

The earliest single-supply IC amplifier is the LM324, developed circa 1974. This is a 1 MHz op-amp that set the definition of a single-supply circuit:

> A single-supply device works with no minus supply; using 0V and typically +5V for minus and V+ supply voltages, respectively. Inputs will linearly comply with 0 (ground) to some voltage approaching V+. Outputs will provide from 0V or nearly so to a voltage approaching V+.

Figure 1 shows circuitry at the input of these amplifiers. The input PNP differential pair is followed by an NPN folded cascode that performs level-shifting. The cascode emitter resistors have typically only 200 mV across them, allowing the input PNP bases to comply with ground-level inputs, and even a bit below ground, without severe saturation. For positive swings, the current-source transistors and the V_{BE}'s of the input transistors set the input positive headroom, between 1.1V and 1.7V. The DC input offset will not degrade until input swings are within millivolts of the headroom limits, but AC characteristics can vary hundreds of millivolts from the limits. Usually bandwidth is the non-constant parameter, but in some circuits transient responses are also distorted.

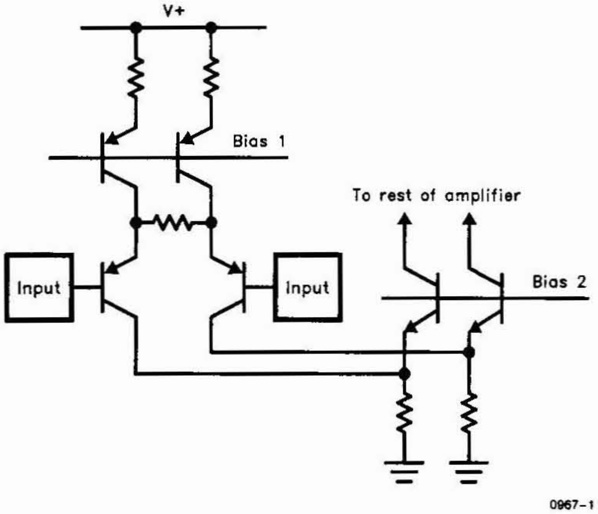

Figure 1. Typical Single-Supply Amplifier Input Stage

The maximum output swing below V+ usually is about the same as input headroom. A complication is that output stages in bipolar technology cannot inherently sink current all the way to ground, and minimum output low swing depends on the polarity and magnitude of load current. A grounded pull-down resistor is often used to help the output to drop all the way to ground. Figure 2A shows an NPN/PNP output stage. A load resistor keeps the output NPN properly biased all the way to ground, but the output PNP has turned off well above. Figure 2B shows an all-NPN output stage. This design cannot swing as close to ground as 2A with a pull-down resistor, but it can swing somewhat lower than 2A when sinking load current. The all-NPN circuit does exhibit generally greater distortions and load capacitance sensitivity than the NPN-PNP design.

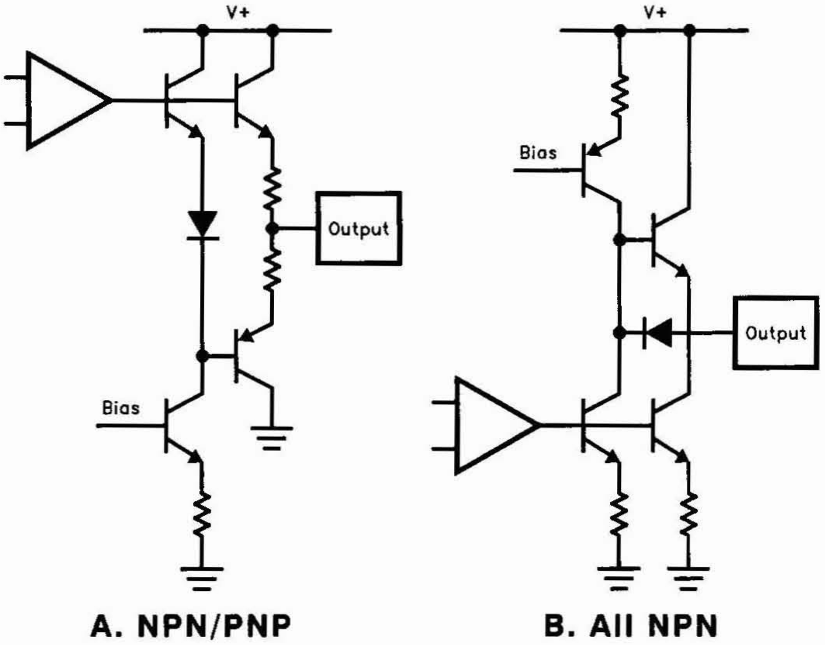

Figure 2. Typical Single-Supply Output Stages

Output linearities are generally quite good within the headroom range for DC signals, but high AC distortions occur when levels approach clipping. Figure 3 shows the differential gain and phase errors, that is, the constancy of small-signal gain and phase as DC level varies, for several commercial amplifiers. Amplifier A is an EL2044, a general-purpose video amplifier; B is an EL2210, a low-cost video amplifier; C is an EL2150, a 125 MHz true single-supply video amplifier; and amplifier D is another vendor's 90 MHz single-supply amplifier. In Figure 3, all amplifiers are wired for a gain of +1, the input is a 50 mV_{p-p} 3.58 MHz AC signal with DC offset sweeps from 0V to 5V, the load is 500Ω to ground, and the supply voltage is +5V. Here is a summary of amplifier swings, with 0.4% or 0.4° gain and phase deviations from the center of the span:

Table 1. Amplifier Output Swings [V] for 0.4% or 0.4° Deviation from Curves in Figure 3

Amplifier	Low Swing	High Swing	Span Center	Total Span
A	1.05	3.00	2.03	1.95
B	0.65	2.80	1.73	2.15
C	0.22	3.50	1.86	3.28
D	0.22	4.10	2.16	3.88

For small signals, differential gain is similar to linearity error or harmonic distortion, although the scale factor between them is not 1:1. Differential phase is a specification important to preserving color quality in NTSC video. Differential gain and phase errors of 0.5% and 0.5° are sufficient for consumer or overlay NTSC video; 0.1% and 0.1° or better is required for professional NTSC video; and 0.5% gain linearity is sufficient for high-quality component video signals.

Note that each amplifier has a unique set of swings and center of span. Note that the single-supply amplifiers simply cannot operate linearly all the way to ground. If the maximum linear spans are to be obtained, the input signal must be offset by the Span Center. If offset, all of these amplifiers can pass an NTSC video signal with low distortion, even the non-single-supply models.

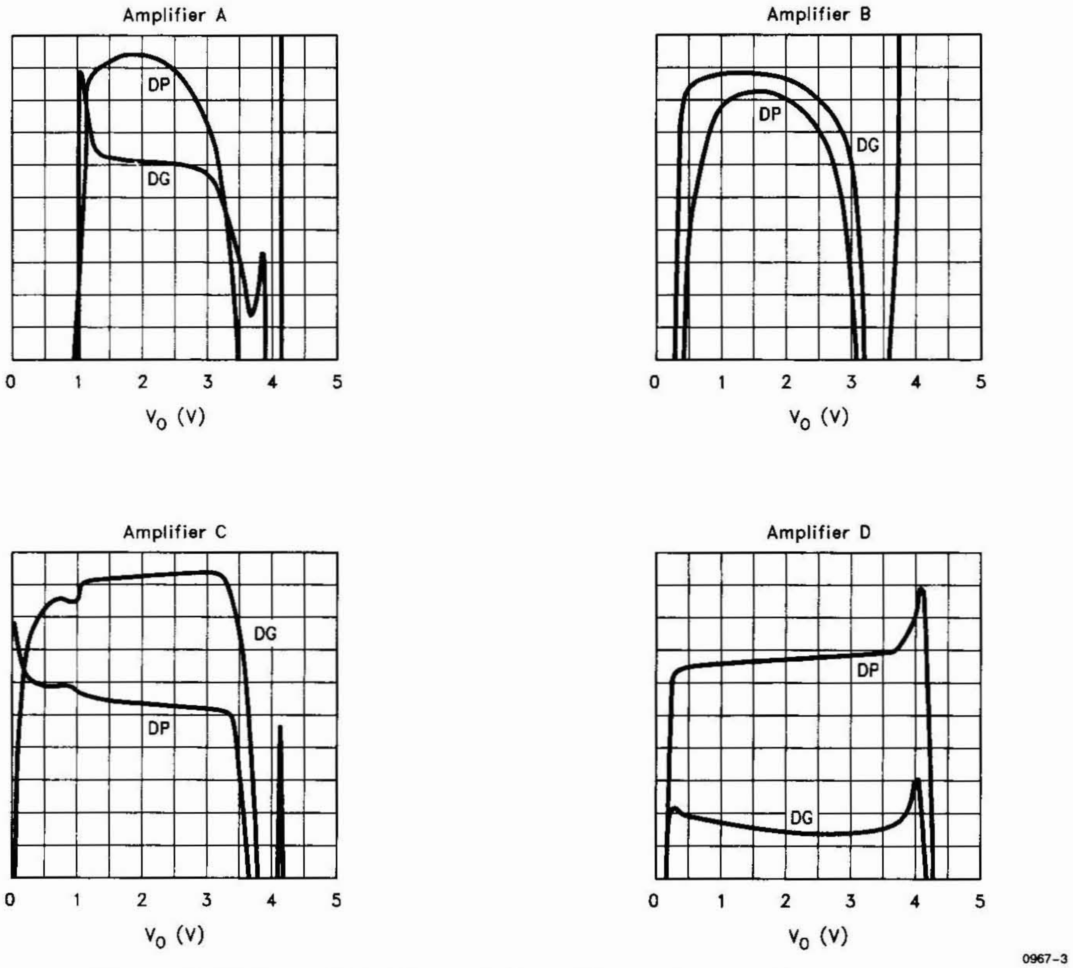

Figure 3. Differential Gain and Phase Error, $A_V = 1$, $R_L = 500$, $V_{IN} = 0V–5V$, DG = 0.2%/div, DP = 0.2°/div

Figure 4 shows the amplifiers wired for a gain of +2 and driving a 150Ω load to ground, as in driving a back-terminated 75Ω cable service. The input is a 50 mV_{p-p} 3.58 MHz AC signal with DC offset sweeps from 0V to 2.5V. The amplifiers all have more distortion with the heavier load:

Table 2. Amplifier Output Swings [V] for 0.4% or 0.4° Deviation from Curves in Figure 4

Amplifier	Low Swing	High Swing	Span Center	Total Span
A	1.05	2.50	1.78	1.45
B	0.50	2.15	1.33	1.65
C	0.30	3.13	1.72	2.83
D	0.45	4.00	2.23	3.55

The amplifier A cannot linearly swing the 2V span of double-sized NTSC signal and is not applicable to this task. Amplifier B can be used if the input is offset such that the worst distortion occurs in the non-critical sync portion of the signal. Neither of the true single-supply amplifiers will have trouble with video signals, and the output can be allowed to go all the way to ground in the sync tip.

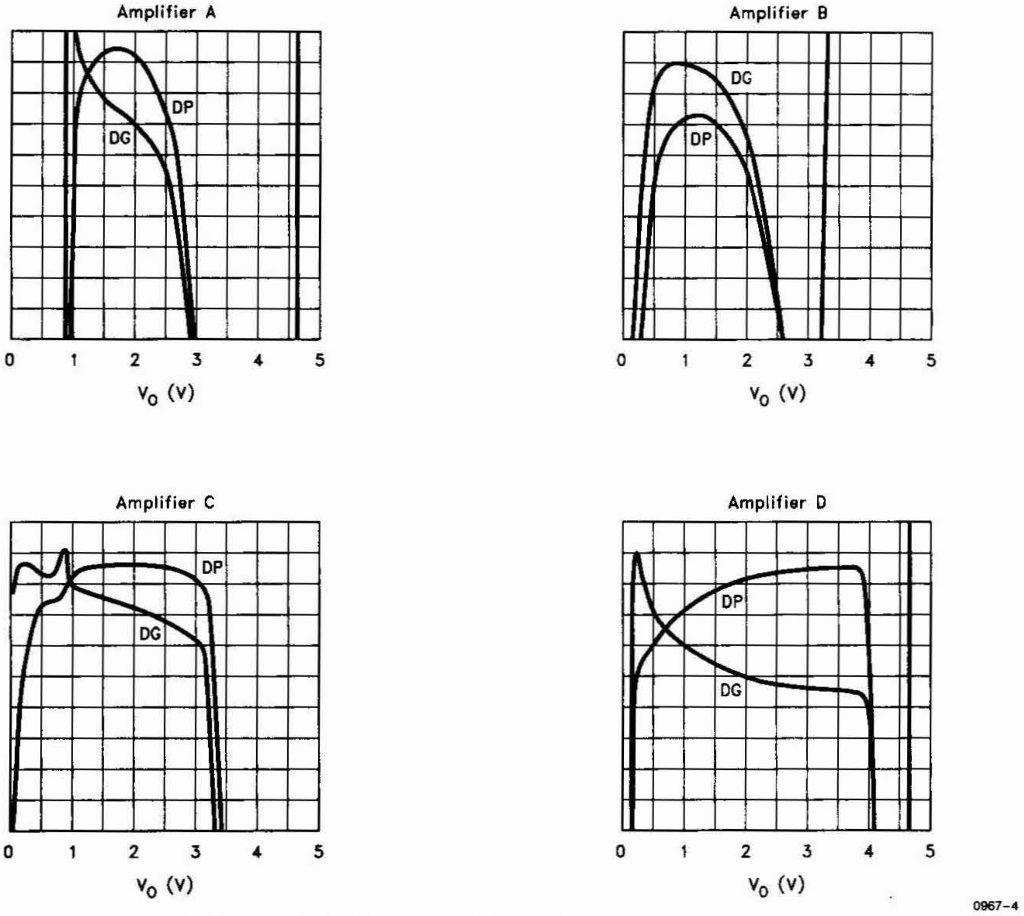

Figure 4. Differential Gain and Phase Error, $A_V = 2$, $R_L = 150$, $V_{IN} = 0V{-}2.5V$, DG = 0.1%/div, DP = 0.2°/div

The worst trouble occurs when the load is capacitor-coupled. This is very common for instrument inputs and outputs. In this case, AC load currents can be positive or negative. Figure 5 shows the performance of the amplifiers driving 300Ω to ground and 300Ω to V+, emulating a capacitor-coupled 150Ω load.

Generally, then, in single-supply amplifier circuits, signals will be offset above ground with capacitor coupling and DC-restoration used to regain offset levels.

Table 3. Amplifier Output Swings for 0.4% or 0.4° Deviation from Curves in Figure 5

Amplifier	Low Swing	High Swing	Span Center	Total Span
A	1.70	2.83	2.27	1.13
B	2.45	2.80	2.63	0.35 —requires pull-down
C	1.15	3.45	2.30	2.30 —0.5%/0.5°
D	0.73	2.00	1.36	1.27

Again amplifier A does not have enough swing for our video signal. Amplifier B fails altogether without a pull-down resistor. With the pulldown B's performance will be very close to that of Figure 4. Amplifier C shows crossover distortion but has a good swing, if we allow the error to increase to 0.5% and 0.5°. Amplifier D has terrible crossover distortion and a very restricted output range, so is useless for driving bi-directional load currents.

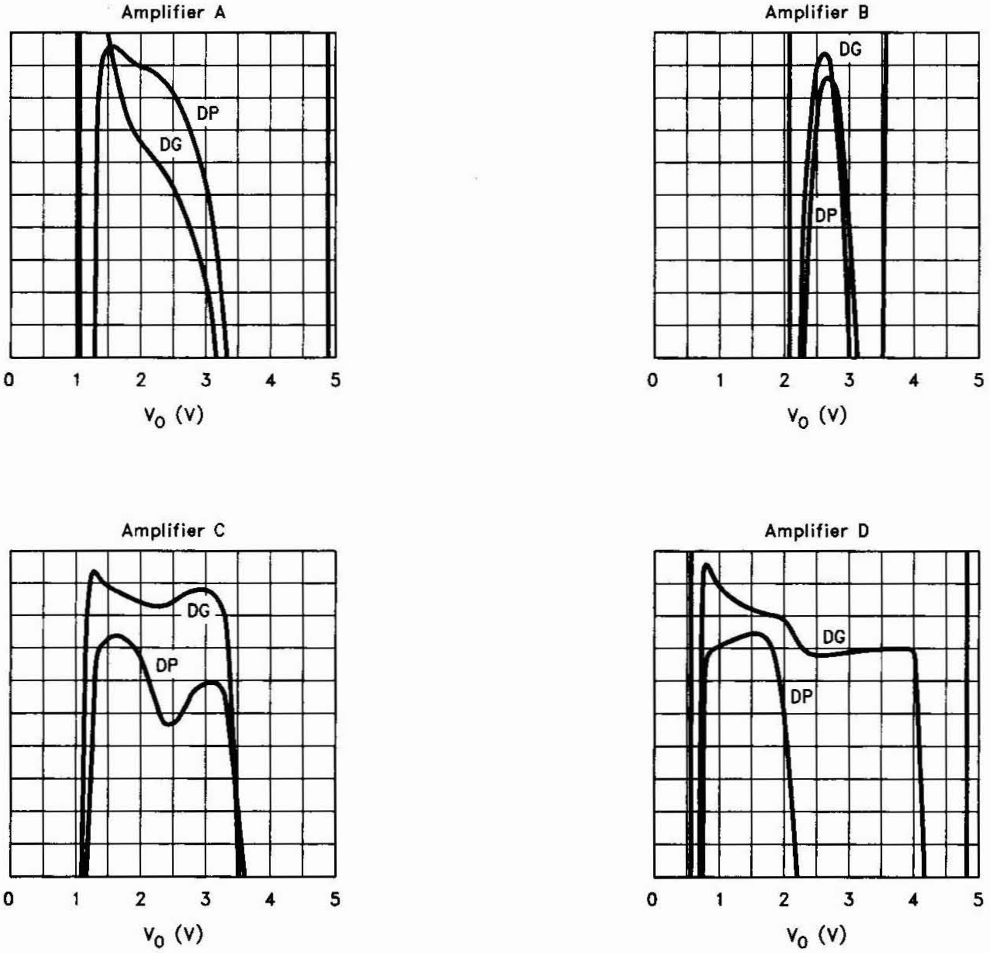

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Figure 5. Differential Gain and Phase Error, $A_V = 2$, $R_L = 300$ to V_{CC} and 300 to Ground, $V_{IN} = 0V-2.5V$, DG = 0.1%/div, DP = 0.2°/div

The transient response curves shown in Figure 6 present another approach to studying distortion when the output is driven toward ground. All amplifiers are wired in unity gain configuration and powered with a +5V single supply and drive 150Ω load. The input is a 1 MHz 4 V_{p-p} sinewave with its minimum voltage at 0V. Amplifier A output clips are around 250 mV. Amplifiers B and C output linearly go down to 50 mV above ground. Amplifier D, even though it can reach 80 mV from ground, shows a saturation recovery step at 475 mV. Voltage clipping and saturation recovery directly translate to differential gain and phase errors.

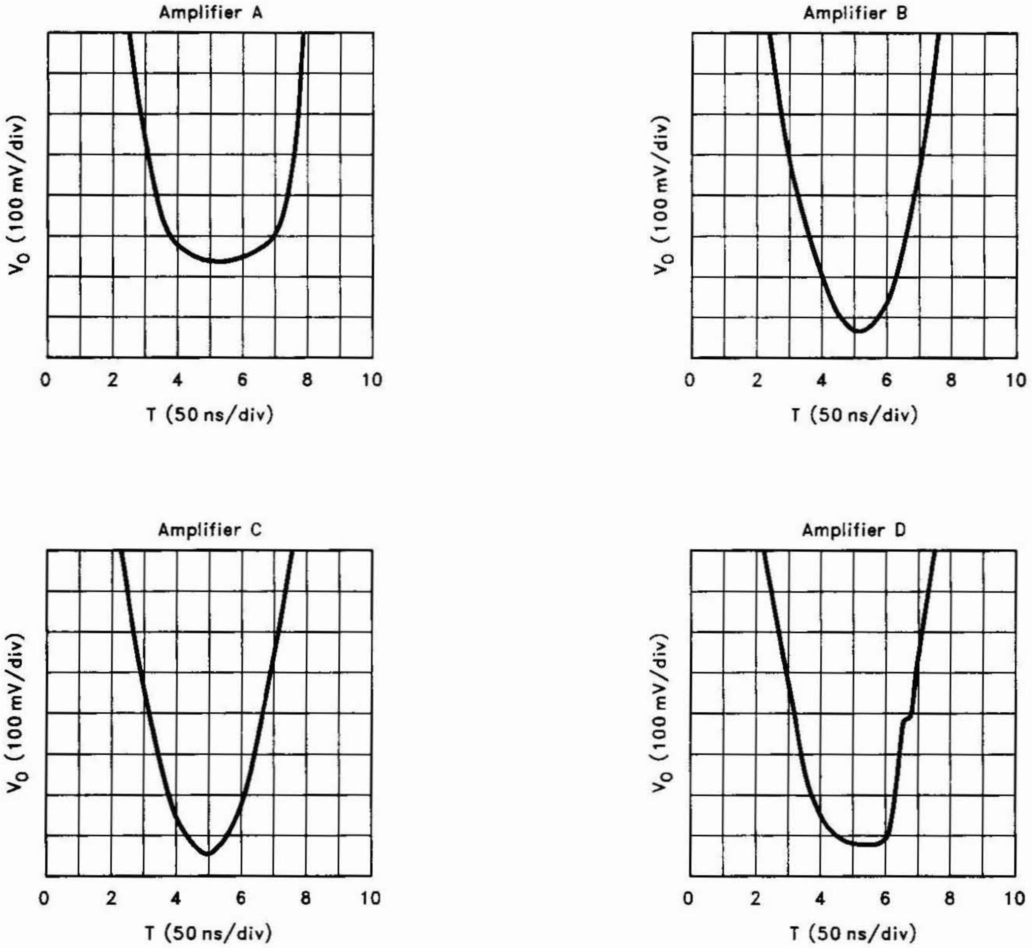

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Figure 6. Transient Response, $A_V = 1$, $R_L = 150$

Conclusion

High-frequency op-amps' linearities suffer greatly in single-supply service. To optimize video performance it is helpful to level-shift the signal, possibly with a DC-restore system. Specially designed single-supply amplifiers offer the widest swings, but have serious limitations and behaviors that must be measured individually.

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
Reliability and the Electronic Engineer
Application Note #21

Reliability and the Electronic Engineer

by Barry Siegel

Introduction

There is probably no more crucial issue than Reliability at the system level to both the component vendor and the systems house, and surprisingly there is very limited understanding of the mechanisms that yield to failures. This paper sets forth simply what the electronic Design Engineer needs to know with regard to calculating a given component's Mean Time Between Failure (MTBF), Failure Rate (FR), Failures In Time (FITS), and what all this jargon means.

Reliability Overview

Contrary to popular opinion, all integrated circuits begin "dying" the moment they are born, and in general, raising the average junction temperature will result in increasing the failure rate. The Arrhenius relationship which is common in many physical and chemical processes has been found to fit the failure rates in IC's as well. Equation (1) expresses the relative failure rate for temperatures, T1 and T2, and the ratio, R2/R1, is often referred to as the Acceleration Factor.

$$\frac{R2}{R1} = e - \left(\frac{EA}{KT2} - \frac{EA}{KT1} \right) \tag{1}$$

Where:

R = Failure Rate

EA = Activation Energy (typically 0.5 eV to 1 eV)

T = Absolute Temperature (°K)

K = Boltzmann's Constant (1.38×10^{-23})

One very significant issue is the assumed Activation Energy. Illustrated in Figure 1 is the Failure Rate for 0.5 eV and 1 eV as a function of temperature. Significantly, at junction temperatures above 100°C, the failure rate at 1 eV is 1,000 times that of 0.5 eV.

Reproduced in Figure 2 are the reported Activation Energies for various kinds of components. At Elantec, we use 0.8 eV to 1.0 eV, which is best suited to the kinds of processes that we employ.

In order to calculate MTBF we will also need to obtain reliability data from the IC vendor. Virtually all manufacturers routinely run life tests on devices which span their product line and package repertoire. Life test usually means placing devices in a burn-in oven, under power, at temperatures which are typically set at 125°C for 1,000 hours or more. Shown in Figure 3 is data taken from a slice in time for a variety of devices manufactured by Elantec. As indicated, a total of 692 devices were tested at 125°C, and the total device hours were 867,520. Failure Rate and MTBF are given by:

$$FR = \frac{\text{No. of Failures}}{\text{Total Device Hours}} \tag{2}$$

$$MTBF = \frac{1}{\text{Failure Rate}} \tag{3}$$

Since we had two failures in 867.5K hours, the FR is 2.3 per million hours, and the MTBF is 433.8K hours (at 125°C). Suppose we wanted to know what the FR and MTBF would be at 25°C. Using Equation (1) and assuming that the Activation Energy is 1 eV, we calculate an Acceleration Factor of:

$$\begin{aligned} \frac{R2}{R1} &= e - \left(\frac{EA}{KT2} - \frac{EA}{KT1} \right) \\ &= e - \left[\frac{1.6E-19}{1.38E-23} \left(\frac{1}{398°K} - \frac{1}{298°K} \right) \right] \\ &= 17{,}698 \end{aligned}$$

Then we multiply the 125° MTBF of 433.8 hours by 17,698 to obtain 7.7 billion hours and corresponding FR of 0.13 per billion hours.

Another often heard term is FITS which stands for Failures in Time and is defined as the number of failures per billion hours. For the example above, FITS is equal to 0.13.

The Real World

It turns out that the foregoing analysis isn't quite right, and the reason is that our calculation was based on a relatively small sample of devices. To prove the point without thinking about it too much, suppose that we had observed zero failures in the earlier example. That would lead us to the false conclusion that the MTBF was infinite and the FR was zero. What do we do now?

Fortunately, we can turn to Poissan statistics to bail us out. And we all thought that the statistics course in school would never be of any benefit. Equation (4) predicts the probability (of failure), P(X), of finding X failures in a sample whose average failure rate is A.

$$P(X) = \frac{e^{-A} A^{X}}{X!} \tag{4}$$

P(X) = Probability (of failure)
X = Failures observed
A = Average number of failures

Suppose we ran a large number of such life tests (say 1,000) which actually had an average failure rate of 3.12. Figure 4 summarizes the statistics of equation (4). The table predicts that 4.4% of the time (or in 44 life tests) we would observe no failures, 13.7% of the time we would observe one failure, 21.5% of the time we would observe 2 failures, etc. We could say that 39.6% of the time we would observe either no failures, 1 failure, or two failures. Probably a better way of looking at this data is that in 1,000 tests we would anticipate observing more than 2 failures 60.4% of the time. Therefore, if we ran only one test and observed 2 failures, we would have to say, "with a confidence level of 60.4%, that the actual failure rate is 3.12."

We should use 3.12 average failures in all of our calculations instead of our 2 observed failures, and we should always add, "to a 60% confidence level" to all the numbers we quote. So, our experimental data from Figure 3 boils down to an MTBF of 867,520 hours divided by 3.12 or 278,051 hours at 125°C to a 60% confidence level.

Fortunately, we don't have to go through all this convoluted reasoning each time we want to make calculations because the statisticians have calculated fudge factors for us which are summarized in Figure 5.

Note that this solves our "zero observed failure problem" by assigning 0.916 average failures to the case of zero observed failures to a 60% confidence level.

On the other hand, 60% confidence level doesn't sound very confident. If we wanted to be more conservative, we could use a fudge factor from a 90% confidence level. Now our 3.12 average failures become 5.3, and that makes our failure rate and MTBF look a lot worse. Most semiconductor manufacturers have historically used 60% confidence levels.

The Bottom Line

To ascertain the system level FR and MTBF, we must perform a thermal analysis for a given device to calculate average junction temperature. We will then use the Arrhenius Relationship and the IC manufacturer's reliability data and Activation Energy to predict FR and MTBF. For example, an EL2044 packaged in a plastic DIP is operated from 15V rails at an ambient temperature of 70°C. The output voltage is 2V and the load, R_L, is 150Ω; the feedback resistor, R_F, is 300Ω. Th quiescent power, Pq, is simply:

$$Pq = (V+ \; - V-)(Is) \tag{5}$$

The power dissipated due to load, Pl, is:

$$Pl = (V+ \; - V_{OUT})\left(\frac{V_{OUT}}{R_L \,||\, R_F}\right) \tag{6}$$

The total power is given by:

$$Pt = Pq + Pl \tag{7}$$

From the datasheet, we obtain an Is of 7.6 mA, so Pq is 228 mW. Pl is 260 mW, and Pt is equal to 488 mW.

$$T_J = (Pt)(\theta_{JA}) + T_A \tag{8}$$

θ_{JA} obtained from the datasheet is 95°C per watt which results in a junction temperature of 116°C. The datasheet states that the maximum allowable junction temperature is 150°C, so the application is okay from that point of view.

The life test circuit for the EL2044 indicates that the test is done with 15V supplies and essentially no load at 125°C under "ambient" conditions; hence, the life test data reported by Elantec would be under these conditions. The average power dissipation using equation (5) would be 228 mW, and the corresponding junction temperature per equation (8) would be 147°C.

We can now examine the predicted impact on MTBF and FR resulting from operating the junctions at 116°C. Using the Arrhenius Relationship we derive an Acceleration Factor of:

$$\begin{aligned} \mathrm{AF} &= \frac{\mathrm{R2}}{\mathrm{R1}} \\ &= e - \left[\frac{1.6\mathrm{E} - 19}{1.38\mathrm{E} - 23} \left(\frac{1}{389^\circ\mathrm{K}} - \frac{1}{420^\circ\mathrm{K}} \right) \right] \\ &= 9.0 \end{aligned}$$

The corrected (for finite sample size) MTBF with a 60% Confidence Factor that we calculated earlier was 278K hours. To obtain the "worst case" MTBF, simply multiply by 9.0 to obtain 2.5 million hours with a corresponding Failure Rate of 0.4 per million hours.

2.5 million hours seems like a long time, but presumably there could be many devices in the system. If, for example, there were 100 amplifiers, we would expect an MTBF of about 34 months.

The moral of the story is that heat is the implacable enemy of integrated circuits. In order to insure the system reliability, junction temperature must be minimized by every available means. This might mean putting a heat sink on the package or reducing the power supply voltages, or increasing the load resistance, or all of the above.

In summary, in order to calculate MTBF or FR in a system, we need to determine the device's average junction temperature in our system, obtain the Activation Energy and Failure Rate data from the vendor, calculate the Acceleration Factor for our specific application, and correct the failure rate for finite sample size at a Confidence Factor commensurate with the system's needs.

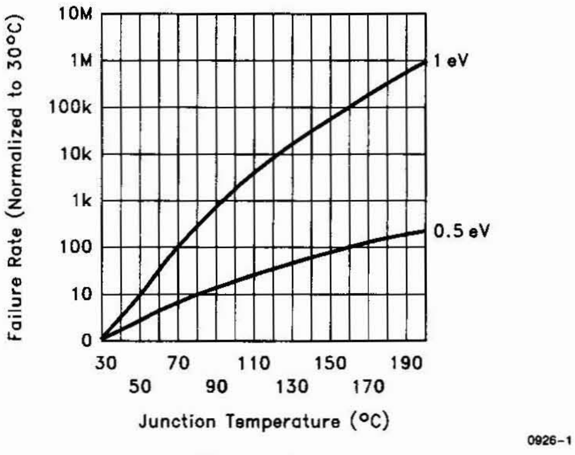

Figure 1

Activation Energy

Component and Mechanism	Reported EA (eV)	
	Main Population	Weak Population
Silicon Semiconductor Devices		
Silicon Oxide and Si/Sio2 Interface		
Surface Charge Accumulation, Bipolar	1.0	
Surface Charge Accumulation, MOS	1.2	
Slow Trapping Charge Injection	1.3–1.4	
Metalization		
Electro-Migration	0.5–1.2	
Corrosion (Chemical, Galvanic, Electrolytic)	0.3–0.6	
Bonds		
Intermediate Growth Al/Au	1.0	
N-Channel Si Gate Dynamic RAM		
Slow Trapping	1.0	
Contamination	1.4	1.4
Surface Charge	0.5–1.0	
Polarization	1.0	
Electro-Migration	1.0	
Oxide Defects	0.3	0.3
FAMOS Transistors		
Charge Loss	0.8	

Source: *Burn-In*, F. Jensen, N. Petersen, Wiley and Sons, New York, 1982

Figure 2

Device Type	Quantity	Failures	Hours	Device-Hours
EL2020CN	45	0	1,000	45,000
EL2020CN	45	0	1,000	45,000
EL2028J	105	1	1,000	105,000
EL2020J/883	105	0	1,000	105,000
EL2030CN	77	1	1,234	95,020
EL2033CN	105	0	1,000	105,000
EL2037CM	105	0	2,500	262,500
EL2190L/883	105	0	1,000	105,000
TOTALS	692	2	9,732	867,520

Figure 3. Partial Summary of Elantec Reliability Data

Poisson Distribution Table

X	Average = X!	3.12 P(X)	Sum (P(X))
0	1	0.044157	0.044157
1	1	0.137770	0.181927
2	2	0.214921	0.396849
3	6	0.223518	0.620367
4	24	0.184344	0.794712
5	120	0.108790	0.903503
6	720	0.056571	0.960074
7	5040	0.025214	0.985289
8	40320	0.009833	0.995123
9	362880	0.003409	0.998532
10	3628800	0.001063	0.999595
11	39916800	0.000301	0.999897
12	4.8E+08	0.000078	0.999975
13	6.2E+09	0.000018	0.999994
14	8.7E+10	0.000004	0.999998
15	1.3E+12	0.000000	0.999999

Figure 4

Number of Failures	50%	60%	70%	80%	90%	95%
0	0.693	0.916	1.204	1.990	2.305	2.990
1	1.678	2.022	2.439	2.990	3.890	4.740
2	2.674	3.120	3.615	4.280	5.300	6.300
3	3.672	4.160	4.762	5.500	6.700	7.750
4	4.671	5.250	5.891	6.700	8.000	9.150
5	5.970	6.300	7.005	7.900	9.250	10.50
6	6.669	7.350	8.111	9.100	10.55	11.85
7	7.669	8.400	9.209	10.25	11.75	13.15
8	8.669	9.450	10.30	11.40	13.00	14.45
9	9.668	10.50	11.38	12.50	14.20	15.70
10	10.66	11.55	12.47	13.65	15.40	16.95

Figure 5. Average Failures Confidence Level

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

High Frequency Amplifier Instability

High Frequency Amplifier Instability

by Barry L. Siegel

Introduction

High frequency amplifiers pose unique, often puzzling, and frustrating instability problems which can manifest themselves as oscillation, peaking, or overshoot. This paper will address the classic causes of instability starting with the Bode plot and phase margin. Problems unique to high frequency amplifiers will then be addressed covering input capacitance, load capacitance, power supply inductance and decoupling, the use of buffers in the feedback loop, the effects of source and feedback impedance on stability and settling time, and driving loads such as flash Analog-to-Digital converters.

Classical Instability

The classical cause of instability; i.e., the one we learned in school, was due to phase shift through the amplifier which results in a feedback phase of zero degrees "around the loop." Illustrated in Figure 1 is the Bode plot of an amplifier whose unity gain crossing frequency is about 100 MHz with a Phase Margin of about 45°. Phase margin is simply the difference between the output's phase lag relative to the input at unity gain and 180°. Since the op amp gives us 180° gratis, the circuit would oscillate under closed loop conditions if we somehow lost the 45°. The key thing to remember is that any loss of Phase Margin will result in peaking, overshoot, or degraded settling time. Figure 2 illustrates Normalized Gain for various Phase Margins for a single pole response system. For the purpose of our discussion, any departure from an ideal response of an amplifier which results in degraded settling time, overshoot, peaking, or oscillation will be called instability.

Buffers in the Feedback Loop

There are occasions when an open loop buffer is inserted within the feedback loop to drive heavy load currents or to isolate perturbations on the output from the input. The parameter to pay attention to is the phase shift of the buffer at a frequency equal to the unity gain crossing frequency of the amplifier. The reason, of course, is that the phase lag through the buffer may be sufficient to erode or eradicate the phase margin of the amplifier, and the net result is instability. The only solution, assuming that the bandwidth of the amplifier is mandatory, is to select a buffer with sufficient bandwidth and minimum phase lag, or to put the buffer outside of the loop.

Power Supply Decoupling

Unfortunately, in the real world of high speed amplifiers, there are many and often more dominant causes for instability. Illustrated in Figure 3 is an amplifier whose power supply leads exhibit significant self inductance. The time varying load current flowing through the supply inductance induces a voltage which is essentially in phase with the input. A vestige of this voltage can be coupled to the input through parasitic capacitance on the printed circuit board (or on the amplifier) which results in instability particularly if the source impedance is high.

The obvious solution is to decouple the power supply leads. The question is with what kind of capacitor. The answer is, in general, with a ceramic disc capacitor. A surprising aspect is that 0.01 μF capacitors actually do a better job than 0.1 μF in that the latter exhibits more self inductance. Chip capacitors reduce the inductance to a minimum and should always be used when the manufacturing process allows. Recently, Tantalum electrolytics have improved but tend to cost more and take up more space. In applications requiring large output currents, Tantalum electrolytics are mandatory, and a good rule of thumb is 4.7 μF per 100 milliampere. Clearly, both rails have to be bypassed, the capacitors placed as close to the package pins as possible, and must be terminated in the ground plane.

More often than not, the compensation capacitor on the chip uses one of the rails as "AC ground", and many amplifiers (and comparators) oscillate due to poor bypassing of the rails. Futhermore, the PSRR of most amplifiers is degraded at high frequency, and "system" noise will corrupt the signal.

Input Capacitance

The source impedance and any parasitic capacitance at the amplifier's input form a low pass filter and its attendant phase shift which can and will degrade the Phase Margin of the system. The change in Phase Margin is given by:

$$d\phi = \arctan(f_u/f_c) \qquad (1)$$

where f_u is the amplifier's unity gain crossing frequency and:

$$f_c = \frac{1}{2\pi(R_G \| R_F)(C_S)}$$

For the "simple" voltage follower of Figure 4 (C_S = 2 pF), the degradation in Phase Margin is 51°, which means that the 100 MHz amplifier of our earlier example would oscillate.

The feedback resistor, R_F, can be bypassed with a capacitor, but the optimum value is largely a function of parasitics and is always a low and non-standard number. The best solution is to keep the impedance levels as low as possible. Some amplifiers will require a small value for R_F when operated as a voltage follower. The issue in this instance is isolating the input capacitance from the output.

Current Feedback Amplifiers are simply a special case in that R_F is selected for bandwidth. The main issue here is minimizing capacitance at the inverting input.

Load Capacitance

A simple way looking at instability resulting from loading the amplifier with a capacitor is to assume that the open loop output impedance and the load create a low pass filter and its attendant phase shift akin to the problem created by input capacitance as shown in Figure 5. A formula similar to equation (1) results:

$$d\phi = \arctan(f_u/f_c) \qquad (2)$$

where f_u is the amplifier's unity gain crossing frequency and:

$$f_c = \frac{1}{2\pi(R_O)(C_L)}$$

R_O = The Amplifier's open loop output impedance

A better way is to realize that, to the first order, the output impedance of the amplifier behaves very much like an inductor. Most amplifiers employ class AB compound emitter follower output stages, and since hfe decreases as a function of frequency, R_O increases from 10Ω or 20Ω at low frequency to 100Ω or more at high frequency—precisely the behavior of an inductor. An inductor in parallel with a capacitor creates a tank circuit, and a tank circuit can and will oscillate. Whereas, this analysis is not rigorous, it does lend an intuitive insight to a straightforward technique for eliminating or minimizing load induced instability.

The technique employs the use of a "snubber"; i.e., a resistor in series with a capacitor from the amplifier's output to ground as illustrated in Figure 6. The obvious question is what value R and C should be used? The quickest answer can be obtained using an oscilloscope and operating the amplifier under conditions that it will see in the end application. The frequency of the "ring" in response to step input (or oscillation frequency) is observed, and R is calculated by:

$$R = \frac{1}{2\pi f C_L} \qquad (3)$$

where f is the "ring" frequency, and C_L is the load. The value for C should be made equal to C_L.

The values may have to be iterated somewhat to achieve optimum performance, but as illustrated in Figure 7, excellent results can be achieved in very short order. In this instance, the 100 MHz op amp can be tamed quite nicely using this technique.

High Frequency Amplifier Instability

Current feedback amplifiers offer a unique solution to this problem in that the bandwidth is determined by the feedback resistor. In this instance, R_F can be increased to a value sufficient to kill the instability but small enough to achieve the desired slew rate and bandwidth.

The classical technique is shown in Figure 8, which appears on many datasheets in applications in which the amplifier is used to drive the input (capacitance) of a flash A-to-D. The primary limitation of this approach is that 6.9 time constants will be required for the input to settle to 0.1%, and R is chosen to keep the amplifier from peaking. The net result is that the time constant and settling time may not be compatible with the required conversion time of the system. The "snubber", on the other hand, does not impact the settling time except to eliminate the peaking.

Ground Planes and Layout Considerations

There is, of course, no such thing as "ground" outside of the classroom. The use of ground planes is mandatory in high speed applications. It is frankly difficult to communicate the "art" involved in the design of good ground planes in a paper like this, but there are some general rules that we will discuss. Contrary to popular notion, the ground plane should be terminated in the vicinity of the inputs to minimize input capacitance. The ground plane is also selectively removed to prevent load and supply currents from flowing near the input nodes. At Elantec, we use ground planes on both sides of a test fixture which are selectively connected at various points on the printed circuit board.

We also make extensive use of semi-rigid coaxial cable to route signals to and from a device under test. Stripline techniques can also be employed, but take longer to develop. We "breadboard" critical applications using double-sided copper clad board, hand cutting the ground plane to achieve optimum performance. The final production fixture usually employs a gold plated pattern identical to the "breadboard" which we have found eliminates subtle parasitic changes. For example, one such series of boards which was developed for frequency domain testing is flat to under 0.1 dB at frequencies in excess of 500 MHz. In the final analysis, most manufacturers offer "demo boards" for use with their products, and they are an excellent platform to initiate breadboard testing and a basis for your artwork.

Component Selection

Let's eliminate one component right off the bat. Don't use a socket particularly for SO packages. If you are compelled to offer removability, use pin jacks for DIP packages.

As suggested earlier, chip capacitors and resistors are best for high frequency applications. Metal film construction may be mandated in some applications, and it is, therefore, very prudent to ascertain a given resistor's self-inductance on an impedance bridge before using in production. Clearly, an inductive resistor used as a gain setting resistor is an invitation to disaster. Carbon film resistors with their leads cut to $1/16$ of an inch exhibit excellent high frequency characteristics.

Oscilloscope Probes

We have no quarrel with probes, but they do require matching and calibration, exhibit fairly high input capacitance, and grounding is always a problem. For example, the Tektronix P6137 10 MΩ probe recommended for use with 2465 oscilloscope exhibits an input capacitance of about 12 pF which translates to 37Ω at 400 MHz. The first thing to do is to throw away the alligator clip. Chassis mounting probe tip jacks such as the Tektronix part number 131-0258-00 can be soldered directly to ground plane, or alternatively, the Tektronix 013-0084-01 probe tip adaptor can be used in conjunction with a standard BNC coaxial connector. Lastly, remember there can be bandwidth or rise time contraction which results from "RMS-ing" the probe and instruments bandwidths.

At Elantec, we tend to "roll your own" scope and network analyzer probes as illustrated in Figure 9. The mismatch created by the 450Ω resistor is minimal, tpd skew is much, much less than 1 ns for equal lengths of coax, any gain ratio can be used assuming that the amplifier can drive the impedance, and capacitive loading is minimal.

Diagnostics and Conclusion

The frequency at which an amplifier is oscillating or peaking can, ironically, be a clue as to the cause. For example, if the amplifier is oscillating at several hundred Megahertz, the odds on bet is that the output stage whose transistors exhibit ft's in that range is the problem. If the load is capacitive, a snubber may be in order. Power supply bypassing problems also result in oscillations (or ring frequencies) in that range. If the oscillation is detectable on the power supply, the bypassing is inadequate. On the other hand, if the problem is at or close to the gain-bandwidth product, loop oscillations caused by input capacitance or source impedances is the likely culprit.

High speed analog applications stripped of their mystery are no more difficult to design or troubleshoot than precision circuits, for example. Follow a few simple rules, and when all else fails, call the vendor's Applications department.

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3. Frederiksen, T. *Intuitive IC Op Amps*, National Semiconductor Technology Series, 1984

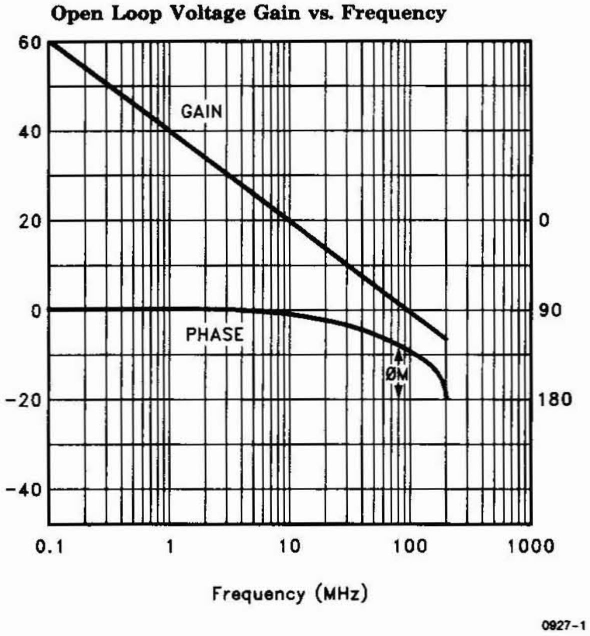

Figure 1. EL2041 Bode Plot

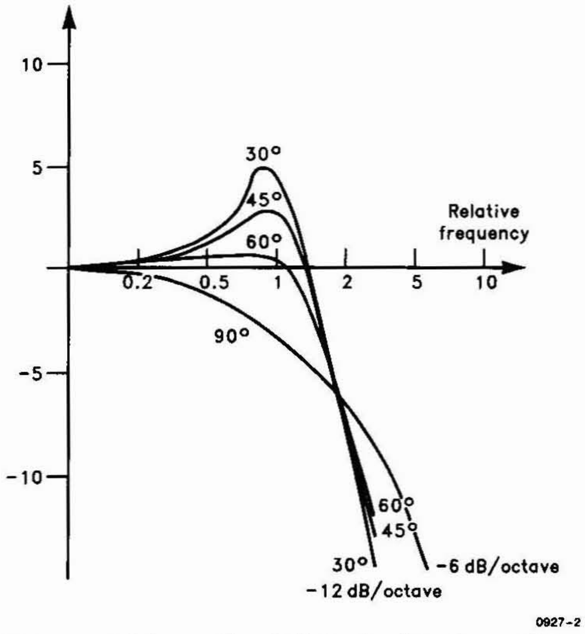

Figure 2. Normalized Gain for Various ϕM

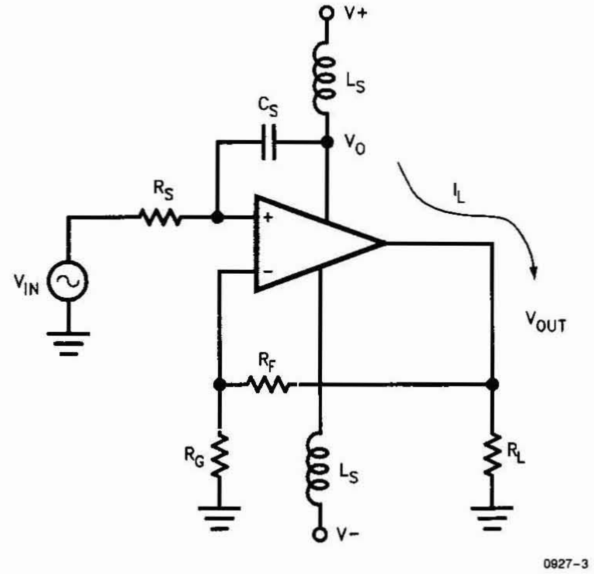
V+
L_S
C_S
V_O
I_L
R_S
+
−
V_{IN}
V_{OUT}
R_F
R_G
L_S
R_L
V−
0927-3

Figure 3. Power Supply Induced Oscillations

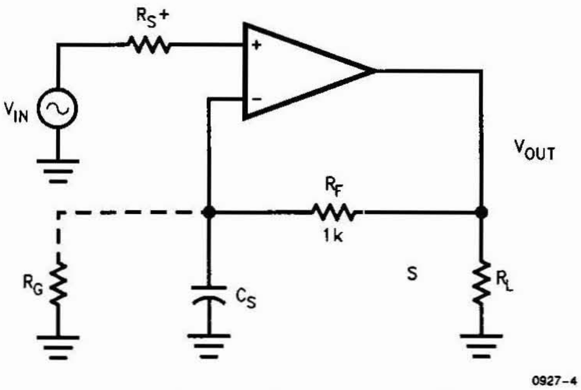
R_S+
+
−
V_{IN}
V_{OUT}
R_F
1k
R_G
C_S
S
R_L
0927-4

Figure 4. Source Impedance Effects

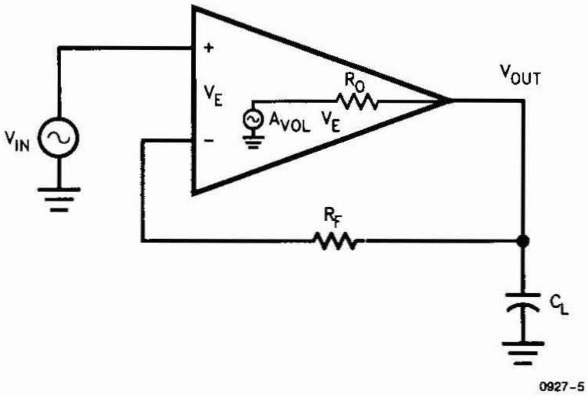
+
V_E
R_O
V_{OUT}
A_{VOL} V_E
V_{IN}
−
R_F
C_L
0927-5

Figure 5. Capacitive Loads

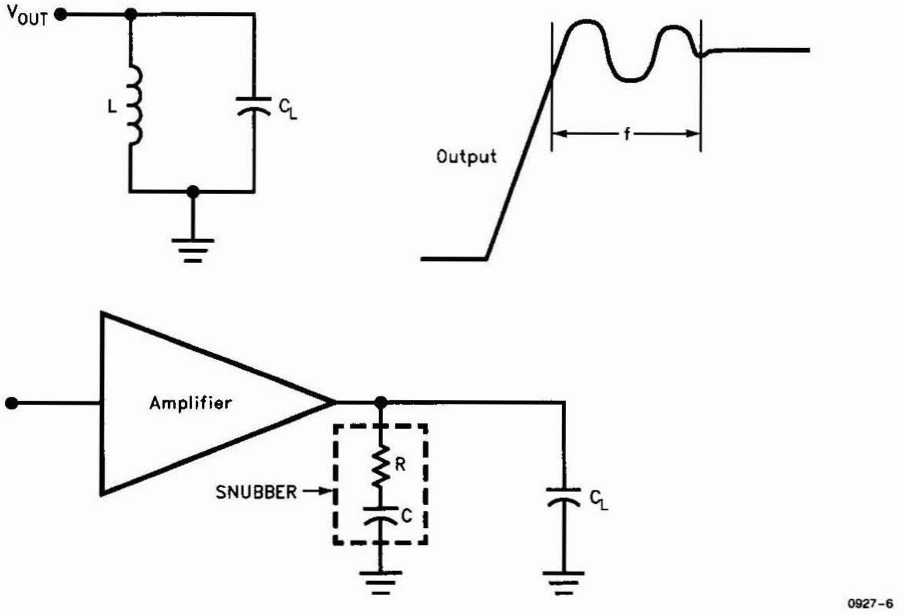
V_{OUT}
L
C_L
Output
f
Amplifier
R
SNUBBER
C
C_L
0927-6

Figure 6. Snubbers

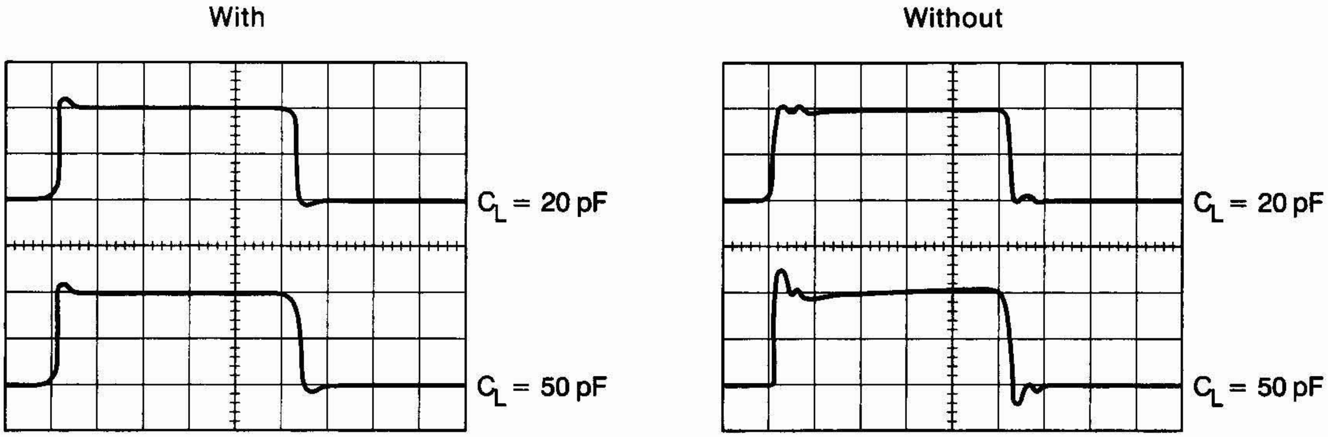

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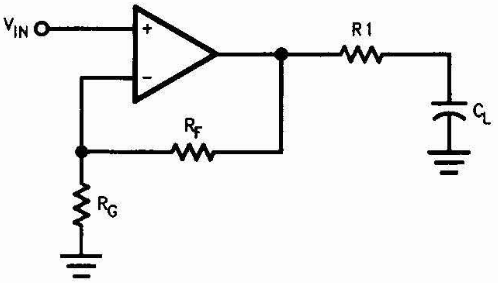
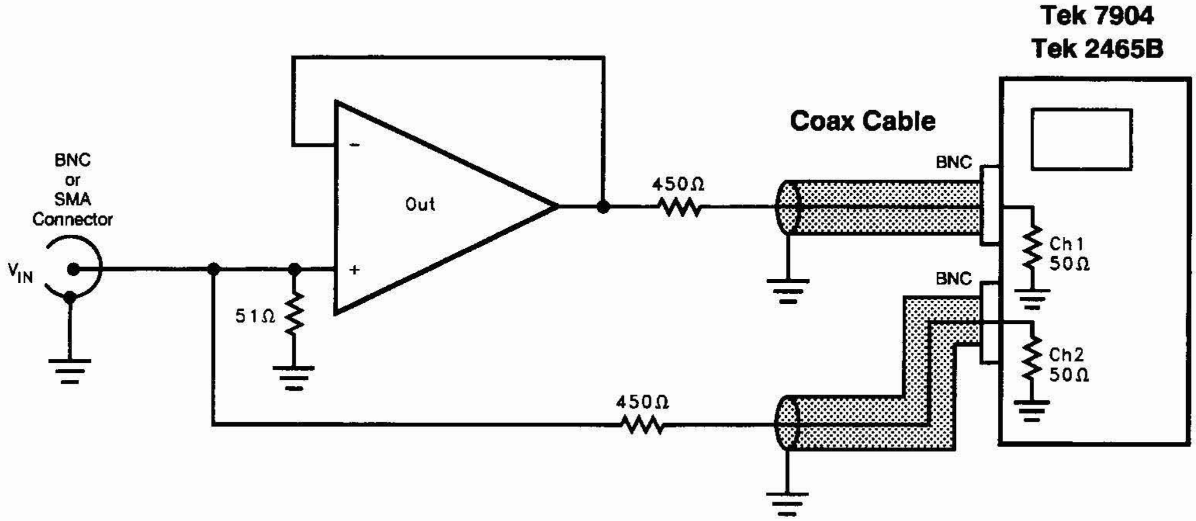
Figure 7. Response with and without a Snubber


V_{IN}
+
−
R1
C_L
R_F
R_G

0927-8

Figure 8. "Standard" Technique


Tek 7904
Tek 2465B
Coax Cable
BNC or SMA Connector
V_{IN}
−
+
Out
450Ω
51Ω
450Ω
BNC
BNC
Ch1 50Ω
Ch2 50Ω

0927-9

Equal Length Coax, L ≤ 1M

Figure 9. Make Your Own Oscilloscope Probe

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Practical Current Feedback Amplifier Design Considerations

Practical Current Feedback Amplifier Design Considerations

by Barry Harvey

The current-feedback (CMF) amplifier is a fundamentally different approach to high-frequency gain blocks. Not just an input stage, it is a full amplifier topology. It has outstanding characteristics in several areas: very high slewrates, −3 dB bandwidth which is almost constant with increasing circuit gain, and low high-frequency distortion. Almost all commercial CMF products offer these benefits, but, sadly they also exhibit limitations that are seldom publicized. This article is intended to point out the theoretical basis for the CMF amplifier's strengths and weaknesses, and some ways of coping with its problems.

Figure 1 shows the modern fundamental CMF circuit, with feedback applied through R_F to implement an operational voltage follower. Q1 through Q4 form a complementary buffer. The terminal called −Input is thus actually an output, a buffered replica of the voltage at +Input. Q3 and Q4 idle at a quiescent current proportional to the geometric mean of I1 and I2 and a scale factor dependent on the relative sizes of Q1 through Q4. When the feedback loop is at null, no error current will flow to the −Input, and Q3 and Q4 draw equal collector currents (we will ignore base current errors in this discussion). Q3's collector current is mirrored by Q8 and Q9 and delivered to the gain node. Q4's collector current is mirrored by Q5 and Q6 and sent to the gain node to balance against the previous mirrored current. Transistors Q11 through Q14 buffer the voltage at the gain node and present it as the output voltage.

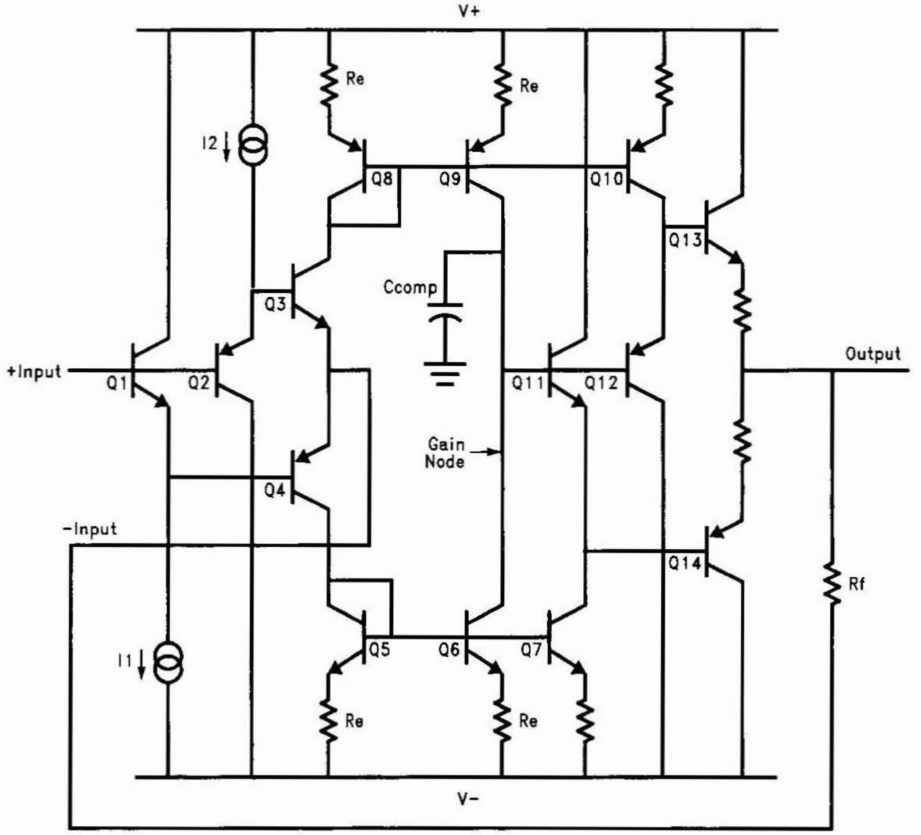

Figure 1. A Typical Current-Feedback Amplifier Connected as a Unity-Gain Follower

To understand the behavior of the circuit, imagine that the +Input and the output had been resting at zero volts and a one-volt positive step is delivered to the +Input. The input buffer Q1 through Q4 will very quickly replicate the step at the −Input terminal and the step voltage is thus impressed upon the feedback resistor R_F, since the output has not yet had time to move. Let us assume that R_F is 1 kΩ, a typical value. The one-volt step then will cause a transient one milliampere current to flow through R_F, increasing Q3's current by 500 μA and decreasing Q4's current by 500 μA. Q9's collector current will then increase by 500 μA and Q6's collector current will decrease by 500 μA, assuming the current mirrors have a gain of one. The milliampere of transient error current through R_F thus is transferred to the gain node of the amplifier and serves to slew the node positive, at a rate determined by C_{COMP}. The output, following the gain node, will move positive until equilibrium is reached where no current flows through R_F and currents to the gain node balance.

Slewrate

The output slewrate is the feedback current divided by C_{COMP}. If the input step were increased to two volts, twice the previous error current would flow through R_F and twice the slew current delivered to C_{COMP}, yielding twice the previous slewrate. Even if the error current through R_F exceeded the quiescent idle currents through Q3 and Q4, one of the two transistors would simply turn off and all error current would be delivered through the other transistor and associated current mirror in class A-B operation. In essence there is no slewrate limit in the conceptual CMF amplifier, and all step inputs produce the ideal single-pole exponential output response.

The high-frequency advantages of the CMF topology are manifold. The absence of slew limitation yields low distortion for large and high-frequency signals, even up to the normal small-signal bandwidth limitation. Since slew current is produced by the feedback error signal, the idle currents can be low without seriously affecting slew rate. And as we will see, the bandwidth is determined mainly by R_F and C_{COMP} and does not diminish rapidly with increasing closed-loop gain.

As in all circuits, there are limitations. We will consider time domain aberrations first. For increasingly large input steps and slewrates, the error current through R_F also increases. A fast 10V input step could produce a 10 mA peak error current, and this would not be supportable in many amplifiers. Typically, transistors in the current mirrors would saturate during the transient, causing slew and settling aberrations. Monolithic amplifiers support 500V/μs to 2000V/μs slewrates, but many devices display full-out step response that is "out of control". Saturation also occurs more readily at high temperatures, and takes longer to settle out, so amplifiers that seem to not exhibit saturation distortions at room temperature often do when hot.

The other slew distortion mechanism is input stage slew limitations. Q1 has an essentially unlimited positive slew capability, but its negative-going slewrate is limited by I1 and parasitic capacitance at Q1's emitter. Q2 similarly is not restricted in its negative-going slewrate, but I2 limits its positive slewrate. The result is that the replicated voltage presented at −Input is limited in each direction of slew by the respective current-source and parasitic capacitance. The maximum input slewrate might be less than the output slewrate (the slew allowed by the supportable error current from R_F mirrored to C_{COMP}), or it may be more. If the input slewrate is less than the output slewrate, −Input will "float" toward the new +Input voltage and the output will follow that slew-limited response.

Some CMF amplifier designs are simply not recommended for positive gain connections. These amplifiers are to be connected in inverting gain mode so that the +Input does not see signals at all. Their +Input is not a high impedance and does not offer good input slewrate.

This is the ultimate workaround to input stage limitations: connect the amplifier as an inverter.

This runs counter to most instrument designs, and as we will see, can often be inconvenient in many other ways. Fortunately, there are many CMF amplifier products designed to work well in the non-inverting mode.

Settling Behavior

With their large slewrates, one would expect the CMF amplifier to settle very quickly to high accuracies. This is only partly true; the CMF amplifier can settle very fast to moderate accuracies but displays large thermal settling tails. To see why this is true, consider the offset voltage between −Input and +Input. There is the difference of V_{be}(PNP) − V_{be}(NPN) at −Input relative to +Input. If we raise +Input by one volt, Q1 will dissipate less power since its V_{ce} was reduced, and V_{be}(NPN) will increase slightly as the transistor cools. Conversely, Q4 will gain a volt in V_{ce}, so its V_{be}(PNP) reduces as it warms. Unfortunately, the drift in V_{be}'s do not cancel. Note that these are *device* thermals; the device dissipates power just under its emitter in the collector region. The heat source is so physically small that it spreads and diminishes in a space smaller than the overall size of a transistor, and no device-to-device thermal coupling can be employed in an integrated layout to remove the effect.

To get an idea of the magnitude of the thermal settling errors, let us assume all transistors run at quiescent currents of 1 mA and that each device has a 70°C/W thermal coefficient. Each transistor changes dissipation by 1 mW, causing a 0.07°C temperature change. Since a silicon junction voltage changes by 1.7 mV/°C each device V_{be} changes 120 μV, for a total thermal error of 240 μV per volt of input. This 0.024% thermal error eliminates any concept of 0.01% settling, at least in positive-gain connections, and most CMF amplifiers are specified for 0.1% settling times instead. Figure 2 shows the settling response for an EL2020 to a 10V step in unity-gain connection. It settles very quickly to 0.1% bounds, 70 ns for a 10V step, but has a thermal input tail that pushes 0.01% settling much longer out.

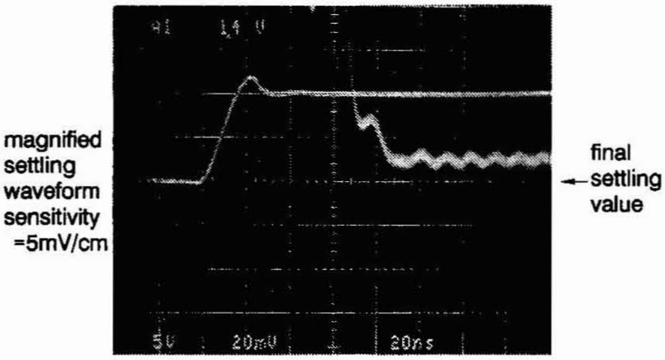

Figure 2. Short-Term Settling Characteristic of EL2020 (Unity Gain Mode)

Further settling aberrations can be generated as feedback current errors into the −Input terminal. The current errors are multiplied by R_F to contribute an output voltage error. Assuming the current mirrors have a unity gain, any current variation into the gain node has a direct contribution to the feedback error current. The main source of error current, as far as settling is concerned, is thermal error within the current mirrors. There are two popular topologies of CMF design where in one case the current mirrors add little to feedback current errors and in the other case their effect dominates all other settling errors. The simple two-transistor current mirrors Q5/Q6 and Q8/Q9 shown in Figure 3 is an example of the error-prone kind.

Settling Behavior — Contd.

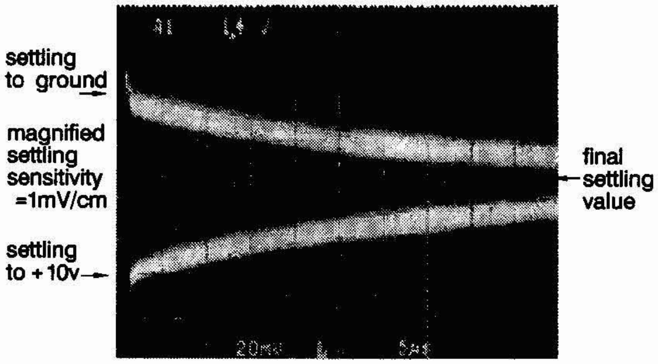

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Figure 3. Long-Term Settling Tail of EL2020 (Unity Gain Mode)

Let us assume that $R_F = 1\ k\Omega$ and $Re = 300\Omega$. Assume the gain node and output voltage move by one volt in response to a signal. Further assume that Q6 and Q9 have 1 mA quiescent current and have a 70°C/W thermal coefficient. As in the previous thermal calculation, the volt of V_{ce} change across the transistors will cause a 0.07°C temperature change in the device, for a V_{be} change of 120 μV. The diode-connected transistors Q5 and Q8 do not share in this temperature change, so the V_{be} change, divided by $Re = 300\Omega$, creates a 0.4 μA error into the gain node. This error is doubled and reflected as a current error into −Input. The 0.8 μA error, multiplied by $R_F = 1\ k\Omega$, yields an additional 0.08% thermal settling error.

This simple current mirror offers the widest bandwidth, greatest high-frequency linearity, most docile behavior for its bandwidth, and transient current capability, but much worse thermal errors than the more common Wilson type. Generally, CMF amplifiers whose transimpedance is greater than 150 kΩ have Wilson mirrors.

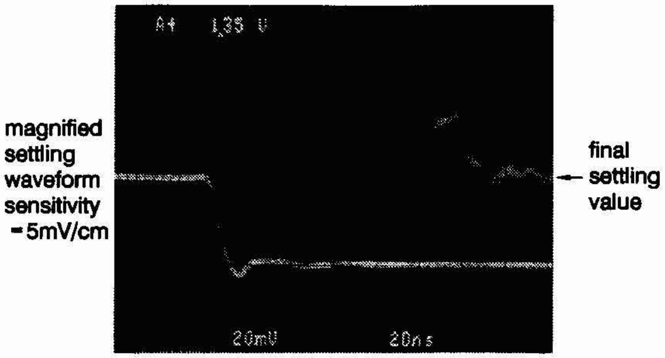

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Figure 4. Short-Term Settling Characteristic of EL2020 (Inverting Gain of −1)

Settling Behavior — Contd.

Figure 4 shows the settling response of the EL2020 connected in inverting mode (Av = −1). Because the input stage does not have to move with the signal, it does not add thermal error and only −Input error current limits settling quality. Although the 0.1% settling time is slowed to about 100 ns, the amplifier can now settle to 0.01% in 130 ns. As the figure shows, the settling tail reduced from the 0.024% size of Figure 2 to 0.007% in this connection.

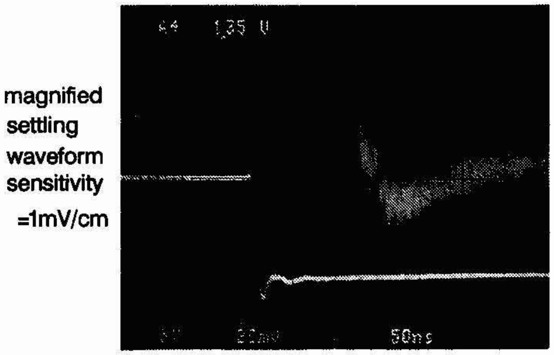

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Figure 5. Magnified Short-Term Settling Characteristic of EL2020 (Inverting Gain of −1)

In any event, the CMF amplifier is still prone to load-driving thermal feedback effects. The input and current mirror stages are very hard to place on an IC so as to completely reject temperature changes on the die emanating from the output transistors. In general, if quality settling or best DC accuracy is desired, the CMF amplifier should be loaded as lightly as possible. 50Ω or 75Ω systems are poor choices for moving quality settling signals; direct device-to-device connection is best to avoid load-induced thermals.

Ultimately, the CMF is not the best choice for very high-accuracy settling, although it excels in the 8–10-bit realm. At 12-bit accuracy and above, properly designed traditional voltage feedback amplifiers dominate.

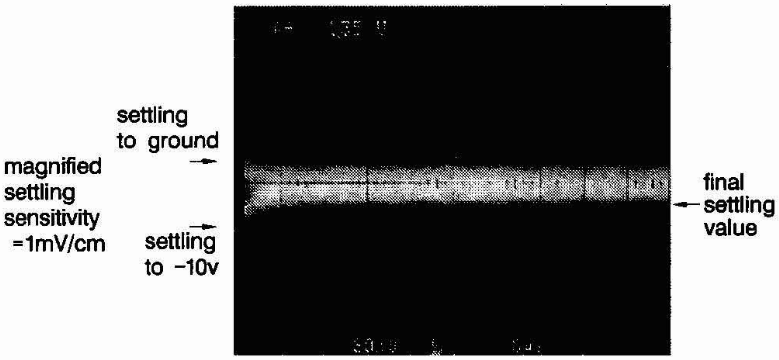

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Figure 6. Long-Term Settling Tail of EL2020 (Inverting Gain of −1)

Gain Accuracy

Figure 7 shows the small-signal macro-model of a CMF, used in positive-gain connection. The input buffer presents a copy of the +Input to the −Input terminal, but has an output impedance of R_{IN}^{-}. The dotted line emanating from the side of the input buffer represents a connection to a current source whose value is a copy of the current flowing into −Input. This current is applied to the gain node, which is loaded at DC by R_{OL} and over frequency by C_{COMP}, the compensation capacitor. The external gain-setting resistors are the previous R_F and an added R_G. Finally, C_{IN}^{-} is the external parasitic capacitance at the −Input terminal.

The ideal gain of the fed-back amplifier is:

$$\frac{V_O}{V_{IN}} = \frac{R_F + R_G}{R_G}$$

which we will term A_0.

The precise expression for the fed-back gain is

$$\frac{V_O}{V_{IN}} = A_0 * \frac{1}{1 + \dfrac{R_F + A_0 * R-}{R_{OL}}}$$

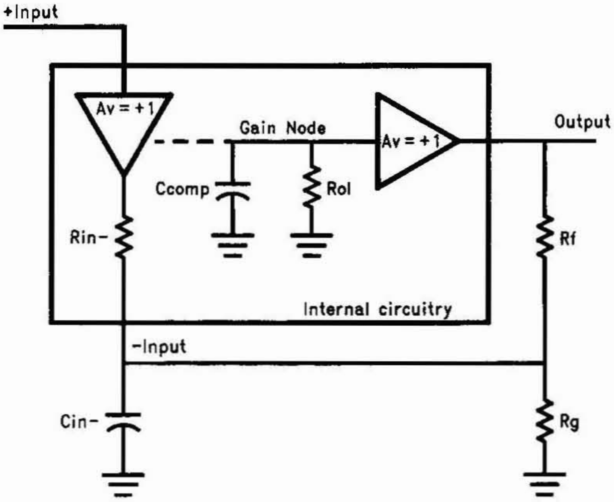

Figure 7. Small-Signal Equivalent Circuit of the Current-Feedback Amplifier

The added term is near unity since R_{OL} is a large number. This term is the gain accuracy expression as a function of amplifier characteristics and feedback resistors. The gain error can be approximated as

$$\text{Gain Error} = \frac{R_F + A_0 * R-}{R_{OL}}$$

There is no occurrence in the equations of A_{VOL}, the open-loop gain of the CMF amplifier. Actually, A_{VOL} is an "imaginary" parameter which is a holdover from voltage-feedback days and has no meaning with respect to the CMF amplifier. Unfortunately, few data sheets offer R−. R− can be estimated as

$$R- = \frac{R_{OL}}{A_{VOL}}$$

Gain Accuracy — Contd.

This is mathematically exact, but the typical R_{OL} and A_{VOL} numbers offered in data sheets may not give precise estimates of R−. For CMF amplifiers drawing supply currents around 16 mA, R− ranges from 10Ω to 25Ω; for lower currents around 8 mA, R− typically increases to 50Ω. Using $R_{OL} = 1\ M\Omega$, $R- = 50\Omega$, and $R_F = 1\ k\Omega$, the gain error is 0.105% for unity fed-back gain and increases rapidly beyond a gain of 20. This is a key consideration in the CMF amplifier: gain accuracy is seldom as good as in most voltage-feedback amplifiers.

Furthermore, gain accuracy reduces with heavy output loading since the output buffer reflects the load as a reduction in R_{OL}. The CMF is seldom used for closed-loop gains of more than 50, since amplifier gain and the value of R_G become too small to retain gain accuracy.

On the other hand, the gain accuracy did not reduce appreciably between the closed-loop gains of 1 and 10. This gain range is the "sweet range" of CMF amplifiers. Note that this relatively limited gain accuracy does not suggest a non-linear situation; the CMF is much more linear open-loop than voltage-feedback amplifiers and does not rely on massive voltage gain to be linear in feedback.

This discussion of gain accuracy was based on open-loop gain; there are three subtle aberrations that make this value optimistic. The first effect is the input common-mode rejection ratio, or CMRR. This effect places an offset on −Input proportional to the signal level on the +Input terminal. The offset is indistinguishable from an input signal, and in non-inverting gain configuration creates a gain error. The typical CMRR for the CMF amplifier is 50 dB to 60 dB, so that gain error can be as poor as 0.3%.

The second gain error is due to voltage sensitivity in the −Input terminal's bias current. As the +Input terminal voltage moves with signal, early errors between Q3 and Q4 modulate their alphas and thus mismatch their quiescent collector currents. The mismatch in currents must be made up for as −Input bias current variation. The term for this effect is −ICMR. A −ICMR error, multiplied by R_F, creates an output error similar to CMRR errors. −ICMR quantities range from 0.2 μA/V to 10 μA/V. In our CMF amplifier example −ICMR would be around 1 μA/V. Using a 1 kΩ feedback resistor would create an output error of 1 mV/V, indistinguishable from a 60 dB CMRR input error in unity gain connection. The −ICMR error is an output error, and reduces in input effect as the overall fed-back gain is increased. For instance, a gain of +10 causes −ICMR errors to be ten times less significant.

The third such error source is the thermal settling error previously discussed. At frequencies below 1 kHz, the settling error is indistinguishable from CMRR or open-loop gain limitations. At frequencies above 100 kHz, however, thermal time responses are too slow to make appreciable errors, and gain accuracy can actually improve. The amplifiers will show a small drop in gain below these frequencies and a small increase in gain above. The variation in gain is about the same magnitude as the settling tail. Thus, the better-settling CMF amplifiers will show thermal errors too small to affect overall gain accuracy over (low) frequency, while the poorest-settling amplifiers can display as much as a 0.2% gain bump in mid-band frequencies.

Frequency Response

For the best gain accuracy, therefore, the inverting connection should be used. Ideal frequency response is calculated by inserting C_{COMP} in parallel with R_{OL}:

$$\frac{V_O}{V_{IN}} = A_0 * \frac{R_{OL}}{(R_{OL} + R_F + A_0 * R-) + s\,C_{COMP}\,R_{OL}\,(R_F + A_0 * R-)}$$

Frequency Response — Contd.

The −3dB bandwidth of this expression occurs at a frequency of

$$F_0 = \frac{1}{2\pi C_{COMP}(R_F + A_0 * R-)} * \frac{R_{OL} + R_F + A_0 * R-}{R_{OL}}.$$

The term on the right is quite close to unity for any CMF application and will be ignored. Since $A_0 * R-$ is usually much less than R_F, R_F dominates the expression for bandwidth over a wide range of closed-loop gain. This gives a bandwidth relatively independent of gain (or R_G), a major advantage for the CMF amplifier. The bandwidth falls to ½ of maximum when the gain is equal to $R_F/R-$, or 20 in our example.

This first-order analysis ignores the effect of C_{IN}^- and is an expression of what we will refer to as the "natural bandwidth" of the CMF amplifier. We will use the term natural instead of dominant pole because the pole is not completely dominant in every CMF design. The effect of C_{IN}^- is to insert a secondary pole in the frequency response of the circuit. This secondary pole usually coincides with the output resonance of both the input and the output buffers, and the overall frequency response is further complicated by phase delays in the current mirrors.

Figure 8 is a simulation of the frequency response of the idealized circuit of Figure 7 at unity gain with a variety of C_{IN}^- values, for a C_{COMP} of 3 pF. With a C_{IN}^- of zero, the frequency response is single-pole in nature and the −3dB bandwidth coincides with the "natural bandwidth". With increasing C_{IN}^-, a high-frequency zero is introduced which tends to maintain gain over frequency. At a gain of +1, the zero caused by $C_{IN}^- = C_{COMP}$ would potentially cancel the pole caused by C_{COMP} itself. Unfortunately, nature is not so generous and this is an unattainable trick.

Figure 9 shows the effect of C_{IN}^- on a realistic CMF model. The current mirrors and output stage were modeled as having 200 MHz single-pole bandwidths each, a realistic value in our example where the natural bandwidth is 50 MHz. The limited bandwidths of the mirrors and output stage cause C_{IN}^- to produce different abberations. C_{IN}^- still causes the bandwidth to expand, but at the expense of peaking. Peaking causes undesirable ringing in transient responses, and about 2dB of peaking is generally a gracious maximum. Only about 2.5 pF of C_{IN}^- can be tolerated for 2dB of peaking in our example, and this is a practical value. However, R_F and R_G must be connected directly to the −Input pin on the package to maintain so small a parasitic capacitance, and a socket is probably too capacitive to use.

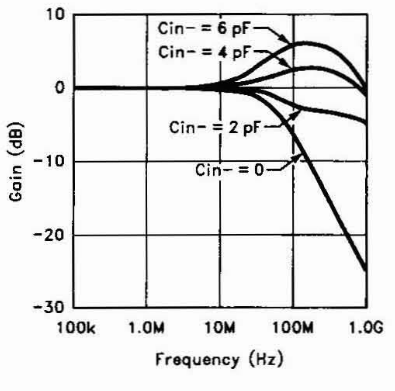

Figure 8. Ideal CMF Response with Various Values of C_{IN}

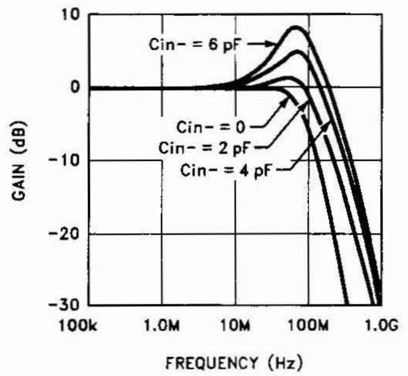

Figure 9. Realistic CMF Response with Various Values of C_{IN}^-

Settling Behavior

The small tolerated values of C_{IN}^- scale with the effective C_{COMP} of the CMF amplifier. Higher values of feedback resistor require smaller C_{COMP} for a given natural bandwidth and thus less C_{IN}^- can be tolerated. Since 1.5 pF is a minimum practical value for the parasitic C_{IN}^-, almost no CMF designs use R_F values greater than 1.3 kΩ. Higher frequency amplifiers use R_F values around 300Ω to mitigate the C_{IN}^- problem.

As shown in Figure 9, our natural bandwidth of 50 MHz was expanded to a −3dB frequency of over 100 MHz. This design is typical for the moderate supply current devices; there is not enough quiescent current to maximize the current mirror and output stage bandwidths. Higher supply current amplifiers or amplifiers built from very high-frequency IC processes have more bandwidth in the mirrors and output stage and display less peaking for a given bandwidth and give more reproducible frequency responses. Our definition of "moderate" supply current will again be CMF amplifiers that draw about 8 mA–10 mA; optimized amplifiers draw around 16 mA.

The ratio of −3dB frequency to natural bandwidth is an interesting number. In high frequency circuits it is always greater than unity. The closer to unity this "Bandwidth Expansion" ratio is, the better-behaved the amplifier. That is, a ratio close to one makes the CMF more tolerant to C_{IN}^- and varying values of R_F, and it also makes the −3dB bandwidth at higher gains maximized. If the bandwidth ratio is high, say around 2, then the natural bandwidth of the amplifier is substantially lower than the unity-gain −3dB frequency, and the peaking which caused a −3dB bandwidth increase at unity gain fades and allows the more modest natural bandwidth to dominate the higher gains. Figure 11 shows this effect. The higher gains do not show peaking and the ideal bandwidth loss-vs.-gain relationship holds.

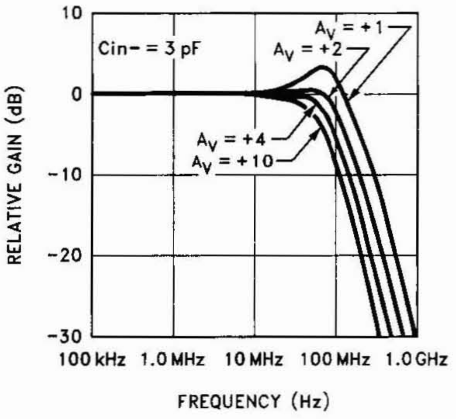

Figure 10. Realistic CMF Response with Various Closed-Loop Gains

The higher-gain bandwidths can be made closer to the unity-gain −3dB frequency by reducing R_F. The strategy is to make the quantity $R_F + A_0 * R-$ constant by reducing R_F as A_0 increases. In our example, the natural bandwidth was based on $R_F + A_0 * R- = 1050\Omega$. At a gain of +10, we could reduce R_F to 550Ω and obtain maximum −3 dB bandwidth

The Inverting Connection

When the CMF amplifier is configured as an inverting operational amplifier, as shown in Figure 11, the ideal gain in this configuration is

$$\frac{V_O}{V_{IN}} = -\frac{R_F}{R_G}$$

which we will term $-A_0$.

The precise expression for the fed-back gain is

$$\frac{V_O}{V_{IN}} = -A_0 * \frac{1}{1 + \frac{R_F + (A_0 + 1) * R-}{R_{OL}}}.$$

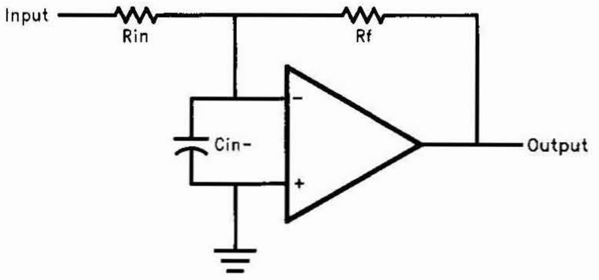

Figure 11. The CMF Connected as an Inverting Amplifier

The Inverting Connection — Contd.

The ideal gain error is close to that of the non-inverting case, and the ideal bandwidth also almost the same, with the A_0 term replaced by $(A_0 + 1)$. Because the amplifier inputs remain near ground as signals are passed, CMRR and −ICMR errors do not occur, and the ideal gain terms are maintained.

The inverting connection's input impedance is essentially R_{IN}. With $R_F = 1\ k\Omega$, a practical maximum gain for the inverting connection is about −20, since the input impedance drops to 50Ω. Even if the signal source could comfortably drive very low input impedances, simple interconnect inductances reduce bandwidths beyond 100 MHz. The practical maximum gain is even less for CMF amplifiers that use lower value feedback resistors.

Another virtue of the inverting connection is that the sensitivity to C_{IN}^- is substantially reduced. The inverting input is a virtual ground for low frequencies, and is a naturally low impedance R− at medium and high frequencies. Thus, the signal magnitudes are low at the inverting input and little current will flow into a C_{IN}^- to upset the ideal frequency response. Figure 12 shows our previous realistic CMF amplifier model's frequency responses with various values of C_{IN}^-. Note the reduced peaking from C_{IN}^-. With the flatter frequency response, the 0.1dB bandwidth improves, since the gain does not peak up and out of the ±0.1dB bound, as does the response of the non-inverting connection due to C_{IN}^-. The −3dB bandwidth is usually less than that of the non-inverting connection because of the diminished peaking.

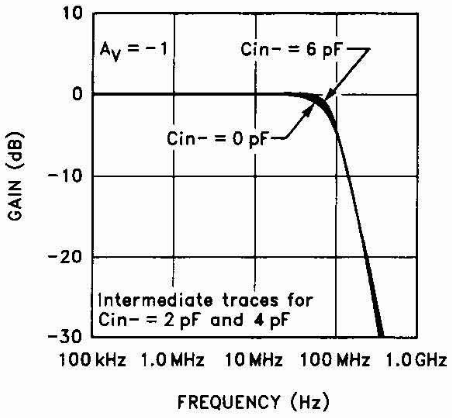

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Figure 12. Inverting CMF Response with Various Values of $C_{IN}-$

It must be remembered that the input and output impedances of the integrated amplifiers are quite complex over frequency. The terminals themselves can exhibit resonances with connected impedances independent of feedback. These resonances will be exhibited generally between one and five times the natural bandwidth of the CMF amplifier. For instance, few amplifiers tolerate load capacitance well. Those that can tolerate capacitive loading are designed to simply "wimp out" at high frequencies and lose gain accuracy and load-driving capacity. Many amplifiers do not like to see inductive or high input impedances, and some amplifiers built with very high-frequency processes resonate with $C_{IN}-$ even in the inverting mode. This term "resonance" can mean oscillation.

Noise

Noise performance of the CMF amplifier is characterized by four quantities, as shown in Figure 13. There is the typical input voltage noise V_n, generally placed in series with the +in terminal, the noises generated by R_F and R_G, and a noise current i_n which is peculiar to CMF amplifiers. This noise current is represented as being sent to the −in terminal from internal sources.

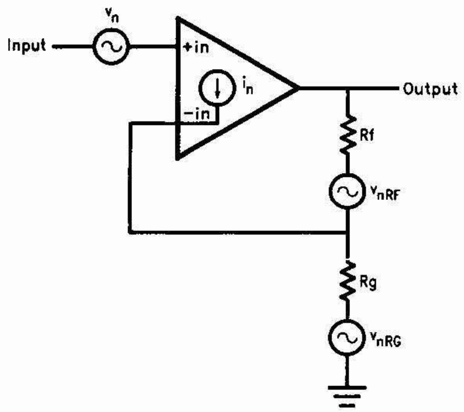

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Figure 13. Noise Sources in a Positive-Gain CMF Amplifier

Noise — Contd.

For positive-gain connections, the noise contributions are so:

$$v_{in,total}^2 = v_n^2 + \left(\frac{4\,K\,T\,R_F}{A_V^2}\right) + \left(\frac{4\,K\,T\,R_G\,(A_V - 1)^2}{A_V^2}\right) + \left(\frac{i_{in}\,R_F}{A_V}\right)^2$$

Input-referred noise is in volts-squared per hertz here. K is the Boltzmann constant, and T is absolute temperature. The noise terms are, left to right, the −Input noise current, R_F resistor noise, R_G resistor noise, and input noise current. Note that all noise contributors except the input voltage noise itself reduce in magnitude as the gain A_V increases. Since R_G can be expressed in terms of R_F and A_v, we can simplify the expression:

$$v_{in,total}^2 = v_n^2 + \left(\frac{4\,K\,T\,R_F}{A_V}\right) + \left(\frac{i_n\,R_F}{A_V}\right)^2$$

CMF amplifiers have low values of v_n, ranging from 2 nV/$\sqrt{hz}$ to 8 nV/$\sqrt{hz}$. A 1 kΩ resistor has a thermal noise of 4 nV/$\sqrt{hz}$, a value that can be neglected at even modest gains. The current noise has values ranging from 10 pA/$\sqrt{hz}$ to 40 pA/$\sqrt{hz}$. A CMF amplifier designed to use a 1 kΩ feedback resistor would convert a typical 20 pA/$\sqrt{hz}$ noise current to a 20 nV/$\sqrt{hz}$ voltage, the largest term in the expression until A_V is greater than about 3.

Figure 14 shows the input-referred noise versus A_V for two CMF designs. One amplifier uses a 1 kΩ feedback resistor, and has a 6 nV/$\sqrt{hz}$ input noise. The other is designed for a 250Ω feedback resistor and has a 4 nV/$\sqrt{hz}$ input noise. Both amplifiers have a 20 pA/$\sqrt{hz}$ noise current. The first amplifier is typical of lower-power designs; the second typical of the fastest designs. Clearly, the higher supply-current amplifiers that use low-value feedback resistors are the quietest.

At low frequencies, in the audio region, v_n and i_n have 1/F excess noise. For v_n, the 1/F corner is typically around 200 Hz. For i_n, it is typically at 2000 Hz. These 1/F extra noise quantities do not typically increase the total integrated noise voltage much, due to the large bandwidth beyond the audio frequencies that the CMF amplifier has to accumulate thermal noise over, but they do prevent instrumentation-quality DC performance.

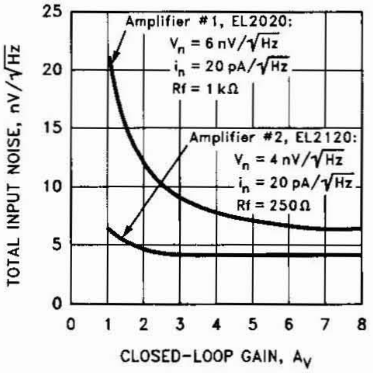


Figure 14. Noise vs Gain for Two CMF Amplifiers

Summary

The CMF amplifier has virtues unavailable in the traditional voltage-feedback design and it also has its own weaknesses. Enough variety exists among CMF products so that attention to individual amplifier characteristics is required to assure optimum circuit performance.

Dielectric Isolation

Introduction

In an integrated circuit, the individual transistors must be isolated from each other for correct circuit operation. In most IC processes, this is done by using reverse biased PN junctions and the technology is referred to as junction isolation (J.I.). The degree of isolation is limited by collector-substrate leakage currents and voltage modulated collector-substrate capacitance. An ideal isolation technology would not have leakage and capacitive coupling between devices.

Elantec uses a Dielectric Isolation (D.I.) bipolar process which differs radically from conventional bipolar J.I. processes in that the individual transistors are electrically isolated from their neighbors by a layer of glass. With the Elantec D.I. process, a layer of glass (SiO_2) surrounds the transistors on all four sides and the bottom. This totally isolates the individual transistors and provides essentially ideal isolation.

Dielectric Isolation (D.I.) is a way of building monolithic integrated circuits which have performance that rivals a multi-chip hybrid.

Elantec D.I. Process

Elantec uses D.I. to make both NPN transistors and PNP transistors in a high frequency vertical structure as shown in the figure. There are two collector, two base, and two emitter diffusions. Therefore, each transistor type can be optimized without compromising its complement. In analog circuit design, both NPN and PNP transistors are in the signal path. Thus the slower of the two transistors determines the overall circuit speed limitations. Most J.I. processes use lateral structure PNP transistors which have speed characteristics (f_t) that are 50 to 100 times slower than the NPNs. Thus most J.I. processes are 50 to 100 times slower than Elantec's D.I. process.

D.I. also has the capability of operating at a given high frequency with lower power consumption than conventional bipolar processes of similar geometry due to the reduced collector-substrate capacitance. These stray capacitances require extra supply current to charge them, supply current that is otherwise unnecessary in the circuit. Collector to substrate capacitances in D.I. are about one-tenth of those in J.I.

D.I. is an isolation technique and as such is a process technology platform which may be used as a starting point in more esoteric process development. Elantec's advanced D.I. process today uses implanted resistors, MOS capacitors, and Schottky diodes in addition to high performance, totally implanted complementary transistors. Other elements may be added such as BiFETS and thin film resistors. CMOS or even combined CMOS and bipolar (BiCMOS) can be implemented on D.I. In all cases, the D.I. lend its superb isolation, low leakage, and high-speed characteristics to the process.

Elantec's patented D.I. technology has been improved substantially from the original process. Performance and device density have been increased resulting in costs equaling that of standard J.I. Elantec's latest process has NPN and PNP Ft's of 4 GHz at 40 V, 2 micron CMOS and very low defect density.

D.I. Benefits

Speed

Speed is improved in D.I. integrated circuits for two reasons. First, since the collector substrate capacitance is smaller than J.I. by a factor of 10, the slew rate of an internal node can be 10 times as fast as the same node in J.I., using the same amount of current. Second, it is very difficult to build fast vertical PNP transitors with J.I., so most J.I. circuits settle for using a lateral PNP transistor somewhere in the signal path. With D.I., fully isolated fast vertical PNP and NPN transistors can be made on the same chip, and therefore performance need not be compromised by a slow transistor.

Temperature Performance

All junctions have leakage currents directly impacted by temperature. Higher temperatures create higher leakages. Many integrated circuits stop working if stray leakages between adjacent transistors are too high. Thus at high temperatures, these I.C.s cease working. With D.I., the high temperature leakages between adjacent transistors do not exist and the circuit can continue to work at high temperatures. Applications such as oil wells, where the temperatures may reach 200°C, are prime examples where D.I. is necessary for its temperature characteristics.

Radiation Hardness

The same leakages affected by temperature are also affected by radiation. The radiation may be from either a nuclear event or from deep space radiation. Because the D.I. glass layer is unaffected by radiation, the performance of D.I. circuits in the presence of radiation makes D.I. the mandatory technology for many military applications.

Freedom From Latch-up

Many J.I. devices are prone to latch-up. That is, under some external conditions the circuit will become stuck in a particular internal condition and will not function properly until the power is removed. Sometimes the circuit will self destruct due to latch-up. A key factor in this latch-up is the participation of the isolation junction in the circuitry that creates a parasitic SCR (Silicon Controlled Rectifier). In D.I., since there is no isolation junction, there can be no latch-up.

Elantec D.I. Advantages Over J.I.

- Speed

—Fast (vertical) PNP's and NPN's

—Lower Collector to substrate capacitance

—Collector to substrate capacitance not modulated by collector voltage

- No Possibility of Circuit Latch-up via Parasitic SCR's

—No parasitic devices with D.I.

- Operates in High Temperature and Radiation Environments

—Leakage currents are blocked by D.I. walls

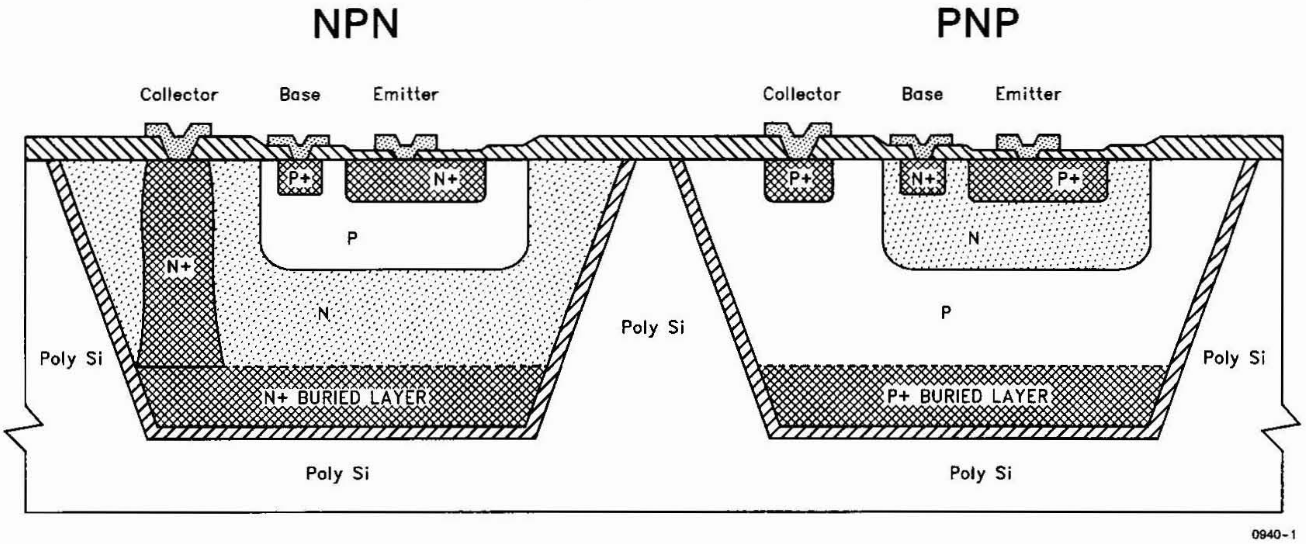
- High Voltage Operation

—Device to device breakdown >2000 V

- Mixed Technologies on Same Chip

—Bipolar transistors, diffused resistors and MOS can be done on the same monolithic chip

Elantec Complimentary D.I. Process



Applying Power MOSFET Drivers

by Bruce Rosenthal

Overview

The EL7xxx series of high speed power MOSFET drivers achieve noteworthy improvements in speed, efficiency, input impedance, and functionality thru the application of advanced CMOS technology and novel circuit design. However, their ability to deliver high peak currents with rapid d_V/d_T's makes them susceptible to over stress. Recommended design practices will be discussed to assist the designer in achieving reliable operation.

Common Causes Resulting in MOSFET Driver Problems

Cause 1

CMOS Latch-up: Inherent to CMOS integrated circuitry, is a parasitic SCR which can be triggered by injecting current thru any input or output pad. This occurs whenever the input/output pins exceed the supply rails by more than 0.6V. This condition may exist for any one of the following reasons.

1. During the power up/power down sequence, when voltage is applied to an input without supply voltage.
2. Ground or V_{DD} "bounce" (relative to the input) during switching. This is often attributed to inductance in the current path.
3. Inductive kick-back from the output load.

Cause 2

Over-Voltage Spikes: Power line spikes will occur when a rapid change in current (typical during switching) is present on an inductive supply line. Exceeding the maximum supply voltage can rupture the internal transistor gate oxide, causing catastrophic failure.

Cause 3

Insufficient Overdrive: During switching, some ground bounce is going to occur. If the ground bounce is greater than the overdrive to the input, oscillation may result as the effective drive to the input is modulated. Since the typical input delay is only 20 ns, a slowly rising drive waveform will still be very close to the threshold when the output switches. The ensuing ground bounce may be enough to toggle the input.

Cause 4

Thermal Overload: The high peak drive capability of the Elantec power MOSFET drivers, far exceeds their continuous rating. Limited by the high thermal resistance associated with PDIP and SOIC packages, junction temperatures can exceed the 125°C rated maximum. Users should be aware of those factors which contribute to the total power dissipated, including quiescent current, conduction losses, and switching losses.

Guidelines for Improved Operation

The most important thing to remember in applying CMOS drivers is to minimize inductance to the power pins as illustrated in Figure 1.

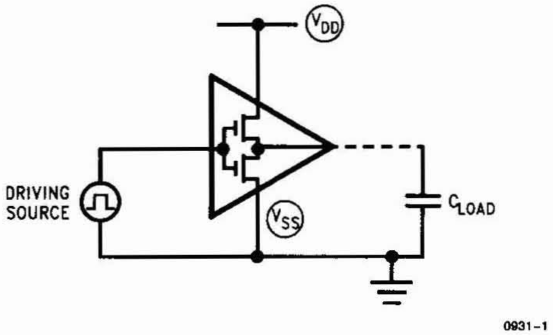


Figure 1. Trouble Prone Configuration

Guidelines for Improved Operation — Contd.

To prevent CMOS latch-up restrict the inputs/outputs from exceeding the power rails. This may require the use of clamping diodes, output snubbers, power supply bypassing and decoupling. Effective bypassing requires a minimum path length between capacitor and supply pins. Choose a capacitor with good high frequency characteristics, such as ceramic and/or tantalum construction. Refer to Figure 2.

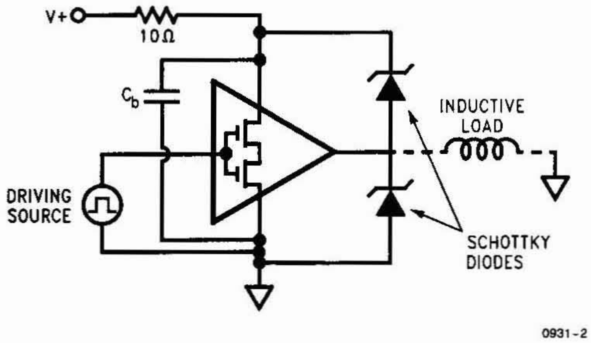
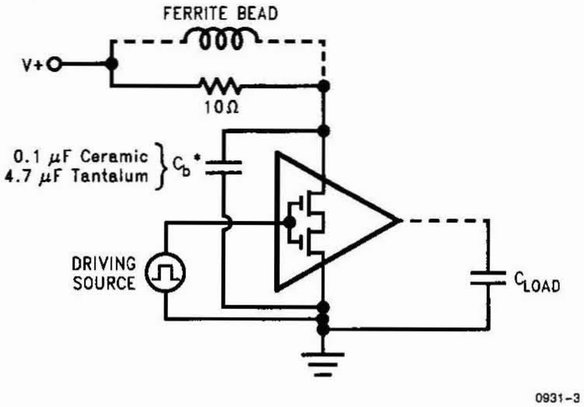


Figure 2. Suggested Configuration for Driving Inductive Loads

Overvoltage spikes can be controlled with decoupling. A small resistor (10Ω) from the supply, or a ferrite bead, followed by a 4.7 μF tantalum capacitor with short leads to the power pins is very effective. The suggested configuration is shown in Figure 3.



*C_b should be physically located close to the power pins.

Figure 3. Suggested Decoupling/Bypassing

Sensitivity to insufficient drive is most pronounced at supply voltages greater than 12V due to the higher internal peak currents. Where high supply voltage operation is required, 0V to 5V input drive is suggested, with a minimum rise/fall time of 200 ns.

Excessive power dissipation typically results when driving large capacitive loads at high frequencies. These losses are described by:

$$P = CV^2F \quad \text{where}$$

P = Power
C = Capacitance (Internal and External)
V = Supply Voltage
F = Clock Frequency

Internal dissipation can be reduced by adding an external resistor or inductor, as shown in Figure 4. Also, since the power varies as the square of the voltage, a reduction in supply voltage from 15V to 12V results in a 33% power savings.

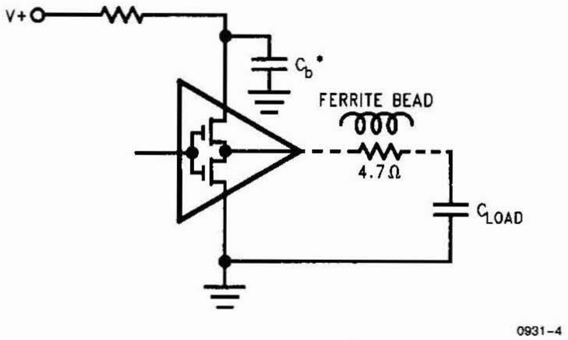


Figure 4. Reducing CV^2F Losses

A High Speed Differential Analog to Digital Converter Driver

Introduction

A class of Analog to Digital Converters require closely matched differential inputs in terms of amplitude and phase. At the same time, it is also important to provide input signals that exhibit distortion levels that are at least −60 dB down from nominal inputs of nominal 1V at frequencies in excess of 25 MHz. A to D's which run on a single 5V supply can be damaged or misbehave if the input range is exceeded. The circuit of Figure 1 satisfies these diverse requirements.

Circuit Description

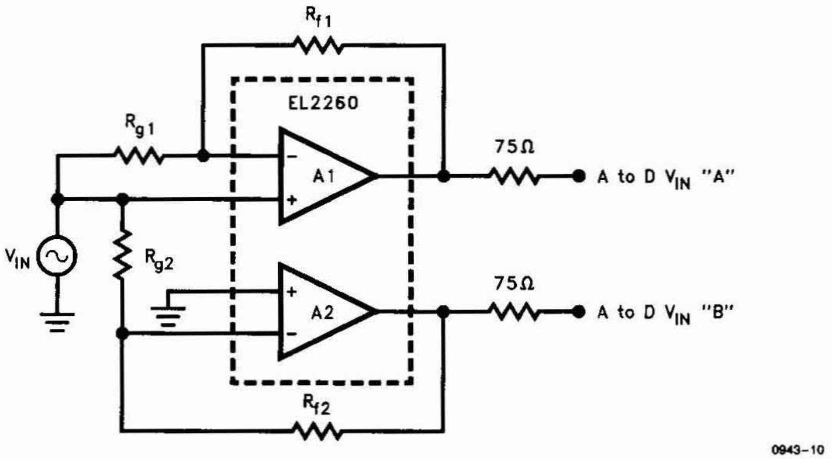
A1, one half of an EL2260 (Dual Current Feedback Amplifier—CFA) is operated as a non-inverting gain of 2 amplifier, while A2 is connected for an inverting gain of 2. The bandwidths of these current feedback amplifiers are adjusted with R_{f1} and R_{f2} with the (noise) gains set by R_{g1} and R_{g2}. The outputs are terminated in 75Ω allowing the circuit to drive a remotely located A to D through coaxial cable or isolating the outputs from the capacitive loads of the converter. Operating the EL2260 from ±5V supplies ensures that the input signals will not exceed the requirements of the A to D converter while using a dual CFA ensures close matching of the AC characteristics of the driver.

Performance Results

The circuit of Figure 1 achieves less than 0.1 dB and 0.1° matching between channels 1 and 2 at 20 MHz and output voltages of 1V peak to peak. Distortion was less than −62 dB at the same frequency.

Conclusion

A cost effective driver suitable for driving A to D's requiring closely matched differential inputs has been presented. The driver also exhibits superb distortion and precludes damage to the A to D in the event if an overdriven situation.



$V_{CC} = V_{CC} = 5V$
$R_{f1} = R_{g1} = 590\Omega, 1\%$
$R_{f2} = R_{g2} = 610\Omega, 1\%$

Figure 1.

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Linearized Voltage Control of Delay On A Dual Rising Edge Delay Driver

Linearized Voltage Control Of Delay On The EL7962/72/82C Dual Rising Edge Delay Drivers

by Stephen G. Brickles

Summary

The EL7962/72/82C Dual Rising Edge Delay Driver IC provides up to 1A of peak current for many driver applications. The rising edge of the output can be delayed from 60ns up to 1.5μs from the corresponding input edge. The block diagram of the EL7962C is shown in Figure 1. A resistor from the DSet A Pin to GND sets the delay time for Channel A and a resistor from the Dset B Pin to GND sets the delay time for Channel B. Connecting the Dset A Pin to V_{DD} disables the delay blocks for both channels giving approximately 30 ns of delay on each channel. This programmable delay is useful in applications requiring compensation for long switch turn off times and also applications using resonant mode technology. The inputs of the EL7962/72/82C are T.T.L. compatible and the Peak to Peak output voltages are dependant on the supply voltage.

In all cases, the value of the resistor is approximately proportional to the resulting delay.

This article describes an alternative method of controlling the delay, using a voltage source instead of a resistor. Unfortunately, the relationship between applied voltage and resulting delay is a non linear function. This means that the voltage must be converted before it is used to control the delay. Two methods of converting the voltage are presented here together with their relative advantages and disadvantages.

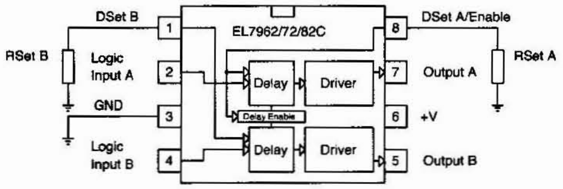


Figure 1. EL7962/72/82C Block Diagram

Controlling The Delay Input

The delay between the *Rising Edge* of the input and output waveforms is normally controlled by a resistor *RSet* connected from the Dset Pin to Ground which varies the flow of current. This sets the value of a current mirror inside the chip which controls the rate of charge of an internal capacitor (See Figure 2).

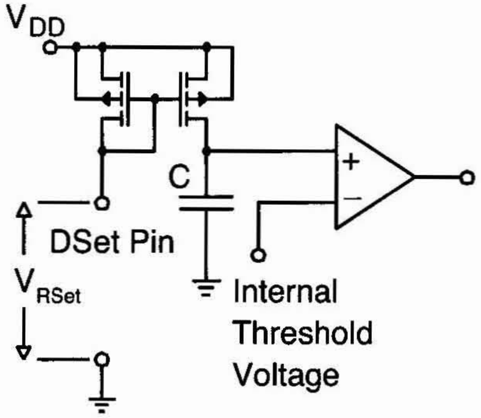


Figure 2. DSet Input Circuitry

This results in the following relationship between the charging current *I*, flowing through *RSet*, and the capacitor *C* :-

$$I_{RSet} = C\frac{dV}{dt}$$

If we relate this to *RSet*, this gives :-

$$\frac{V_{RSet}}{RSet} = C\frac{dV_C}{dt}$$

Since we want to know the relationship between *R* and *dt*, the delay time, we can re-arrange the equation to give :-

$V_{RSet}dt = C(dV_C)(RSet)$ hence $dt \infty RSet \infty$ 1/I

This can be seen from the graph in Figure 3 which shows delay *(dt)* versus current *(I)* flowing through RSet.

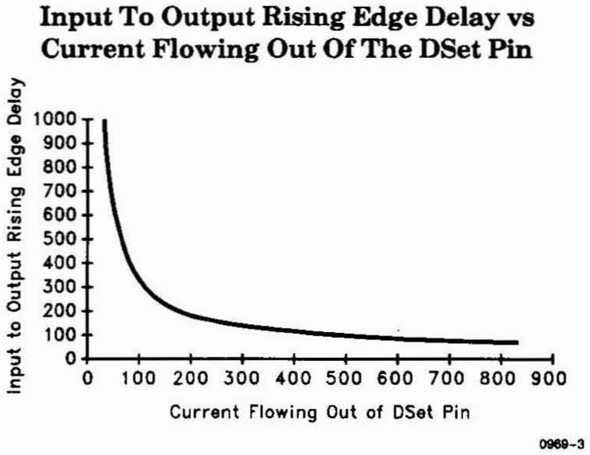


Figure 3. Rising Edge Delay vs Current Out of the DSet Pin

However, if we want to control dt using a voltage we can see that:-

$$dt = \frac{C(dV_C)(R_{Set})}{V_{RSet} - V_{Th}} \text{ hence}$$

$$dt \infty 1/V_{RSet} - V_{Th}$$

Where V_{Th} is the internal threshold voltage in Figure 2.

Thus any external circuit attached to the Dset Pin which uses voltage as the controlling parameter must perform a *1/V* operation on the input voltage first.

Since the controlling factor in this circuit is current, then any circuit which is attached to the Dset Pin must *sink* current. This means that we must convert the controlling voltage to a variable current sink of some description.

Using The EL4451C Multiplier

If we wish to perform a *1/V* operation on the input control voltage, we need some kind of mathematical circuit - one way of doing this is to use a multiplier IC. The best IC to use for this operation is the EL4451C, a two quadrant multiplier. The V_{IN} input is two-quadrant whereas the V_{GAIN}, V_{REF} and V_{FB} inputs are only single quadrant.

The block diagram of this IC is shown in Figure 4.

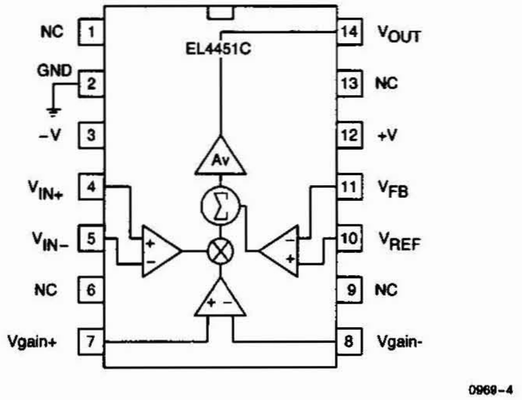


Figure 4. EL4451C

The transfer function of this chip is as follows :-

$$V_{OUT} = A_V((V_{IN+} - V_{IN-})^* (V_{GAIN+} - V_{GAIN-}) + (V_{REF} - V_{FB}))$$

Since A_V is approximately 600, then $V_{OUT}/A_V \cong 0$

This means that

$$((V_{IN+} - V_{IN-})^*(V_{GAIN+} - V_{GAIN-}) + (V_{REF} - V_{FB})) \cong 0$$

$$((V_{IN+} - V_{IN-})^*(V_{GAIN+} - V_{GAIN-}) = -(V_{REF} - V_{FB})$$

$$(V_{GAIN+} - V_{GAIN-}) = \frac{-(V_{REF} - V_{FB})}{(V_{IN+} - V_{IN-})}$$

If we make $(V_{IN+} - V_{IN-}) = -V_{OUT},$

$$(V_{GAIN+} - V_{GAIN-}) = V_{IN} \text{ and}$$

$$(V_{REF} - V_{FB}) = 1V \text{ then}$$

$$V_{IN} = \frac{1V}{V_{OUT}}$$

which is what we need to achieve.

Linearized Voltage Control of Delay On A Dual Rising Edge Delay Driver

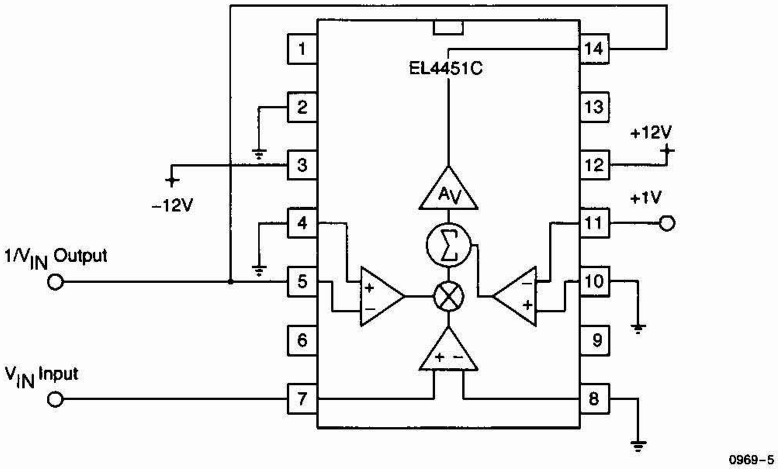


Figure 5. 1/V Convertor Using The EL4451C

Realization Of 1/V Using The EL4451C

The circuit for a 1/V convertor using the EL4451C is shown in Figure 5.

As has been previously stated, for this application, we need to convert the voltage to a variable current sink.

Two easy ways of doing this are presented here.

Method 1 - Using An OpAmp

This method uses the classic textbook voltage to current convertor consisting of an opamp plus an NPN transistor and a resistor to sink the current. The circuit is shown in Figure 6.

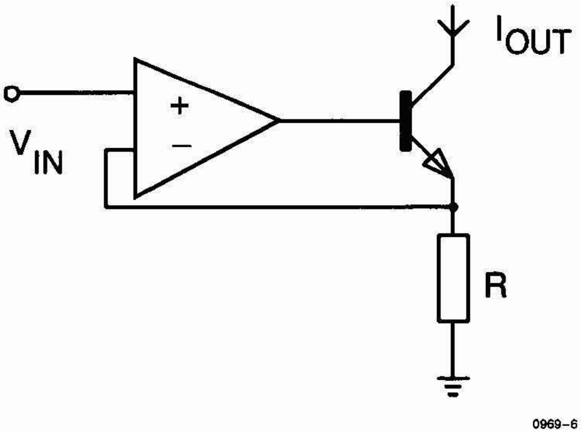


Figure 6. Voltage To Current Convertor

The transfer equation for this circuit is :-

$$I_{OUT} = V_{IN}/R$$

This circuit can be added directly onto the output of the previous 1/V circuit. The Iout line is connected to the Dset Pin on the EL7962/72/82C.

The complete circuit is shown in Figure 7.

Any opamp fast enough to respond to the input will do. Any standard NPN transistor such as a 2N4400 or equivalent will suffice for TR1 here. R may have to be adjusted to maintain stability. 12K works well with an EL2044C amplifier. In addition, it can be seen from the graphs in Figure 8, that VR1 must be set to greater or equal to −0.5V for best results.

Test Results

Graphs of Output Voltage of the EL4451C versus Control Input Voltage and Input to Output Rising Edge Delay versus Control Input Voltage are shown in Figure 8.

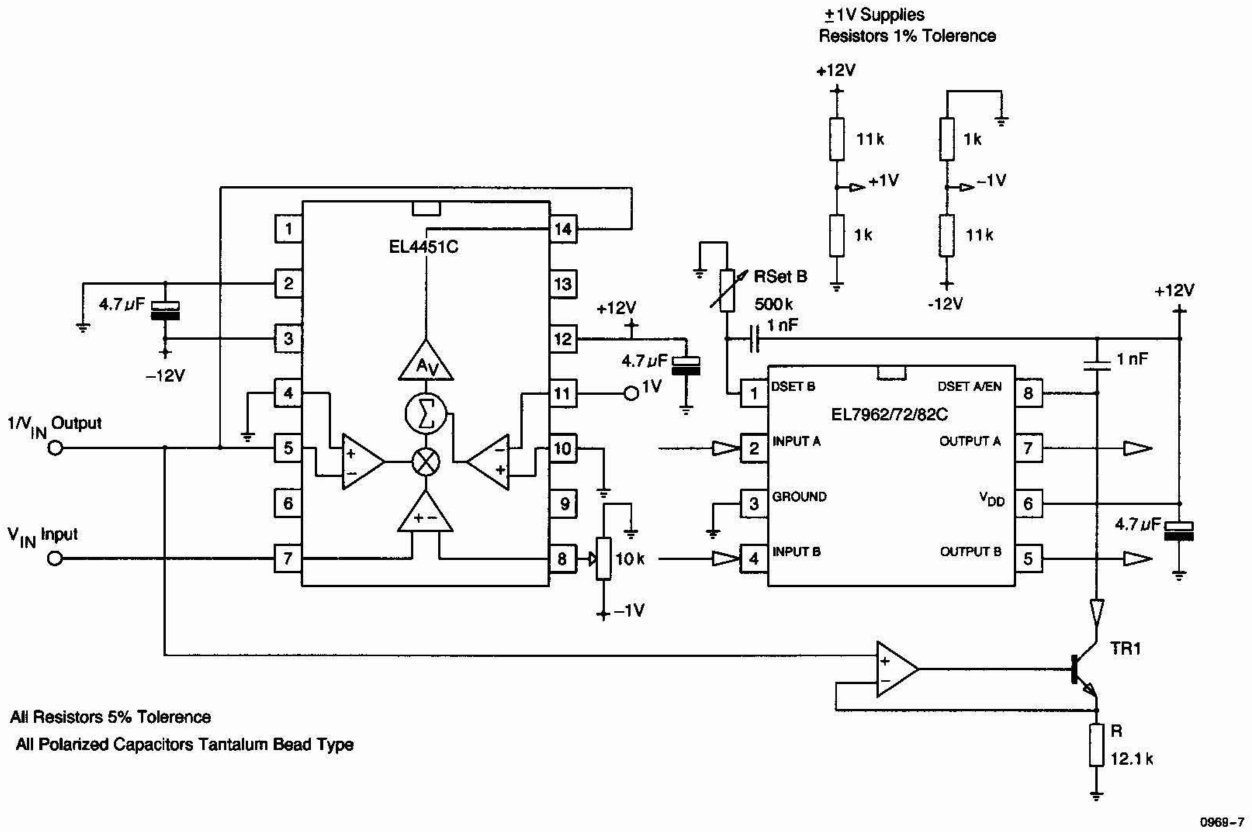
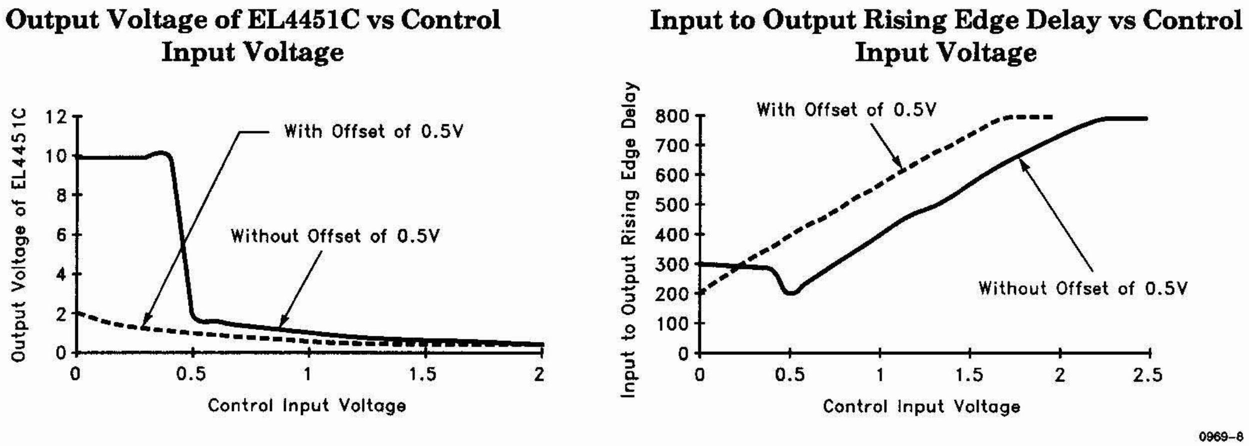

±1V Supplies
Resistors 1% Tolerence
+12V
11k
1k
+1V
–1V
1k
11k
-12V
EL4451C
1
2
3
4
5
6
7
14
13
12
11
10
9
8
4.7µF
–12V
1/V$_{IN}$ Output
V$_{IN}$ Input
A$_V$
+12V
4.7µF
1V
10k
–1V
RSet B
500k
1 nF
+12V
1 nF
DSET B
DSET A/EN
EL7962/72/82C
INPUT A
OUTPUT A
GROUND
V$_{DD}$
INPUT B
OUTPUT B
4.7µF
TR1
R
12.1k
All Resistors 5% Tolerence
All Polarized Capacitors Tantalum Bead Type
0969-7

Figure 7. Voltage To Current Conversion Using An OpAmp


Output Voltage of EL4451C vs Control Input Voltage

Input to Output Rising Edge Delay vs Control Input Voltage

Figure 8. Graphs For Method 1

Method 2 - Stand Alone Variable Voltage To Current Convertor

The second method involves a direct modification to the multiplier circuit and is shown in Figure 9. In this configuration, the current flowing out of the Dset Pin of the EL7962/72/82C is dependent on the voltage across the resistor R. The voltage across R will vary as the control voltage varies. Thus the current through R will vary accordingly.

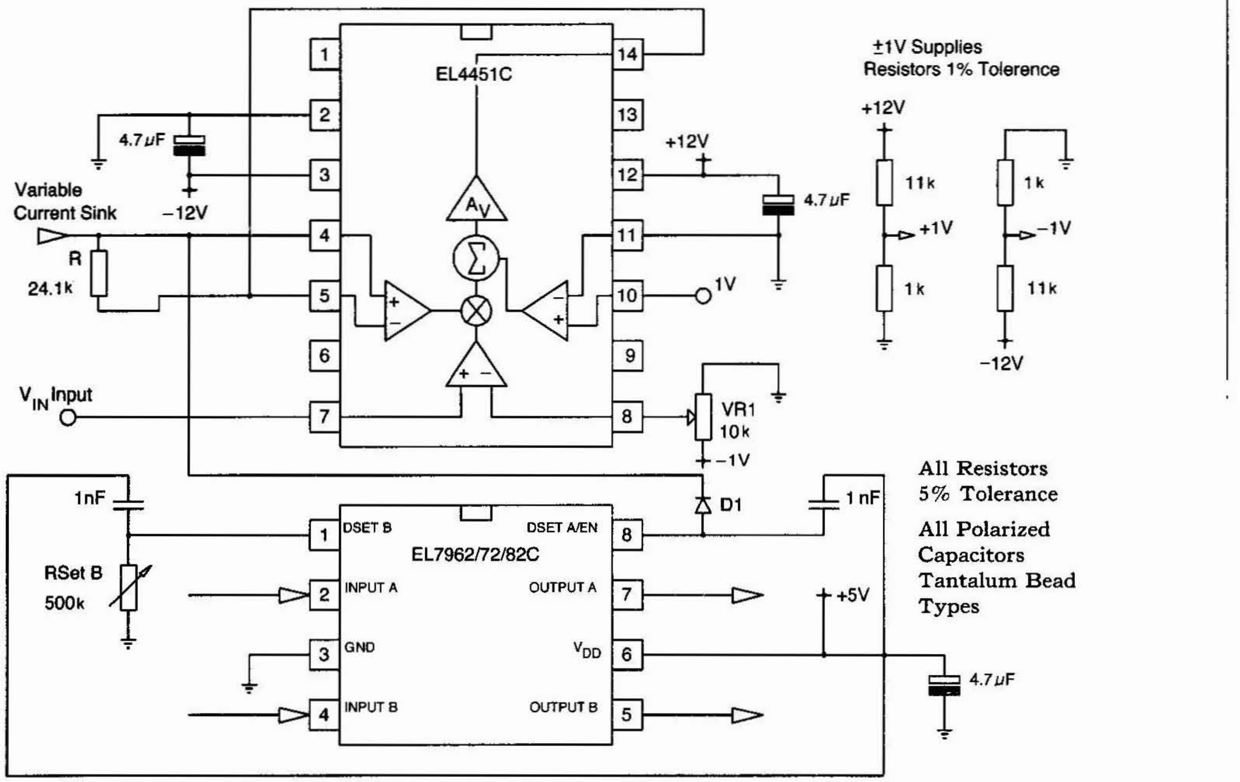
Note that the V_{REF} and V_{FB} inputs (Pins 10 and 11 respectively) must be reversed from the previous configuration to ensure correct polarity of the current which must flow *out* of the EL7962/72/82C. The V_{GAIN}- Pin (Pin 8) needs a variable negative voltage which can be adjusted as needed using VR1. The variable V_{GAIN}- input control is to compensate for non - linearities in the 1/V circuit below about 0.5V. This means that the V_{GAIN}- input will be about −0.5V for stable operation.

D1 is included to protect the EL7962/72/82C Dset Pin from any negative voltage and can be any diode with a suitable voltage rating.

VR1 should be a Multiturn type for best adjustment. I recommend that the minimum value of R is not less than 24.1K for stable operation - this corresponds to a minimum delay of 200 ns.

IMPORTANT NOTE

It is recommended that the EL7962/72/82C be powered off a 5V to 6V supply - increasing the supply voltage will cause a corresponding increase in maximum delay, however it introduces greater instability at the lower end of the control range. The suggested values of power supply voltage, the setting of VR1 and the value of R have been chosen to provide the best configuration for greatest control range and stability.

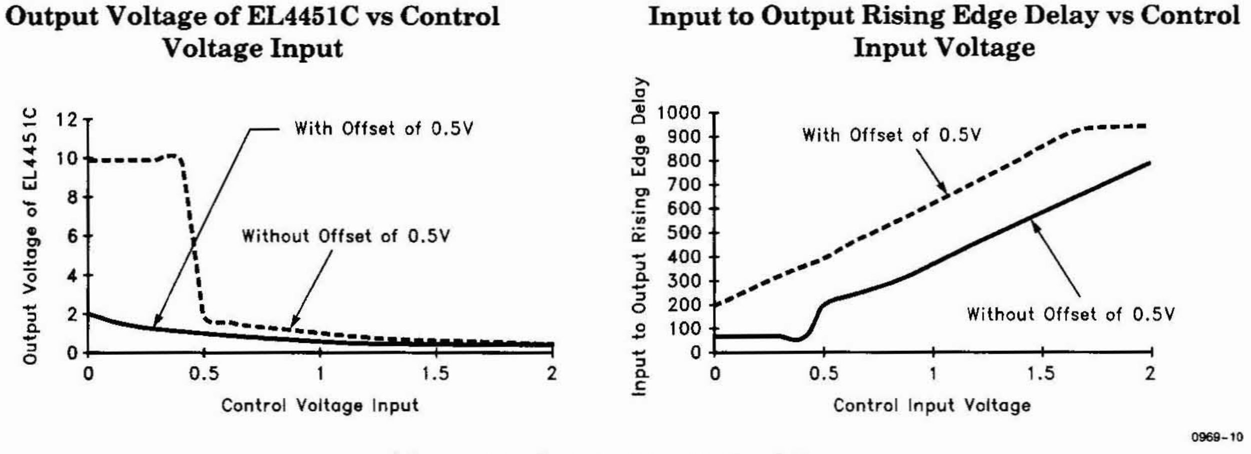

EL4451C
1
2
3
4
5
6
7
8
9
10
11
12
13
14
4.7µF
−12V
Variable Current Sink
R
24.1k
A_V
Σ
+12V
4.7µF
1V
V_{IN} Input
VR1
10k
−1V
D1
1 nF
±1V Supplies
Resistors 1% Tolerence
+12V
11k
+1V
1k
1k
−1V
11k
−12V
1nF
RSet B
500k
DSET B
EL7962/72/82C
DSET A/EN
INPUT A
OUTPUT A
GND
V_{DD}
INPUT B
OUTPUT B
+5V
4.7µF

All Resistors 5% Tolerance

All Polarized Capacitors Tantalum Bead Types

0969-9

Figure 9. Standalone Variable Current Source


Output Voltage of EL4451C vs Control Voltage Input

Input to Output Rising Edge Delay vs Control Input Voltage

Figure 10. Graphs For Method 2

Test Results

Graphs of Output Voltage across R versus Input Control Voltage and Input to Output Rising Edge Delay versus Input Control Voltage are shown in Figure 10.

Setting Up VR1

To set up VR1, measure the voltage at Pin 8 and set it to −1V. Observe the delay between input and output waveforms of the EL7962/72/82C on an oscilloscope. Adjust VR1 until instability is observed then back off VR1 until the display is stable. This should correspond to a setting of −0.5V and a minimum delay of approximately 200 ns. After setting up, in both methods, VR1's value should be measured either side of the wiper terminal and replaced by two 1% tolerence resistors to ensure temperature stability.

Conclusions

Two methods have been presented here - the first method allows the driver IC to be powered from the same supply rail as the multiplier, the second requires a lower supply for the driver which could be a limitation in certain applications. The main disadvantage of the first method is the component count - two IC's, a transistor and a resistor, the second method only needs one IC and a resistor. Both need ±1V supplies for the control inputs and ±12V supplies for the IC's. However over a certain delay span both methods achieve the objective of linearized voltage control of input to output rising edge delay.

Bibliography

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Page 182

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Elantec 1995 New Products Supplement
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A Cost Effective Method for Transmitting Composite Video

Introduction

Historically. video designers have used coaxial cables to route and transmit composite video signals over distances up to several hundred feet (> 100 meters). In the last few years, however, telephone lines such as twisted pairs have been used successfully in local area networks to transmit data between data terminals and computers. Techniques similar to these may be used by video designers who want to trade the cost of a coaxial cable for the more cost effective twisted pair. For example, RG59 is currently priced at 20 to 25 cents per foot; whereas, a twisted pair cable is under 10 cents a foot. Clearly, in applications in which cable lengths are 500 feet or more, a cost trade-off can be made between a simple single-ended circuit employing a single op amp used to drive coax and a slightly more complicated differential driver using a twisted pair. Presented in this paper is such a device.

Circuit Description

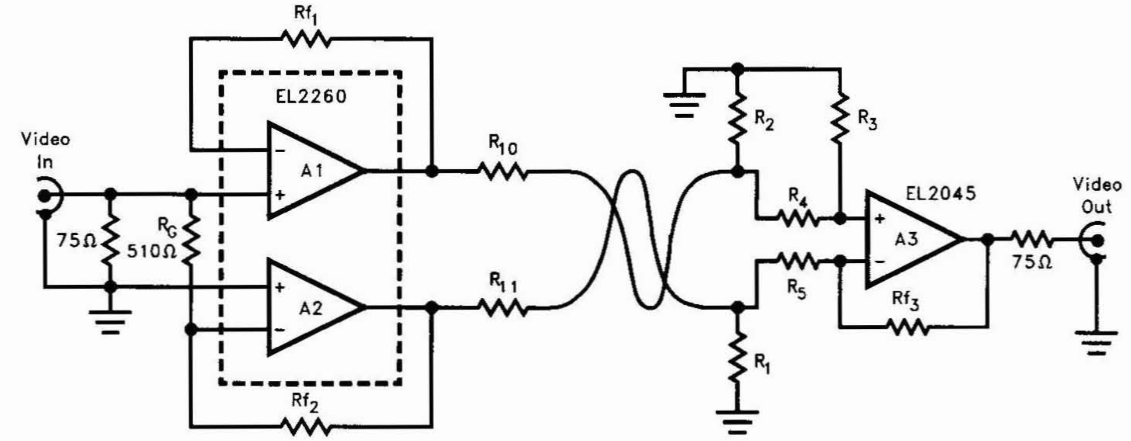
In order to preserve good common mode noise rejection, a differential amplifier comprised of an EL2260, Dual 130 MHz Current Feedback Amplifier (CFA) is employed to convert the single-ended video to a differential signal as shown in Figure 1. CFA's require a known feedback resistor to set the bandwidth and slew rate, and the nominal value for the 2260 is 560Ω. The receiver invoked the EL2045, Gain of 2 stable 100 MHz operational amplifier hooked for a gain of 2 differential amplifier. A gain of 2 was taken in this stage to make up for the attenuation at the output A1 and A2 by resistors R10, R11, R1, and R2. R10 and R11 were used to isolate the outputs of A1 and A2 from the capacitive reactance of the line. R_G may be varied to achieve unity gain at the video output.

Performance Results

The circuit of Figure 1 provided a 3 dB bandwidth in excess of 35 MHz at the Video output, 0.1 dB gain flatness to over 5 MHz. Using a Tektronix 520 NTSC Vector Oscilloscope, the differential gain and phase were under 0.3% and 0.5° respectively. In fact, there was immeasurable difference between driving 100 meters of twisted AWG26 cable and 100 meters of RG59.

Conclusion

A lost cost alternative has been presented for distributing composite video signals. In fact, for about $5 plus a handful of 5% resistors, a significant cost savings can be realized using twisted wire in lieu of the traditional coaxial cables.


Rf1
EL2260
Video
In
75Ω
RG
510Ω
A1
A2
Rf2
R10
R11
R2
R3
R4
R5
R1
EL2045
A3
Rf3
75Ω
Video
Out
0968-1

$R_1 = R_2 = R_{10} = R_{11} = 100\Omega$, ±5%
$Rf_1 = Rf_2 = 560\Omega$, ±5%
$R_4 = R_5 = 220\Omega$, ±5%
$V_{CC} = V_{CC} = 5V$

Figure 1

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Doubling the Output Current to a Load with a Dual Op Amp

Doubling the Output Current to a Load with a Dual Op Amp

Introduction

Standard linear output current for high speed op amps is on the order of 30 mA–40 mA. When more is required, the next available options provide around 200 mA, but with a significant increase in cost and quiescent current. In these cases, it may be more cost efficient to configure a dual op amp to provide adequate output current.

Circuit Description

A common solution is shown in Figure 1. The overall gain is $1 + (R_2/R_1)$ and the output current is $I_1 + I_2$. This is only acceptable at low frequencies such as audio where the intrinsic delay of the op amp is negligible with respect to the wavelength of the input signal. At higher speeds, the output of A_1 will drive the load significantly before A_2 and the output drive will never reach twice the current.

In high frequency applications, the circuit in Figure 2 is preferable. Here the two op amps work in parallel. Since the dual package ensures the similar delay through each op amp, there will be no fighting at the output and twice the current will be delivered to the load. The overall gain is still $1 + (R_2/R_1)$.

Resistors R_{bm1} and R_{bm2} are back match resistors. When driving a transmission line, R_{bm1} and R_{bm2} should equal twice the characteristic impedance of the line to terminate it properly since they are driving it in parallel. If proper matching to a load is not necessary, then R_{bm1} and R_{bm2} simply isolate the outputs of A_1 and A_2, limiting the current from any output offsets. For example, if the offset voltage was 10 mV between the outputs of the two op amps, then $R_{bm1} = R_{bm2} = 5\Omega$ would limit the offset current to 1 mA, while allowing the maximum output voltage swing.

Conclusion

A low cost option for increasing the effective output current drive of an op amp has been presented. Twice the output current is achieved with minimal addition of complexity.

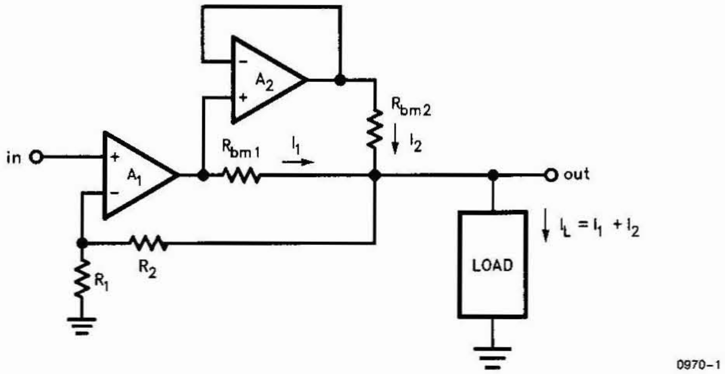

Figure 1

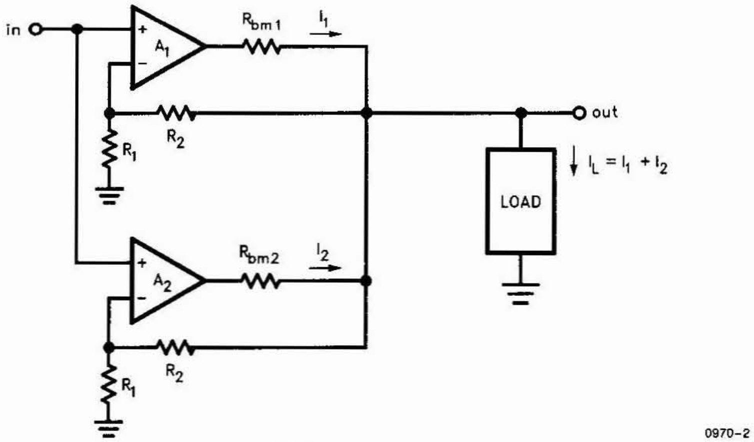

Figure 2

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

An HDSL 2B1Q Modulator Using a Multiplexed-Amplifier

Application Note #30

An HDSL 2B1Q Modulator Using a Multiplexed-Amplifier

by Barry Harvey

In HDSL telephony, a four-level analog modulation is used to represent two simultaneous bits of information per clock (hence 2B1Q). The leels must be accurate in voltage and have clean transitions. A 4:1 multiplexer switch is commonly used that switches between the voltage divisions between a positive and a negative reference according to code. Although the components are inexpensive, the realization requires a lot of devices. Here is the classic approach:

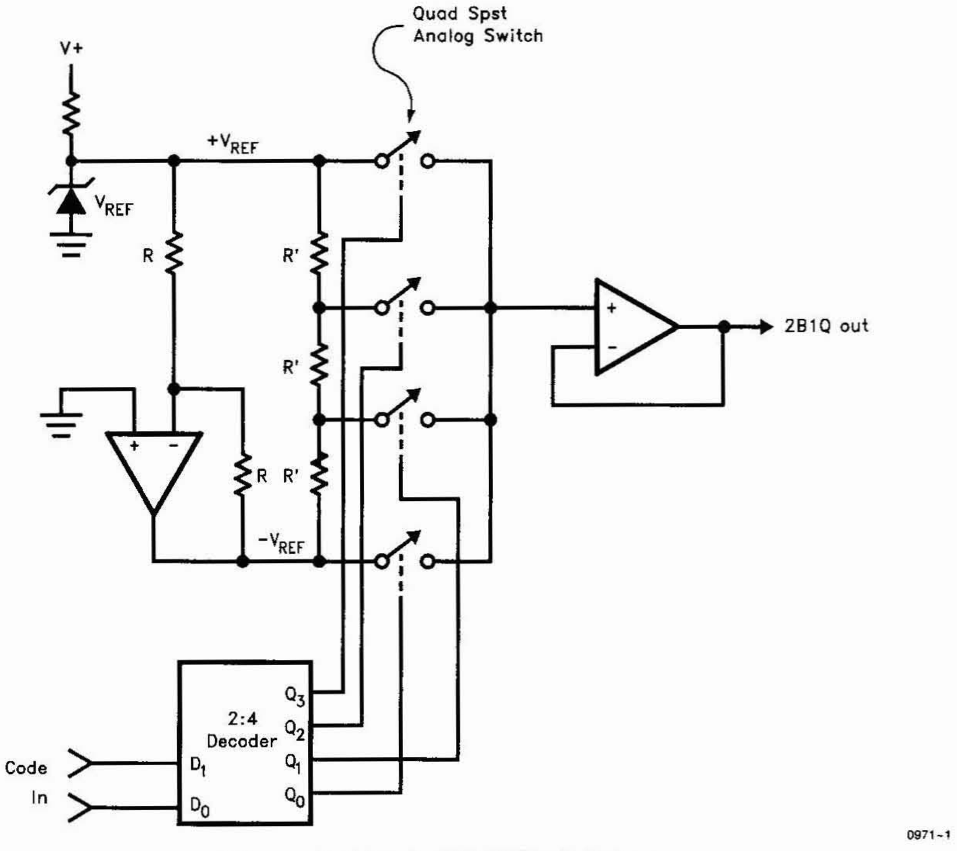

Quad Spst
Analog Switch
V+
$+V_{REF}$
V_{REF}
R
R'
R'
R
R'
$-V_{REF}$
+
-
+
-
2B1Q out
2:4
Decoder
Q_3
Q_2
Q_1
Q_0
D_1
D_0
Code
In
0971-1

Figure 1. Classic 2B1Q Modulator

An HDSL 2B1Q Modulator Using a Multiplexed-Amplifier

Here we need two op-amps, a quad analog switch, a 2:4 logic decoder, and a reference.

The clock rate is 2 MHz, and common analog switches do not switch quickly in this time scale, especially on ±5V supplies. The time delays can vary depending on the DC level of the divider. Further, CMOS analog switches generate large charge transients which are voltage-variable, making the received signal more difficult to decode.

Figure 2 shows the use of an EL4443 four-input multiplexed-amplifier to do the job. The logic inputs select one of four op-amp inputs which are wired for different gains to perform level selection. The gains of input stages A, B, C, D are −1, −1/3, +1/3, +1 respectively. The circuit is greatly simplified and switching transitions are over in 50 ns. The non-linearity of the circuit is around 0.2% for R = 1 kΩ. Errors are caused by offset voltage and bias current of the input stages, as well as a limited open-loop voltage gain of 500.

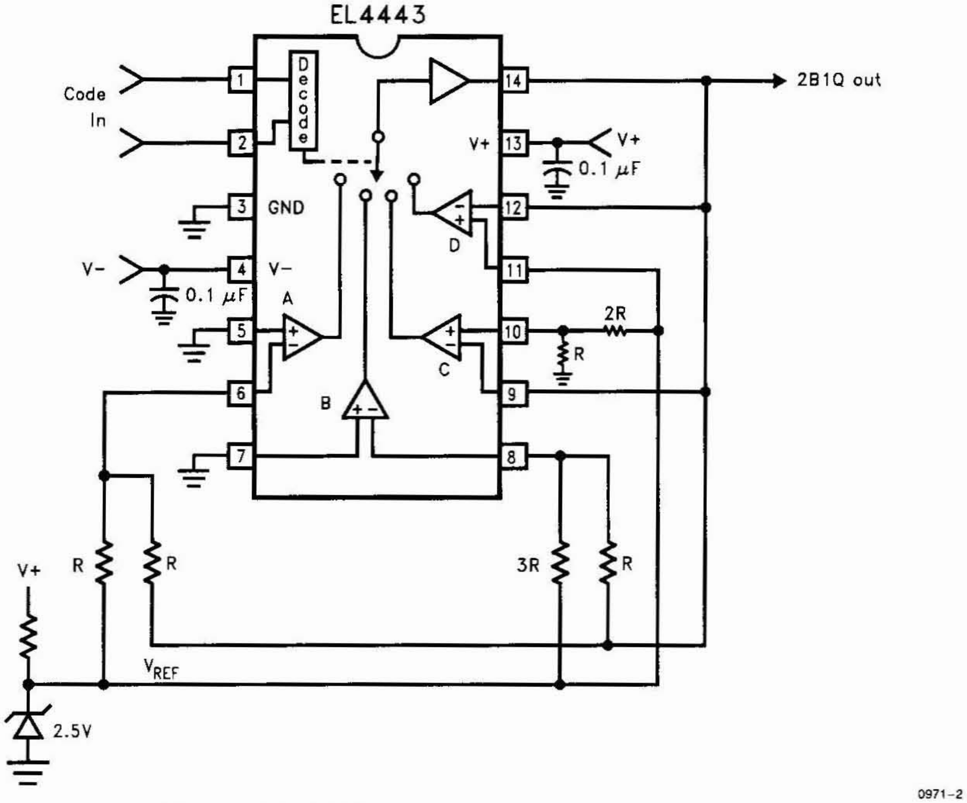


Figure 2. EL4443 in Simple 2B1Q Modulator

HDSL 2B1Q Modulator

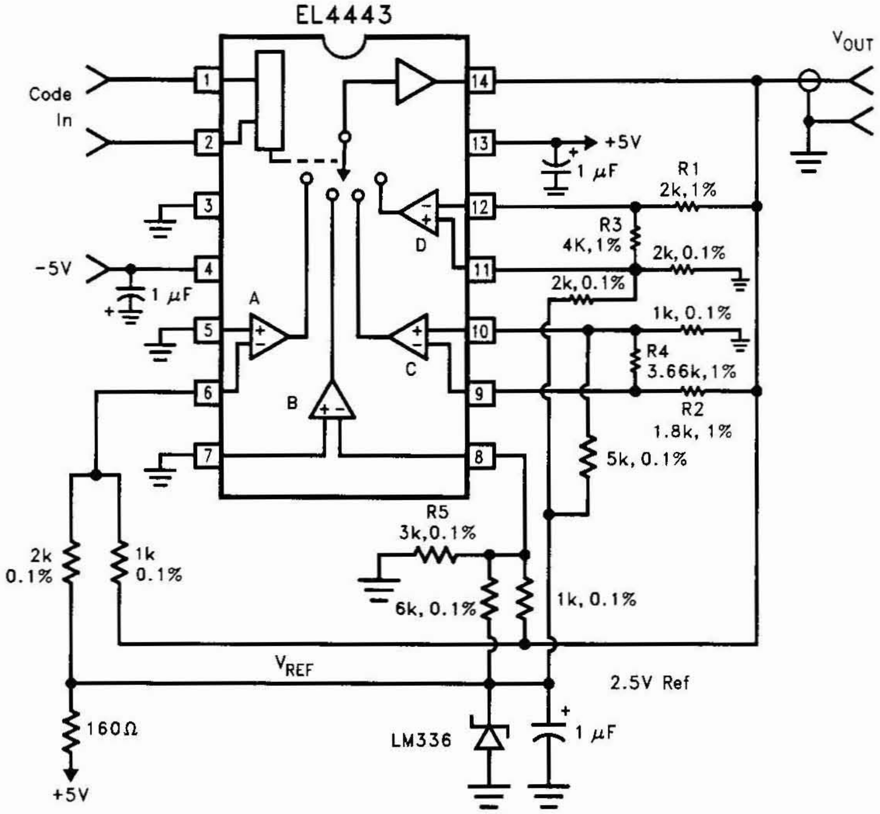
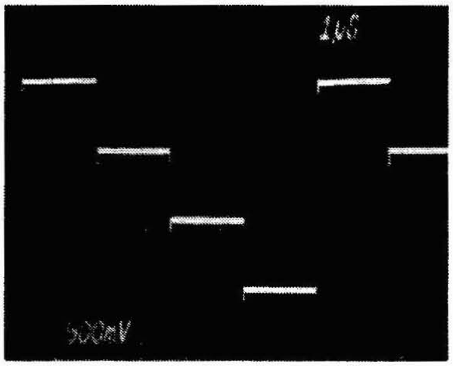

EL4443
Code In
-5V
1 µF
+5V
1 µF
R1 2k, 1%
R3 4K, 1%
2k, 0.1%
2k, 0.1%
1k, 0.1%
R4 3.66k, 1%
R2 1.8k, 1%
5k, 0.1%
R5 3k, 0.1%
6k, 0.1%
1k, 0.1%
2k 0.1%
1k 0.1%
V_REF
2.5V Ref
160Ω
LM336
1 µF
+5V
V_OUT
A
B
C
D
1
2
3
4
5
6
7
8
9
10
11
12
13
14
0971-3

Figure 3. More Accurate 2B1Q Modulator with EL4443

Figure 3 shows a similar modulator where these errors are all addressed. The resistors R1 and R2 balance feedback resistor errors caused by bias currents caused by the + inputs of the non-inverting stages. R3, R4, and R5 provide identical magnification of input offset voltages at each stage's closed-loop gain. Once the circuit sensitivities are so matched between stages, the inherent matching of offsets and bias currents bring overall nonlinearities down to 0.06%, as measured from four samples of EL4443.

The photograph shows the clean and fast transitions of Figure 3's output:


1µS
500mV
0971-4

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Frequency Doubling Through Full-Wave Rectification to 150 MHz

Frequency Doubling Through Full-Wave Rectification to 150 MHz

Introduction

Diode bridges are commonly utilized in full-wave rectification circuitry. However, they are incapable of handling small input signals or high frequencies. When precision and speed are desired, one must design with active devices.

Circuit Description

The circuit in Figure 1 utilizes the speed of a current feedback amplifier (EL2186) and the precision of a differential amplifier (EL2142) to provide full-wave rectification. The input signal is fed through the current feedback amplifier where only one of the two feedback paths is engaged each half-cycle. When the output is positive, current flows through D1 while D2 isolates the other feedback path. Conversely, when the output is negative, current can only flow through D2. Schottky diodes (HP 5082-2835) have been selected as D1 and D2 for their speed and low capacitance.

Each of these half-wave rectified signals is passed selectively into the high impedance differential amplifier, the positive half-cycles at its non-inverting input and the negative half-cycles at its inverting input. Since only one of the signals is active at any given time, the differential amplifier basically combines the signals. Full-wave rectification or frequency doubling is the result.

This circuit has been designed for unity gain. If more gain is desired, the gain setting resistor of the EL2186, Rgain, may be adjusted. The feedback ratio of the EL2142 could also be adjusted; but since its inherent bandwidth is smaller than the EL2186, this is not recommended for the highest operating speeds. For smaller signal inputs at midband frequencies, the gain could be split between the two stages. However, remember to limit the gain of the first stage so that it does not exceed the input voltage range of the second stage.

Conclusion

An option for full-wave rectification is presented that surpasses the limitations of standard diode bridges. High-speed active devices enable this high-frequency doubler to handle input voltages as small as 300 mV and output frequencies up to 150 MHz.

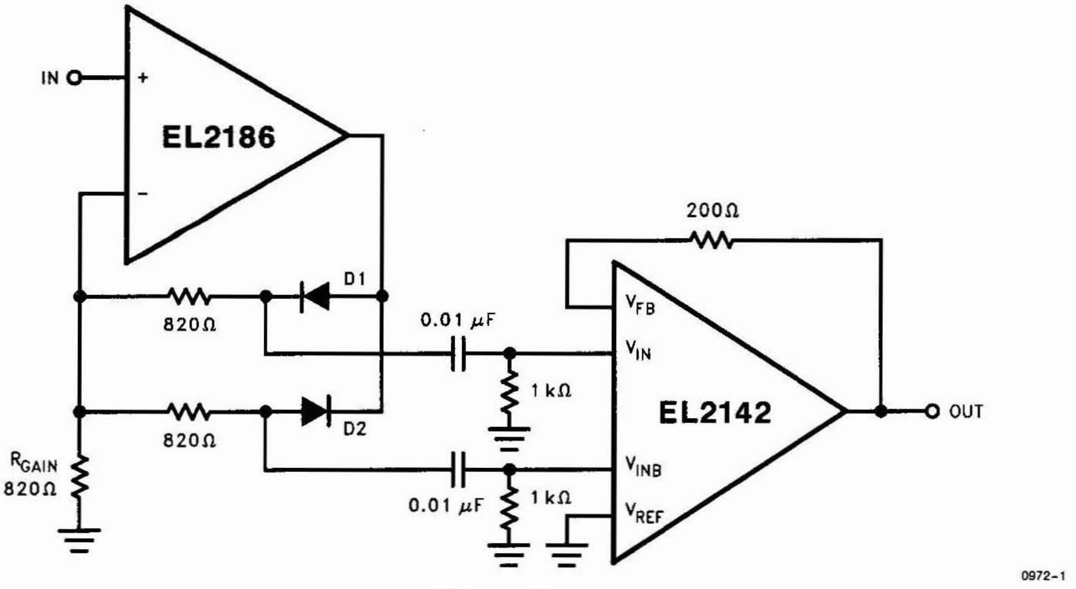


Figure 1

EL4083C

Current Mode Four Quadrant Multiplier Application Note

Introduction

Eight stand alone applications of the EL4083 are presented in the parts' datasheet. These are four quadrant multiplication, squaring, mixing, modulating, demodulating, frequency doubling, gain control and video switching. All of these are possible with either of the two basic applications schematics (see datasheet Figures 18 and 19). Also included in the sheet is a detailed discussion of the parts' features and characteristics on a pin by pin basis in the general operating information section. This can be very useful in developing new applications or modifying the ones presented to perform a more specific task.

The applications presented in this note, except for the first divider circuit, are more elaborate designs that involve more than one multiplier or apply feedback around a multiplier. The examples chosen were either to demonstrate that the EL4083 can perform one of the classic four quadrant multiplier applications or to show some of the design's unique capabilities. More applications are planned so contact Elantec if you want to be sure your revision of this note is the most current.

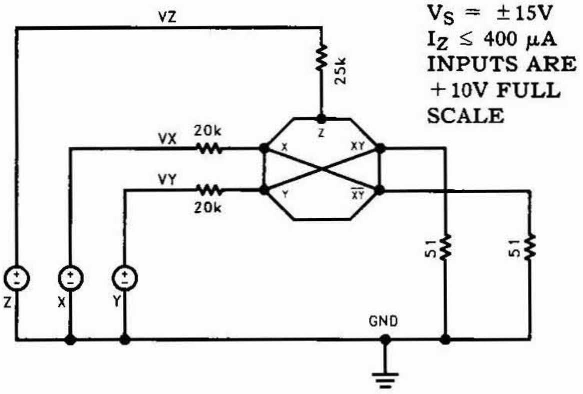
Division by Control of I_Z

In Figure 1, the I_Z pin is used as a denominator input to perform division. However, since the value of the current into the Z_{IN} pin also determines the input impedance and frequency response of all the inputs as well as the supply current of the part, this considerably restricts the computational range and accuracy of this approach. It is presented for its simplicity and can produce acceptable results for a 30 dB (~30-1) range of I_Z.

The key to this circuit is to run it from higher voltage supplies so that the input voltage ranges and the input resistors can be chosen large enough to minimize the input impedance modulation caused by a changing I_Z. The maximum value of I_Z is about 400 μA to stay within the power dissipation rating of the package. The frequency response of the denominator and the numerator inputs over a range of signal levels is shown in Figures 2 and 3 respectively. The circuit performs a multiplication as well as a division and obeys the transfer equation;

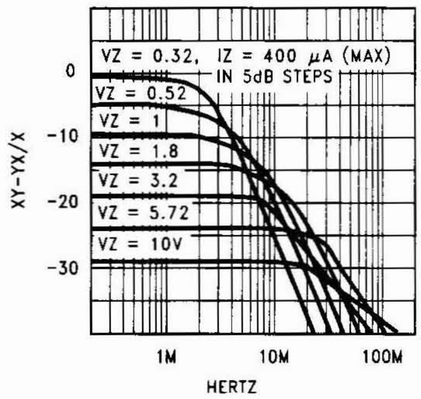
$$(Ixy - \overline{Ixy}) = Ix \times Iy/I_Z$$

See RMS #2 on page 8-154, and performance curves 10 and 11 in the datasheet for other hints on using the I_Z pin as an input signal. A second divider circuit using feedback with a 40 dB to 50 dB denominator range and differential numerator inputs is presented at the end of this note.



83AP-1

Figure 1. I_Z Divider



83AP-2

Figure 2. I_Z Divider Frequency Response of XIN for 5 dB D.C. Steps of V_Z

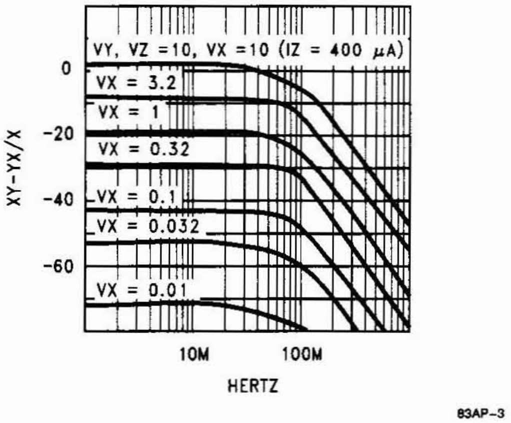


Figure 3. I_Z Divider Frequency Response of XIN for 10 dB D.C. Steps of V_X

Square Rooter

The circuit shown in Figure 4 calculates the function:

$$V_{OUT} = \sqrt{(V_{IP} - V_{IN})},\ V_{IP} - V_{IN} > 0;$$
$$V_{OUT} = 0 \text{ for } V_{IP} - V_{IN} < 0$$

Like the feedback divider circuit below, it has differential inputs. An unused input in either application can simply be omitted with its series resistor. The bandwidth of this circuit is proportional to the square root of the instantaneous input signal value (see Figure 5). The Ccomp capacitors are required for loop stability and their value is chosen to be appropriate to the output op amp selected. As a rule, the faster the op amp, the smaller the value that Ccomp needs to be and the wider the bandwidth of the circuit. The critical condition for stability is at the largest input signal level since this is where the loop will have its highest bandwidth.

A square root circuit can be thought of performing a signal compression function in that the output changes 1 dB in amplitude for every 2 dB amplitude change at the input. The Figure 4 circuit can process an input referred dynamic range of about 50 dB with good accuracy. This is limited mostly by the output referred offset of the multiplier. If more dynamic range or better accuracy is required, the optional trim network shown on the figure can be used.

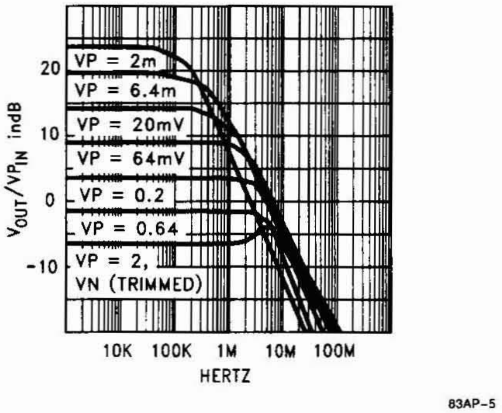


Figure 5. Gain/Frequency Response in 10 dB D.C. Steps at the Input

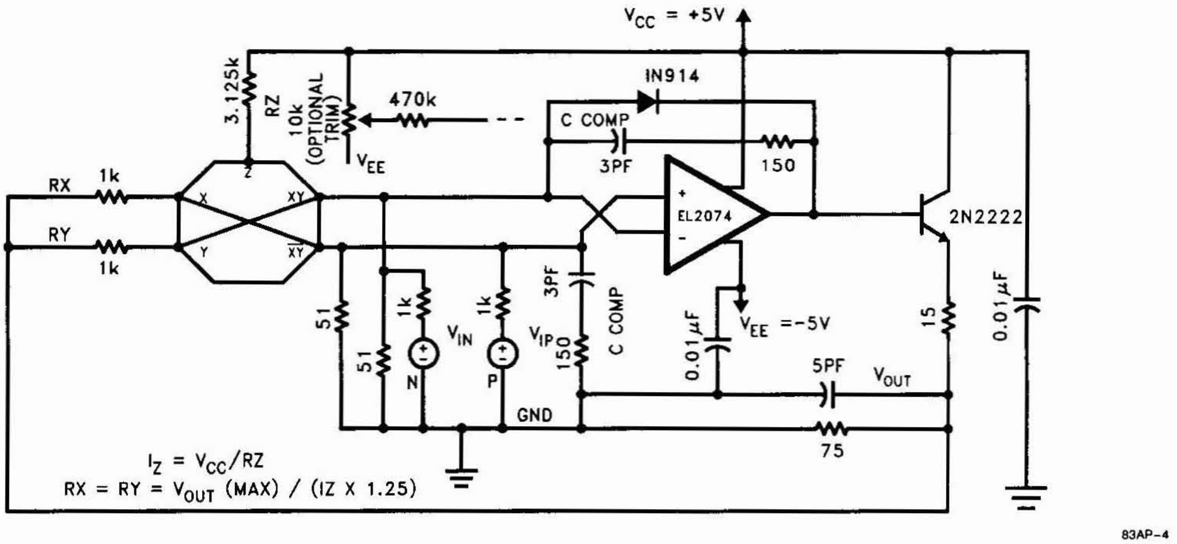
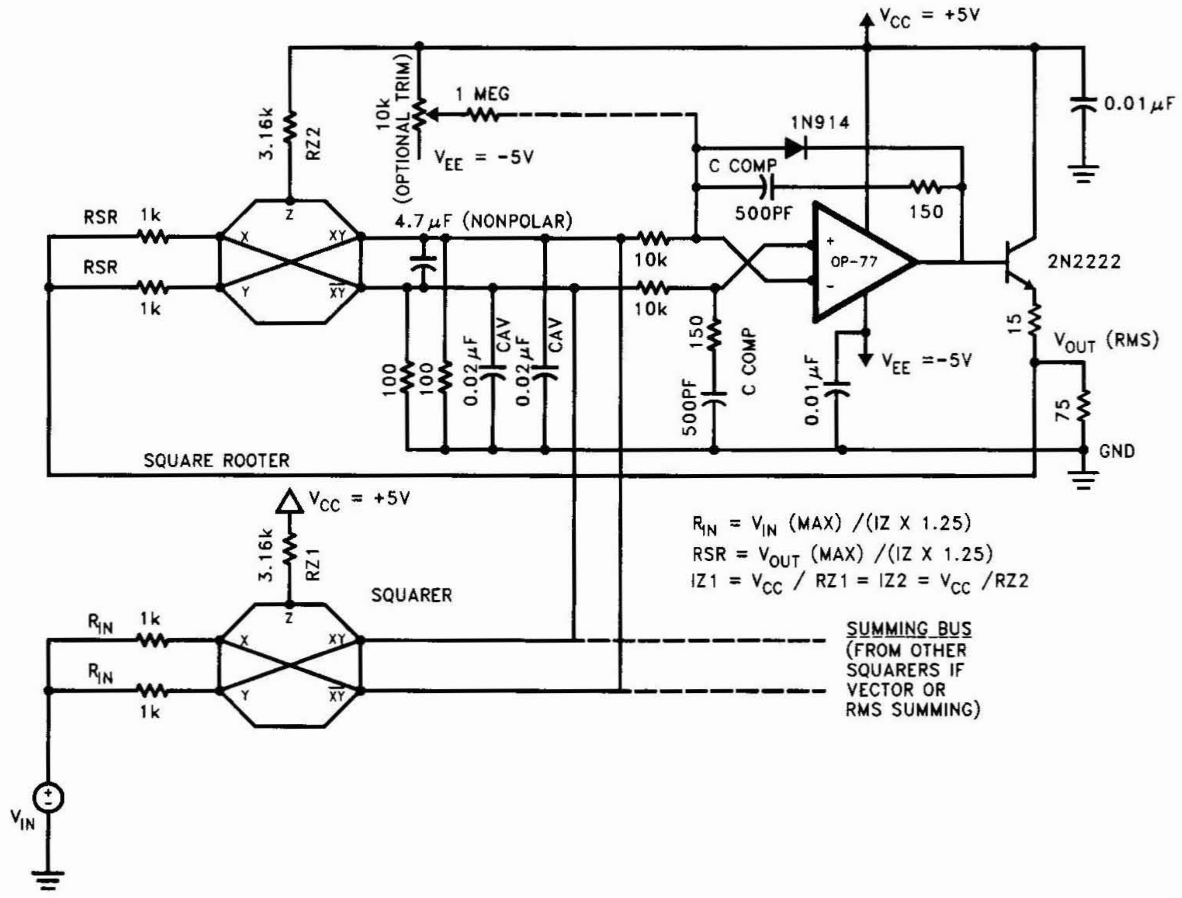

VCC = +5V
IN914
3.125k
RZ
10k (OPTIONAL TRIM)
470k
VEE
C COMP
3PF
150
RX
1k
RY
1k
Z
X
XY
Y
XY
EL2074
2N2222
51
51
1k
1k
VIN
VIP
N
P
3PF
150
C COMP
0.01μF
VEE = -5V
5PF
VOUT
15
0.01μF
GND
75
IZ = VCC/RZ
RX = RY = VOUT (MAX) / (IZ X 1.25)
83AP-4

Figure 4. Fast Square Rooting Circuit (with Inverting and Non-inverting Inputs)


V_{CC} = +5V
0.01µF
1 MEG
10k (OPTIONAL TRIM)
3.16k
RZ2
1N914
V_{EE} = -5V
C COMP
500PF
150
RSR 1k
RSR 1k
Z
X
XY
Y
$\overline{XY}$
4.7µF (NONPOLAR)
10k
10k
OP-77
2N2222
15
V_{OUT} (RMS)
100
100
0.02µF
CAV
0.02µF
CAV
150
500PF
C COMP
0.01µF
V_{EE} =-5V
75
GND
SQUARE ROOTER
V_{CC} = +5V
3.16k
RZ1
SQUARER
R_{IN} = V_{IN} (MAX) /(IZ X 1.25)
RSR = V_{OUT} (MAX) /(IZ X 1.25)
IZ1 = V_{CC} / RZ1 = IZ2 = V_{CC} /RZ2
R_{IN} 1k
R_{IN} 1k
SUMMING BUS (FROM OTHER SQUARERS IF VECTOR OR RMS SUMMING)
V_{IN}

83AP-6

Figure 6. Wideband RMS (RMS #1) Computing Circuit

Wideband RMS Computing Circuit (RMS #1), Vector Addition-RMS Summing

Two EL4083s can be used to calculate the root-mean-square of a wideband input signal (see Figure 6). The first multiplier calculates the mean square of the input signal by squaring and then averaging the output signal with capacitors. This signal, which is differential, is then processed by the square rooting circuit presented above. The squarer acts as a dynamic range expander in that its output changes 2 dB in level for every 1 dB change at the inputs. Its low level output referred errors limit the untrimmed system dynamic range performance to 30 dB or 40 dB. An optional trim network is shown in the applications figure.

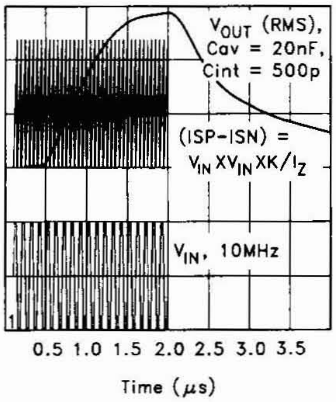
The I_Z bias current of the squaring multiplier must be high enough so that the bandwidth of the squarer will pass the highest frequency of interest. The op amp in the square rooter need not be particularly fast since the squarer's output is immediately averaged by the capacitors. One may also need to provide D.C. blocking capacitors in front of the squarer to prevent offsets in the input signal source from causing errors. Figure 7 shows the response of the circuit to a 10 MHz signal burst. The "lazy" tail of the decay waveform is caused by the bandwidth of the square root circuit contracting with signal level. With the I_Z of the squaring multiplier at its maximum of 1.6 mA, the system is accurate for input frequencies up to 100 MHz.

The outputs of additional squaring multipliers can be summed into the averaging nodes which are inputs to the square root circuit. The value computed is;

Vvectsum =

$$\sqrt{\text{avg}\,(V_1 \times V_1) + (V_2 \times V_2) + \ldots + (V_n \times V_n)}$$

This is the RMS or vector sum of inputs V_1 to V_n.



83AP-7

Figure 7. RMS #1 Response to a 10 MHz Signal Burst

Single Multiplier Implicit RMS Computing Loop (RMS #2)

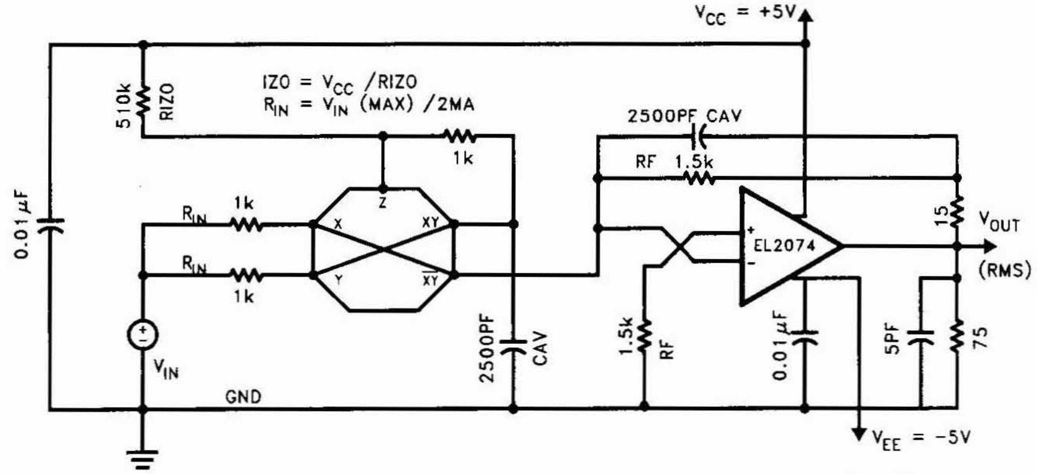
The circuit of Figure 8 uses the I_Z pin of the EL4083 as a divisor input to perform the implicit computation:

$$V_{RMS} = \text{avg}\,(V_{IN} \times V_{IN}) / V_{RMS}$$

Note that the averaging function is provided by a capacitor at the noninverting current output which sources positive current only since the part is performing a squaring function. This point is then connected to the I_Z input through a resistor which completes the computing loop. The inverting current output is fed to the virtual ground input of an op amp where it is averaged and converted to a buffered voltage.

The fact that one is using a current output to drive the I_Z pin overcomes the problem that the voltage on the pin is not constant at low driving currents (see datasheet Figure 10). However, other problems associated with using the I_Z pin as a signal input, notedly the bandwidth and multiplier input impedance dependence on I_Z, remain.

The IZO resistor provides a default current into the I_Z pin to prevent the bandwidth from collapsing and the input impedances from becoming too high as the signal amplitude goes to zero. The value of this current is determined by the application as a trade off between dynamic range and accuracy on the one hand and bandwidth and input impedance modulation, which also affects accuracy, on the other. Figure 9 shows the circuit's response to a signal burst. Note the effect of bandwidth modulation when the output is near zero. This circuit can be quite useful over about a 20 dB to 30 dB dynamic range given these limitations.



83AP-8

Figure 8. Single Multiplier Implicit RMS Computing Loop (RMS #2)

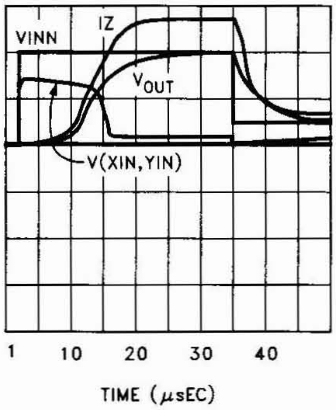


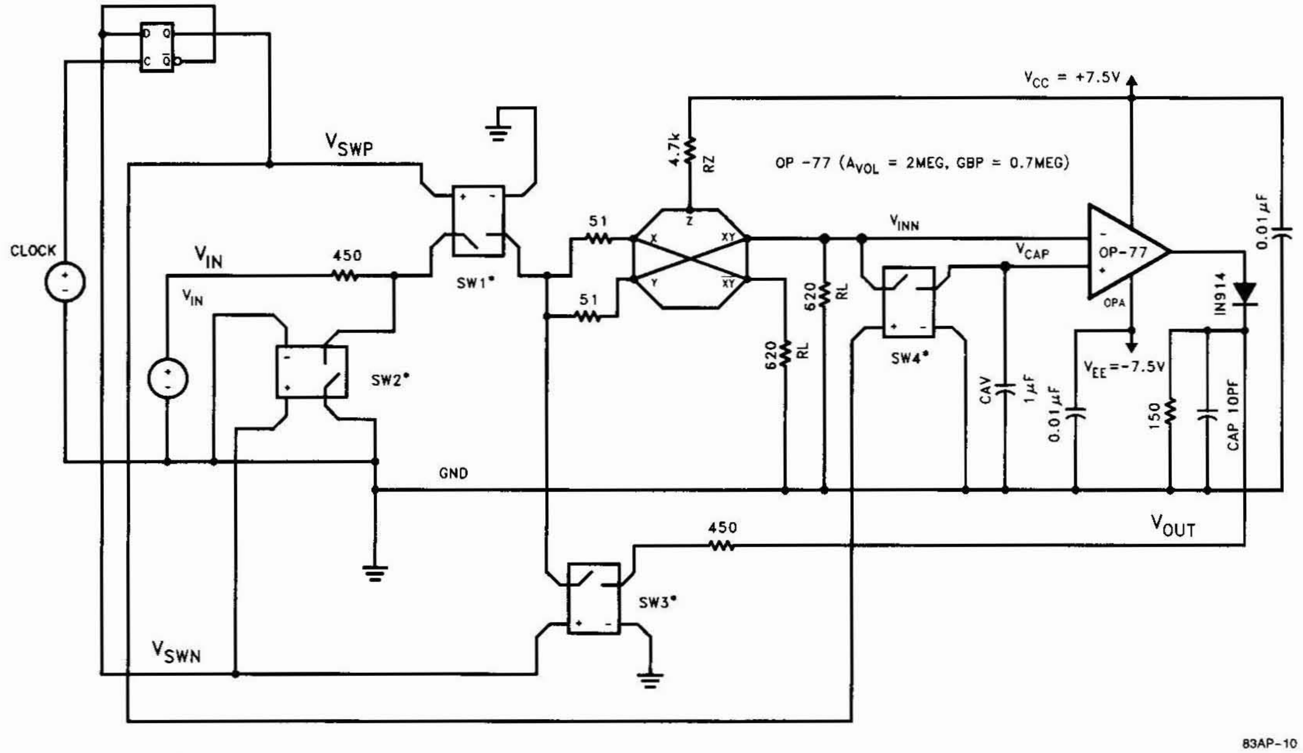
Figure 9. RMS #2 Signal Burst Response

Single Multiplier Switched RMS Circuit (RMS #3)

The circuit of Figure 10 operates by switching alternately between two modes of operation. The first computes the mean square of the input and the second computes the square root of this value. The output value is not valid until it is settled at the end of the second phase. This circuit is useful in applications which do not require continuous monitoring of an input signal as in digital metering. It would be inappropriate, for example, as the level detection portion of an AGC circuit since a sudden level change could go uncorrected for as much as a full computing cycle.

The major advantage of this circuit is the improvement in accuracy achieved by having the same inputs of the same multiplier do both the mean square and the square root computations. The gains are therefore identical and the effects of the offsets tend to cancel out. A high gain low offset op amp like the OP-77 is recommended at the output for the best results. Inexpensive switches such as the standard CMOS 4000 series can be used for input frequencies up to about 10 MHz. The Siliconix SD5000 series quad DMOS FET switches work well to over 200 MHz which is the maximum operating frequency of the EL4083.

An Overall detection bandwidth of 100 MHz and a dynamic range of over 40 dB can be achieved with this circuit without trimming.


D Q
C Q̄
CLOCK
VSWP
VIN
450
VIN
SW1*
SW2*
51
51
4.7k
RZ
Z
X
XY
Y
X̄Y
VCC = +7.5V
OP -77 (AVOL = 2MEG, GBP = 0.7MEG)
VINN
VCAP
OP-77
OPA
620 RL
620 RL
SW4*
CAV 1µF
0.01µF
VEE=-7.5V
150
CAP 10PF
IN914
0.01µF
GND
450
VOUT
SW3*
VSWN
83AP-10

*Note: SD 5000 substrate pin connected to V_{EE}.

Figure 10. Single Multiplier Switched RMS Circuit
RMS #3 (SW1-4 are Siliconix SD5000 Series Quad DFETS for F_{IN} > 10 MHz)

Polynomial Functions (CRT Focus and Geometry Correction)

The current inputs and differential current outputs of EL4083 lend this device extremely well to the computation of high frequency polynomial functions. Two practical examples, CRT focus and geometry correction, are shown in Figures 11 and 12. The final outputs can be used single ended or recovered differentially as discussed in the Basic Product Functions section of the datasheet. Since the seriesed EL4083 multiplier is a current mode device, very little bandwidth is lost through a complex signal chain. This idea can be expanded to arbitrary weighted sums of first order terms, squares, cubes, cross products and perhaps higher order functions.

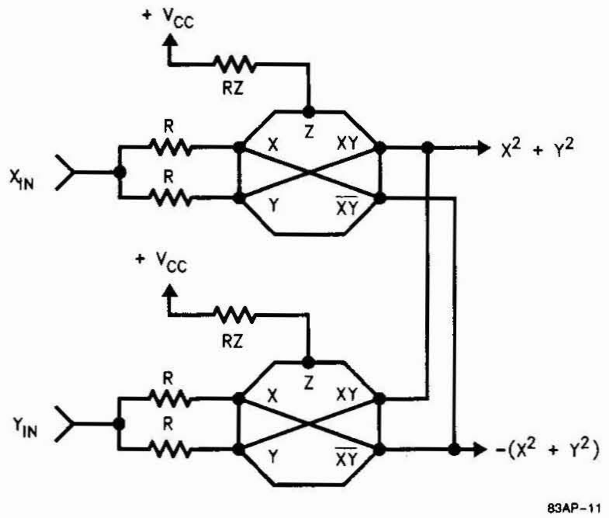

+ VCC
RZ
R
R
XIN
X
Z
XY
Y
XY
X2 + Y2
+ VCC
RZ
R
R
YIN
X
Z
XY
Y
XY
-(X2 + Y2)
83AP-11

Figure 11. CRT Focus Correction

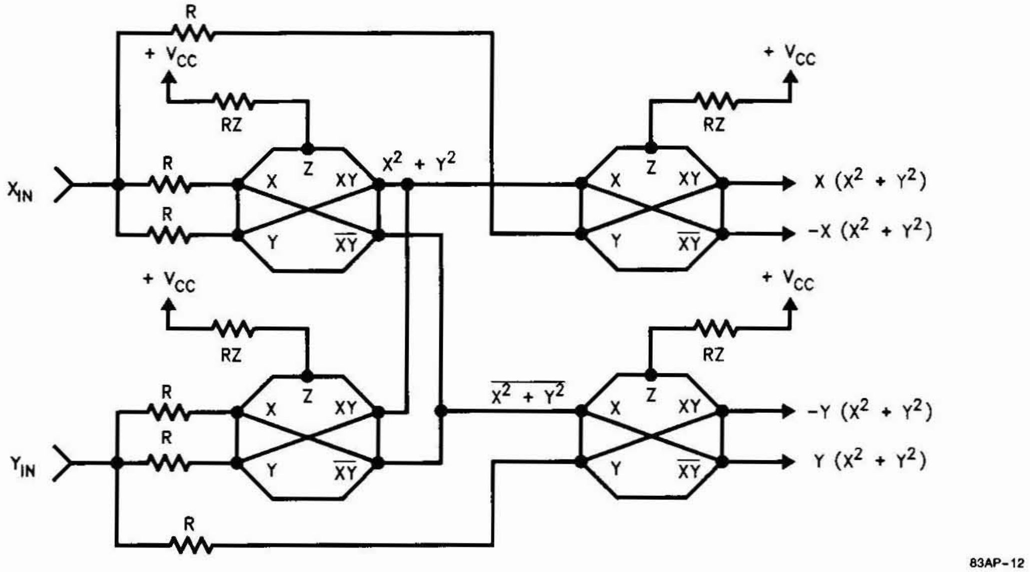

R
+ VCC
RZ
R
R
XIN
X
Z
XY
Y
XY
X2 + Y2
+ VCC
RZ
X
Z
XY
Y
XY
X (X2 + Y2)
-X (X2 + Y2)
+ VCC
RZ
R
R
YIN
X
Z
XY
Y
XY
X2 + Y2
+ VCC
RZ
X
Z
XY
Y
XY
-Y (X2 + Y2)
Y (X2 + Y2)
R
83AP-12

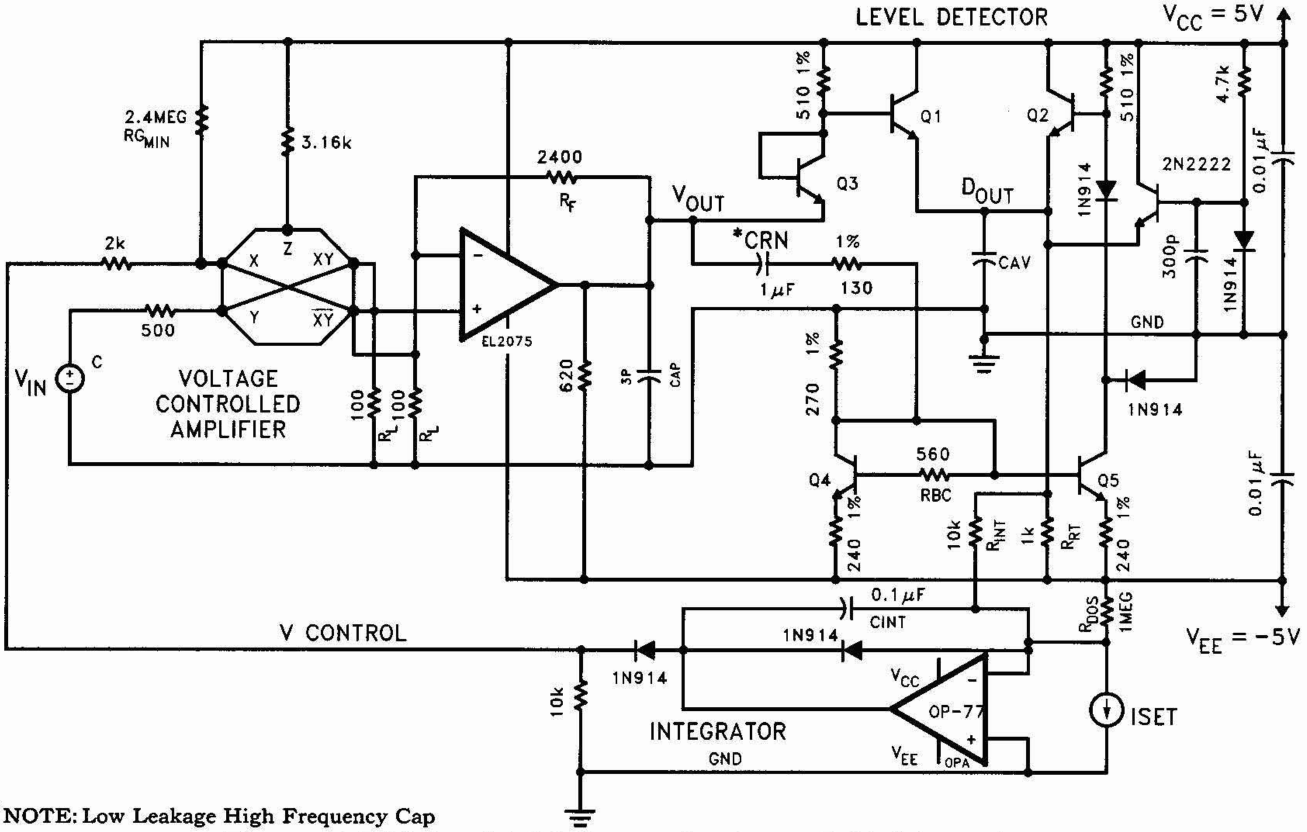
Figure 12. CRT Geometry Correction

Wideband AGC Amplifier

The circuit in Figure 13 is a very wideband output regulating type AGC amplifier. It consists of a VCA (see datasheet Figure 23), a 100 MHz full wave rectifier/level detector and an op amp integrator. The level detector is built around the RCA CA3246 3 GHz Ft five transistor array. Transistors Q3 and Q1 rectify the positive portion of the output waveform while transistors Q4, Q5 and Q2 form an inverting amplifier which when connected to the output of Q1, completes the full wave rectifier. The Crn capacitor level shifts and D.C. blocks the signal into the input of the inverting amplifier. The Rbc resistor compensates for the effects of base currents. The 2N2222 acts as a negative clamp on the output of the inverting amplifier which enhances its speed. The Cav capacitor averages the rectified output and its value together with the value of the Rrt resistor determines the recovery time of the circuit to a signal level decrease. By connecting Rrt to the negative supply, bandwidth is maintained at low signal levels by keeping a D.C. standing current in Q1 and Q2. The nonzero value at D_{OUT} with zero input due to current density mismatches can be compensated at the integrator input by choosing the value of Rdos such that;

Rdos = V_{EE}*Rint/Vdos where Vdos is the zero input offset voltage.

The current source I_{SET}, which can be fixed or variable, determines the output level to which the AGC will try to regulate. The feedback is such that a level detected above this point will cause the integrator to reduce the forward gain. The diode at the integrator output insures that only positive voltages can be presented to the control input of the multiplier. This together with Rgmin, whose value determines the minimum forward gain, prevents gain foldback around a control input of zero.


LEVEL DETECTOR
VCC = 5V
510 1%
510 1%
4.7k
Q1
Q2
Q3
2N2222
0.01μF
2.4MEG
RGMIN
3.16k
2400
RF
VOUT
DOUT
1N914
*CRN
1%
1μF
130
CAV
300p
1N914
GND
2k
X
Z
XY
Y
XY
500
EL2075
VIN
C
VOLTAGE CONTROLLED AMPLIFIER
100 RL
100 RL
620
5P CAP
270 1%
1N914
560
RBC
Q4
Q5
240 1%
10k RINT
1k RRT
240 1%
0.01μF
0.1μF
CINT
RDOS 1MEG
VEE = −5V
V CONTROL
1N914
1N914
VCC
OP-77
VEE
OPA
ISET
10k
INTEGRATOR
GND

*NOTE: Low Leakage High Frequency Cap

Figure 13. Wideband AGC Circuit (Q1-Q5 are RCA CA3246 Array)

83AP-13

The maximum forward gain of the signal path is 15 dB with a -3 dB bandwidth of 115 MHz. One can trade off bandwidth for more gain in the EL2075 in the usual manner by scaling the RL and RF resistor values. The 500Ω input resistor is appropriate for a full scale input voltage swing of ±1V and maximizes the the gain of the multiplier for this signal level. Figure 14 shows the regulated output vs input signal level over a range of values of I_{SET}.

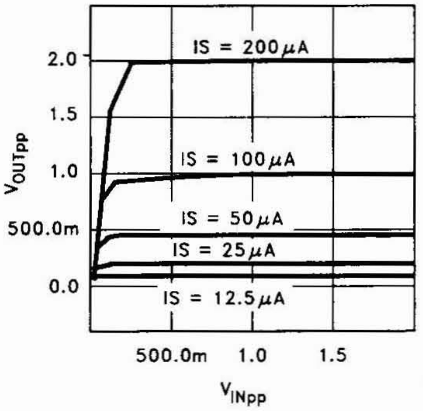


Figure 14. AGC Circuit Output Level Regulation vs Input Level at Several Values of I_{SET}

Controlled Signal Summer/Multiplexer and Video Fader for HDTV

A circuit that can produce the controlled sum or mix of two input signals is shown in Figure 15. This idea can be extended to any number of signal inputs if one keeps in mind that there will be some sacrifice of speed due to the summing of the device output capacitances. For producing either a final dual single ended or a differential recovered output, all the comments in the Basic Product Functions section of the datasheet apply.

A video cross fader function can be realized by a slightly modified version of the Figure 15 circuit shown in Figure 16. Note that the control voltage is common to both multipliers and one control input is offset by the current in a resistor connected to the negative supply. A control voltage moving from ground to some positive maximum value will cause the output mix to go continuously from signal 2 only to signal 1 only. The negative D.C. offset on the control input of second multiplier would invert signal 2's polarity in the sum if it's outputs were not cross connected with the first.

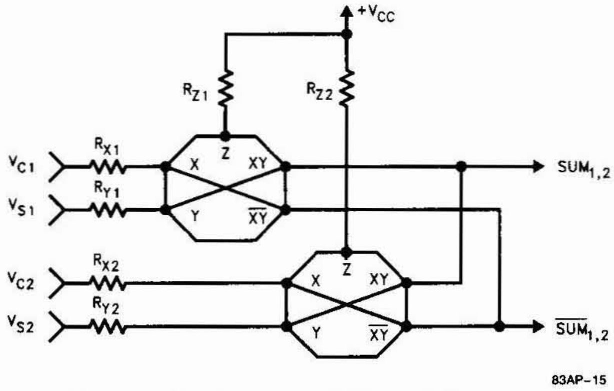


Figure 15. Controlled Signal Summer

In Figure 17 a complementary current output DAC such as the DAC-08 or DAC-10 is used to provide the control currents for the cross fading function. Since the current outputs of the DAC are directly connected to the virtual ground inputs of the 4083s, the full current bandwidth of the DACs can be realized. The optional capacitor shown in the figure can be used to reduce switching transients if needed. The reference current for the DAC should be chosen to be equal to the full scale current selected for the multipliers. Note that the sense of both multiplier outputs have been flipped because of the negative only current sink outputs of the DAC.

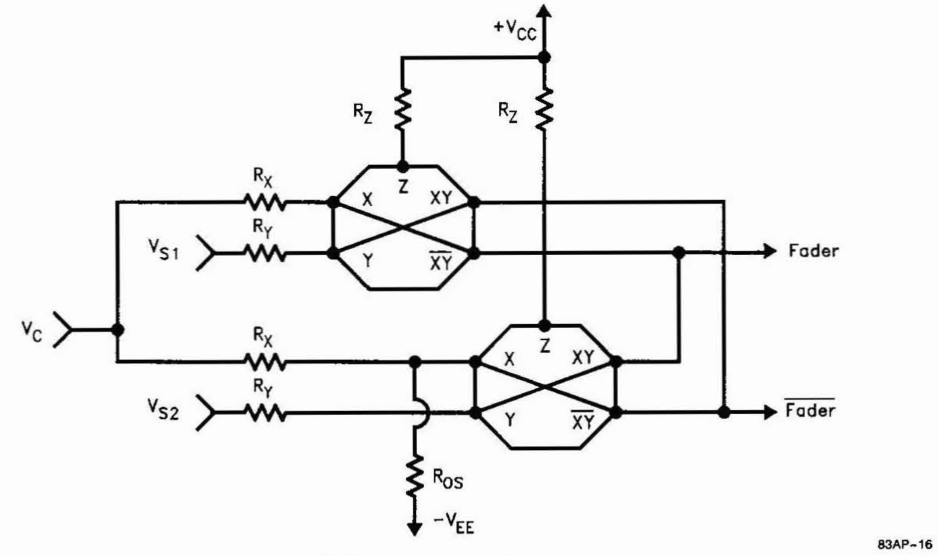
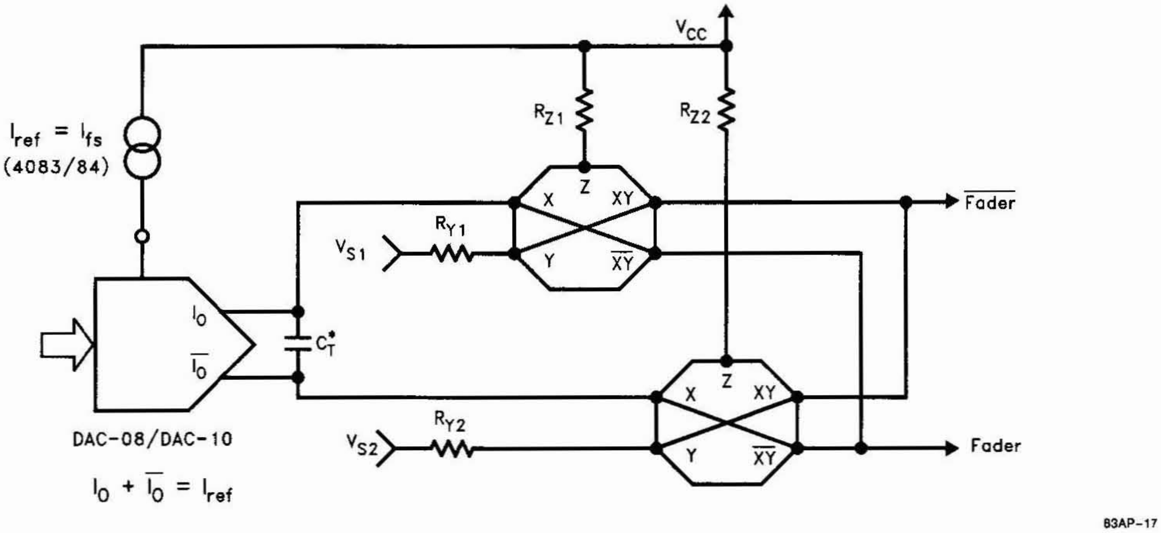

+V_CC
R_Z
R_Z
R_X
R_Y
V_S1
X
Z
XY
Y
$\overline{XY}$
Fader
V_C
R_X
R_Y
V_S2
X
Z
XY
Y
$\overline{XY}$
$\overline{Fader}$
R_OS
-V_EE
83AP-16

Figure 16. Fader


V_CC
R_Z1
R_Z2
I_ref = I_fs
(4083/84)
X
Z
XY
Y
$\overline{XY}$
$\overline{Fader}$
R_Y1
V_S1
I_O
$\overline{I_O}$
C_T*
DAC-08/DAC-10
$I_O + \overline{I_O} = I_{ref}$
X
Z
XY
Y
$\overline{XY}$
R_Y2
V_S2
Fader
83AP-17

*Optional Transient Filter Capacitor

Figure 17. Digitally Controlled Fader

Feedback Divider

The circuit of Figure 18 performs the function V_{OUT} = (Vzp − Vzn)/Vy. This expression complies with the conventions established in the literature for such circuits and the Zs in the numerator should not be confused with the Z_{IN} pin which, in this example, is run at a constant (bias) current. This type of circuit is called a feedback divider.

Figure 19 shows the frequency response of the Z(numerator) inputs as a function of amplitude with I_Z = 1.6 mA and the Y(denominator) input at it's 2 mA maximum. The response is monotonic (no foldback) and has about a 50 dB to 60 dB range with good accuracy. The frequency response of the Y(denominator) input is shown in Figure 20. Note that the bandwidth is proportional to the value of the divider input. Since a division function has a singularity with the denominator at zero, a divider's performance will degrade as this value is approached. One can obtain about a 40 dB computational range with reasonable accuracy using an untrimmed part. If higher accuracy or greater range is required of this input, one can use the optional trim network shown in the figure.

The performance curves in Figures 19 and 20 are for I_Z = 1.6 mA. For lower values of I_Z the cutoff frequencies will be proportionally lower.

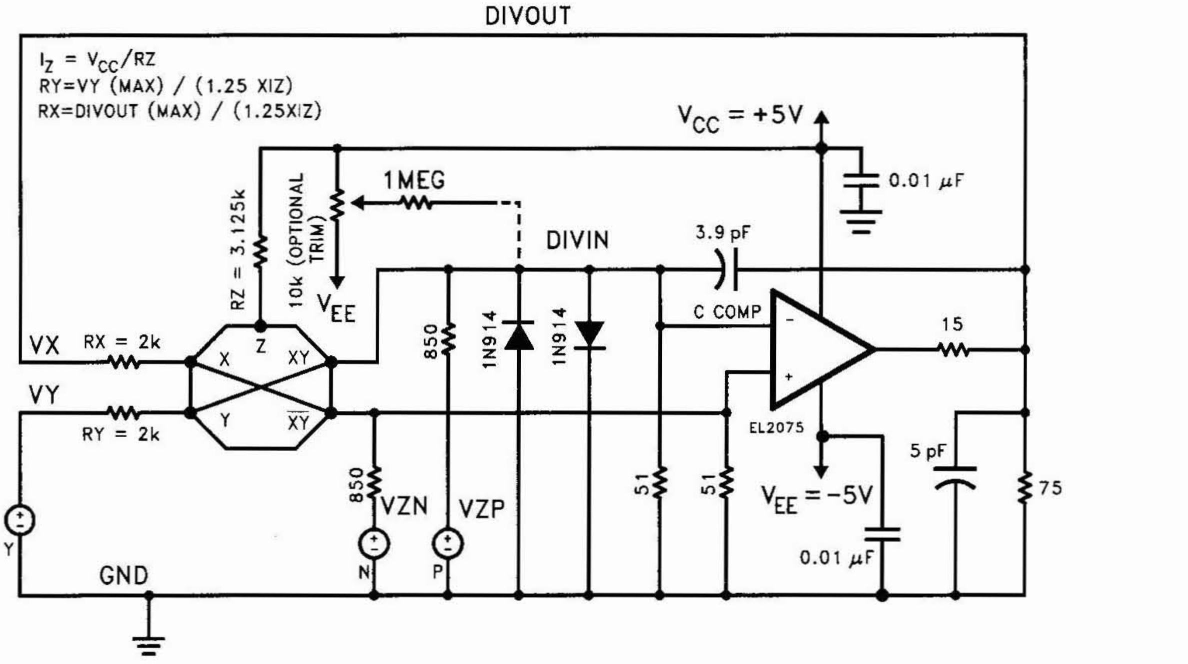
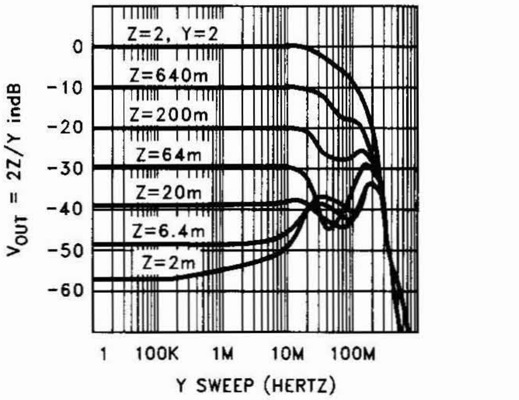
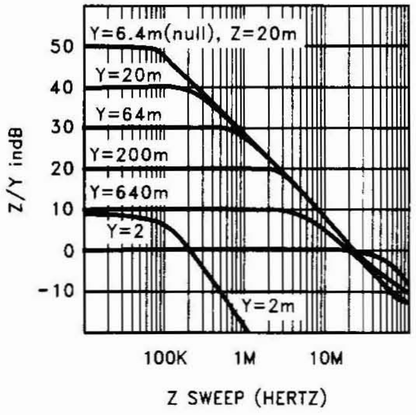

DIVOUT
$I_Z = V_{CC}/RZ$
RY=VY (MAX) / (1.25 XIZ)
RX=DIVOUT (MAX) / (1.25XIZ)
V_{CC} = +5V
0.01 µF
1MEG
RZ = 3.125k
10k (OPTIONAL TRIM)
V_{EE}
DIVIN
3.9 pF
C COMP
VX
RX = 2k
X
Z
XY
VY
Y
$\overline{XY}$
RY = 2k
850
1N914
1N914
15
EL2075
5 pF
850
VZN
VZP
51
51
V_{EE} = −5V
75
0.01 µF
Y
GND
N
P
83AP-18

Figure 18. Fast Feedback Divider (with Inverting and Non-inverting Inputs)



83AP-19

Figure 19. Divider Frequency Response (Denomination at Maximum, 10 dB Numerator Steps



83AP-20

Figure 20. Divider Frequency Response (Numerator at −40 dB of Full Scale, Denominator in 10 dB Steps)

Quality Programs

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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PERFORMANCE ANALOG INTEGRATED CIRCUITS

Summary of Elantec's Reliability and Quality Assurance Policy and Procedures
QRA-1

Forward

This document summarizes Elantec's philosophy and policies towards Quality Assurance and Reliability for both MIL-STD-883 and commercial products. It is intended as an overview only, to give the reader a quick visualization of Elantec's capabilities and standard procedures. Elantec's quality system is structured on/and certified to ISO 9001.

Customers wishing more detail should refer to either "QRA-3, Elantec's 883B program for Hybrid Integrated Circuits", or contact us at the factory. Also available are "QRA-4 Hybrid S-Flow" and "QRA-5 Monolithic Class S Flow". Our facilities and process documentation are available for customer inspection at any time. We welcome you to visit us at your earliest convenience, as we believe our factory to be "our best salesman".

Philosophy

Elantec was founded on the principle of supplying Analog Integrated Circuits of advanced performance with quality levels beyond that normally available from the semiconductor industry. Our product range has been intentionally limited to service commercial, industrial and Military/Areospace applications only. It is our firm belief that by placing quality and reliability over all other objectives, we will achieve our goal of providing our customers maximum cost-effectiveness and long term satisfaction.

Using both monolithic and hybrid technologies, Elantec provides leading edge Analog Integrated Circuit devices whose performance routinely exceeds that of most commercial manufacturers.

It is our policy to insure that each and every device is:

1) Designed to provide maximum long-term reliability.
2) Manufactured in strict compliance with thoroughly documented procedures in a tightly controlled environment.
3) Tested to insure that every device meets each parameter specified on the data sheet or customer specification.
4) Covered by a rigorous regularly scheduled Quality and Reliability Audit Program.

Commercial/Industrial Program Summary

Elantec:

- Provides the most thoroughly tested product available.
- Specifies clearly on each data sheet exactly which parameters are 100% tested, Q.A. sampled, or guaranteed by design and characterization.
- Performs 100% A.C. testing of critical performance parameters (see individual data sheets).
- Operates to extremely tight AQL sampling plans (see Table I).
- Provides 100% Temperature Cycling, Centrifuge, Fine and Gross Leak checks on all hermetic package commercial devices (see Table II).
- Uses superior manufacturing processes for microcircuit devices to eliminate failure modes inherent in conventional assembly techniques.
- Maintains traceability on production lots.
- Manufactures thick film substrates and performs final electrical testing of commercial devices 100% in our Milpitas, California facility.

Military/Aerospace Program Summary

Elantec:

- Provides product screened and quality performance tested in accordance with MIL-STD-883.
- Is an approved supplier to DESC/SMD drawing numbers:

78013—similar to ELH0002H/883B
80013—similar to ELH0032G/883B
80014—similar to ELH0033G/883B
85087—similar to ELH0041G/883B
85088—similar to ELH00021K/883B
85089—similar to ELH0101K/883B or
ELH0101AK/883B

Summary of Elantec's Reliability and Quality Assurance Policy and Procedures
QRA-1

- Maintains an on-going product qualification and reliability monitor program. Current quality conformance data is always available to support military product.
- Manufactures MIL-STD-883 Hybrid products 100% in the United States in our facility in Milpitas, California.
- Specifies clearly on each data sheet exactly which parameters are 100% tested, Q.A. sampled, or guaranteed by design and characterization.
- Performs 100% A.C. testing of critical performance parameters (see individual data sheets).
- Operates to extremely tight AQL sampling plans (see Table I).
- Facilities have been surveyed and approved by major military/aerospace customers—names available upon request.
- Maintains complete traceabilty and manufacturing history on each production lot.
- Has been audited, certified, and qualified by DESC to MIL-STD-1772.
- Maintains shelf stock of MIL-STD-883 product for rapid delivery at competitive prices.
- Welcomes customer Source Control Drawings, special selections and custom reliability processing.

Facility

The Milpitas factory has been certified by many customers to meet the requirements of MIL-I-45208. Defense Electronics Supply Center (DESC) has performed an audit and certified Elantec to the Hybrid Line Certification Specification, MIL-STD-1772.

All military hybrid product manufactured by Elantec is completely built in the U.S.A. at our factory in Milpitas, California, all testing is performed in Milpitas. Commercial product thick film processing and all electrical testing is done in Milpitas. Commercial assembly may be done either in Milpitas or offshore.

The factory has 46,000 square feet of space. 10,000 square feet is a Class 1000 clean room (Fed. Std 209) where wafer fabrication, assembly and electrical test are performed. All assembly operations are done under Class 100 laminar flow hoods. Temperature and humidity are monitored and controlled in accordance with MIL-STD-883. Gases are filtered at point of use. De-ionized water is filtered and bacteria controlled, and resistivity is continuously monitored. All semiconductor work-in-process is stored in nitrogen-purged dessicators.

A comprehensive ESD program is in effect. All work surfaces are either stainless steel or conductive laminate. Every work surface is grounded for Electrostatic Discharge protection in accordance with OSHA requirements. Shelving at all inventory locations is grounded. Floors in all manufacturing and inventory areas are covered with conductive tile attached with conductive tile cement. Conductive heel straps are worn by all operators. All product, commercial and military, is marked with an equalateral triangle to indicate static sensitivity in accordance with MIL-I-38535 and MIL-H-38534. Finished product is packaged in anti-static materials which are completely shielded by aluminum-lined boxes or conductive bags.

Elantec maintains complete *in-house* capability to 100% process devices to the requirements of MIL-STD-883 Class B. Additional in-house capability includes Particle Impact Noise Detection (PIND). All testing for initial product qualification and periodic quality conformance is performed in-house except for moisture resistance, internal water vapor, mechanical shock and vibration which are performed at DESC certified laboratories.

All manufacturing equipment is calibrated in accordance with MIL-STD-45662 as modified by MIL-I-38535 and MIL-H-38534.

Elantec maintains a complete Quality manual (QAP9000). The plan is available for review by customers at Elantec. Included within the Program Plan is a complete equipment and facilities list.

Quality System

All quality assurance functions at Elantec report to the President and are totally independent of the manufacturing organization. These functions include Incoming Quality Control, In-Process Quality Control, Product Qualification, Quality Conformance, Document Control, Customer Specification Review, Internal Quality Audit, and Failure Analysis.

Elantec's operation is controlled by a thorough documentation system. Peripheral support systems such as document control, calibration, customer specification review, the ESD program, and archives are fully documented as to procedure and responsibility. All manufacturing operations have specifications describing the equipment operation and procedures. Product manufacturing flow charts define precise operational sequences to insure each lot is built in conformance to Elantec and Military requirements. All raw materials are purchased to Elantec Procurement Documents. Military package materials and finishes are in accordance with MIL-I-38535 and MIL-H-38534.

Raw materials are inspected to rigorous requirements by Incoming Quality Control prior to release for manufacture. Minimum inspections for hybrid military products are those specified in MIL-STD-883 Method 5008 for Element Evaluation. Many of these tests are performed more often than required by the military standards. In addition, various other tests are performed to insure the integrity of each raw material. Similar tests are performed on raw materials destined for commercial products.

Travelers used throughout Elantec are structured to maintain traceability of raw materials and operators to each manufacturing lot. Lots are shipped with accurate lot numbers on the containers to provide backward traceability should this ever be required.

In-line Quality Control gates monitor the process to insure critical manufacturing operations are under control. These include wire bond pull, die shear, die and preseal visual inspection, mark permanency, and electrical test.

Before release of any Elantec product, an exhaustive product qualification is performed. This includes life testing on multiple lots and various mechanical package tests. On-going Reliability Monitor testing is done on all Commercial product and package families. The reliability monitors include electrical and mechanical test as described in QAP0073 Military products subsequently receive complete Group A, B, C, and D per MIL-STD-883 testing prior to shipment of the first part. Military Quality Conformance testing is done in compliance with Method 5005 or Method 5008.

In Conclusion

It has been and continues to be Elantec's goal to provide product of the highest quality available. We believe the extra effort we have expended in the design, construction techniques, testing and quality control procedures results in a product which is observably superior in performance, consistently higher in quality, and provides greater reliability in the actual application. We also believe such product will provide the overall lowest cost and greatest long term satisfaction to the customer.

Table I. QA Inspection Sampling Plan

Die Visual:	0.25% AQL			
Precap Visual:	0.25% Military, 1.5% Commercial			
Mark Permanency:	4 Parts/Day/Package			
Electrical Test (All Products):				
Non-Military Lots	**LTPD** (%)	**Sample Size**	**Accept No.**	**Equiv. AQL(%)**
Computer Tests at Room Temp	2	116	0	0.04
Computer Tests Hot	3	76	0	0.07
Computer Tests Cold	5	45	0	0.11
A.C. Bench Tests at Room Temp	2	116	0	0.04
Military Lots				
Computer Tests at Room Temp		116	0	0.04
Computer Tests Hot		116	0	0.04
Computer Tests Cold		116	0	0.04
A.C. Bench Tests at Room Temp		116	0	0.04

Note 1: Computer tests are all D.C. tests plus A.C. on those products where A.C. can be tested on the enhanced LTX automatic tester.

Note 2: All military lots are Q.A. sampled at all temperatures.

Note 3: All non-military lots (E+, Prime, Commercial) are Q.A. sampled at room temperature (D.C.) Until adequate history is developed on these new products, each lot is sample tested at temperatures and on the bench. Non-military lots of mature products with adequate history are skip lot tested at temperatures or on the bench, e.g., they are Q.C. sampled every fourth or fifth lot. (This frequency may change with time as more product history is developed.)

Note 4: If a device which is in skip lot mode should suffer a lot failure, every lot is then tested until three lots in succession are passed before returning to skip lot mode.

Table II. Elantec Hybrid Metal Can Process Flow Summary

Operation	Commercial	/883B(1)
Incoming QC		
Die Evaluation	X	X
Package Evaluation	X	X
Raw Material Evaluation	X	X
Assembly		
Wire Bond Pull QC	X	X
Die Shear QC	X	X
Internal Visual	X	X
Seal	X	X
Stabilization Bake	2 Hours	24 Hours
Temperature Cycling	5 Cycles	10 Cycles
Constant Accel.		
TO-3, LCC (5KG)	X	X
TO-5 (30KG)	X	X
TO-8 (20KG)	X	30KG
Fine Leak		
TO-3 (2x10^7 cc/sec)	X	X
TO-5 (5x10^8 cc/sec)	X	X
TO-8, LCC (5x10^8 cc/sec)	X	X
Gross Leak		
With Pressurization		X
No Pressurization	X	
Class Test		X
Burn-in		160 Hours
Electrical Test 25°C(2)	X	X
Q.C. 25°C(2)	X	X
Electrical Test Cold(2)		X
Q.C. Cold(2)	X	X
Electrical Test Hot(2)		X
Q.C. Hot(2)	X	X
External Visual	X	X
Group B, C, D Testing		X

Note 1: For complete details of Elantec's "/883B" military program see "QRA-3, Elantec's 883B Program for Hybrid Integrated Circuits."

Note 2: Electrical tests performed are as documented on the individual device data sheet.

Table III. Elantec Monolithic Process Flow Summary

Operation	Commercial
Incoming QC	
Package Evaluation	X
Raw Material Evaluation	X
Assembly	
Wire Bond Pull QC	X
Die Shear QC	X
Internal Visual	X
Seal	X
Temperature Cycling	5 Cycles
Constant Accel. (30KG)	X
Fine Leak (5x10^8 cc/sec)	X
Gross Leak	
With Pressurization	
No Pressurization	X
Class Test	
Burn-in	
Electrical Test 25°C(1)	X
Q.C. 25°C(1)	X
Electrical Test Cold(1)	
Q.C. Cold(1)	X
Electrical Test Hot(1)	
Q.C. Hot(1)	X
External Visual	X
Group B, C, D Testing	

Note 1: Electrical tests performed are as documented on the individual device data sheet.

Electro Static Discharge (ESD) Sensitivity

All semiconductor devices are sensitive to Electro Static Discharge (ESD) to some degree. For this reason, Elantec treats *all* of our devices as sensitive. Customers are urged to use similar controls throughout their facilities. This will optimize yields, prevent latent reliability problems, and eliminate component quality complaints which are due to ESD. Even components which are returned to Elantec for analysis should be handled with proper ESD procedures.

Device Design and Processing

Wherever possible, ESD protection networks are used on device pins. Metal routing and oxide thicknesses are carefully considered for optimum ESD performance. Testing per MIL-STD-883 Method 3015 is used to determine device and process performance.

Work Areas

Floors are covered with conductive tiles, attached with conductive adhesive.

Operators wear non-static generating or static dissipative smocks. Heel straps are used to ground the operators. Heel straps are checked daily for effectiveness.

Work station surfaces are conductive laminates or stainless steel. These are tied to Earth ground through protective resistors. Grounds are routinely inspected. Air ionizers are used to neutralize charges in areas which may generate static.

Storage shelving is grounded through protective resistors.

Handling

All handling containers (boxes, bags, etc.) are conductive. Pink poly which depends on surface properties and may wear out is not used. Common plastics (such as polystyrene and polypropylene) which are nasty static generators are *never* used in the work area.

Marking

All devices are marked with an equalateral triangle to warn the user that they are ESD sensitive.

Packaging

Devices are packed in either antistatic materials which are surrounded by a conductive Faraday shield or directly in conductive materials. The shielded containers are labeled with a yellow ESD warning label. Only antistatic treated "popcorn" is used as filler material in shipping boxes.

Macromodel Information

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Intro Macromodel Information

The selected macromodels provided at the end of product datasheets are being supplied to users as an aid to circuit designs. While it reflects reasonably close similarity to the actual device in terms of performance, it is not suggested as a replacement for breadboarding. Simulation should be used as a forerunner or a supplement to traditional lab testing.

Users should very carefully note the following factors regarding these models:

Model performance in general will reflect typical baseline specs for a given device, and certain aspects of performance may not be modeled fully to keep the model as simple as possible thus minimizing computer running time. For example, PSRR and CMRR effects, parametric variation with temperature, operation under output short circuit conditions, and input noise sources are not included in the models. The current mode feedback amplifiers are not slew rate limited and yield optimistic values for large signal pulse responses.

While reasonable care has been taken in their preparation, we cannot be responsible for correct application on any and all computer systems. Model users are hereby notified that these models are supplied "as is", with no direct or implied responsibility on the part of Elantec, Inc. for their operation within a customer circuit or system. Further, Elantec, Inc. reserves the right to change these models without prior notice.

In all cases, the current data sheet information for a given real device is your final design guideline, and is the only actual performance guarantee. For further technical information, refer to individual device data sheets.

The Elantec engineering staff is in the process of improving these models, and we welcome your comments and feedback. Inquiries should be made to:

Applications Engineering Manager
Elantec, Inc.
1996 Tarob Ct.
Milpitas, CA 95035

Voice Telephone: (800) 333-6314
FAX: (408) 945-9305
TELEX: 910-997-0649

*MACROMODELS ON DISK ARE AVAILABLE UPON REQUEST.
CONTACT FACTORY OR LOCAL AREA REPRESENTATIVE.
Disks are 5¼″ Low Density for IBM PC Compatible Computers.

Glossary of Technical Terms

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

AC Coupled. AC coupling is a method of connecting a signal to any circuit in a way that removes the DC offset. The DC offset is the overall voltage level that the video signal "rides" on. One way to find the signal is to remove the DC offset by AC coupling, and then do a DC restore to add in a known DC offset (one that we selected). Another reason AC coupling is important is that it can remove harmful DC offsets.

Analog-to-Digital (A/D). This device is what all digital imaging systems use to get real-world pictures—from a TV camera, for example—into a computer. An A/D for digitizing video must be very fast, capable of sampling at clock rates of 10 to 30 million samples per second (MSPS).

Back Porch. The area of the composite video waveform following the horizontal sync pulse and right before the active video or before the terminating edge of horizontal blanking.

Bandwidth or 3 dB Bandwidth (BW, SSBW). A figure of merit of an amplifier or buffer which delineates the frequency at which the output is reduced to 0.707 (−3 dB) of the low frequency value when passing a small signal sine wave.

Black Burst. The video waveform without the active video part. Black burst is used to sync various video boxes together so that their video output is all aligned. Black burst tells the video gear the vertical sync, horizontal sync, and the chroma burst information.

Black Level. This level represents the darkest an image can get. This defines what black is for the particular image system. If for some reason the video dips below this level, it is referred to as blacker-than-black.

Blanking. On the screen, the scan line moves from the left edge to the right edge, jumps back to the left edge, and starts out all over again, on down the screen. When the scan line hits the righthand limit and is about to be brought back to the lefthand edge, the video signal is blanked so that one can't "see" the return path of the scan beam from the right to the lefthand edge. To blank the video signal, the video level is brought down to the blanking level, which may or may not be the black level if a pedestal is used. The vertical retrace is also blanked between fields.

Blanking Level. That level of the video waveform defined by the system to be where blanking occurs. This could be the black level if a pedestal is not used or below the black level if a pedestal is used.

Breezeway. The portion of the video waveform that sits between the end of the horizontal sync and before the start of burst.

Brightness. This is the intensity of the video level and refers to how much light is emitted by the display.

Burst Gate. This is a signal that tells the systems where the color burst is located within the scan line (video waveform).

Channel Separation (CHSp, CS). A figure of merit applicable to a dual, triple, or quad amplifier which specifies the ratio of the (spurious) output voltage of an undriven amplifier to the output of a driven amplifier.

Chroma Bandpass. In an NTSC or PAL video source the luma (black and white) and chroma (color) information are combined together. If you want to display an NTSC or PAL source, the luma and chroma must be split apart. The chroma bandpass filter removes the luma information from the chroma information, leaving the chroma information relatively intact. The NTSC or PAL video signal is fed into the chroma bandpass filter, where only a certain portion of the video signal is let through the portion containing the chroma information. This works reasonably well except in certain images where the luma information and chroma information overlap, meaning that we have luma and chroma information at the same time.

Glossary of Terms

Chrominance. The NTSC or PAL video signal contains two pieces that make up what you see on the screen: the black-and-white part, and the color part. Chrominance is the color part—a.k.a. chroma.

Clamp. This is basically another name for the DC-restoration circuit. It can also refer to a switch used within the DC-restore circuit. When it means DC restoration, then it's usually used as "clamping." When it's the switch, then it's just "clamp."

Closed Loop Gain (Avcl, Av). The ratio of the output voltage to the input voltage for an amplifier which is established with feedback using one or more resistors. The non-inverting closed loop gain is given by:

$$Av = \frac{Rf}{Rg} + 1$$

where: Rf = The feedback resistor (output to V_{IN-})

Rg = The gain setting resistor (V_{IN-} to ground)

Inverting closed loop gain is given by:

$$Av = \frac{Rf}{Rg}$$

Color Bars. This is a test pattern used to check whether a video system is calibrated correctly. A video system is calibrated correctly if the colors are the correct brightness, hue, and saturation. This can be checked with an oscilloscope and vector scope in the NTSC space, or by looking at the RGB levels in the RGB space.

Color Burst. Often referred to as "burst." That portion of the video waveform that sits between the breezeway and the start of active video. It tells the color decoder in the receiver how to decode the color information contained in the next line of active video. By looking at the burst, the receiver can determine what's blue, orange, or magenta. Essentially, the receiver figures out what the correct color is.

Color Decoder. This is the circuit in the video system that uses the chrominance portion of NTSC/PAL to derive the two color difference signals. The color decoder sits right after the Y/C split and before the color space convertor. The color decoder needs a 3.58 MHz signal that is accurately phase locked (PLL) to the burst. If it isn't locked well enough, then the color decoder can't figure out the right colors.

Color Encoder. The color encoder does the exact opposite of the color decoder. It takes the two color difference signals, such as I and Q in the NTSC system, and combines them into the chroma signal. The color encoder, or what may be referred to as the color modulator, uses the color subcarrier to do the encoding.

Common Mode Rejection Ration (CMRR). A figure of merit of an amplifier or buffer which delineates the ratio of the change in input common mode voltage (peak to peak) to the change in input offset voltage (peak to peak) usually specified over the common mode range of the device.

Common Mode Range or Input Voltage Range (CMIR, CMR). A figure of merit of an amplifier, buffer, or comparator which delineates the range of the input common mode voltage relative to the power supply voltage beyond which the device will malfunction. This parameter is often "specified" implicitly by CMRR by use of a specific common mode voltage.

Common Mode Voltage (Vcm). The average of the voltages applied to the inputs of a differential input amplifier. In the case of an operational amplifier, the feedback loop strives to make the inverting input equal to the non-inverting input, and the common mode voltage is essentially equal to either input.

Composite Video. If a video system is to receive video correctly, it must have several pieces of the puzzle in place. It must have the picture that is to be displayed on the screen, and it must be displayed with the correct colors. This piece is called the active video. The video system also needs information that tells it where to put each pixel. This is called sync. The display needs to know when to shut off the electron beam so the viewer can't see the spot retrace across the display. This piece of the video puzzle is called blanking. Now, each piece could be sent in parallel over three separate connections, and it would still be called video and would still look good on the screen. This is inefficient, however, because all three pieces can be combined together so that only one connection is needed. Composite video is a video stream that combines all of the pieces required for displaying an image into one signal, thus requiring only one connection. NTSC and PAL are examples of composite video. Both are made up of: active video, horizontal sync, horizontal blanking, vertical sync, vertical blanking, and burst. RGB is not an example of composite video, even though each red, green, and blue connection may contain composite sync, because all three conections are required to display the picture with the right colors.

Contrast. A video term referring to how far the whitest whites are from the blackest blacks in a video waveform. If the peak white is far away from the peak black, the image is said to have high contrast. With high contrast, the image is very stark and very "contrasty." If the two are very close to each other, the image is said to have poor, or low, contrast. With poor contrast, an image may be referred to as being "washed out"—you can't tell the difference between white and black, and the image looks gray.

Cross Conduction. A common problem in half bridge and full bridge topologies resulting in extra current flow between the upper and lower transistors during switching. This occurs when the turn-off of one transistor overlaps the turn-on of the alternate transistor.

Cross Talk (CT). See Channel Separation.

Current Feedback Amplifier (CFA). A type of operational amplifier wherein the inverting input impedance is low and is a buffered version of the voltage at the non-inverting input. A feedback resistor is always required (even when a CFA is used as voltage follower). CFA's offer very high slew rates, high frequency linearity, and exhibit bandwidths which are substantially independent of closed loop gain.

dV/dT. The change in voltage relative to time.

di/dT. The change in current relative to time.

DAC. DAC is short for digital-to-analog convertor.

DC Restoration. DC restoration is what you have to do to a video waveform after it has been AC coupled and has to be digitized. Since the video waveform has been AC coupled, we no longer know absolutely where it is. In fact, not only don't we know where it is, it also changes over time, since the voltage level of the active video changes over time. Since the resistor ladder on the flash A/D is absolutely tied to a pair of voltage references, the video waveform needs to be referenced to some known DC level in order to digitize it correctly. DC restoration is essentially putting back the DC component that was removed to make an AC coupled signal. In trying to digitize video, the DC level that we DC restore to is such that the back porch, or the blanking level if a pedestal is present, is set to the A/D's $-V_{REF}$ DC level. Therefore, when black is digitized it will be assigned the number zero and when peak white is digitized, it will be assigned the number 255, in an 8-bit system.

Decoder. The word "decoder" has several meanings:
Color Decoder. See definition under Color Decoder.
Image Compression Decoder. This is the part of an imaging system that takes the compressed image and restores it to look like the original.

Differential Gain (dG). A figure of merit of an amplifier or buffer that relates the incremental change in closed-loop gain resulting from a change in input and output voltage referenced to zero volts for a specific frequency. The gain of most amplifiers is not constant with varying DC offsets added to a constant frequency AC input signal. The parameter is most useful in applications of composite video signals and is usually expressed in percent. A standard measurement condition is for input offsets which are changed from zero to ±0.714V with an input signal of 100 mV at 3.58 MHz for NTSC and 4.43 MHz for PAL.

Differential Phase (dP). A figure of merit of an amplifier or a buffer that relates the incremental change in closed-loop phase resulting from a change in input and output voltage referenced to zero volts for a specific frequency. The phase shift through an amplifier is not completely constant with varying DC offsets added to a constant frequency AC input signal. The parameter is most useful in applications of composite video signals and is usually expressed in degrees. A standard measurement condition is for input offsets which are changed from zero to ±0.714V with an input signal 100 mV at 3.58 MHz for NTSC and 4.43 MHz for PAL.

Disable Time (t_{dis}, t_{off}). Some amplifiers provide a logic pin which enables and disables the amplifier. Usually, the supply current is reduced and the output stage is placed at a high impedance when disabled. Disable time is defined as the time from the edge of the disabling pulse to the time that the output of the amplifier falls to 50% of the pre-disabled value.

Enable Time (t_{dis}, t_{off}). Some amplifiers provide a logic pin which enables and disables the amplifier. Usually, the supply current is reduced and the output stage is placed at a high impedance when disabled. Enable Time is defined as time from the edge of the enabling pulse to the time that the output of the amplifier has increased to 50% of its final (non-disabled) value.

Encoder. As with decoder, there are two meanings to this word:
Color Encoder. See definition under Color Encoder.
Image Compression Encoder. This is the part of the imaging system that takes the original image and squeezes out redundant information so that the image will take up less space than before.

Equalization Pulses. These are two groups of pulses, one that occurs before the serrated vertical sync and another group that occurs after. These pulses happen at twice the normal horizontal scan rate. The reason these pulses exist are to ensure the 2:1 interlacing of the NTSC or PAL systems. (See "field.")

Fade. Fading is a method of switching from one video source to another video source.

Fall Time (tf). See Transient Response Time.

Field. A TV screen is made using two fields, each one containing half of the scan lines needed to make up one frame of video. One field contains the even-numbered scan lines while the other field is made up of the odd-numbered scan lines. Each field is displayed in its entirety-therefore, all of the odd-numbered scan lines are displayed, then the even, then the odd, and so on.

Fields only exist for interlaced scanning systems such as NTSC or PAL. So for NTSC, which has 525 lines per frame, a field has 262½ lines, and two fields make up a frame.

Filter. In general, a filter is used to remove unwanted information from the input signal. Every signal has a spectrum, which is the amount of different frequencies contained within the signal. Filtering lets you subtract or "filter" out certain frequencies. If you have some high-frequency information, such as noise, in with the signal that you really want, then a low-pass filter is used. A low-pass filter "passes" frequencies below a certain point and stops frequencies above that same point. A high-pass filter does just the opposite—it stops low frequencies and passes the high frequencies. A bandpass filter lets through frequencies within a certain range of "band," but stops frequencies outside of the band.

Flash A/D. This is a really fast method for digitizing a signal. The signal to be digitized is provided as the source for one input of a whole bank of comparators. The other input is tied to a tap of a resistor ladder, with each comparator tied to its own tap. This way, when the input voltage is somewhere between the top and bottom voltages connected to the ladder, the comparators output a code. This means that all the comparators output a "yes" up to the input voltage and a "no" above that. The A/D then takes this string of Yes's and No's and converts them into a binary number which tells where the Yes's turned into "No's." See the definition of resistor ladder for more details, if you're interested.

Flicker. Flicker occurs when the frame rate of the video is too low.

Front Porch. This is the area of the video waveform that sits between the start of horizontal blank and the leading edge (start of) horizontal sync.

Full Bridge. Two half bridges. (See Half Bridge.)

Gain Bandwidth Product (GBW). The frequency where the open loop gain of a voltage feedback amplifier falls to one (0 dB). Sometimes the Gain is measured at a frequency lower than the one at which the gain is equal to unity. The product of the measured gain at the test frequency is then cited as GBW on the data sheet.

Gain Flatness (GFP, GFR). A figure of merit of an amplifier that delineates the closed loop deviation of the gain over a range of frequencies. It is an expression of how constant the response of an amplifier or network is over a specified range of frequencies.

Gate Oxide. The dielectric between the channel and control gate of an mos transistor.

Genlock. A video source provides all of the information necessary to view—or in the case of a computer, grab—the picture. This includes the information from the scene itself, color decoder information, and synchronization information so the receiver knows where to put the picture. When a computer is involved, it has its own sync signals that are running independently of the sync signals sent by the camera. Genlocking is the act of getting the computer's sync signals to line up with the camera's sync signals. The sync signals from the camera and the computer must be locked together if the picture from the camera is to be shown correctly on the computer's screen. This is performed by a genlock circuit. A genlock circuit may employ several techniques to do its job, with the most popular being a phase locked loop.

Glossary of Terms

Half Bridge. A circuit topology consisting of an upper transistor going to V_{DD}, a lower device going to V_{SS}, and a common node in between.

Horizontal Scan Rate. This is how fast the scanning beam in a display or a camera is swept from side to side. In the NTSC system this rate is 63.556 µs, or 15.734 kHz.

Horizontal Sync. This is the portion of the composite video signal that tells the receiver where to place the image in the left-to-right dimension. The horizontal sync pulse tells the receiving system where the beginning of the new scan line is.

Hysteresis. Positive feedback applied to increase noise immunity by varying the switch point depending on which state the device is in.

Input Bias Current (I_b, I_I, I_b+, I_b-). A figure of merit an amplifier, buffer, or comparator which delineates the input currents of the amplifier under linear (normal) operating conditions. Input bias current is often the average of the two input currents and may be sensitive to the common mode input voltage.

Input Impedance (R_{IN}). A figure of merit of an amplifier, buffer, or comparator which delineates the ratio the change in input voltage to the change in input current. In general, voltage feedback amplifiers and comparators exhibit high input impedance at both the inverting and non-inverting inputs, but current feedback amplifiers exhibit low input impedance at the inverting input by design. Users should be aware that the "Input Impedance" is a DC figure of merit and that, in general, there is an input capacitance as well in parallel with the input impedance. The inverting input of a Current Feedback Amplifier can also appear to be inductive.

Differential Input Impedance applies to amplifiers with differential inputs and is measured by applying a small differential voltage to the inputs while measuring the change in bias current.

Input Noise Voltage ($\overline{en}$). A figure of merit of an amplifier, or buffer that delineates the average noise voltage referred to the input under specific operating conditions. Usually, a curve of the noise characteristics is presented in the typical performance curves of the data sheet. A simple way of thinking of noise is to consider it "AC" offset voltage which dictates the overall system accuracy and the minimum signal which can be resolved. The noise source is often modeled as noise generator in series with one of the (differential) inputs of the amplifier.

Input Noise Current ($\overline{in}$). A figure of merit of an amplifier or buffer that delineates the average noise current at the inputs. Since the noise current usually flows through resistors in a typical application, it is converted to a noise voltage referred to the input. It is usually modeled as a current source from each input to ground.

Input Offset Current (I_{OS}). A figure of merit of an amplifier or comparator which delineates the difference in the currents into or out of the input terminals when the output is zero for an amplifier or to a specified output voltage for a comparator.

Input Offset Voltage (V_{OS}). A figure of merit of an amplifier or comparator which is the voltage that must be applied to the inputs of an amplifier to make the output zero or the output of the comparator a specified voltage.

Input Resistance. See Input Impedance.

Large Signal Voltage Gain (A_{VOL}). An open loop figure of merit for an amplifier or comparator which is the ratio of the output voltage to the change in input voltage required to move the output from zero volts to the specified voltage.

Latch-up. Results from parasitic action of the scr in CMOS circuits.

Locked. When one signal is synchronized to another by feedback, usually using a PLL.

Loop Gain. The difference between the open loop gain and closed loop (noise gain) of the circuit.

Luminance. As mentioned in the definition of chrominance, the NTSC and PAL video systems use a signal that has two pieces: the black-and-white part, and the color part. The black-and-white part is the luminance. It was the luminance component that allowed color TV broadcasts to be picked up by black-and-white TVs and still remain viewable.

Monochrome. A monochrome signal is a video source having only one component of color.

NTSC. An abbreviation for National Television Standards Committee.

Open Loop Transimpedance (R_{OL}). A figure of merit for a Current Feedback Amplifier which delineates the ratio of the change in output voltage to the change in current of the inverting input. R_{OL} is similar to Large Signal Voltage Gain, A_{VOL}, of a voltage feedback operational amplifier and is usually expressed in megohms.

Output Current (I_{OUT}). A figure of merit of an amplifier or buffer which delineates the current that can be sinked or sourced by the device under linear operating conditions.

Output Impedance (R_{OUT}). A figure of merit for an amplifier for a buffer or an amplifier which delineates that ratio of the change in output voltage to the change in output current usually for a specific load (R_L) and source (R_S) resistance. In general, output impedance for an amplifier is not particularly meaningful since the open loop output impedance is reduced by the loop gain of the amplifier. The output impedance for an (open loop) buffer, on the other hand is very meaningful in that, to the first order, it dictates the voltage gain of the device for a given load resistance (R_L).

Output Resistance. See Output Impedance.

Output Voltage Swing (V_{OUT}). A figure of merit of an amplifier which delineates the voltage that can be obtained from the device under linear conditions without clipping.

Offset Voltage Drift (dV_{OS}/dT or TCV_{OS}). A figure of merit of an amplifier, buffer, or comparator which delineates the average change in input offset voltage due to thermal effects over the specified operating temperature range of the device. It is often expressed in μV per degree Centigrade.

Overshoot (OS). A figure of merit of an amplifier or buffer which delineates the departure from the output from the final value usually on the rising or falling edge under small signal closed loop conditions.

PAL. PAL stands for Phase Alternate Line and PAL is to Europe as NTSC is to North America and Japan. In other words, PAL is the video standard used in Europe and a few other countries. There are a few differences. PAL uses 625 lines per frame while NTSC has 525 lines. Therefore, PAL has higher resolution. The frame rate of NTSC is 60 fps while for PAL it is 50 fps. This means the update rate for NTSC is higher and therefore there is more flicker with PAL. PAL uses the YUV color space while NTSC uses YIQ. PAL alternates the phase of every line color. The color-phase sequence of the chrominance signal is periodically reversed to cancel out hue errors. It is becoming increasingly important for imaging systems suppliers to produce equipment that can be sold worldwide without many manufacturing difficulties.

Peak White. Peak white is the highest point in the video waveform that the video level can reach and still stay within spec. If for some reason the level does become greater than peak white, it's referred to as whiter-than-white.

Pedestal. Pedestal is an offset used to separate the active video from the blanking level. When a video system uses a pedestal, the black level is above the blanking level by a small amount. When a video system doesn't use a pedestal, the black and blanking levels are the same.

Phase Margin. A figure of merit of an amplifier that delineates the difference between the phase of the output voltage and 180 degrees when the gain is one.

Pixel Clock. The pixel clock is used to divide the incoming horizontal video into pixels. This pixel clock has to be stable (a very small amount of jitter) relative to the incoming video or the picture will not be stored correctly. The higher the frequency of the pixel clock, the more pixels that will appear across the screen.

Power Supply Rejection Ratio (PSRR). A figure of merit of an amplifier, buffer, or comparator that delineates the ratio of the change in input offset voltage to the change in power supply voltage producing it.

Rails. Refers to the positive and negative supplies.

Response Time (tpd). A figure of merit of a comparator that delineates the time between the application of input step and the time that the output crosses a specified logic threshold.

Retrace. Retrace is what the electron beam does when it gets to the righthand edge of the display to get back to the lefthand edge. Retrace happens during the blanking time.

Rise Time (tr). See Transient Response Time.

S-VHS. S-VHS is an enhancement to regular VHS. S-VHS provides better resolution and less noise than VHS. S-VHS requires the luma and chroma components to be separate inputs to the VCR, while standard VHS only requires the composite NTSC signal. That's one of the reasons for the improved quality. S-VHS doesn't combine the luma and chroma so they don't have to be split apart. In the world of electronics, any time you combine two signals together, generally the two signals are degraded somewhat after you split them back out.

Saturation. Saturation is the amount of color present. For example, a lightly saturated red looks like pink, while a fully saturated red looks like the color of a red crayon. Saturation does not mean the brightness of the color, just how much "pigment" is used to make the color. The more "pigment," the more saturated the color is.

Scan Line. A scan line is an individual sweep across the face of the display by the electron beam that makes the picture.

Secam. This is another TV format similar to PAL. The difference between the two is that in secam, the chrominance if FM modulated.

Serration Pulses. Serration pulses appear in the broad vertical sync pulse interval at a 2H line rate in order to maintain H-lock during vertical retrace.

Settling Time (ts). A figure of merit of an amplifier or buffer that relates the time between the initiation of an input step to the time that the output voltage has settled to a specified error band. If the output is ringing, the last reentry into the settling bound is defined as the end of the settling event. Settling time is usually a function of the input step size.

Shoot-Thru. Same as Cross Conduction.

Skew (clock). When two complementary signals have unbalanced delay.

Slew Rate (SR). A figure of merit of an amplifier or buffer which delineates the ability of the amplifier to accurately follow a large input step voltage. It is usually measured from the 20% to 80% point (and vice versa) of the output wave form.

Super Invertor. A circuit configuration which minimizes cross conduction.

Supply Current (Is, I_{CC}, I_{EE}, Is+, Is−). A figure of merit of an amplifier, buffer, or comparator that delineates the current required from the power supplies to operate the device with no load and the output at zero volts.

Sync. Sync is a fundamental piece of information for displaying any type of video. Essentially, the SYNC signal tells the display where to put the picture. The horizontal sync, or HSYNC for short, tells the display where to put the picture in the left-to-right dimension, while the vertical sync (VSYNC) tells the display where to put the picture from top to bottom.

Sync Generator. A sync generator is a circuit that provides sync signals. A sync generator may have a genlock input, or may not.

Sync Noise Gate. The sync noise gate is used right before the sync stripper to define an area within the video waveform where the sync stripper is to look for the HSYNC pulse. Anything outside of this defined window will be rejected by the sync noise gate and won't be passed on to the sync stripper.

The main purpose of the sync noise gate is to make sure that the output of the sync stripper is nice, clean, and correct.

Sync Stripper. A composite video such as RS-170, NTSC or PAL contains the video information, which is the picture to be displayed, and information that tells the receiver where to put this video information on the display. The latter piece of information is called sync. A sync stripper pulls out the sync information from the composite video waveform and throws the rest away.

Transient Response Time (tr, tf). A figure of merit of an amplifier or buffer that delineates the closed loop response of the output of an amplifier in response to a small signal step input. Rise Time (tr) is usually specified from the 10% to the 90% point of the output and refers to the positive going edge; whereas Fall Time (tf) refers to the negative going edge of the output (or from 90% to 10%).

Unity Gain Bandwidth. A figure of merit of an amplifier that delineates the frequency where the amplifiers Large Signal Voltage Gain, A_{VOL}, has rolled off to unity. For amplifiers that are unity gain stable, the unity gain bandwidth and Gain Bandwidth product are identical, but decompensated amplifiers often specify Gain Bandwidth Product at frequencies that are below the point where the amplifier's A_{VOL} is one.

Vertical Sync. This is the portion of the compositie video signal that tells the receiver where the top of the picture is.

Video Mixing. Video mixing is taking two independent video sources and editing them together to create a new, third video source. This can be done by fading from a one source to the other.

Video Waveform. The video waveform is what the signal "looks" like to the receiver or TV. The video waveform is made up of several parts that are all required to make up a TV picture that can be accurately displayed. Each component is necessary.

White Level. This level represents the lightest an image can get, and defines what white is for the particular image system. By calibration, this is the highest video level allowed in the system. If for some reason the video goes above this level, it is referred to as "whiter-than-white."

Y/C. The Y/C designation is shorthand for luminance and chrominance. You will also see this term used in the description of the S-VHS video tape format. The S-VHS format records the luma and chroma separately while standard VHS records them together.

Y/C Split. A Y/C splitter circuit is what's used in a TV set or imaging device to pull the luminance and chrominance apart in an NTSC or PAL system. This is the first thing that any NTSC or PAL receiver must do. The composite video signal is first fed to the Y/C splitter so that the luma and chroma can then be decoded further. The two popular methods for implementing a Y/C split are a chroma bandpass/chroma trap combo or a comb filter arrangement.

YIQ. YIQ is the color space used in the NTSC color system. The Y component is the black-and-white, (luma) portion of the image. The I and Q parts are the color components placed over the black-and-white, or luma, component.

YUV. YUV is the color space used by the PAL color system. As with the YIQ colorspace, the Y is the luma component while the U and V are the color components.

Package Outlines

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Soldering Packages to PC Boards

DIP Packages

Wave soldering is recommended for DIP packages. Solder plated boards are recommended. Rosin mildly activated (RMA) flux is needed. Wave soldering using a dual wave system at 250°C ±10°C for two seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Hand soldering, Elantec's DIP packages will survive a peak temperature of 300°C (at leads) for a maximum period of 10 seconds.

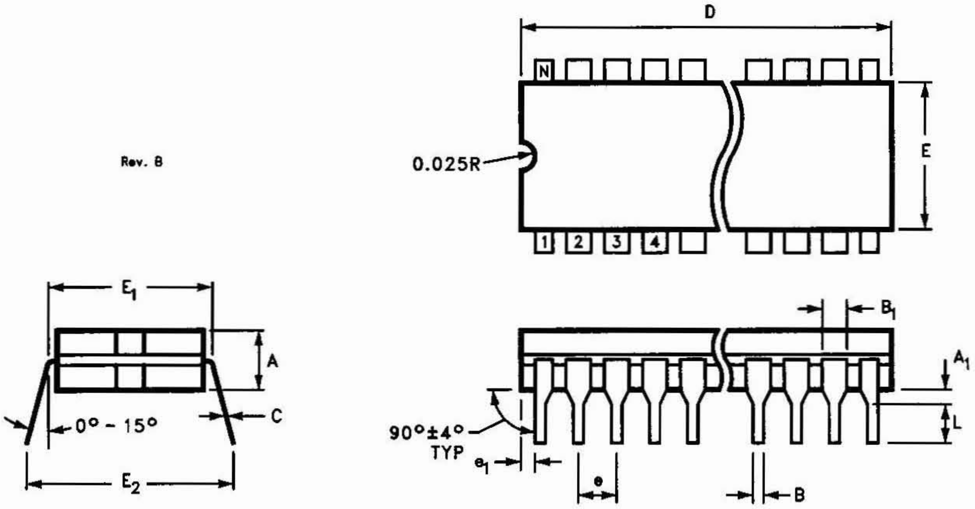
Surface Mount Packages

Wave soldering and vapor phase or infrared (IR) reflow can be used for soldering surface mount packages to PC boards. Solder plated boards are recommended for wave soldering and vapor phase or IR reflow methods.

Wave Soldering: Adhesive is used to hold components on the boards during wave soldering. Place components on the board and cure adhesive before wave soldering. Rosin mildly activated (RMA) flux or organic flux is needed. Wave soldering using a dual wave system at 250°C ±10°C for a maximum of two seconds per wave is preferable. Thorough cleaning of boards after soldering is required.

Reflow Soldering: Screen solder paste on board and attach components to board. Solder paste with RMA flux is recommended. Bake boards at 65°C–90°C for 15 minutes. Preheat boards to within 60°C–70°C of the solder temperature. To reflow solder paste with vapor phase method, the solder paste temperature must be maintained at or above 200°C for at least 30 seconds. The components temperature can not exceed 215°C. For the IR reflow method, the solder paste temperature must be maintained at or above 200°C for at least 30 seconds. The components temperature can not exceed 220°C. The temperature/time ramp-up during vapor phase or IR reflow shall be no greater than 2°C/sec.

Hand soldering, Elantec's surface mount packages will survive a peak temperature of 260°C (at leads) for a maximum period of 10 seconds.

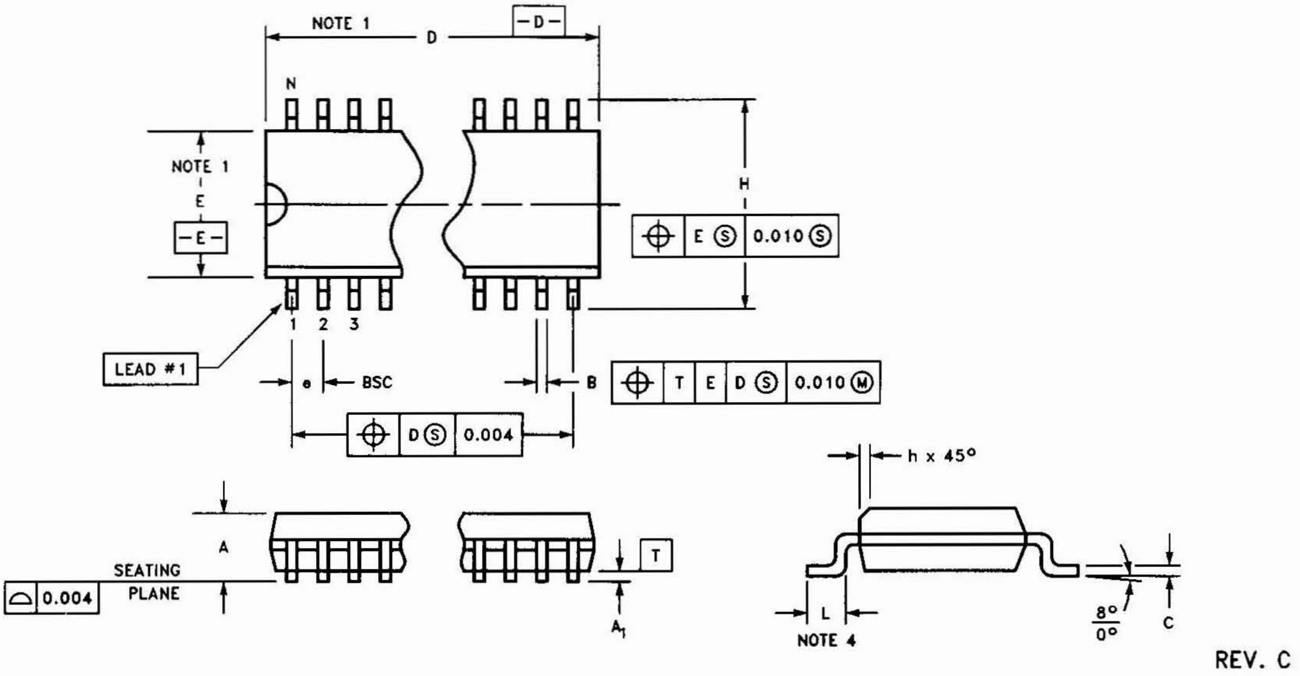


MDP0016 Rev. B

CerDIP Package

Lead Finish (Coml)—Tin Plate or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP

Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max
A	0.140	0.160	0.140	0.160	0.140	0.160	0.140	0.160
A_1	0.115	0.055	0.020	0.050	0.015	0.060	0.020	0.050
B	0.016	0.023	0.016	0.021	0.014	0.026	0.016	0.021
B_1	0.050	0.065	0.050	0.060	0.038	0.068	0.050	0.060
C	0.008	0.012	0.008	0.012	0.008	0.018	0.008	0.012
D	0.375	0.395	0.760	0.785	0.940	0.960	1040.925	1.060
E	0.245	0.265	0.220	0.291	0.220	0.310	0.2780	0.298
E_1	0.300	0.320	0.300	0.320	0.290	0.320	0.300	0.320
E_2	0.340	0.390	0.340	0.390	0.360	0.410	0.340	0.390
e	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
e_1	0.020	0.055	0.078	0.098	0.068	0.098	0.078	0.098
L	0.125	0.150	0.125	0.150	0.125	0.150	0.130	0.150
N	8-Lead		14-Lead		18-Lead		20-Lead	



Note 1: These dimensions do not include mold flash or protrusions. Mold flash protrusion shall not exceed .006" on any side.

Note 2: SO-8, SO-14, S0-16 packages are narrow body (0.150").

Note 3: Dimensions and tolerancing per ANSI Y14.5M-1982.

Note 4: Flat area of lead foot.

Note 5: SOL-24T2 (thermal package) has 2 fused leads on each side of package.

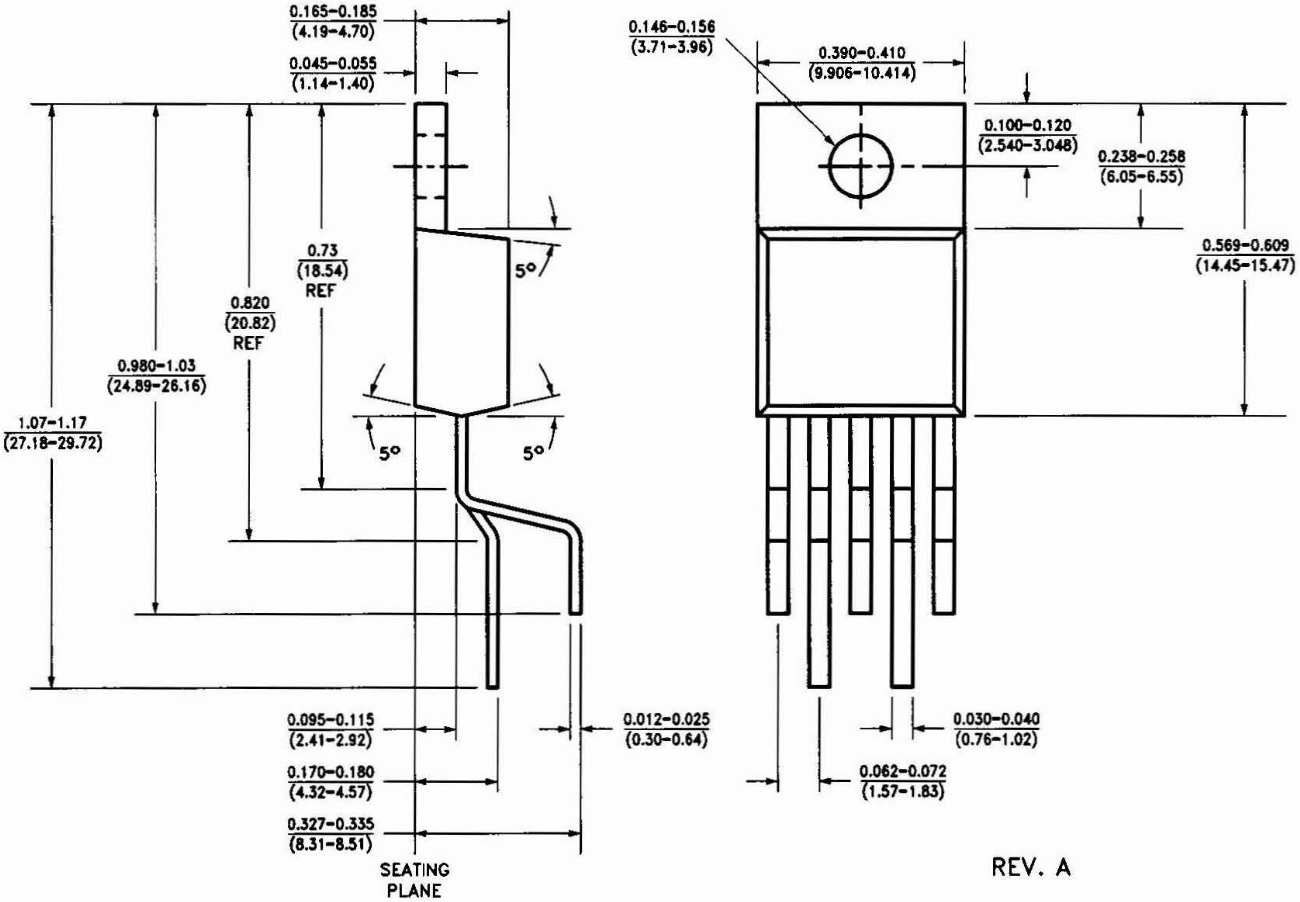
Note 6: SOL-20T (thermal package) has 4 fused leads on each side of package.

Note 7: SOL-28T contains a thermal metal slug.

MDP0027 Rev. C
Package Outline—SOIC

Lead Finish—Solder Plate

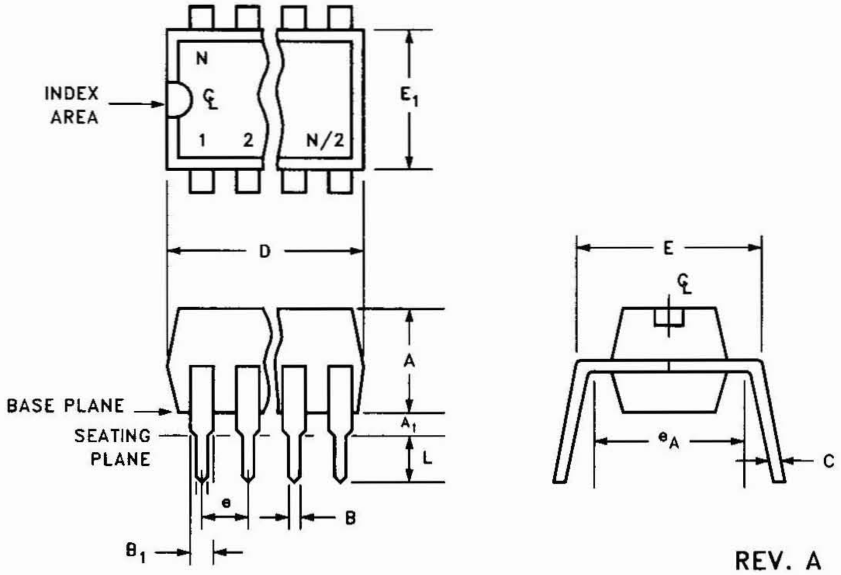
Symbol	Lead Count													
	SOL-28		SOL-20		SOL-16		SO-16		SO-14		SO-8		SOL-24	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.061	0.068	0.061	0.068	0.061	0.068	0.096	0.104
A_1	0.004	0.011	0.004	0.011	0.004	0.011	0.004	0.010	0.004	0.010	0.004	0.010	0.004	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.008	0.010	0.008	0.010	0.008	0.010	0.009	0.012
D	0.696	0.712	0.498	0.510	0.397	0.430	0.386	0.394	0.337	0.344	0.189	0.196	0.598	0.614
E	0.291	0.299	0.291	0.299	0.291	0.299	0.150	0.157	0.150	0.157	0.150	0.157	0.291	0.299
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC	
H	0.398	0.414	0.398	0.414	0.398	0.414	0.230	0.244	0.230	0.244	0.230	0.244	0.398	0.414
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024


0.165–0.185
(4.19–4.70)
0.045–0.055
(1.14–1.40)
0.146–0.156
(3.71–3.96)
0.390–0.410
(9.906–10.414)
0.100–0.120
(2.540–3.048)
0.238–0.258
(6.05–6.55)
0.569–0.609
(14.45–15.47)
0.73
(18.54)
REF
0.820
(20.82)
REF
0.980–1.03
(24.89–26.16)
1.07–1.17
(27.18–29.72)
5°
5°
5°
0.095–0.115
(2.41–2.92)
0.012–0.025
(0.30–0.64)
0.030–0.040
(0.76–1.02)
0.170–0.180
(4.32–4.57)
0.062–0.072
(1.57–1.83)
0.327–0.335
(8.31–8.51)
SEATING
PLANE
REV. A

MDP0028 Rev. A

5-Lead TO-220

Lead Finish—Solder Plate



MDP0031 Rev. A

Plastic Package

Lead Finish—Hot Solder DIP

Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A_1	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
A	0.125	0.145	0.125	0.145	0.125	0.145	0.125	0.145	0.125	0.145
B	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.015	0.021
B_1	0.050	0.070	0.050	0.070	0.050	0.070	0.050	0.070	0.050	0.070
C	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
D	0.350	0.385	0.745	0.755	0.745	0.755	0.875	0.905	0.925	1.045
E	0.295	0.320	0.295	0.320	0.295	0.320	0.295	0.320	0.295	0.320
E_1	0.245	0.255	0.245	0.255	0.245	0.255	0.245	0.255	0.245	0.255
e	0.100 Typ		0.100 Typ		0.100 Typ		0.100 Typ		0.100 Typ	
e_A	0.300 Ref		0.300 Ref		0.300 Ref		0.300 Ref		0.300 Ref	
L	0.115	0.135	0.115	0.135	0.115	0.135	0.115	0.135	0.115	0.135
N	8		14		16		18		20	

Note: Package outline exclusive of any mold flashes. Mold flash protrusion shall not exceed 0.006″ on any side.

Ordering Information

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Ordering Information

In North America, Elantec has three levels of sales support. Regional Sales Managers are located in the Boston and San Jose areas. Field Applications Engineers are located in the Boston and San Jose offices. Elantec also maintains a network of sales representatives covering the United States and Canada. Finally, major nationwide and regional distributors provide local stock. Elantec maintains an up-to-date distributor inventory status and provides an inventory referral service through Distribution Sales in San Jose. Orders may be placed through the sales representatives or distributors. A list of sales representatives and distributors is included in this databook, or please contact any of the regional sales offices.

The application specific products listed below are not generally available through U.S. Distribution channels. For information regarding price and availability, please contact your local Elantec representative or regional sales office.

- EL6251C Laser Diode Driver
- EL7556C Adjustable CPU Power Supply Unit
- EL7560C Programmable CPU Power Supply Unit
- EL7561C Programmable CPU Power Supply Unit
- EL7571C Programmable DC:DC Controller

In Europe, Elantec has a Regional Sales Office in London. Local sales support is provided through stocking representatives in all of the major countries. A current list of representatives and distributors may be obtained from the London office.

Elantec has stocking agents in all Pacific Rim Countries, Australia, and New Zealand. A list may be obtained from Elantec's headquarters in Milpitas, California.

In Asia, local sales support is provided through stocking representatives in all of the major countries. A current list of representatives is included in this databook or contact the factory.

Elantec Product Alpha/Numeric Description

E L 2006 A G

PREFIX
ELANTEC

FAMILY
L Proprietary Linear

PART
NUMBER

OPTIONAL SUFFIX
A Selected Electrical Performance
C −40°C to +85°C
E −40°C to +150°C
None −55°C to +125°C

PACKAGE
N Plastic DIP
J CerDIP
T TO-220
M Large Body SOIC
S Narrow Body SOIC
W SOT-23
SOT Marking Specifications
eYW?
e-Elantec
Y-Year code: last digit of year
W-Bi-weekly code: alpha only, example: A = ww1-2
?-Part Code: A = EL2150CW
B = EL2170CW
C = EL2180CW

Applications Assistance/ Sample Ordering Information

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Making Applications and Sample Requests Easier

Elantec's Policy

Elantec receives many applications inquiries every day which vary widely in nature. We believe that Application assistance is as inherently important to our customers as the performance and quality of our products. To assist our customers in getting the best and fastest support possible, the following information is provided.

Sample and Literature Requests

If you know what product sample or literature you need, probably the best and fastest way to obtain them is to call Elantec's local sales office, sales representative, or distributor. A complete listing is on pages 11-3 through 11-15 of this book. If you are not sure what you need, call our Applications hot line 1 (800) 333-6314. For literature only, touch or request extension 234. For applications assistance, touch or request extension 311.

New Applications Assistance

Technical assistance for a new application is a toll free phone call away. Call 1 (800) 333-6314 and touch or request extension 311. Probably the most important information that Elantec needs to assist you is a clear picture of what the circuit needs to do. What we mean by that is the cost and performance objectives of the circuit or system. If you have a preliminary topology or schematic, feel free to FAX that to the Factory at 1 (408) 945-9305 in confidence. The following is a check list which will expedite our assistance to you:

What does the circuit need to do?

What power supply voltages are available?

What is the temperature range?

What is the load?

What are the key specs: bandwidth, slew rate, settling time, noise, output voltage, etc. and what are your expectations?

Problems with an Existing Circuit and Other Issues

Applications assistance for an existing application is a toll free phone call away. Call 1 (800) 333-6314 and touch or request extension 311. Probably the most important information that Elantec needs to assist you is a clear picture of what the circuit is doing or not doing. The following is a check list which will expedite our assistance to you:

What is the part number?

What is the device's date code?

What are the symptoms?

Are scope photos or frequency plots available?

How many devices are involved?

Unreleased Product

As a general rule, Elantec does not sample new devices that have not completed our rigorous formal release cycle. However, occasionally we will "beta " site customers with advanced Engineering samples. We view this as a productive exchange between our Factory and customer Engineering teams to pin point problems and issues. In all instances, these devices will be marked "Engineering Sample." If you are interested in such a device, call your nearest Elantec sales office, local sales representative, or the Factory at 1 (800) 333-6314 and touch or request extension 252.

Demo Boards

Contact factory applications for demo board availability.

Quality or Reliability Issues

On the rare occasion that you experience what may be a Reliability or Quality issue, please contact the nearest Elantec sales office, local sales representative, or distributor. You may choose to call the Factory directly at 1 (800) 333-6314, and touch or request extension 310 or 279.

Price Quotes/Delivery Status

For pricing and delivery information, please contact the appropriate full service representative or local Elantec franchised distributor as listed on page 11-6. For additional information you may contact the Elantec Customer Service Department @ 1 (800) 333-6314.

Terms and Conditions of Sale

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELANTEC, INCORPORATED ("SELLER") TERMS AND CONDITIONS OF SALE

1. ACCEPTANCE OF ORDER

THIS ACKNOWLEDGEMENT AND ACCEPTANCE IS EXPRESSLY LIMITED TO AND MADE CONDITIONAL UPON THE TERMS AND CONDITIONS CONTAINED HEREIN AND ANY OF THE BUYER'S TERMS AND CONDITIONS WHICH ARE IN ADDITION TO OR DIFFERENT FROM THOSE CONTAIN HEREIN WHICH ARE NOT SEPARATELY AND SPECIFICALLY AGREED TO IN WRITING ARE HEREBY OBJECTED TO AND SHALL BE OF NO EFFECT.

Only those orders accepted by Seller as its home office in Milpitas, California shall be binding upon Seller.

2. PRICES

Irrespective of any prices quoted by Seller or listed on Buyer's order, Seller's acceptance of any order is subject to the prices shown on Seller's acknowledgment. Said prices are firm and are not subject to adjustment other that "precious metals adjustments" or "precious metals surcharges" at Seller's option to cover Seller's cost of fluctuations in the price of precious metals utilized in the manufacture of Seller's products.

3. TAXES

All prices are exclusive of all federal, state and local excise, sales, use and similar taxes. Such taxes shall be paid by Buyer, or in lieu thereof Buyer shall provide Seller with a tax exemption certificate acceptable to the taxing authorities. When applicable, such taxes will appear as separate additional items on the invoice unless Seller receives a proper tax-exemption certificate from Buyer prior to shipment.

4. PAYMENT

Unless Seller has extended credit to Buyer as described below, Buyer shall pay Seller, at Seller's option either by: Cash with Order, C.O.D., Letter of Credit or Sight Draft.

Should Seller elect to extend credit to Buyer, payment shall be made in full within thirty (30) days of the date of Seller's invoice. Seller reserves the right at any time to change the amount of or to withdraw any credit extended to Buyer.

Any payments made in excess of thirty (30) days may be subject to late charges.

5. TITLE AND DELIVERY

Seller shall deliver products sold hereunder to Buyer F.O.B. Seller's factory. Partial deliveries shall be permitted. Upon such delivery to a carrier at Seller's factory, title to the products and all risk of loss or damage shall pass to Buyer.

6. SHIPMENT

All shipping charges and expenses shall be paid by Buyer. Seller will not insure the products sold hereunder unless requested by Buyer in which case Buyer will pay for such insurance.

Shipments will be made, at Seller's option, either by Parcel Post, Railway Express. Air Express, Air Freight, or as otherwise determined by Seller.

Shipping dates are approximate and are dependent upon Seller's prompt receipt of all necessary information from Buyer.

7. PATENTS

With respect to products manufactured soley to Seller's designs and specifications, Seller shall defend any suit or proceeding brought against Buyer insofar as such suit or proceeding is based on a claim that any such products furnished hereunder infringe any patent of the United States. If Seller is notified promptly in writing of such suit or proceeding and given full and complete authority, information, and assistance by Buyer for such defense, Seller shall pay all damages and costs finally awarded against Buyer in any such suit or proceeding, but Seller shall not be responsible for any compromise thereof made by Buyer without the written consent of Seller. In the event that such products are held in such suit or proceeding to infringe a patent of the United States and their use is enjoined, or if in the opinion of Seller such products are likely to become the subject of a claim of infringement of a patent of the United States, Seller, in its sole discretion and at its won expense, may either: (a) procedure for Buyer the right to continue using such products with noninfringing products; or (b) modify such products so that they become noninfringing; or (c) replace such products with noninfringing products; or (d) accept the return of such products, granting Buyer a refund therefor equal to the depreciated value thereof.

Seller shall have no liability to Buyer under any provision hereof if any patent infringement or claim thereof is based upon (a) a modification of the products not introduced by or approved by Seller; or (b) the interconnection or use of the products in combination with products with other devices not made by Seller; or (c) the use of the products in other than an application recommended by Seller.

The foregoing states the entire liability of Seller for infringement of patents by Seller's products or any part(s) thereof.

8. INDEMNITY

Buyer shall indemnify, defend, and hold Seller harmless from and against any and all liability, damages, expenses, costs or losses resulting from any suit or proceeding brought for infringement of a patent(s), copyright(s), or trademark(s), or for a misappropriation of use of any trade secret(s), or for unfair competition arising from Seller's compliance with Buyer's design, specifications or instructions.

9. SECURITY INTEREST

Notwithstanding passage of title of products sold hereunder to Buyer F.O.B. Seller's factory, Seller shall retaln a security interest in the products until payment has been made in full by Buyer for such products. Buyer shall perform all acts necessary to perfect and maintaln such security interest.

10. WARRANTIES

Seller warrants to Buyer that Seller's standard products sold hereunder (and any services furnished therewith) which are not used in any medical or life support application shall be free from defects in material and workmanship and shall conform to the applicable specifications (if any) for a period of one year from the date of shipment. For products which are not standard products of Seller, such as dice and developmental or custom designed products. Seller warrants to Buyer that such products sold hereunder (and any services furnished therewith) shall be free from defects in material and workmanship and shall conform to the applicable specifications (if any) for a period of thirty (30) days from the date of shipment.

Should products sold hereunder fall to meet the above applicable warranty, Seller, at its option, shall repair or replace such products or issue Buyer a credit provided that (a) Seller is notified in writing by Buyer within thirty (30) days after discovery of such failure; (b)Buyer obtains a Return Material Authorization from Seller prior to returning any defective products to Seller; (c) the defective products are returned to Seller, transportations charges prepaid by Buyer; (d) the defective products are received by Seller for adjustment no later than four (4) weeks following the last day of the warranty period, and (e) Seller's examination of such products shall disclose, to its satisfaction, that such failures have not been caused by misuse, abuse, neglect, improper installation or application repair, alteration, accident or negligency in use, storage, transportation or handling.

In the event of failure to meet the above applicable warranty with respect to products sold hereunder cannot be corrected by Seller's reasonable efforts, the Seller and Buyer shall negotiate an equitable adjustment in price.

The foregoing warranty provisions set forth the Seller's sole liability and the Buyer's exclusive remedies for claims (except as to title) based on defects in or failure of any products sold hereunder or services furnished hereunder whether the claim is based in contact, tort, (including negligence), warranty or otherwise and however instituted. Upon the expiration of the applicable warranty for any products sold hereunder, all such liability shall terminate.

The above warranty periods shall not be extended by the repair or replacement of products pursuant to any of the above warranties. The above warranties shall apply only to Buyer and shall not apply to Buyer's customers or any other third parties.

SELLER PRODUCTS ARE NOT DESIGNED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS WITHOUT THE SPECIFIC WRITTEN CONSENT OF THE PRESIDENT OF ELANTEC. LIFE SUPPORT SYSTEMS ARE EQUIPMENT INTENDED TO SUPPORT OR SUSTAIN LIFE AND WHOSE FAILURE TO PERFORM WHEN PROPERLY USED IN ACCORDANCE WITH INSTRUCTIONS PROVIDED CAN BE REASONABLY EXPECTED TO RESULT IN SIGNIFICANT PERSONAL INJURY OR DEATH. USERS CONTEMPLATING APPLICATION OF SELLER PRODUCTS IN LIFE SUPPORT SYSTEMS ARE REQUESTED TO CONTACT SELLER FACTORY HEADQUARTERS TO ESTABLISH SUITABLE TERMS AND CONDITIONS FOR THESE APPLICATIONS. SELLER'S WARRANTY IS LIMITED TO REPLACEMENT OF DEFECTIVE COMPONENTS AND DOES NOT COVER INJURY TO PERSONS OR PROPERTY OR OTHER CONSEQUENTIAL DAMAGES.

11. LIMITATION OF LIABILITY

In no event, whether as a result of breach of contract, warranty or tort (including negligence) or otherwise shall Seller be liable for any special, consequential, incidental or penal damages, including but not limited to, loss of profit or revenues, loss of the product or any associated equipment, damaged to associated equipment, cost of captial, cost of substitute products, facilities, service or replacement power, down time costs or claims of Buyer's customers for such damages. If Buyer transfers title to or leases products sold hereunder to any third party, Buyer shall obtain from such third party a provision affording the Seller the protection of the preceding sentence.

Except as provided in the above "Patents" article, whether a claim is based in contract, tort (including negligence) or otherwise, the Seller's liability for any loss or damage arising out of, or resulting from any products sold hereunder or services furnished hereunder shall in no case exceed the price of the specific product(s) or service(s) which gives rise to the claim. Except as to title, any such liability shall terminate upon the expiration of the applicable warranty period specified in the above "Warranties" article.

12. U.S. GOVERNMENT CONTRACTS

If the products to be furnished hereunder are to be used in the performance of a U.S. Government contract or subcontract, no Government requirments or regulations shall be binding upon Seller unless specifically agreed to by Seller in writing.

If the Government terminates such a contract or subcontract in whole or in part through no fault of or failure to perform by Buyer, this order may be canceled in writing in the same proportion, and the liability of Buyer for termination allowances shall be determined by the then applicable regulations of the Government regarding termination of contracts.

13. EXCUSABLE DELAYS

Seller shall not be liable for delays in delivery or performance due to any cause beyond its reasonable control, including, without limitation, acts of God, acts of Buyer, strikes or other labor disturbances, inability to obtain necessary materials, components, services or facilities.

14. CANCELLATIONS OF STANDARD PRODUCTS

Should Buyer terminate any order accepted hereunder or should Seller terminate any order accepted hereunder due to Buyer's nonperformance of its obligations hereunder, then Buyer shall pay Seller its reasonable termination charges within fifteen (15) days from the date of invoice of same.

Buyer may request rescheduling or cancellation by providing thirty (30) days written notice to Elantec provided however, that elantec is not obligated to accept such notice, but if such notice is given and accepted by Elantec, then Elantec has the right to deliver and be paid by Buyer for:

1. 100% of quantity of devices scheduled for delivery within thirty (30) days following receipt of said notice.

2. 50% of quantity of devices scheduled for delivery within 30–60 days following receipt of said notice.

15. CANCELLATION OF PRODUCTS MANUFACTURED TO BUYER'S DESIGN/SPECIFICATIONS INCLUDING ALL NON-STANDARD AND DISK DRIVE PRODUCTS

Charge for engineering, design, generation of data, lot charges or any other special charges that are not for product are non-cancelable except with prior written permission from Seller.

Buyer may request rescheduling or cancellation of product by providing 60 day notice to Elantec provided, however, that Elantec is not obligated to accept such notice but if such notice is given and is accepted by Elantec, then Elantec has the right to deliver and be paid by the Buyer for:

1. 100% quantity within 60 days following written receipt of said notice;
2. All additional work in process scheduled within the 16 week delivery time period shall be paid for by Buyer at a price based on the percentage of completion of such inventory applied to the price for the finished product. Buyer shall also promptly pay to Elantec; (a) costs of settling and paying claims arising out of termination of work under Elantec's subcontracts or vendors; (b) reasonable costs of settlement, including engineering, development, accounting, legal and clerical costs; (c) twenty percent (20%) of the purchase price of the purchase order to be canceled.

16. ASSIGNMENT

Any assignment by Buyer of this order or of any rights or obligations in connection therewith shall be void without the written prior consent of the Seller.

17. EXPORT TO NON-APPROVED COUNTRIES

Buyer agrees to take all reasonable and necessary precautions to prevent ultimate exportation of Elantec products to countries prohibited by rules or regulations of the United States Government, and to obtain all export licenses and other governmental approvals necessary prior to the export of any Elantec products.

18. MISCELLANEOUS

The validity, performance and construction of these terms and conditions of sale and any sale hereunder shall be governed by the laws of the state of California.

The invalidity, in whole or in part, of a y provision herein shall not affect the validity or enforce ability of any other provision herein.

Any representation, warranty, course of dealing or trade usage not contained or referenced herein shall not be binding on Seller.

No modification, amendment, recision, waiver or other change in these terms and conditions shall be binding on Seller unless assented to in writing by Seller's duly authorized representative.

Seller reserves the right to manufacture and/or assemble its products in any of its worldwide facilities unless otherwise agreed to in writing with Buyer.

Sales Representatives and Distributors

élantec

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FAX 205-881-1490
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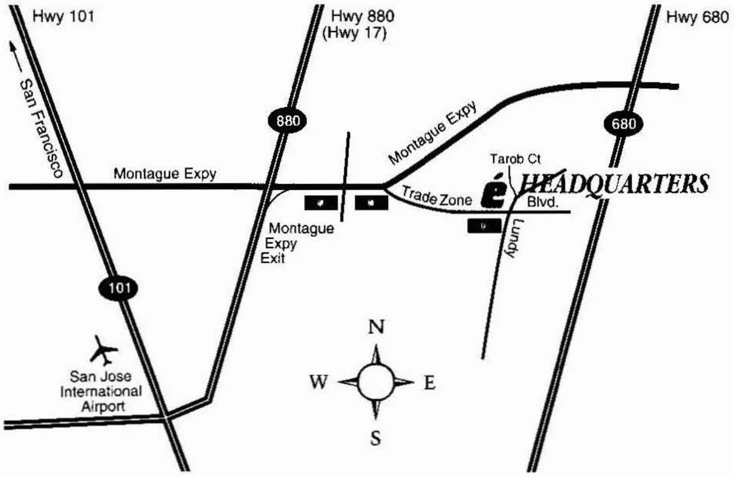
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